IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 25 July 2022, accepted 29 September 2022, date of publication 5 October 2022, date of current version 10 October 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3211562

RESEARCH ARTICLE

A Reliable and Energy-Efficient Nonvolatile Ternary Memory Based on Hybrid FinFET/RRAM Technology

ARAM YOUSEFI, NIMA ESLAMI, AND MOHAMMAD HOSSEIN MOAIYERI, (Senior Member, IEEE)
Faculty of Electrical Engineering, Shahid Beheshti University, Tehran 1983969411, Iran
Corresponding author: Mohammad Hossein Moaiyeri (h_moaiyeri@sbu.ac.ir)

ABSTRACT With the successful development of information technology, particularly in big data and neural network scopes, the appetency for denser memory compositions has exponentially outreached. Accordingly, multi-valued logic has extensively been explored as a promising solution for data storage density enhancement and interconnect complexness declining, integrating with emerging nonvolatile nanodevices. This paper presents a reliable nonvolatile 3-transistor 1-RRAM (3T1R) ternary memory cell and its compact array architecture fulfilled on hybrid RRAM/FinFET logic, in which the cell layout can be densely plugged into the memory array architecture. Comprehensive post-layout simulations based on 7nm FinFET technology have been conducted to assess the proposed design's functionality, performance, and reliability. Our proposed ternary 3T1R cell has exceptional immunization confronting radiations availing the RRAM radiation immunity and innovative circuit structure. Meanwhile, the RRAM's engrossing nonvolatile nature induces no static power dissipation in the hold state, certified for low-power applications. Moreover, Monte-Carlo simulation results demonstrate the roughly 20% functional failure of the 1T1R cell's ternary implementation facing process-voltage-temperature (PVT) variations. However, the proposed design operates robustly in the presence of PVT variations with no functional failure while offering lower delay and energy consumption. Meanwhile, it is also well-designed for addressing the Fin quantization impact of FinFET.

INDEX TERMS Nonvolatile memory, RRAM, ternary logic, FinFET, SEU, PVT variations.

I. INTRODUCTION

Most state-of-the-art semiconductor memories and computing systems are based on binary logic, which has touched perfection in recent decades. With the technology enhancements and emergence of the big data concept, the need for high-capacity and high-performance memories has significantly increased [1], [2], [3]. Meanwhile, the necessity of reducing interconnect complexity and chip areas has motivated more investigations on cutting-edge solutions such as multi-valued logic systems.

MVL is a logical calculus method that utilizes more than two logic values [2], [4]. High-density data storage, high-rate data transfer, fewer logic operations, reduction of pin count, and lower energy dissipation due to diminished interconnects are the great potential advantages of MVL. However, these advantages come at the cost of lower noise margins [5], [6]. Considering non-binary radices, the radix three (ternary logic) can lead to the optimized complexity in switching systems [7], [8], [9]. Moreover, ternary neural networks can effectively make a trade-off between efficiency and accuracy [10].

Embedded memories contribute to most occupied areas in contemporary integrated circuits and systems. Moreover, the need for semiconductor memories with significantly higher densities has increased significantly. A promising approach to meet this demand is to use MVL [9], [11]. MVL has been widely used in ultra-high-density and low-cost commercial semiconductor memories [1], [12]. On the other hand, by reducing the feature size below 10nm, conventional

The associate editor coordinating the review of this manuscript and approving it for publication was Ye Zhou.

memory technologies have faced critical challenges such as loss of stored data and lower reliability [13]. Furthermore, high latency and energy dissipation of data transmissions between the memory and processor during data processing has caused a bottleneck in the conventional von Neumann architecture [14], [15].

A promising solution is using nonvolatile memories such as resistive random-access-memory (RRAM). Implementing logic through memristive elements is an efficient approach to overcome the memory wall in von Neumann architecture [13], [16]. It is worth mentioning that RRAM technology can store data in multi-level resistances. The RRAM arrays can also be used for implementing efficient ternary neural networks and ternary content-addressable memory (TCAM) [17], [18]. TCAMs are mainly utilized in network applications. It is worth mentioning that the nature of data storing in a TCAM is entirely different compared to a ternary RRAM memory. The data stored in a TCAM can be '0', '1', or don't care ('X'). Moreover, the TCAM memory element mainly consists of two storage elements that map the mentioned logic. Meanwhile, the data in ternary RRAM memory stores three-level data in a single memory element [18].

As a non-charge-based device, RRAM has more advantages, such as high endurance, denser integration, radiation immunity, and lower power than conventional memories [9], [15]. Besides, the nonvolatility feature of RRAM enables the system to be entirely powered off during the idle mode without imposing any additional circuit requirements, which remarkably reduces power dissipation.

Although scaling the CMOS technology to nanometer dimensions has led to denser chips, it has caused critical issues like gate control degradation and short channel effects. Therefore, new technologies have evolved to address these bottlenecks. FinFET is one of the leading industrial technologies to reach smaller cell areas with higher reliability [19], [20]. Due to the three-dimensional gate coverage over the ultra-thin channel region of FinFETs, they have excellent gate control and lower short-channel effects. Moreover, FinFETs have a considerably higher I_{ON}/I_{OFF} ratio than the conventional CMOS transistors for a given gate width [20], [21].

Notwithstanding that FinFET brings numerous benefits, the width quantization challenge in FinFETs can raise serious concerns, specifically in ratioed circuits and memory elements [22]. Although RRAM can be considered a promising solution for designing MVL memories, the width quantization constraint can lead to significant concerns in the FinFET-based peripheral circuits, from functionality to optimization characteristics. This is because the RRAM-based memories require a particular current flow to perform the read/write operations and multi-level resistance designation. Therefore, designing an RRAM-based MVL memory with FinFET-based peripheral circuits alongside considering the width quantization limitation attracts a tremendous interest in hybrid RRAM-FinFET memory design.

From another essential perspective, the capacitance of nodes and supply voltage will decrease by downscaling the feature size. Therefore, the electric charge amount collected on a node is reduced [19], [23]. Hence, nanoscale circuits are more vulnerable to particle-induced charges, creating reliability issues [24]. If the impulsive current induced by particle strikes causes a memory element to flip wrongly, a single-event upset (SEU) occurs [25]. As a result, SEU tolerance of memory elements has become more critical and should be considered, specifically in ternary RRAM arrays.

This paper proposes a hybrid RRAM/FinFET-based ternary nonvolatile memory cell and its associated array architecture. In this approach, the RRAM device performs as a nonvolatile ternary storing element, and the FinFETs realize the peripheral circuitry. The proposed ternary memory cell is a simple 3-transistor 1-RRAM (3T1R) structure. Two p-type FinFETs are employed to perform the write operation, and an n-type FinFET accomplishes the read operation. By configuring a dual-step ternary write operation and benefiting from a write-isolated read operation, remarkable improvements in the read and write delays are achieved. Furthermore, the compact well-shaped layout of the proposed cell fits well in the proposed memory array architecture structure. Our proposed design facilitates power gating in ternary integrated circuits, and ternary blocks can be power gated efficiently during idle times.

The prominent 1T1R cell proposed in [26] is a binary implementation with a limited numeral of voltage level requirement and superior tolerance against PVT variations and SEU for its read/write operations. In contrast, the ternary 1T1R implementation encounters severe constraints such as requiring numerous voltage levels for the ternary Read/Write operations. Also, the intermediate gate voltage level demand for these operations leads to a significant vulnerability to process, voltage, and temperature (PVT) variations. According to these bottlenecks in ternary 1T1R cell implementation, our novel 3T1R configuration will be an excellent alternate for ternary RRAM-based memory architectures due to considerably fewer voltage levels, high robustness to PVT variations, and a compatible FinFET-based circuitry concerning the width quantization. It is also worth mentioning that most of the state-of-the-art ternary circuits have been developed based on emerging technologies, which have not yet been commercialized [4], [8], [27], [28], [29]. However, our work stands on FinFET and RRAM as the leading industrial technologies, commercialized by several semiconductor manufacturers [30], [31], [32]. The layouts of the proposed designs and the post-layout simulations are provided. Our extensive simulations indicate the significant robustness of the proposed ternary nonvolatile 3T1R structure to PVT variations and radiations. Our results conclude that the proposed structure can be a milestone for presenting commercial ternary nonvolatile RRAM structures.

The rest of this paper is organized as follows: Section II provides a brief review of the preliminaries of this study, including metal-oxide RRAM, ternary logic, and the

1T1R cell for ternary logic. The proposed ternary RRAM cell and array architecture are described in Section III. Section IV presents the simulation results and functionality analyses, and finally, Section V concludes the study.

II. BACKGROUND

In this section, the preliminaries and background of the research are reviewed.

A. METAL-OXIDE RRAM

The metal-oxide RRAM device as a two-terminal component has extended its influence beyond memories to the world of logic circuits and computing. The fabrication process of this device is entirely compatible with the fabrication processes of the current semiconductor technologies [13], [26], [33]. This device has tremendous potential for designing multi-valued memories and in-memory computing because it stores data at several resistance levels [6], [9], [13], [16]. Meanwhile, nonvolatility, excellent scalability, low programming voltage, energy-efficient operations, and zero standby leakage energy are the other noteworthy benefits of the RRAM device [13], [26], [34].

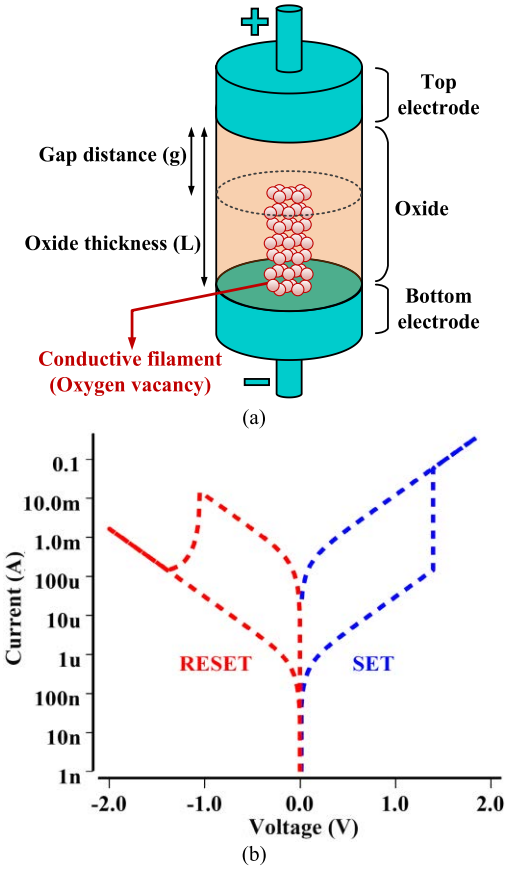


FIGURE 1. Metal-oxide bipolar RRAM (a) Device structure schematic (b) I-V characteristic.

Fig. 1a shows the schematic of a metal-oxide bipolar RRAM device. This device has a thin insulator layer sandwiched between the top electrode (TE) and the bottom electrode (BE). The working mechanism of this device relies on the formation and rupture of a conductive filament (CF), which is an Oxygen vacancy growing structure between TE and BE [35]. The principal variable used to model the behavior of this device is the gap distance (g), which is the average spacing between TE and the summit of CF. Adjusting the value of g can alter the RRAM resistance exponentially through the electron tunneling conduction mechanism. The RRAM resistance has a non-linear relationship with the voltage across to RRAM (V). Generally, the RRAM resistance shows a low slope linear (exponential) dependency for low (high) applied voltages.

Accordingly, a hyperbolic sine relation can express the I-V characteristic of an RRAM shown in Fig. 1b as follows:

$$I = I_0 \exp\left(-\frac{g}{g_0}\right) \sinh\left(\frac{V}{V_0}\right) \tag{1}$$

where V_0, g_0, and I_0 are fitting parameters [26].

Due to the generation (recombination) of oxygen vacancies and ions at the summit of the CF caused by a positive (negative) voltage applied across the RRAM, the CF will grow (dissolute). The following equations can model this process:

$$\gamma = \gamma_0 - \beta\left(\frac{g}{g_1}\right)^3 \tag{2}$$

$$\frac{dg}{dt} = v_0\left[-\exp\left(-\frac{qE_{ar}}{kT}\right)\exp\left(-\frac{\gamma a_0}{L}\frac{qV}{kT}\right) \times \exp\left(-\frac{qE_{ag}}{kT}\right)\exp\left(\frac{\gamma a_0}{L}\frac{qV}{kT}\right)\right] \tag{3}$$

$$g\,(t+dt) = g\,(t) + dg \tag{4}$$

where γ is the gap-dependent local field enhancement factor, calculated in (2). This parameter reflects high-k dielectrics' polarizability and the device structure's non-uniform potential distribution. Equation (2) is obtained from the experimental pulsed I-V fitting of HfO_x-based RRAM devices. γ_0, β, and g_1 are fitting parameters.

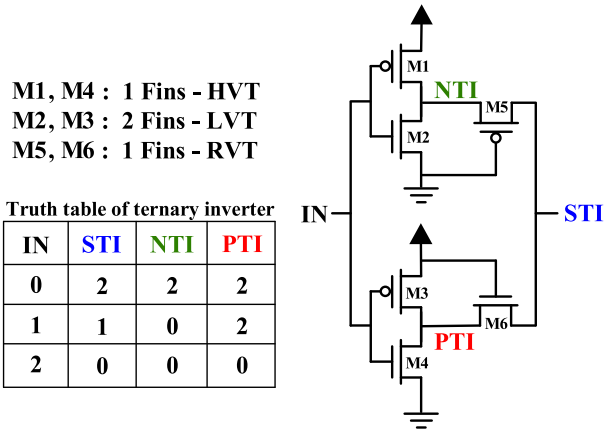
In (3), dg/dt is the gap growth/dissolution velocity, E_{ag} (E_{ar}) is the activation energy of oxygen vacancy in the generation (recombination) process, L is the oxide thickness, and a_0 is the atomic hopping distance [26].

B. TERNARY LOGIC

Ternary logic presents three logic levels, expressed by '0', '1', and '2' digits corresponding to the 0, 1/2 V_{DD}, and V_{DD} voltage levels [4], [28]. The fundamental ternary logic and arithmetic circuits have been widely studied in the literature [4], [28], [29].

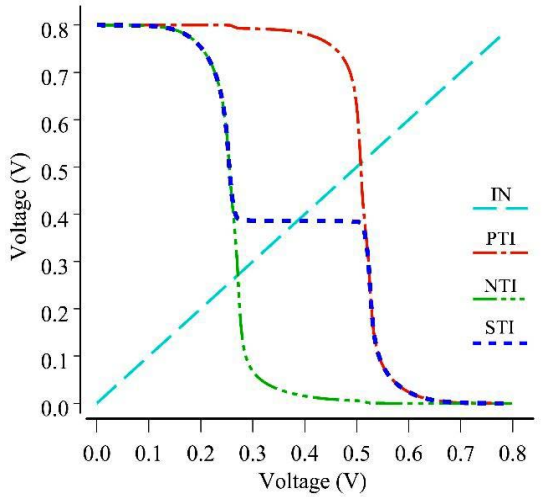
The truth table and circuit structure of the ternary inverter are shown in Fig. 2a. The standard ternary inverter (STI) is realized based on the negative ternary inverter (NTI) and the positive ternary inverter (PTI). The NTI (PTI) function is realized by employing a high-V_t (low-V_t) p-type transistor and a low-V_t (high-V_t) n-type transistor. Then, the PTI and NTI nodes are attached using a p-type (M5) and an

n-type (M6) transistors with the same geometries. Consequently, the voltage of the STI node is generated by a voltage division as $V_{STI} = 1/2\ (V_{NTI}+V_{PTI})$. Fig. 2b shows the ternary inverter's voltage transfer characteristic (VTC), including NTI, PTI, and STI functions. Two STIs can be cascaded to form a standard ternary buffer (STB).



IN	STI	NTI	PTI
0	2	2	2
1	1	0	2
2	0	0	0

(a)



(b)

FIGURE 2. Ternary inverter (a) Truth table and schematic (b) VTC.

III. PROPOSED DESIGNS

In this section, the proposed designs are presented and described in detail.

A. THE 1T1R CELL IN TERNARY LOGIC

The well-known 1T1R cell is shown in Fig. 3 [26]. This cell, which has been well established for binary logic, requires a few voltage levels for the read and write operations in binary logic. Moreover, the circuit does not operate in the variation-susceptible intermediate zone due to applying only the 0V and V_{DD} voltage levels on its transistor's gate in binary logic.

Accordingly, the 1T1R cell is adequately tolerant to PVT variations and SEU in binary logic.

However, this structure cannot be utilized well for ternary logic. Unlike the binary 1T1R with dual resistance states,

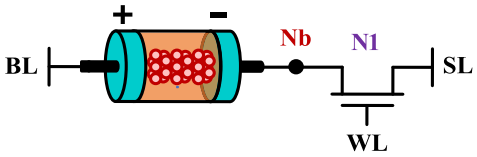


FIGURE 3. Circuit schematic of the 1T1R configuration.

three resistance states should be written on RRAM in ternary logic. This is very challenging to deliver the required distinct write currents using one transistor. In this situation, intermediate voltage levels should be applied to the transistor's gate for accurate write operations on RRAM, significantly intensifying the susceptibility to PVT variations. Meanwhile, the write delay increases due to the lower current flowing through the transistor when an intermediate voltage is applied to its gate.

Furthermore, an accurate write operation on RRAM demands sufficient current flow (by increasing the number of Fins), making the transistor ON resistance (R_{ON}) incomparable to the ternary resistances of the RRAM. Thus, the read operation requires an intermediate gate voltage level to acquire lower resistance for the transistor and achieve an appropriate voltage division for the read operation. Accordingly, numerous voltage levels (six voltage levels in addition to the 0V, 1/2 V_{DD}, and V_{DD} logical voltage levels) are required in the ternary 1T1R's Read/Write operations.

Besides noted bottlenecks in the ternary 1T1R realization, another serious concern is associated with the width quantization of FinFETs. Specifying ternary resistance levels via the write operation and performing a successful read operation (voltage division between RRAM and FinFET) with these resistance levels by utilizing only one FinFET in 1T1R results in a significant degradation in energy efficiency and reliability. Consequently, we suggest proposing a design that addresses all the mentioned challenges in ternary 1T1R.

B. THE PROPOSED TERNARY RRAM CELL

The proposed ternary RRAM cell is a 3T1R structure, as shown in Fig.4a. This memory cell operates in three modes (write, read, and hold). The RRAM device acts as a storage element, and the FinFETs realize the peripheral circuitry to satisfy a distinct purpose in each operation mode. The threshold voltage type, fin number, and task of each FinFET in the proposed cell are tabulated in Table 1.

The layout of the proposed ternary cell, designed by the Cadence Virtuoso tool using the 7nm FinFET technology [36], is shown in Fig. 4b. The layout of our proposed cell with a $0.054\mu m^2$ area is well shaped to fit in the memory array structure with the least number of metal layers required and the smallest occupied area.

The RRAM device can provide various ternary resistance level configurations of high-resistance-state (HRS), medium-resistance-state (MRS), and low-resistance-state (LRS), and each resistance level can realize a trit ('0', '1', and '2'). In the proposed cell, three resistance levels of 800kΩ (HRS),

TABLE 1. Specification of FinFETs in the proposed ternary RRAM cell.

Transistor	V_t type	Fins	Task
P1	SLVT (Super-low-V_t)	1	Write FinFET transistor
P2		2	Write FinFET transistor
N1	HVT (High-V_t)	1	Read FinFET transistor

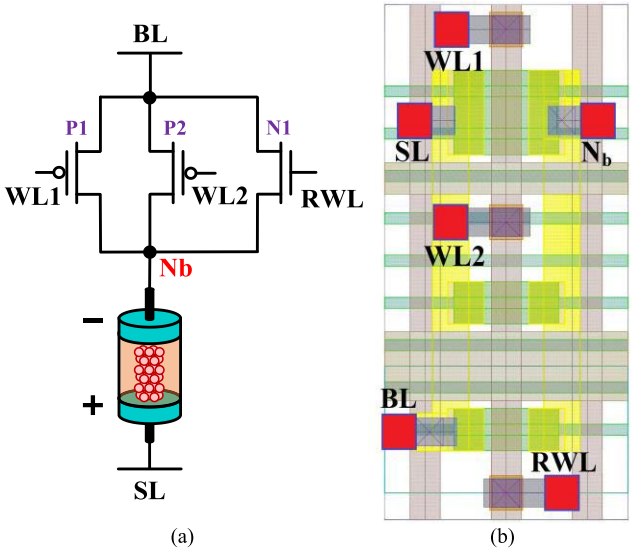


FIGURE 4. The proposed ternary RRAM cell (a) Circuit schematic (b) FinFET-based cell layout.

100kΩ (MRS), and 40kΩ (LRS) are considered for the '0', '1', and '2' trits, respectively, and it is worth mentioning that these resistance levels can vary within ±20% of the mentioned resistances without any functional failure, which is extensively analyzed with Monte-Carlo simulations in section IV. B.

The bottlenecks of the 1T1R cell in ternary logic are well addressed by the proposed 3T1R cell. Table 2 shows that the required voltage levels for read and write operations are reduced to three levels (in addition to the 0V, 1/2 V_{DD}, and V_{DD} logical voltage levels), similar to the binary 1T1R cell. Also, no intermediate voltage levels are applied on transistor gates by employing two transistors for the write operation (P1 and P2), providing a robust ternary write operation.

Considering the required voltage levels for the functional modes in the proposed cell tabulated in Table 2, although the voltage levels of 2.5V, 1.6V, and 1.9V are applied on the SL and BL nodes, the voltage differences between the terminals of the FinFETs are about 1V in any functional mode. Consequently, despite the applied voltages on the cell's input nodes, there will be no concern regarding the voltage stress on the FinFETs in the read and write operations. As an instance, in the first phase of the write operation (initialization), while the BL and SL are driven to 1.9V and 0V, respectively, the intent of applying 0.8V on the read FinFET's gate (RWL) is likewise to eliminate voltage stress on the read FinFET (N1). Moreover, the applied voltage makes no write disturbance in the initialization phase since the read FinFET is off despite applying 0.8V on its gate ($V_{GSN1} < 0V$). This point will be investigated for all operating modes in detail in Section IV.A.

TABLE 2. Input voltages in different operation modes.

Voltages	Write				Read	Hold
	Phase 1	Phase 2				
	Initialization	Write 0	Write 1	Write 2		
V_{BL}	1.9V	0V	0V	0V	0V	0V
V_{SL}	0V	0V	2.5V	2.5V	1.6V	0V
V_{WL1}	0.8V	0V	0V	0.8V	0.8V	0V
V_{WL2}	0.8V	0V	0.8V	0V	0.8V	0V
V_{RWL}	0.8V	0V	0V	0V	0.8V	0V

The operation modes of the proposed ternary RRAM cell are as follows:

1) WRITE MODE

In the write mode, the RRAM resistance switches within three HRS, MRS, and LRS levels. According to (1), this switching occurs by a high enough negative or positive voltage applied across the RRAM. The applied voltage is provided by applying determined voltages to the nodes BL and SL and switching the SLVT FinFETs P1 and P2. As both P1 and P2 FinFETs are of the SLVT type, they can supply a high enough write current with the minimum number of fins. The write operation generally has two phases. P1 and P2 contribute to both phases, while N1 is switched OFF during this procedure.

The RRAM's state should be initialized to HRS in the first phase. Accordingly, V_{BL} = high, V_{SL} = 0V, and V_{WL1} = V_{WL2} = high, and consequently, both P1 and P2 turn ON, and the current flows from BL to SL through P1 and P2. The writable negative voltage applied across the RRAM device initializes its state to HRS in this condition. The input voltages in different operation modes of the cell are given in Table 2. In the second phase, the data of interest is written on the RRAM.

To write '1', V_{BL} = 0V, V_{SL} = High, V_{WL1} = 0V, and V_{WL2} = High; consequently, only the single-fin transistor P1 turns ON, and the positive voltage applied across the RRAM device switches its state to MRS.

To write '2', V_{BL} = 0V, V_{SL} = High, V_{WL1} = High, and V_{WL2} = 0V, and consequently, only the double-fin transistor P2 turns ON, and the high enough positive voltage applied across the RRAM device switches its state to LRS. It is worth mentioning that switching the RRAM from HRS to LRS demands a higher current flow, so the P2 FinFET has more fins than P1 FinFET, as shown in Table 1.

To write '0', no action is required in the second phase as the RRAM state has been initialized to HRS in the first phase.

2) READ MODE

During the read mode, V_{RWL} = High, and N1 contributes to the read operation. Moreover, P1 and P2 (write transistors) are OFF. To start the read operation, the RRAM's state must be

transformed to its corresponding voltage level at node N_b. For this purpose, V_{SL} and V_{BL} are set to high and 0V, respectively, and consequently, a write-isolated and fast voltage division between the RRAM and N1 HVT transistor determines the voltage of node N_b. The main goal for utilizing a single-Fin HVT Read transistor and an MRS of nearly 2.5 times of LRS is to create a proper voltage division between the RRAM and RON of the read transistor with the minimum number of Fin and voltage levels and maximum robustness for the read operation. Accordingly, depending on the state of the RRAM, which can be HRS, MRS, or LRS, the logic of the node Nb will be '0', '1', or '2', respectively. Notably, the potential difference between the nodes SL and BL must be low enough to prevent read disturbance. The change in V_{Nb} is sensed by a ternary read buffer and provided as 0V, 1/2 V_{DD}, or V_{DD} at the memory read output.

3) HOLD MODE

Due to the nonvolatility of RRAM, in the hold state, all of the inputs are grounded, and hence, the leakage dissipation is zero. The only concern in this mode is the possible vulnerability of the stored data to SEU caused by the strike of ionizing particles on the critical nodes of the cells. Fortunately, according to the high voltage value required to switch the RRAM's state, the SEU can barely touch the RRAM data in this mode, and the ternary cell is practically immune to SEU. Further evaluations on the SEU tolerance of the proposed design, particularly during the read and write modes, will be presented in the next section.

C. THE PROPOSED TERNARY RRAM ARRAY

Fig. 5 depicts the scheme of the presented ternary RRAM array architecture, which consists of the cell array (CA), precharge circuit (PRC), row decoder (RD), column decoder (CD), and output ternary buffer (OTB) parts. This array architecture functions in the three modes of write, read, and idle in alliance with a memory control unit (MCU). The MCU manages the RD, CD, OTB, and DEMUX parts. The OTB in each line consists of two cascaded STI inverters (Fig. 2a) as a ternary buffer for sensing RBL line transitions in read mode. The CD is planned to assert the $WL1_j$, $WL2_j$, and BL_j column lines within the particular voltage levels.

In Table 2, both $WL1_j$ and $WL2_j$ switch between V_{DD} and 0V, and the BL_j lines switch between 1.9V and 0V. Hence, RD is designed to control the RWL_i and SL_i lines and switch them within individual voltage levels. Table 2 shows that the RWL_i lines switch between V_{DD} and 0V, and the SL_i lines switch specifically among 2.5V, 1.6V, 1.9V, and 0V.

To obtain an isolated and robust read operation in the array architecture, a pass transistor for each 3T1R cell is employed such that the N_b nodes of the row and read output nodes (RBLs) will be linked only in the read operation by asserting that row's corresponding RWL. Corresponding pass transistor should likewise be considered for the ternary 1T1R array. Consequently, the non-active RWL establishes no connection between the N_b and RBL nodes in the write mode, and the

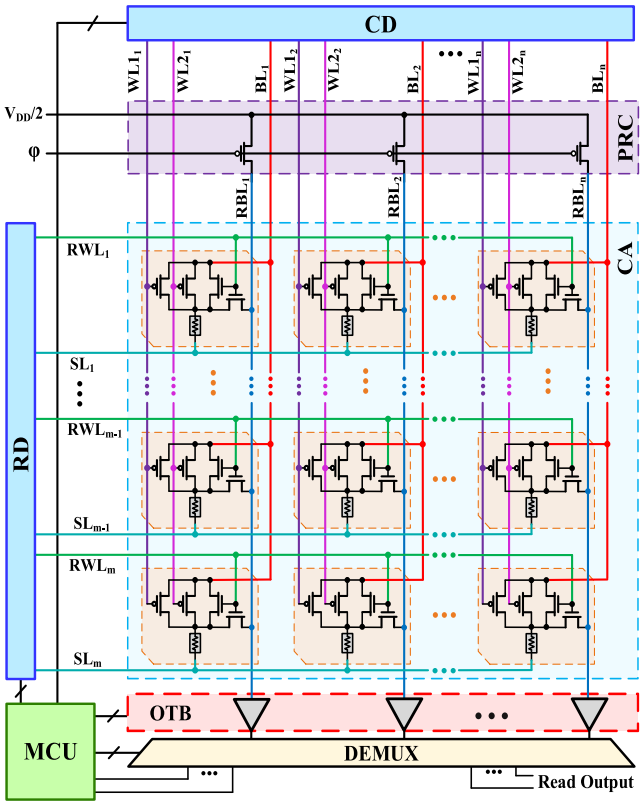


FIGURE 5. The proposed ternary RRAM array architecture.

write circuit becomes entirely isolated from the read part in the proposed array. Therefore, the 3T1R cell has an auxiliary isolated read transistor for array structure design, which alters the cell to 4T1R configuration. Meanwhile, as noted above, the 1T1R cell also alters to 2T1R due to the request for an additional isolated read transistor in the array structure design.

The write operation in the proposed array can be performed in two different configurations. The first one is the single-cell write, in which only an individual cell is written. This configuration can speed up memory performance, especially in in-memory computation. The second configuration is the single-row write, in which the row of interest is written. It is worth mentioning that both of these configurations are attainable for the read mode, and reading data can be performed from either a cell or a row.

The functionality and configurations of the proposed array in each operation mode are as follows:

1) SINGLE-CELL WRITE MODE

Based on the data expected to be written in the selected cell ($cell_{i,j}$), MCU manages the control signals established by the CD and RD units. These units provide the required write/read control signals for the entire array.

To write '1' ('2') on $cell_{i,j}$, two phases are accomplished. In the initial phase, the RD and CD units set the SL_i, BL_j, $WL1_j$, and $WL2_j$ signals of $cell_{i,j}$ to 0V, 1.9V, 0.8V, and 0.8V, respectively. Due to the shared BL_j of the selected $cell_{i,j}$ in

column$_j$, the SL lines of the cells in this column should be connected to 1.9V to prevent any unwanted write operation in column$_j$. In the subsequent phase, to achieve the desired '1' ('2') write operation in the selected cell$_{i,j}$, the SL$_i$, BL$_j$, WL1$_j$, and WL2$_j$ must be set to 2.5V, 0V, 0V (0.8V), and 0.8V (0V), respectively. Meanwhile, due to the shared SL$_i$ of the cell$_{i,j}$ in row$_i$, the BLs of all columns except column j must be connected to 2.5V. Also, WL1-WL2 of these columns must be connected to 0.8V to prevent any unwanted write operation in the other unselected cells. To write '0' in cell$_{i,j}$, only the initial phase must be performed because the cell data becomes '0' in this phase.

2) SINGLE-ROW WRITE MODE

To write the desired data in the selected row$_i$, the write/read control signals for the entire array are asserted by the CD and RD units handled by MCU. The write operation has two phases. First, to initialize every cell of the row$_i$ simultaneously, the RD and CD units set SL$_i$, BL$_{1ton}$, WL1$_{1\ ton}$, and WL2$_{1ton}$ of the row$_i$ to 0V, 1.9V, 0.8V, and 0.8V, respectively. Due to the shared BL in each column of row$_i$, the SL line of the unselected rows must be connected to 1.9V to prevent any unwanted write operation in the unselected rows.

Then, to achieve the desired write on the selected row (row$_i$), SL$_i$ and BL$_{1\ ton}$ of row$_i$ must be set to 2.5V and 0V, respectively. Accordingly, by adjusting WL1$_j$ and WL2$_j$ to specific values, any of '0', '1', and '2' data can be written on the cells of row$_i$. If WL1$_j$ and WL2$_j$ are connected to the supply voltage, no write operation will be performed, and the cell data remains the initial value. If WL1$_j = 0$V and WL2$_j = 0.8$V, '1' will be written on the cell, and the cell is written to '2' if WL1$_j = 0.8$V and WL2$_j = 0$V.

3) Read mode: Before beginning each read mode, the PRC circuit pre-charges the RBL$_i$ lines to 1/2 V_{DD} (floating 1/2 V_{DD}) through the φ signal. Next, RD activates the RWL$_i$ read signal to turn on the pass transistors in the selected row$_i$ and SL$_i$ is connected to 1.6V to perform the read operation in this row. Moreover, the CD unit turns off the write FinFETs by setting WL1s and WL2s to 0.8V and connects all BLs to the ground. After the resistive voltage division between the read transistors and RRAMs in the memory cells of the selected row$_i$, the changes in V_{Nb} are reflected on the voltage of the pre-charged RBL lines through the pass transistors. Based on the voltage transition of the RBL lines in the OTB part, the sense amplifiers at the end of each RBL line generate the desired read data provided as 0V, 1/2 V_{DD}, or V_{DD} at the memory read output.

4) Idle mode: In this mode, due to the nonvolatility of RRAM, all of the input signals can be grounded. Therefore, the leakage dissipation of this mode is nearly zero.

Fig. 6 presents the proposed ternary RRAM memory array (4 × 4) layout, designed by the Cadence Virtuoso tool using the 7nm FinFET technology [36]. The occupied area of the 4 × 4 array is 1.038μm^2, and only two metal layers are used in this layout. The RRAMs can be fabricated between the Nb and SL nodes in the third or upper metal layers.

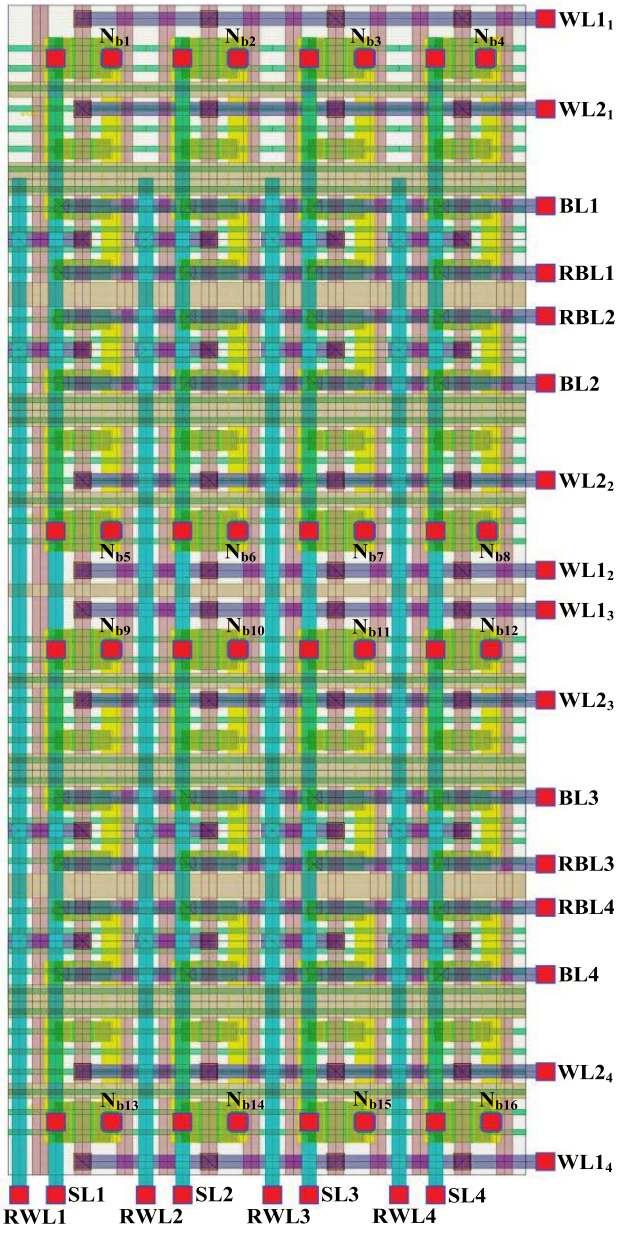


FIGURE 6. The FinFET-based layout of the 4 × 4 proposed ternary RRAM array.

IV. PERFORMANCE EVALUATION

To assess the function and performance of the proposed designs, circuit-level simulations have been performed at 0.8V using the 7nm Trigate FinFET technology model presented in [36]. The Verilog-A RRAM model is also obtained from the Stanford compact model presented in [26]. The employed global parameters of the RRAM device, the default values of the Stanford model, are given in Table 3.

A. TERNARY RRAM CELL FUNCTIONAL SIMULATIONS

In this subsection, we evaluate the performance of the proposed ternary memory cell in terms of delay, power, robustness to process variation, and SEU tolerance.

TABLE 3. RRAM model vital parameters.

Parameter	value	Description
I_0	61.4 μA	I-V fitting parameter
g_0	0.275 nm	I-V fitting parameter
β	1.25	Gap dynamics fitting parameter
v_0	150 m/s	Gap dynamics fitting parameter
g_{min}	1.7 nm	Minimum gap distance
L	5 nm	Oxide thickness
τ_{th}	0.23 ns	Effective thermal time constant
E_{ag}	1.501 eV	Activation energy for vacancy generation
V_0	0.43 V	I-V fitting parameter
g_1	1 nm	Gap dynamics fitting parameter
γ_0	16.5	Gap dynamics fitting parameter
a_0	0.25 nm	Atomic hopping distance
g_{max}	0.1 nm	Maximum gap distance
T_0	298 K	Ambient temperature
C_{th}	0.318 fJ/k	Effective thermal capacitance
E_{ar}	1.5 eV	Activation energy for vacancy recombination
V_0	0.43 V	I-V fitting parameter

Fig. 7 depicts the transient waveforms of the proposed ternary RRAM cell. As the figure shows, three types of dual-phase writing operations ('1', '2', and '0') are performed. The first phase of each write operation initializes the R_{RRAM} to HRS value, and the second changes it to MRS or LRS values or leaves it unchanged. After each write process, a read operation is performed by pre-charging RBL to 1/2 V_{DD} and asserting RWL.

The voltage differences between all terminals of the write and read FinFETs are depicted in Fig.8. Based on the waveforms, the voltage differences are at most about 1V, which verifies the immunization of the FinFETs of the proposed ternary cell to the high voltage stress.

The delay, power, and energy consumption for the read and write operations of the proposed ternary RRAM cell and the ternary 1T1R cell are given in Table 4. As the results demonstrate, writing on the RRAM dissipates considerably more energy than reading from the RRAM, as changing the state of an RRAM through CF growth/dissolution takes more time and consumes more power.

As shown in Table 4, the delay, power, and energy in the pre-layout of the proposed cell are lower than in the post-layout, which attributes to the parasitic elements of the devices and interconnects extracted in the post-layout simulations. However, the differences are not significant due to the compact layout of the proposed cell. The power dissipation of the ternary 1T1R is lower than the proposed cell due to its fewer transistors, which is more significant in the write operation. However, the proposed design offers significantly faster and more energy-efficient read and write operations.

TABLE 4. Simulation results of the proposed cell and ternary 1T1R.

Parameters	Proposed ternary 3T1R cell				Proposed Ternary 1T1R cell			
	Pre-layout		Post-layout		Pre-layout		Post-layout	
	Write	Read	Write	Read	Write	Read	Write	Read
Delay	1.94ns	124ps	2.18ns	126ps	5.98ns	820ps	6.28ns	831ps
Power (μw)	37.8	16.71	38.6	16.72	14.57	10.75	14.68	10.78
Energy (fJ)	73.33	2.07	84.14	2.11	87.28	8.83	92.28	8.93

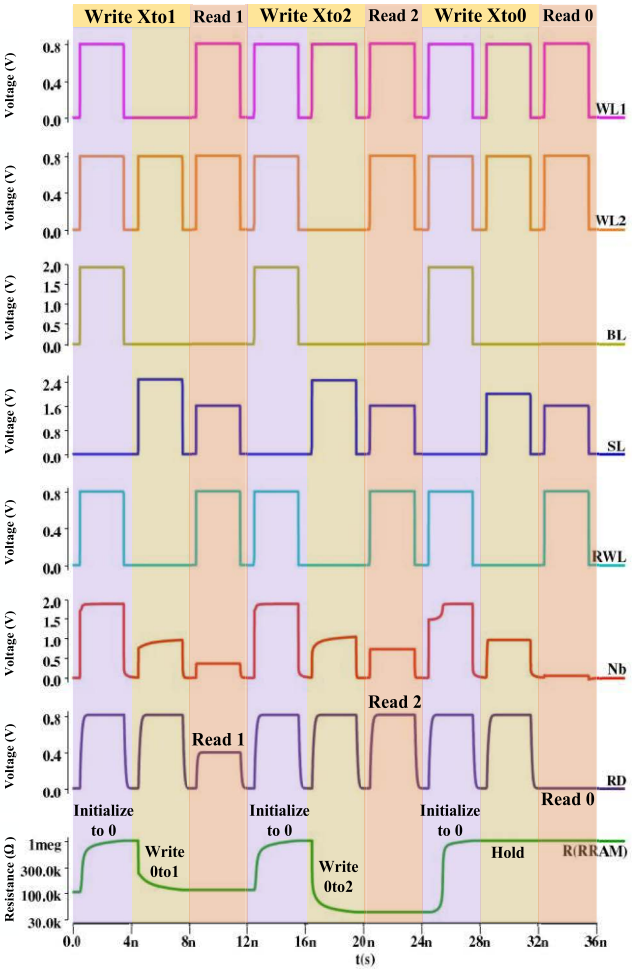


FIGURE 7. The transient waveforms of the proposed ternary RRAM cell.

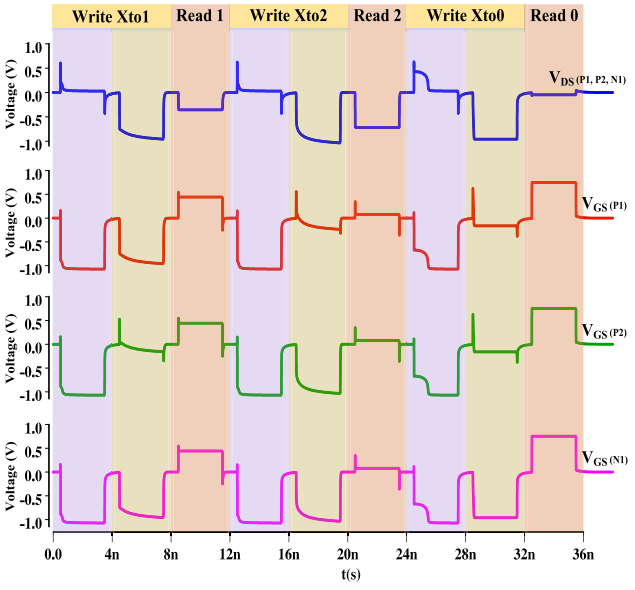


FIGURE 8. The voltage difference between the transistor terminals in the proposed cell in all operation modes.

B. PROCESS, TEMPERATURE, AND VOLTAGE VARIATIONS

To assess the functionality and performance of the proposed ternary RRAM cell in the presence of the inevitable PVT variations, extensive Monte-Carlo simulations with 1000 runs have been conducted considering the variations given in Table 5 with the Gaussian distribution at the 3σ level. It is worth mentioning that the FinFET critical process parameters include fin height, fin thickness, gate length, and gate oxide thickness. For the RRAM, the V_0, I_0, and γ_0 parameters are considered. Moreover, the temperature has been changed between $-30°$ C and $+70°$ C.

Our simulations demonstrate that the proposed ternary RRAM cell functions correctly with no failure, even in the presence of all PVT variations. In contrast, the ternary 1T1R cell has more than 20% failure in the presence of the same PVT variations.

Table 5 shows the impact of the PVT variations on the performance of the proposed ternary cell. According to the results, the effect of the variations of the RRAM parameters, especially γ_0, appears in the RRAM resistance and leads to write delay and write energy variations. Moreover, the overall variations have more influence on the read operation than the write operation mainly because of the voltage division occurring in the read operation, which is more sensitive to variations.

TABLE 5. The impact of the PVT variation on the performance of the proposed ternary RRAM cell.

Variations (at the ±3σ level)		Write power (μW)	Read power (μW)	Write delay (ns)	Read delay (ns)	Write energy (fJ)	Read energy (fJ)
Supply voltage variation (±10%)	Minimum	33.03	13.16	1.63	0.08	57.66	1.08
	Maximum	49.14	24.73	2.18	0.65	91.37	12.15
	Average	37.99	16.63	1.84	0.13	69.97	2.21
	Coefficient of variation (σ/μ)	6.6%	10.9%	3.7%	34%	7.9%	44%
FinFET variations (±10%)	Minimum	36.94	15.97	1.78	0.11	66.04	1.75
	Maximum	37.96	16.41	1.89	0.14	71.13	2.22
	Average	37.41	16.21	1.83	0.12	68.61	1.92
	Coefficient of variation (σ/μ)	0.4%	0.4%	1.0%	2.9%	1.1%	3.1%
RRAM variations (±20%)	Minimum	35.14	15.72	1.47	0.11	57.61	1.91
	Maximum	39.31	17.05	2.71	0.13	96.11	1.97
	Average	37.39	16.22	1.86	0.12	69.51	1.92
	Coefficient of variation (σ/μ)	1.6%	1.2%	9.6%	1%	8.1%	0.3%
Temperature (-30° C to +70° C)	Minimum	34.12	15.56	1.60	0.10	62.87	1.76
	Maximum	41.47	18.12	2.95	0.15	100.81	2.47
	Average	37.59	16.65	1.99	0.12	74.81	2.07
	Coefficient of variation (σ/μ)	2.8%	2.2%	9.1%	5.7%	8.4%	5.7%
All variations	Minimum	30.75	12.15	1.33	0.07	51.86	1.07
	Maximum	49.30	25.31	3.72	0.47	146.9	11.18
	Average	37.96	16.97	2.05	0.13	77.85	2.32
	Coefficient of variation (σ/μ)	7.7%	11.8%	15.6%	30.5%	15.8%	41%

Fig. 9 shows the influence of PVT variation on the performance parameters of the proposed ternary RRAM cell.

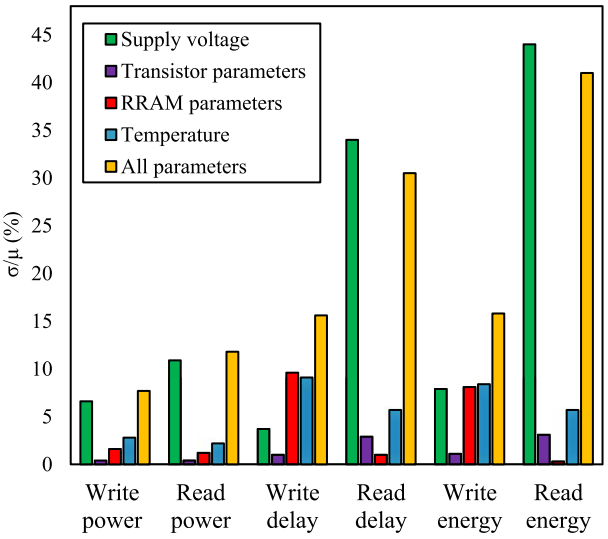


FIGURE 9. Performance parameters of the proposed ternary cell in the presence of PVT variation.

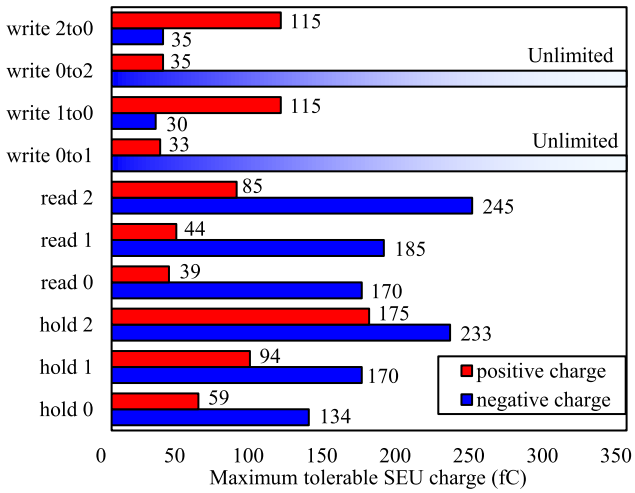


FIGURE 10. SEU tolerance of the proposed ternary cell in the presence of positive and negative SEU charges.

According to the results, the supply voltage variations affect the read delay and read energy but has a minor impact on the write delay and write energy. The RRAM variations significantly affect the write delay more than write power consumptions, and the read delay is less affected than the write delay as the RRAM resistance variation is more effective on the write operation (switching of the RRAM's state) than the read operation.

C. TERNARY RRAM CELL SEU TOLERANCE SIMULATIONS

We have considered charge injection based on the model presented in [37] to evaluate the SEU tolerance of the proposed ternary RRAM cell. This model operates by an exponential current source modeled as

$$I_{inj}(t) = KQ_{inj}\sqrt{\frac{t}{T}}\,e^{(-\frac{t}{T})} \tag{5}$$

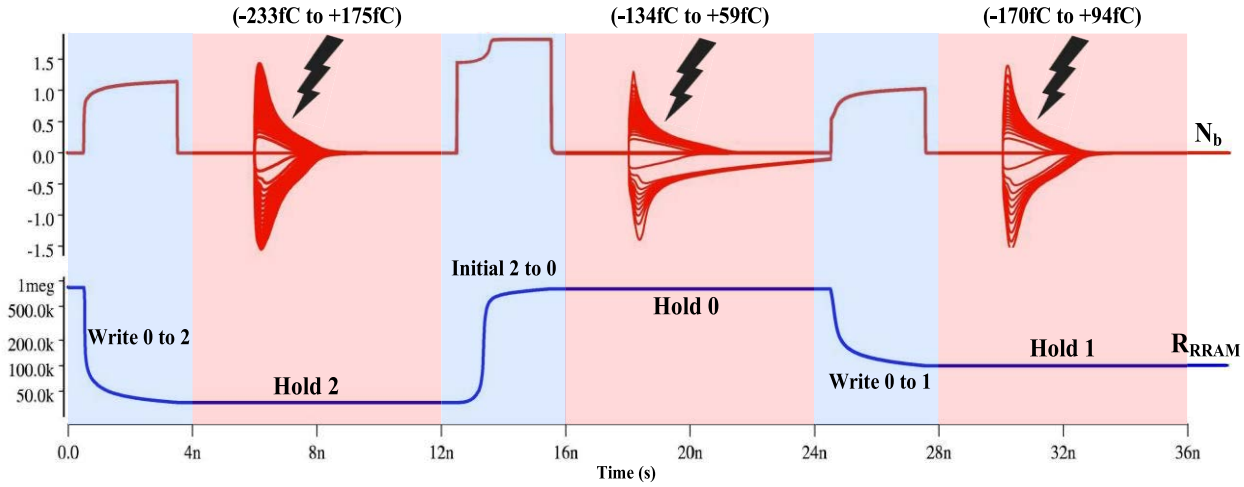


FIGURE 11. The transient effect of SEU injection on the node Nb in the proposed cell in the hold mode considering different Q_{inj} charges.

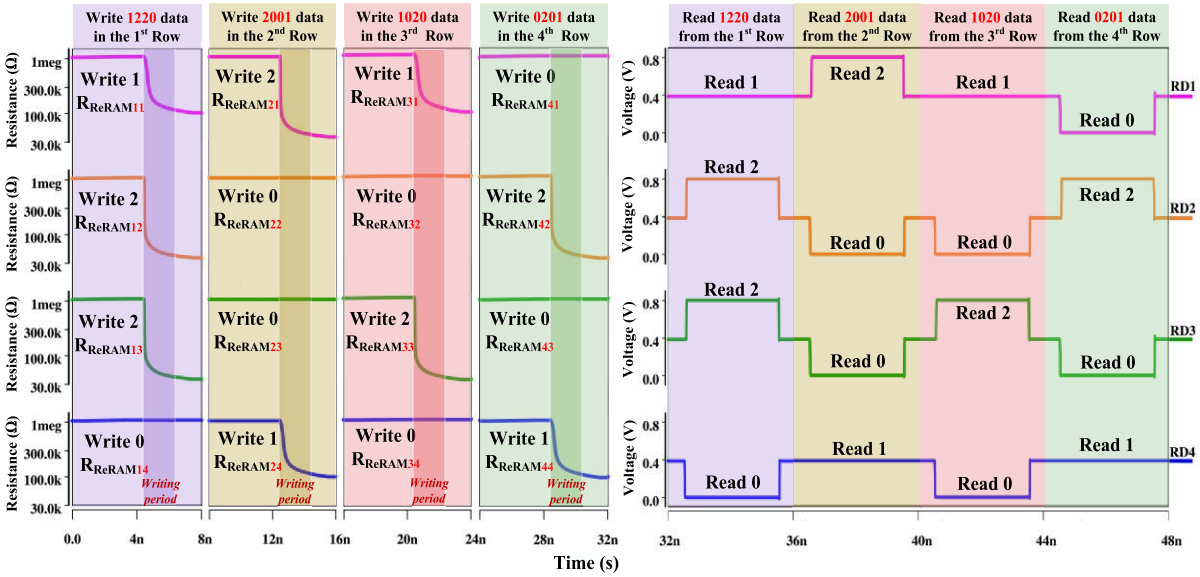


FIGURE 12. The transient waveform of the 4 × 4 memory array in row-write and row-read operation.

where Q_{inj} is the injected amount of charge during radiation strike, K is a constant to make pulse shape integrate to unity, and T is the pulse duration constant (300ps).

Since the striking ionizing particles in SEU are in the order of only a few femtocoulombs charge [19], immunity to large particles with more than a 20fC charge is high enough to confirm the sufficient SEU tolerant capacity [38]. In the case of the proposed ternary RRAM cell, we have applied the charge injection on N_b as the most sensitive node of the cell. Accordingly, the SEU pulses with positive and negative charge amounts are applied to this critical node. These charges have been applied in the read, write, and hold operation modes.

Fig. 10 shows the SEU tolerance of the proposed ternary RRAM cell facing positive and negative SEU charges in each operation mode. Any charge amount in Fig. 10 reveals the maximum injected charge that does not endanger the functionality of the proposed cell. According to the results, the maximum tolerable SEU charge for the hold, read, and write modes are 59fC, 39fC, and 30fC, respectively. The stored HRS state in the RRAM has more susceptibility to SEU in both read and hold modes as the RRAM has its high resistance value because the exponential current can make a voltage pulse with a higher amplitude, which can corrupt the cell's functionality.

For instance, the transient effect of the SEU injection on the N_b node in all three hold conditions is illustrated in Fig. 11. According to the results, by striking high-energy particles, the R_{RRAM} remains unchanged, confirming the potential of the proposed cell in tolerating massive volumes of particle strikes in the hold mode.

D. TERNARY RRAM MEMORY ARRAY SIMULATION

This subsection evaluates the functionality of the proposed ternary memory array architecture. Fig. 12 shows the transient waveform of the 4 × 4 memory array, which authenticates the functionality of the proposed RRAM array. All the cells of the memory array have already been initialized to HRS. Four dual-phase write operations are performed on each row of the proposed array in consecutive 8ns periods, and all four rows of the ternary array are written to arbitrary data. After writing the data in each row, the written data is read. Four read operations are performed on each row of the proposed array in consecutive 4ns periods.

The delay, power consumption, and energy dissipation for each of the read and write modes of the 4 × 4 and 16 × 16 array are tabulated in Table 6. Like the performance results of the proposed cell, writing on the RRAM array demands considerably higher energy than reading data from the RRAM array as more power and time are demanded to change the RRAM's resistance. Moreover, due to the compact layout of the arrays, the performance parameter differences are not quite significant.

TABLE 6. Simulation results of the proposed ternary arrays (4 × 4 and 16 × 16).

Parameters	4×4 Array				16×16 Array			
	Pre-layout		Post-layout		Pre-layout		Post-layout	
	Write	Read	Write	Read	Write	Read	Write	Read
Delay	2.31ns	129ps	2.81ns	132ps	2.44ns	132ps	3.46ns	136ps
Power (μw)	135.1	59.1	137.0	59.1	518.7	240.9	525.3	241.2
Energy (fJ)	312.08	7.62	384.9	7.8	1265.6	31.7	1817.5	32.8

FIGURE 13. (a) original (b) binary (c) ternary.

In application areas such as feature extraction, pattern recognition, and machine vision, increasing the images' gray level (binary to ternary) to eliminate data loss is an important issue. Moreover, the memory unit is one of the most widely used and essential units in each digital system. Accordingly, to better evaluate the performance of the proposed design, we have utilized ternary memory arrays based on the proposed 3T1R cell for storing a 512 × 512 ternary image (see Fig. 13(c)). To this end, each image pixel is translated to a ternary value (based on the desired ternary thresholds) and is stored in the memory. Then the image is read from memory. The energy consumed for writing the image in memory and then reading it from memory is totally 19nJ.

V. CONCLUSION

This paper proposes a hybrid RRAM/FinFET nonvolatile ternary memory cell and its corresponding array architecture. The proposed nonvolatile ternary memory cell is a 3T1R structure that can tolerate the striking of high-energy particles without any malfunction.

Moreover, both read and write operations of the proposed array are isolated from each other, causing enhanced performance and can be a worthy characteristic for ternary logic-in-memory (LIM) applications. Our extensive post-layout simulations based on the 7nm FinFET technology authenticate that the proposed RRAM/FinFET-based ternary cell functions precisely during the read and write operations, even in the presence of PVT variations and massive radiations. Consequently, the overall technical evaluations of this paper prove that RRAM/FinFET hybrid is a long-lasting candidate for ternary memory design and other perspectives like LIM implementations. Extending the application of this hybrid nonvolatile ternary memory structure in momentous areas such as in-memory computation and neural networks can be considered future work.

REFERENCES

[1] E. Dubrova, "Multiple-valued logic in VLSI: Challenges and opportunities," in *Proc. NORCHIP*, vol. 99, 1999, pp. 340–350.

[2] F. Behbahani, M. K. Q. Jooq, M. H. Moaiyeri, and K. Tamersit, "Leveraging negative capacitance CNTFETs for image processing: An ultra-efficient ternary image edge detection hardware," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 12, pp. 5108–5119, Dec. 2021, doi: 10.1109/TCSI.2021.3112798.

[3] S. Basu, R. E. Bryant, G. De Micheli, T. Theis, and L. Whitman, "Nonsilicon, non-von Neumann computing—Part I," *Proc. IEEE*, vol. 107, no. 1, pp. 11–18, Jan. 2019, doi: 10.1109/JPROC.2018.2884780.

[4] S. Kim, S.-Y. Lee, S. Park, K. R. Kim, and S. Kang, "A logic synthesis methodology for low-power ternary logic circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 9, pp. 3138–3151, Sep. 2020, doi: 10.1109/TCSI.2020.2990748.

[5] M. K. Q. Jooq, M. H. Moaiyeri, and K. Tamersit, "Ultra-compact ternary logic gates based on negative capacitance carbon nanotube FETs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 6, pp. 2162–2166, Jun. 2021, doi: 10.1109/TCSII.2020.3047265.

[6] F. Zahoor, T. Z. A. Zulkifli, F. A. Khanday, and S. A. Z. Murad, "Carbon nanotube and resistive random access memory based unbalanced ternary logic gates and basic arithmetic circuits," *IEEE Access*, vol. 8, pp. 104701–104717, 2020, doi: 10.1109/ACCESS.2020.2997809.

[7] Hurst, "Multiple-valued logic—Its status and its future," *IEEE Trans. Comput.*, vol. C-33, no. 12, pp. 1160–1179, Dec. 1984, doi: 10.1109/TC.1984.1676392.

[8] R. A. Jaber, A. Kassem, A. M. El-Hajj, L. A. El-Nimri, and A. M. Haidar, "High-performance and energy-efficient CNFET-based designs for ternary logic circuits," *IEEE Access*, vol. 7, pp. 93871–93886, 2019, doi: 10.1109/ACCESS.2019.2928251.

[9] W. Liu, Y. Sun, W. He, and Q. Wang, "Design of ternary logic-in-memory based on memristive dual-crossbars," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5, doi: 10.1109/ISCAS51556.2021.9401308.

[10] S. Jain, S. K. Gupta, and A. Raghunathan, "TiM-DNN: Ternary in-memory accelerator for deep neural networks," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 28, no. 7, pp. 1567–1577, Jul. 2020, doi: 10.1109/TVLSI.2020.2993045.

[11] Y. Shrivastava and T. K. Gupta, "Design of high-speed low variation static noise margin ternary S-RAM cells," *IEEE Trans. Device Mater. Rel.*, vol. 21, no. 1, pp. 102–110, Feb. 2021, doi: 10.1109/TDMR.2021.3058159.

[12] V. G. Oklobdzija and R. C. Dorf, *The Computer Engineering Handbook: Electrical Engineering Handbook*. Boca Raton, FL, USA: CRC Press, 2001.

[13] S. Yu, "Resistive random access memory (RRAM)," *Synthesis Lect. Emerg. Eng. Technol.*, vol. 2, no. 5, pp. 1–79, 2016.

[14] S. Angizi, Z. He, A. Chen, and D. Fan, "Hybrid spin-CMOS polymorphic logic gate with application in in-memory computing," *IEEE Trans. Magn.*, vol. 56, no. 2, pp. 1–15, Feb. 2020, doi: 10.1109/TMAG.2019.2955626.

[15] S. S. Ensan, S. Ghosh, S. Motaman, and D. Weast, "Addressing resiliency of in-memory floating point computation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 9, pp. 1–12, Sep. 2022, doi: 10.1109/TVLSI.2022.3170542.

[16] S. S. Ensan and S. Ghosh, "ReLOPE: Resistive RAM-based linear first-order partial differential equation solver," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 29, no. 1, pp. 237–241, Jan. 2021, doi: 10.1109/TVLSI.2020.3035769.

[17] Z. Li, P.-Y. Chen, H. Xu, and S. Yu, "Design of ternary neural network with 3-D vertical RRAM array," *IEEE Trans. Electron Devices*, vol. 64, no. 6, pp. 2721–2727, Jun. 2017, doi: 10.1109/TED.2017.2697361.

[18] Y. Halawani, B. Mohammad, M. Abu-Lebdeh, M. Al-Qutayri, and S. F. Al-Sarawi, "ReRAM-based in-memory computing for search engine and neural network applications," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 9, no. 2, pp. 388–397, Jun. 2019, doi: 10.1109/jetcas.2019.2909317.

[19] F. Razi, M. H. Moaiyeri, and R. Rajaei, "Design of an energy-efficient radiation-hardened non-volatile magnetic latch," *IEEE Trans. Magn.*, vol. 57, no. 1, pp. 1–10, Jan. 2021, doi: 10.1109/TMAG.2020.3033229.

[20] M. Rostami and K. Mohanram, "Dual-V_{th} independent-gate FinFETs for low power logic circuits," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 30, no. 3, pp. 337–349, Feb. 2011, doi: 10.1109/TCAD.2010.2097310.

[21] F. Sabetzadeh, M. H. Moaiyeri, and M. Ahmadinejad, "A majority-based imprecise multiplier for ultra-efficient approximate image multiplication," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 11, pp. 4200–4208, Nov. 2019, doi: 10.1109/TCSI.2019.2918241.

[22] M. U. Mohammed, A. Nizam, L. Ali, and M. H. Chowdhury, "FinFET based SRAMs in sub-10 nm domain," *Microelectron. J.*, vol. 114, Aug. 2021, Art. no. 105116, doi: 10.1016/j.mejo.2021.105116.

[23] C. Qi, L. Xiao, J. Guo, and T. Wang, "Low cost and highly reliable radiation hardened latch design in 65 nm CMOS technology," *Microelectron. Rel.*, vol. 55, no. 6, pp. 863–872, May 2015, doi: 10.1016/j.microrel.2015.03.014.

[24] M. Moghaddam, M. H. Moaiyeri, and M. Eshghi, "Design and evaluation of an efficient Schmitt trigger-based hardened latch in CNTFET technology," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 1, pp. 267–277, Mar. 2017, doi: 10.1109/TDMR.2017.2665780.

[25] R. Rajaei, "Radiation-hardened design of nonvolatile MRAM-based FPGA," *IEEE Trans. Magn.*, vol. 52, no. 10, pp. 1–10, Oct. 2016, doi: 10.1109/TMAG.2016.2578278.

[26] P.-Y. Chen and S. Yu, "Compact modeling of RRAM devices and its applications in 1T1R and 1S1R array design," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 4022–4028, Dec. 2015, doi: 10.1109/TED.2015.2492421.

[27] M. Huang, X. Wang, G. Zhao, P. Coquet, and B. Tay, "Design and implementation of ternary logic integrated circuits by using novel two-dimensional materials," *Appl. Sci.*, vol. 9, no. 20, p. 4212, Oct. 2019, doi: 10.3390/app9204212.

[28] M. H. Moaiyeri, A. Doostaregan, and K. Navi, "Design of energy-efficient and robust ternary circuits for nanotechnology," *IET Circuits, Devices, Syst.*, vol. 5, no. 4, pp. 285–296, Jul. 2011, doi: 10.1049/iet-cds.2010.0340.

[29] C. Vudadha, A. Surya, S. Agrawal, and M. B. Srinivas, "Synthesis of ternary logic circuits using 2:1 multiplexers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 12, pp. 4313–4325, Jun. 2018, doi: 10.1109/TCSI.2018.2838258.

[30] Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, and T. Mikawa, "Highly reliable TaO_x ReRAM and direct evidence of redox reaction mechanism," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4, doi: 10.1109/IEDM.2008.4796676.

[31] M.-J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y.-B. Kim, C.-J. Kim, D. H. Seo, S. Seo, U.-I. Chung, I.-K. Yoo, and K. Kim, "A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta_2O_{5-X}/TaO_{2-X} bilayer structures," *Nature Mater.*, vol. 10, no. 8, pp. 625–630, Aug. 2011, doi: 10.1038/nmat3070.

[32] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, May 2008, doi: 10.1038/nature06932.

[33] H. Akinaga and H. Shima, "Resistive random access memory (ReRAM) based on metal oxides," *Proc. IEEE*, vol. 98, no. 12, pp. 2237–2251, Dec. 2010, doi: 10.1109/JPROC.2010.2070830.

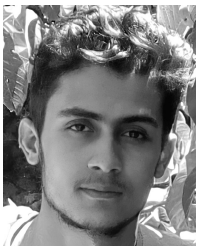
[34] S. Shirinzadeh and R. Drechsler, "Logic synthesis for in-memory computing using resistive memories," in *Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI)*, Jul. 2018, pp. 375–380, doi: 10.1109/ISVLSI.2018.00075.

[35] Z. Jiang, S. Yu, Y. Wu, J. H. Engel, X. Guan, and H.-S.-P. Wong, "Verilog—A compact model for oxide-based resistive random access memory (RRAM)," in *Proc. Int. Conf. Simul. Semiconductor Processes Devices (SISPAD)*, Sep. 2014, pp. 41–44, doi: 10.1109/SISPAD.2014.6931558.

[36] L. T. Clark, V. Vashishtha, L. Shifren, A. Gujja, S. Sinha, B. Cline, C. Ramamurthy, and G. Yeric, "ASAP7: A 7-nm FinFET predictive process design kit," *Microelectron. J.*, vol. 53, pp. 105–115, Jul. 2016, doi: https://doi.org/10.1016/j.mejo.2016.04.006.

[37] L. B. Freeman, "Critical charge calculations for a bipolar SRAM array," *IBM J. Res. Develop.*, vol. 40, no. 1, pp. 119–129, Jan. 1996, doi: 10.1147/rd.401.0119.

[38] J. M. Trippe, R. A. Reed, R. A. Austin, B. D. Sierawsk, L. W. Massengill, R. A. Weller, K. M. Warren, R. D. Schrimpf, B. Narasimham, B. Bartz, and D. Reed, "Predicting muon-induced SEU rates for a 28-nm SRAM using protons and heavy ions to calibrate the sensitive volume model," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 2, pp. 712–718, Dec. 2018, doi: 10.1109/TNS.2017.2786585.



ARAM YOUSEFI was born in Sanandaj, Kurdistan, Iran, in 1996. He received the B.S. degree (Hons.) in electronic engineering from the University of Kurdistan (UOK), Kurdistan, in 2019. He is currently pursuing the M.Sc. degree in digital electronic engineering with Shahid Beheshti University (SBU), Tehran, Iran. His main research interests include low-power VLSI circuit/memory design, beyond-CMOS emerging technologies, multi-valued logic design, and in-memory computing.

NIMA ESLAMI was born in Tehran, Iran, in 1994. He received the M.Sc. degree (Hons.) in digital electronic engineering from Science and Research Branch, Islamic Azad University, Tehran, in 2019. He is currently pursuing the Ph.D. degree in digital electronic engineering with Shahid Beheshti University, Tehran. His research interests include low-power and high-performance VLSI design, memory design, in-memory computing, approximate computing, and multi-valued logic design.

MOHAMMAD HOSSEIN MOAIYERI (Senior Member, IEEE) received the Ph.D. degree in computer engineering from Shahid Beheshti University, Tehran, Iran, in 2012. He is currently an Assistant Professor with the Faculty of Electrical Engineering, Shahid Beheshti University. His research interests include VLSI design for beyond-CMOS emerging devices, low-power VLSI design, and mixed-signal integrated circuits. He has served as an Associate Editor for IEEE Access and *Circuits, Systems, and Signal Processing* journals.