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RESEARCH ARTICLE

Flexible Parylene C-Based RRAM Array for Neuromorphic Applications

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ABSTRACT Resistive random-access memory (RRAM) has been explored to implement neuromorphic systems to accelerate neural networks. In this study, an RRAM crossbar array using parylene C (PPXC) as both a resistive switching layer and substrate was fabricated. PPXC is a flexible and transparent polymer with excellent chemical stability and biocompatibility. We studied PPXC-based RRAM devices with Ti/PPX-C/Cu and Cu/PPX-C/Ti structures. Devices with the Ti/PPX-C/Cu structure offer stable electrical and mechanical characteristics, such as a low set voltage of <1 V, good retention time of $>10^4$ s, endurance cycles of >300, conductance ON/OFF ratio >10, and can withstand >350 mechanical bending cycles. Additionally, the switching and conduction mechanisms of the devices were carefully investigated by analyzing their electrical, structural, and chemical properties. Finally, we demonstrated the feasibility of the fabricated RRAM array for neuromorphic applications through system-level simulations using the Modified National Institute of Standards and Technology database. The simulation results reflecting the variations of realistic devices demonstrated that the artificial neural network developed using the PPXC-based RRAM array works satisfactorily in pattern recognition tasks. The findings of this study can aid in the development of future wearable neuromorphic systems.

INDEX TERMS Neuromorphic, RRAM, parylene C, artificial neural network, memristor, flexible neuromorphic electronics.

I. INTRODUCTION

The human brain processes data at approximately 100 petaflops while consuming less than 20 W of power. Inspired by the human brain, the field of neuromorphic computing and machine learning has received significant attention as a key technology candidate that can overcome the limitations of conventional digital computing systems [1], [2], [3], [4]. Conventional von Neumann architecture-based computing systems operate sequentially with physically separated central processing units (CPUs) and memory units. However, neuromorphic systems operate in an extensively parallel manner based on the arrangement of collocated neurons and synapses. This collocation helps mitigate the von Neumann bottleneck and avoid data access via buses, which consume a considerable amount of energy compared to the compute energy required. Neuromorphic systems can perform vector-matrix multiplication (VMM), which is the core computation method of machine learning algorithms, in parallel inside an array of synapse devices. Several memory devices such as static random access memory (RAM), phase-change memory, spin-transfer torque RAM, floating gate memory, charge trap flash memory, and resistive RAM (RRAM) have been proposed to emulate the functionalities of synapses [5], [6], [7], [8], [9], [10]. Among these, RRAM-based synapse devices have a simple structure comprising

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two terminals, low-power operation, and fast switching speed [11], [12], [13], [14], [15], [16].

In this study, we demonstrate a flexible RRAM-based synapse array developed using an organic material called parylene C (PPXC). PPXC is a flexible, transparent, and Food and Drug Administration approved polymer material that enables the development of flexible neuromorphic electronics for next-generation wearable computing, soft robotics, and neuroprosthetics. Although several studies on RRAM with PPXC switching layers have been conducted, most of them were conducted at a single-device level [17], [18], [19], [20], [21], [22], [23], [24]. However, the applications of neuromorphic computing and machine learning require a crossbar array topology for integration into neuromorphic systems. In some studies [25], [26], [27], [28], [29], [30], PPXC-based RRAM devices were implemented in a crossbar array architecture. However, no research has been conducted on the detailed applications of neuromorphic systems with crossbar arrays on flexible substrates. In this study, a flexible and transparent PPXC-based RRAM array suitable for neuromorphic applications is demonstrated. The fabricated RRAM devices exhibited stable memory characteristics such as low-power operation, good retention time of $>10^4$ s, endurance cycles of >300, conductance ON/OFF ratio of >10, and could withstand >350 mechanical bending cycles. Additionally, to further explore the application potential of machine learning, pattern recognition based on a binary neural network was conducted using the Modified National Institute of Standards and Technology (MNIST) database.

II. EXPERIMENTS

The two RRAM device structures, Ti/PPX-C/Cu and Cu/PPX-C/Ti, were fabricated in a crossbar array structure of 20×20 devices, as shown in Fig. 1(a). Each device had an area of 10×10 μm^2. The fabrication process is as follows: First, 10 μm thick PPXC (OBT-PC300) was deposited via polymer chemical vapor deposition (CVD) onto an SiO_2/Si wafer for application in flexible devices. Note that PPXC can be deposited as thin, conformal, and pinhole-free films using this parylene CVD method [31]. Thereafter, oxygen plasma treatment was applied to the surface of PPXC to enhance the adhesion between PPXC and metal. The oxygen gas of 100 sccm, power of 100 W, and time of 5 sec were set as the treatment condition.

Next, the bottom electrode (BE) was deposited via e-beam evaporation (KVE-E2000 Series, Korea Vacuum Tech) followed by a lift-off process. Thereafter, an approximately 30 nm thick PPXC layer was deposited via polymer CVD at room temperature and 11 mTorr and treated with oxygen plasma under the same conditions as above. Finally, the top electrode (TE) was molded via e-beam evaporation followed by a lift-off process. Additionally, the 30 nm PPXC layer on the BE was removed through reactive ion etching (CUTE, FEMTO SCIENCE) to open the pad. Fig. 1(b) shows the delamination result of the RRAM array fabricated using the SiO_2/Si substrate via simple immersion in deionized (DI) water.

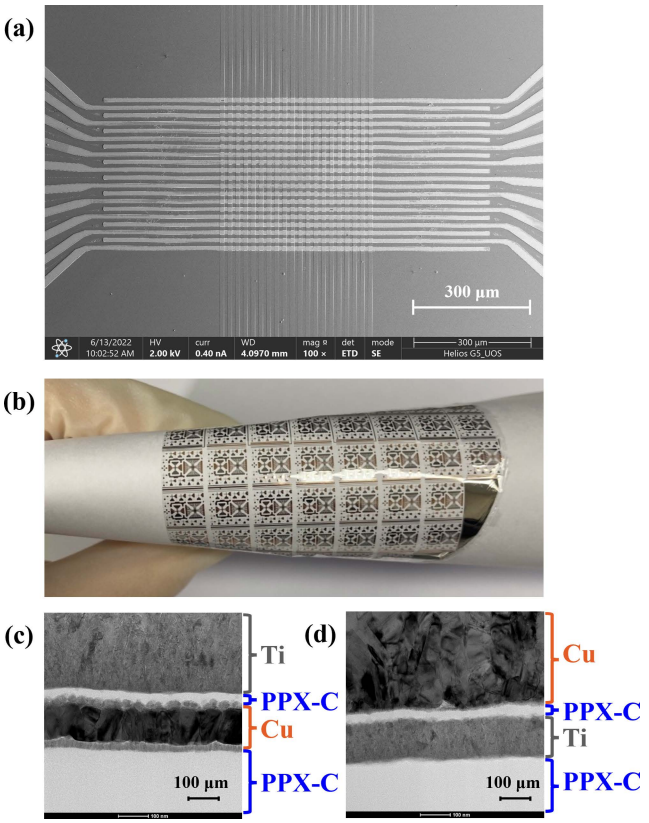

FIGURE 1. (a) Scanning electron microscopy (SEM) image of a crossbar array comprising RRAMs with the Ti/PPX-C/Cu structure. (b) Illustration of flexible RRAM crossbar arrays with a Ti/PPX-C/Cu structure. Cross-sectional transmission electron microscopy (TEM) images of as-fabricated RRAM devices with (c) Ti/PPX-C/Cu and (d) Cu/PPX-C/Ti structures.

Cross-sectional transmission electron microscopy (TEM) images of the devices with Ti/PPX-C/Cu and Cu/PPX-C/Ti structures are shown in Figs. 1(c) and (d), respectively.

The switching characteristics of the devices were measured using a Keithley 4200 semiconductor parameter analyzer at room temperature. To analyze the device configurations, a focused ion beam (FEI, Helios G5 UC), TEM (Talos F200X), and energy-dispersive X-ray spectroscopy (EDS) were used.

III. RESULTS AND DISCUSSION

A. CHARACTERISTICS OF THE PPX-C RRAM ARRAY

The memory characteristics of the devices with Ti/PPX-C/Cu and Cu/PPX-C/Ti structures are shown in Figs. 2(a) and (b), respectively. In both the devices, a sweeping voltage was applied to the Cu electrode and the Ti electrode was connected to the ground. Initially, the molding process was performed by applying a positive voltage to the Cu electrode and consequently, typical bipolar RRAM switching was observed. The SET process, wherein a device switches from a high- resistance state (HRS) to a low-resistance state (LRS), occurs at a positive bias, whereas the reset process, wherein the device switches back to the HRS, occurs at a negative bias. During the SET operation, the conduction current

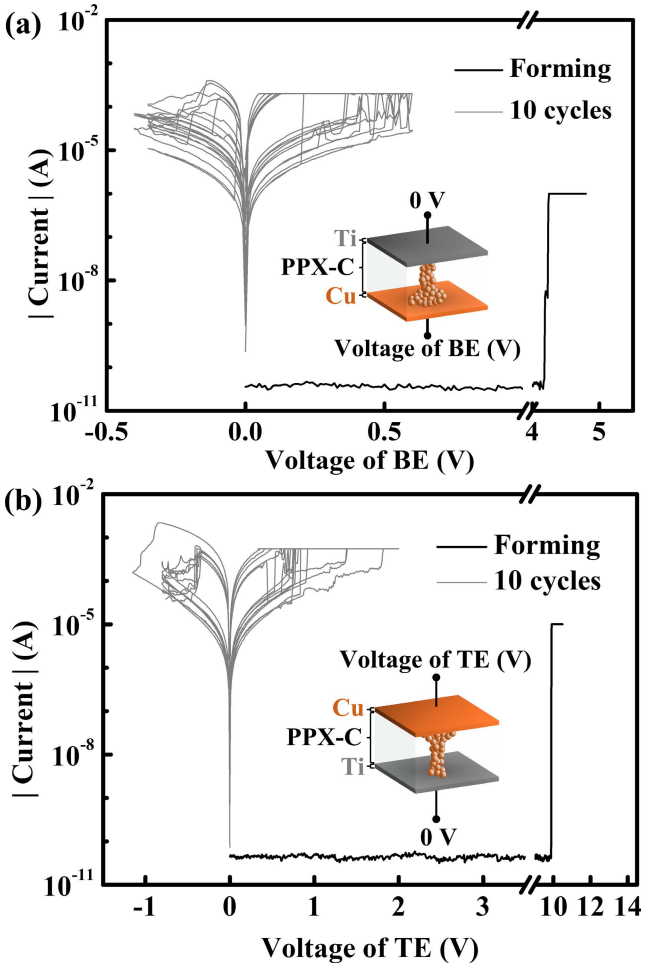

FIGURE 2. Current-voltage characteristics (I–V) of 10 consecutive switching cycles for RRAM devices with (a) Ti/PPX-C/Cu and (b) Cu/PPX-C/Ti structures.

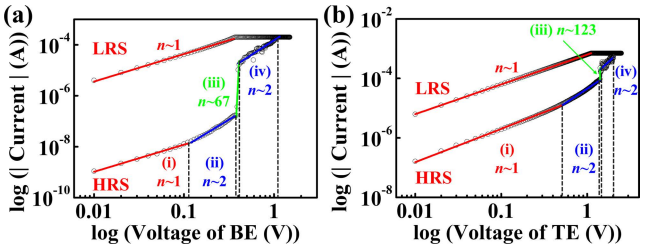

FIGURE 3. Fitting results (I–V^n) of the current-voltage characteristics of RRAM devices with (a) Ti/PPX-C/Cu and (b) Cu/PPX-C/Ti structures. The Ohmic conduction in the low resistance state (LRS) and space-charge limited current (SCLC) in the high resistance state (HRS) can be observed.

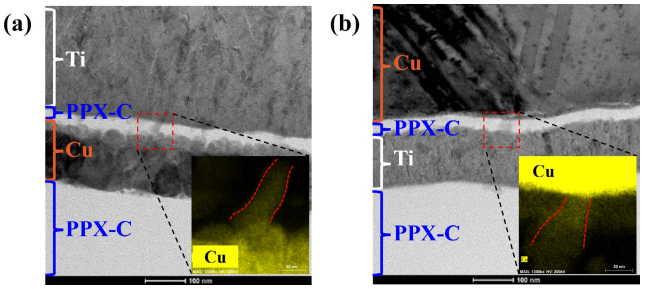

FIGURE 4. Cross-sectional TEM images of RRAM devices in LRS with (a) Ti/PPX-C/Cu and (b) Cu/PPX-C/Ti structures.

was limited using a compliance current of 0.2 and 0.7 mA for the devices with Ti/PPX-C/Cu and Cu/PPX-C/Ti structures, respectively, to protect them from a permanent breakdown. Additionally, the compliance current prevents reset failure that occurs owing to the overgrowth of the conductive filament.

The conduction mechanisms of the devices can be analyzed using the I-V curve on the logarithmic scale and the fitting results of both devices are shown in Fig. 3. The LRS curves are well fitted at slope 1, indicating an ohmic conduction mechanism. In contrast, in the HRS curves, four distinct regions are correlated to the sweeping voltages, which can be described by the space-charge limited current (SCLC) model [32], [33], [34], [35], [36]. In the low-voltage region (i), the I-V characteristics follow Ohm's law, which implies that the injected carrier density is lower than that of the thermally generated intrinsic carriers and the injected carriers redistribute themselves. In region (ii), the injected carriers dominate the thermally generated carriers because the transit time of the injected carrier is insufficient for redistribution (dielectric relaxation). The traps are filled and a space charge emerges. In region (iii), the subsequently injected carriers are free to move after all traps are filled. Consequently, the current rapidly jumps from a low trap-limited current to a high trap-free SCLC. In the high-voltage region (iv), the current is fully controlled by the space charge. The trap-free behavior results in a square law dependence of the current ($I \sim V^2$, Child's law).

Most previous studies [22], [23], [24], [25], [26], [27] on RRAM devices with a PPX-based switching layer reported that resistive switching occurs owing to the formation of a conducting filament, which is a metal bridge comprising atoms from the electrode. In the proposed devices, Cu atoms formed conducting filaments because of electrochemical metallization [37]. To confirm the switching mechanism, TEM investigations on the LRS of the devices were performed. The EDS image of the Cu filaments, shown in Fig. 4, depicts the formation of a Cu conducting filament between the BE and TE.

The forming voltage (V_{FORMING}), set voltage (V_{SET}), and reset voltage (V_{RESET}) distributions of 31 devices are depicted in Fig. 5 through box plots. Their average values (μ) and standard deviations (σ) are listed in Table 1. The average V_{FORMING}, V_{SET}, and $|V_{\mathrm{RESET}}|$ values of RRAM devices with the Ti/PPX-C/Cu structure were lower than those with the Cu/PPX-C/Ti structure. This is attributed to the native CuO layer formed between the PPXC and Cu in the Ti/PPX-C/Cu structure. We confirmed the existence of a native CuO layer in the Ti/PPX-C/Cu structure by analyzing its selected area diffraction pattern, as shown in Fig. 6. The fast Fourier transform (FFT) result in Fig. 6(b) can be attributed to the monoclinic phase of CuO with lattice spacing values of 0.251, 0.251, and 0.235 nm for the $(\bar{1}\bar{1}1)$, $(1\bar{1}1)$, and (200) planes, respectively. Because the Cu-O bond energy in CuO

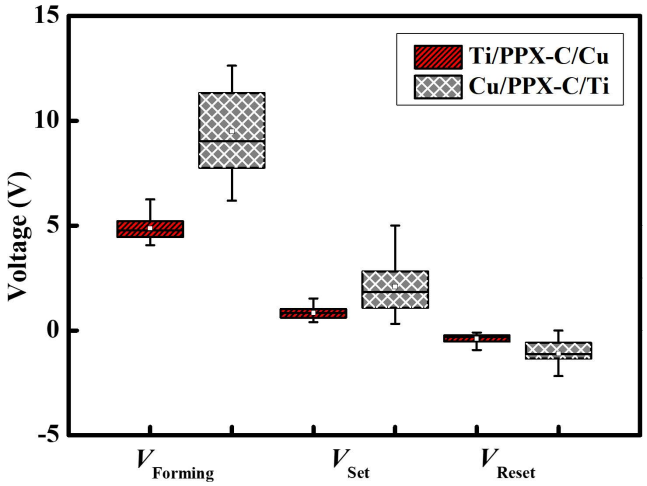

FIGURE 5. Statistical results of V_{Set}, V_{Reset}, and $V_{Forming}$ in a box plot for RRAM devices with Ti/PPX-C/Cu and Cu/PPX-C/Ti structures.

TABLE 1. Device-to-device Statistical values of switching voltage for two RRAM types.

	Ti/PPX-C/Cu			Cu/PPX-C/Ti		
	$V_{Forming}$	V_{Set}	V_{Reset}	$V_{Forming}$	V_{Set}	V_{Reset}
Average (μ) (V)	4.9	0.8	-0.4	9.5	2.1	-1.1
Standard deviation (σ) (V)	0.6	0.3	0.2	1.9	1.2	0.7
V_{Max}-V_{Min} (V)	2.2	1.1	1.1	6.4	4.7	2.9
Variation (σ/(V_{Max}-V_{Min})) (%)	25.3	24.2	22.2	29.4	25.6	24.2

(∼1.5 eV) is lower than the Cu-Cu metallic bond energy (∼2.0 eV), copper ions (Cu^{2+}) can be more easily supplied from CuO and diffused into the PPXC layer than the Cu metal [38], [39], [40], [41]. Additionally, the CuO layers of the devices with the Ti/PPX-C/Cu structure were rougher than the Cu layers of those with the Cu/PPX-C/Ti structure, as shown in Fig. 4. Consequently, the concentrated electric field at the protruding region of the CuO layer could enhance the field emission, promote the release of Cu ions, and limit the formation of conducting filaments. Therefore, RRAM devices with the Ti/PPX-C/Cu structure and a native CuO layer exhibited lower $V_{FORMING}$, V_{SET}, and $|V_{RESET}|$ values than those with the Cu/PPX-C/Ti structure.

Fig. 7 shows the cycling test results of the devices with the Ti/PPX-C/Cu and Cu/PPX-C/Ti structures. The device with the Ti/PPX-C/Cu structure could be operated successfully for more than 270 cycles under a DC sweep, as depicted in Fig. 7(a). In contrast, the one with the Cu/PPX-C/Ti structure achieved 18 cycles of resistive switching, as shown in Fig. 7(b).

This is possibly because the reset current of the device with the Cu/PPX-C/Ti structure (∼2 mA) was larger than that

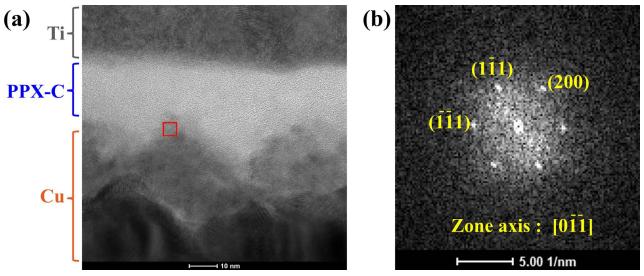

FIGURE 6. (a) Cross-sectional TEM image of a pristine RRAM device with the Ti/PPX-C/Cu structure. The red solid box denotes the region in which we performed a fast Fourier transform (FFT). (b) FFT image of the solid red box in (a).

TABLE 2. Device-to-device Statistical values of HRS and LRS conductance for two RRAM types.

	Ti/PPX-C/Cu		Cu/PPX-C/Ti	
	G_{LRS}	G_{HRS}	G_{LRS}	G_{HRS}
Average (μ) (μS)	890	20	410	20
Standard deviation (σ) (μS)	250	20	220	30
G_{Max}-G_{Min} (μS)	1,260	80	870	80
Variation (σ/(G_{Max}-G_{Min})) (%)	20	20	30	30

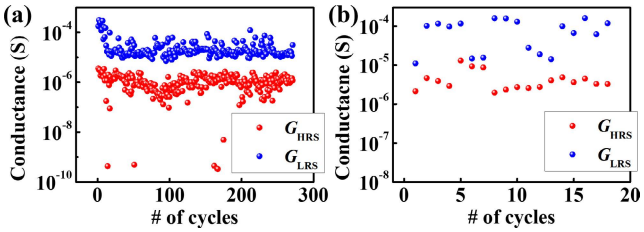

FIGURE 7. DC endurance characteristics of resistive switching in RRAM devices with (a) Ti/PPX-C/Cu and (b) Cu/PPX-C/Ti structures.

of the device with the Ti/PPX-C/Cu structure (∼0.7 mA). Such a large reset current can damage the PPXC switching layer and degrade the endurance performance of the device [42], [43].

The LRS conductance (G_{LRS}) and HRS conductance (G_{HRS}) distributions of the 73 devices with the Ti/PPX-C/Cu structure and 31 devices with the Cu/PPX-C/Ti structure are shown in Fig. 8. The average and standard deviation values of G_{LRS} and G_{HRS} with a read voltage of 0.1 V are listed in Table 2. The coefficient of variance (σ/μ) for the G_{LRS} of the device with the Ti/PPX-C/Cu structure was smaller than that of the device with the Cu/PPX-C/Ti structure. The improved uniformity of the devices with the Ti/PPX-C/Cu structure can be attributed to their low-voltage switching operation and geometric confinement of the conducting filaments.

The retention characteristics of the device with the Ti/PPX-C/Cu structure are shown in Fig. 9(a). Retention time

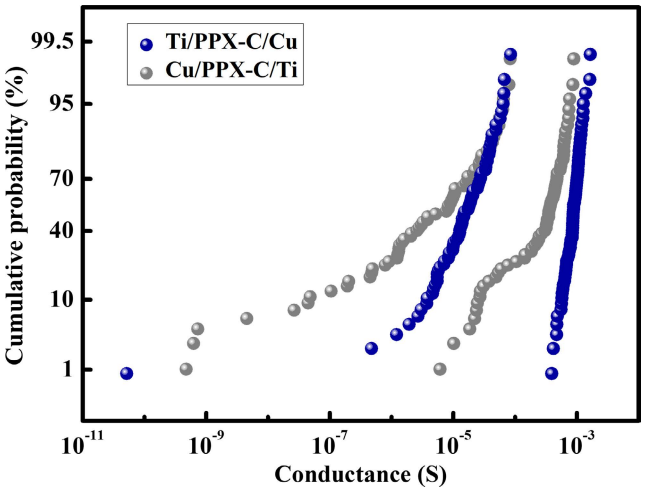

FIGURE 8. Cumulative probability distribution of HRS and LRS conductance of RRAM devices with Ti/PPX-C/Cu and Cu/PPX-C/Ti structures.

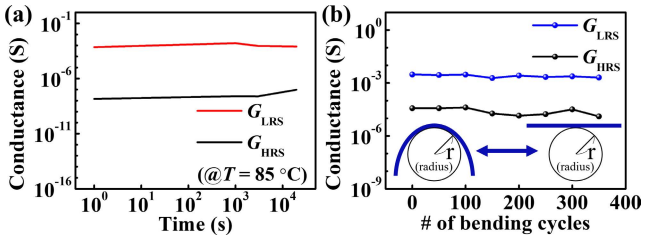

FIGURE 9. (a) Retention characteristics of the RRAM device with the Ti/PPX-C/Cu structure at 85 °C. (b) Continuous mechanical bending fatigue test results of the device with the Ti/PPX-C/Cu structure and a radius of 2 cm for 350 cycles.

of over 10^4 s was obtained at 85°C, with a G_{LRS}/G_{HRS} resistive window value of approximately 10^3.

Evaluation of the electrical performance of RRAM devices under mechanical deformation is another important quality index for flexible electronics. The conductance of the device with the Ti/PPX-C/Cu structure was measured at a bending radius of 2 cm, as depicted in Fig. 9(b). The two conductance states were clearly differentiable even after 350 bending cycles. The conductance of each device in the LRS and HRS states was unvaried after 350 bending cycles. These results demonstrate their suitability for reliable flexible electronics applications.

IV. NEURAL NETWORK IMPLEMENTATION

The operation of a neuromorphic system can be categorized into inference and learning tasks. The inference task calculates the output data for a given input data via VMM in an artificial neural network (ANN). The learning task involves adjusting the synaptic weights of the ANN to improve inference accuracy. There are two types of learning methods: on-chip and off-chip. On-chip learning method in a neuromorphic system chip includes all the functions of neurons and synapses for learning. In off-chip learning, the learning task is performed outside the neuromorphic chip using software.

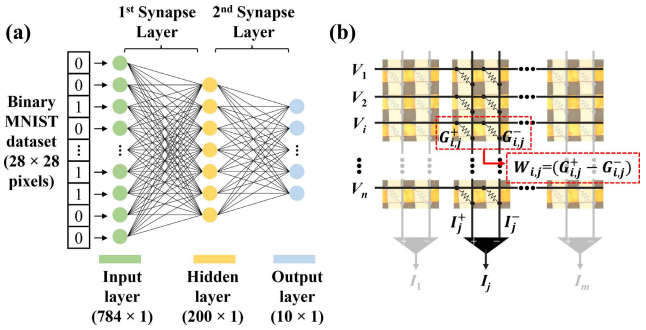

FIGURE 10. (a) Software-based artificial neural network (ANN) structure for MNIST pattern recognition. (b) Crossbar RRAM array structure for implementing ANN.

After ANN-to-synapse array weight mapping, neuromorphic systems support only the inference task. Specifically, a backpropagation algorithm based on software was used for ANN learning [44]. However, no general solution exists for implementing on-chip learning in neuromorphic hardware systems. Therefore, off-chip learning is considered to be a promising solution for the commercialization of neuromorphic systems [45].

In this study, an off-chip learning simulation of pattern recognition was conducted using the binary MNIST dataset to demonstrate the feasibility of the fabricated PPXC-based RRAM array. Fig. 10(a) shows the software-based ANN structure used for the MNIST pattern recognition task. The rectified linear unit and softmax activation functions were used for the hidden and output neurons, respectively. To obtain the optimized synaptic weights, we trained an ANN on a software framework using a backpropagation algorithm and stochastic gradient descent method. After 431 training epochs, the trained ANN achieved a recognition accuracy of 97.92%. The ANN can be realized in a crossbar synapse array and neuron circuits, as illustrated in Fig. 10(b). The synaptic weight of each synapse in the ANN is represented by the difference between the two conductances of the RRAM device pair, $W_{ij} = G^+_{ij} - G^-_{ij}$, where i and j are indices within the crossbar array. To perform a VMM within the array, all horizontal lines are simultaneously activated, with the input signals (V_1–V_n) corresponding to the information of each pixel in the input image. The neuron output (I_j) is determined by the difference between the two currents (I^+_j and I^-_j), as follows:

$$I_j = \sum_{i=1}^{n} V_i \cdot W_{ij} = \sum_{i=1}^{n} V_i \cdot \left(G^+_{ij} - G^-_{ij}\right) = I^+_j - I^-_j. \quad (1)$$

As evident from Equation (1), the multiplications and summations are realized using Ohm's and Kirchhoff's current laws, respectively. Because the input signals are parallelly applied to all the horizontal lines and all outputs are calculated in a single read operation, analog-based neuromorphic systems can significantly reduce the energy required and latency associated with data movement.

When transferring the synaptic weight trained by a software framework to the conductance of the synapse device (ANN-to-synapse array weight mapping), it is necessary to

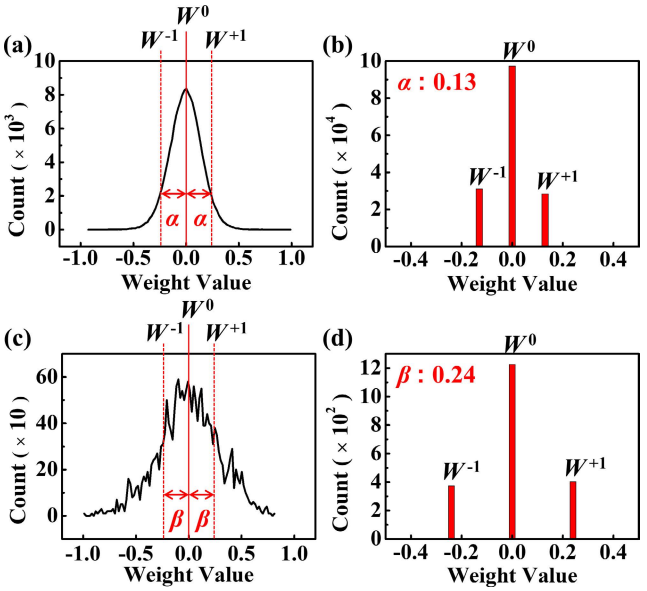

FIGURE 11. Weight distributions of the (a) first and (c) second synapse layers before quantization. Quantized weight distributions of the (b) first and (d) second synapse layers.

quantize the synaptic weights. For this, we used a single-bit synapse operation, wherein each RRAM device had two conductance levels (G_{LRS} and G_{HRS}). Consequently, the synaptic weight could be quantized at three levels, as follows:

$$W^{0} = G_{\mathrm{HRS}}(G_{ij}{}^{+}\ \text{device}) - G_{\mathrm{HRS}}(G_{ij}{}^{-}\ \text{device}) \quad (2)$$

$$W^{+1} = G_{\mathrm{LRS}}(G_{ij}{}^{+}\ \text{device}) - G_{\mathrm{HRS}}(G_{ij}{}^{-}\ \text{device}) \quad (3)$$

$$W^{-1} = G_{\mathrm{HRS}}(G_{ij}{}^{+}\ \text{device}) - G_{\mathrm{LRS}}(G_{ij}{}^{-}\ \text{device}) \quad (4)$$

The synaptic weight distributions of the first and second synapse layers after training on the software framework are shown in Figs. 11(a) and (c), respectively. For quantization at three levels, the weight interval values were assigned as variables α and β for the first and second synapse layers, respectively. Synaptic weights between -1 and $-\alpha$ (or $-\beta$) were quantized as W^{-1}, and those between α (or β) and $+1$ were quantized as W^{-1}, as shown in Figs. 11(b) and (d), respectively.

The MNIST pattern recognition results for various α and β combinations are shown in Fig. 12. The best classification accuracy of 93.65% was obtained when $\alpha = 0.13$ and $\beta = 0.24$. Subsequently, we performed a weight transfer operation based on the actual G_{HRS} and G_{LRS} values measured in the fabricated Ti/PPX-C/Cu RRAM array, as depicted in Fig. 13. The ANN-to-synapse array weight mapping, considering the realistic conductance distribution of the fabricated devices, was evaluated via 1000 Monte Carlo simulations. A classification accuracy of 93.65% was obtained when weight variation was ignored and the ideal quantization was adopted. However, as shown in Fig. 14(a), the average accuracy decreased to 86.39% when the variation in realistic RRAM devices was considered. To further analyze the effect of conductance variation in RRAM devices on the accuracy, MNIST pattern recognition was simulated

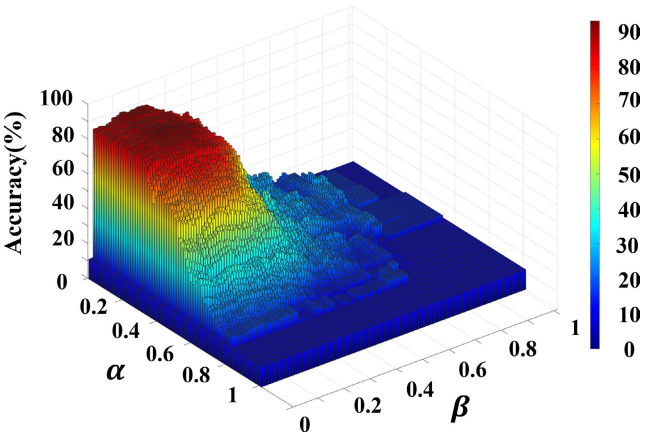

FIGURE 12. Classification accuracy in a 3D plot obtained by varying α and β.

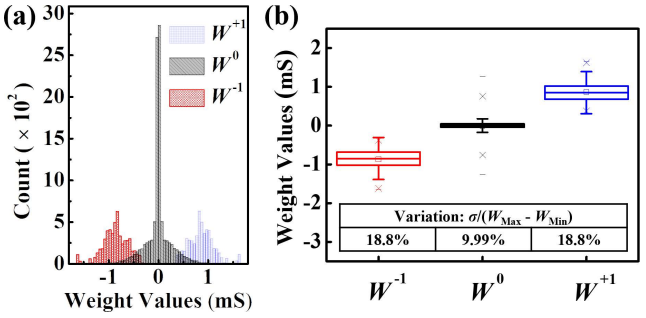

FIGURE 13. Statistical results of weight values in a (a) histogram and (b) box plot created using the measured LRS and HRS conductances of the devices.

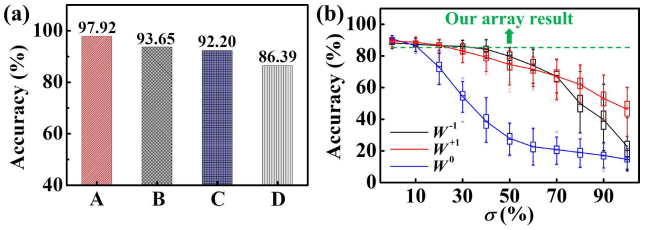

FIGURE 14. (a) Test accuracies of the designed ANN (A and B denote the results of the full-precision training and ternary weight quantization, respectively. C and D denote the maximum and average accuracies, respectively, which are obtained via 1000 Monte Carlo simulations of ANN-to-synapse array weight mapping based on realistic conductance distribution.). (b) Effects of each weight variation on the classification accuracy.

by varying σ from 0% to 100% in steps of 10%, as shown in Fig. 14(b). In the figure, x% variation indicates that the standard deviation is x% of the dynamic range of the device. For generalization, the results were obtained by repeating the simulation 100 times. Overall, it was observed that the accuracy decreased as the variation increased. At the variation level of the fabricated RRAM array (W^0: 9.99%, W^{+1}: 18.8%, W^{-1}: 18.8%), an accuracy of 86.39% was obtained, whereas when σ of W^0, W^{+1}, and W^{-1} was increased to 15, 50, and 60, respectively, the accuracy decreased to less than 80%. Therefore, a more precise conductance variation control is required to achieve high operational accuracies in neuromorphic systems. An iterative write-verify method can be adopted to reduce the variation in synapse devices [46].

V. CONCLUSION

In summary, we successfully demonstrated a flexible PPXC-based RRAM crossbar array that can be used in wearable neuromorphic system applications. Devices with the Ti/PPX-C/Cu structure exhibited the advantages of lower operation voltage and more reliable cycling endurance than those with the Cu/PPX-C/Ti structure. The electrical characteristics of the devices were carefully investigated through I-V measurements and TEM-EDS analyses. It was observed that the set voltage and reset current decreased because of the naturally formed CuO layer in the Ti/PPX-C/Cu structure after Cu deposition. Additionally, the flexible RRAM array was mechanically and electrically stable during the bending test (bending cycles >350). Finally, we demonstrated the feasibility of the PPXC-based RRAM array for neuromorphic systems through a system-level MATLAB simulation. The results of this study indicate that RRAM arrays developed using biocompatible PPXC have potential for application in next-generation wearable neuromorphic systems.

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