IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 3 August 2022, accepted 10 September 2022, date of publication 20 September 2022, date of current version 29 September 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3208116

RESEARCH ARTICLE

Temperature-Dependent Electrical Characteristics of *p*-Channel Mode Feedback Field-Effect Transistors

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This work was supported in part by the National Research Foundation of Korea (NRF) through the Ministry of Science, ICT and Future Planning (MSIP) under Grant NRF-2020R1A2C3004538 and Grant NRF-2022M3I7A3046571, in part by Samsung Electronics Company Ltd. under Grant IO201223-08257-01, in part by the Brain Korea 21 Plus Project of 2022 through the NRF through the Ministry of Science, and in part by Korea University Grant.

ABSTRACT In this study, the temperature-dependent electrical characteristics of p-channel mode feedback field-effect transistors (FBFETs) were examined at temperatures ranging from 250 to 425 K. Their steep subthreshold swings of less than 1 mV/dec were maintained even at temperatures up to 400 K. As the temperature increased to 400 K, the latch-up voltage shifted from −0.951 to −0.613 V, which was caused by a reduction in the potential barriers in the channels of the FBFETs. High I_{on}/I_{off} ratios above 108 were maintained in the temperature range of 250 to 400 K. However, at temperatures over 400 K, the FBFETs were turned on regardless of the gate voltages owing to the generation of a thermally induced positive feedback loop.

INDEX TERMS Field-effect transistor, positive feedback loop, temperature-dependent, simulation.

I. INTRODUCTION

Recently, feedback field-effect transistors (FBFETs) have generated considerable interest because their abrupt switching behaviors and bistable characteristics are suitable for logic-in-memory devices, which have led to revolutionary progress in the semiconductor industry [1], [2], [3], [4], [5], [6]. Recent studies have demonstrated that FBFETs can be utilized for dynamic random-access memory [7], [8], [9]. However, at the circuit level, in which millions of memory cells are integrated, the temperature-dependent analysis of single FBFETs is of primary importance for maintaining the stable operation of memory circuits. Moreover, for temperature-sensitive applications such as embedded memory in logic devices, stable operation at temperatures over 360 K, which have been extensively tested for temperature reliability, is required. However, there have been no reports on temperature-dependent electrical characteristics of single FBFETs. In this study, we experimentally investigated temperature-dependent feedback operation of *p*-channel mode FBFETs in the temperature range of 250 to 425 K. Furthermore, the temperature-dependent electrical characteristics were analyzed by simulations.

The associate editor coordinating the review of this manuscript and approving it for publication was Wenxin Liu.

II. EXPERIMENT

A. DEVICE FABRICATION AND ELECTRICAL CHARACTERIZATION

p-channel mode FBFETs were fabricated using a silicon-on-insulator with a 340-nm-thick Si layer. A silicon active layer was prepared using stepper photolithography and anisotropic dry etching. The active layer was subjected to the *n*-well process by implantation of P^+ ions at a dose of 3×10^{13} cm^{-2} at an ion energy of 60 keV followed by thermal annealing at 1100 °C for 30 min. A silicon dioxide layer for forming a gate dielectric layer was grown by thermal oxidation at 850 °C. A p^+ poly-silicon gate was formed by low-pressure chemical

vapor deposition (LPCVD) and photolithography followed by dry etching. For a lightly doped drain extension, BF_2^+ ions were implanted at a dose of 1×10^{12} cm^{-2} at an ion energy of 10 keV. Gate sidewall spacers were formed using LPCVD-based tetraethyl orthosilicate. Repeated implantation of BF_2^+ ions at a dose of 6×10^{13}cm^{-2} at an ion energy of 40 keV formed a *p*-region, except for the region beneath the gate region. To form p^+ drain and n^+ source regions, BF_2^+ and P^+ ions at a dose of 3×10^{15} each were implanted at ion energies of 30 keV and 100 keV, respectively. Subsequently, the wafer was first annealed at 1000 °C for 30 min and subsequently at 1050 °C for 30 s using a rapid thermal annealing system. In the last step, Ti/TiN/Al/TiN metal alloy-based drain, source, and gate electrodes were formed using sputtering and photolithography.

A temperature-controllable vacuum probe station was constructed to investigate the temperature-dependent electrical characteristics of the FBFETs. All electrical data were obtained in the temperature range of 250–425 K in vacuum using a semiconductor parameter analyzer (Keithley 4200). Cross-sectional images of the FBFETs were captured by transmission electron microscopy (TEM; FEI Tecnai F20).

B. DEVICE STRUCTURE AND SIMULATION

Figure 1 shows a schematic of the fabricated *p*-channel mode FBFET with a p^+–n–p–n^+ silicon layer and the initial energy band diagram. The silicon channel consists of an *n*-doped channel region below the p^+ poly-silicon gate and a *p*-doped non-gated channel region. The *n*-(*p*-)-doped channel region acts as a potential barrier that blocks the injection of holes (electrons) from the p^+ drain (n^+ source). The drain and source regions are heavily doped with *p*- and *n*-type dopants, respectively.

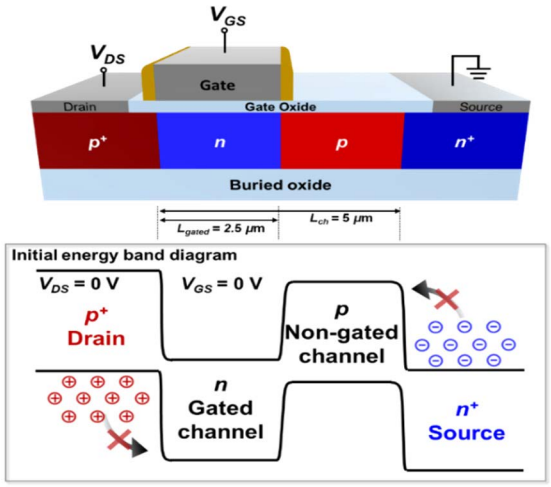

FIGURE 1. Schematics of p-channel mode FBFET and initial energy band diagram.

The dimensional parameters and doping concentrations in the silicon channel used in the simulations are summarized in Table 1. The simulations were performed using a two-dimensional FBFET structure on the Sentaurus TCAD simulator (Synopsys Sentaurus, Version O_2018.06) [10]. In the simulations, we used the following physics models: thermodynamic, Fermi–Dirac statistics, bandgap narrowing, Auger recombination, Shockley–Read–Hall recombination, inversion and accumulation layer mobility, and high field saturation. The default parameters were used for all models. In this study, all simulations were conducted for the FBFETs in the temperature range of 250–425 K.

TABLE 1. Dimensional parameters and doping concentrations for simulations.

Parameter	Value [unit]
Channel length (L_{ch})	5 [μm]
Gate channel length (L_{Gated})	2.5 [μm]
Silicon channel thickness (T_{Si})	340 [nm]
Gate oxide thickness (T_{ox})	25 [nm]
Source/drain doping concentration	$3.0\text{x}10^{19}$ [cm^{-3}]
Gated channel doping concentration	$2.3\text{x}10^{17}$ [cm^{-3}]
Non-gated channel doping concentration	$1.0\text{x}10^{18}$ [cm^{-3}]

III. RESULTS AND DISCUSSION

Figure 2 shows an optical image of the fabricated FBFET and a cross-sectional TEM image of the gate region, where the dimensions and structure of the fabricated device are the same as those shown in Figure 1.

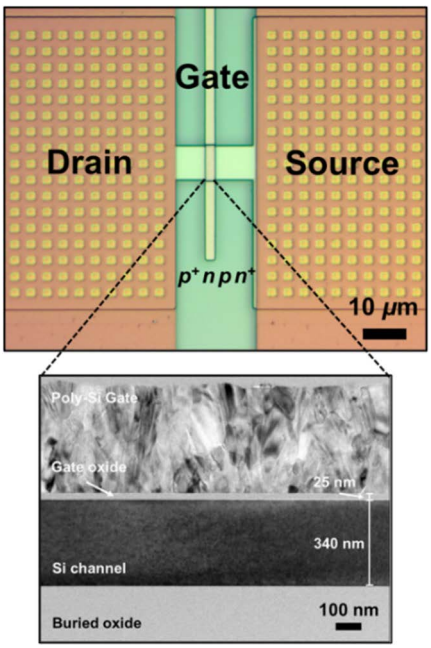

FIGURE 2. Optical image of fabricated p-channel mode FBFET and cross-sectional TEM image of gate region.

The transfer characteristics of the FBFET at 300 K and the band diagrams under the operating state at a V_{DS} of 1 V are shown in Figures 3(a) and (b), respectively. The on and

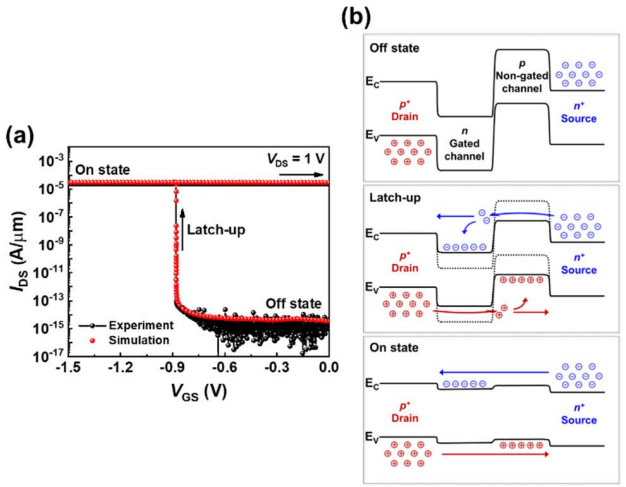

FIGURE 3. (a) Experimental and simulated I_{DS}–V_{GS} transfer curves of p-channel mode FBFET at 300 K. (b) Band diagrams of positive feedback loop with positive V_{DS}.

off states of the *p*-channel mode FBFET before and after the generation of the latch-up are depicted in the band diagrams. In the off state, a potential barrier formed in the valence band of the *n*-gated channel region blocks the flow of holes from the drain region. Simultaneously, a potential barrier created in the conduction band of the *p*-non-gated channel region blocks the flow of electrons from the source region. As the negative V_{GS} increases, the height of the potential barrier in the valence band of the *n*-gated channel region decreases, allowing the injection of holes into the potential well in the valence band of the *p*-non-gated channel region. The injected holes accumulate in the potential well, electrically lowering the height of the potential barrier in the conduction band of the *p*-non-gated channel region.

Subsequently, electrons are injected into the potential well in the conduction band of the *n*-gated channel region owing to the lowering of the height of the potential barrier in the conduction band. The electrons and holes accumulated in the potential wells further accelerate the lowering of the height of the potential barrier in each region, resulting in a positive feedback loop phenomenon in which the potential barriers. collapse in a very short time. The positive feedback loop results in a latch-up phenomenon, in which the drain-to-source current (I_{DS}) abruptly increases; the latch-up voltage is denoted as $V_{latch-up}$. Moreover, the electrons and holes accumulated in the potential wells maintain the abovementioned positive feedback loop even when V_{GS} returns to 0 V, thereby maintaining the on state. Thus, the fabricated FBFET is suitable not only for switching devices but also for memory applications.

Figure 4(a) shows the experimentally measured I_{DS}–V_{GS} transfer curves of the *p*-channel mode FBFET in the temperature range of 250–425 K. The variation in the temperature up to 400 K influences both the $V_{Latch-up}$ and on/off ratio; however, a subthreshold swing (SS) below 1 mV/dec

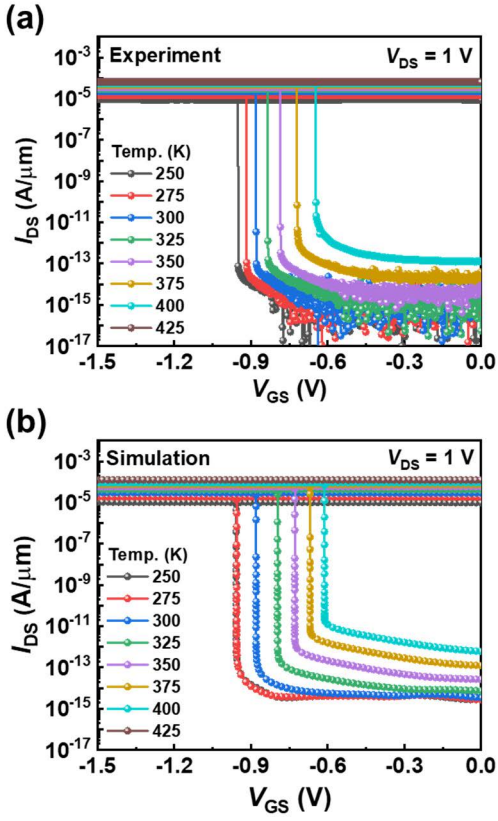

FIGURE 4. (a) Experimental and (b) simulated temperature-dependent I_{DS}–V_{GS} transfer curves of p-channel mode FBFET.

is independent of temperature. As the temperature increases from 250 to 400 K, $V_{Latch-up}$ shifts from −0.951 to −0.647 V. In contrast, at 425 K, the device is turned on regardless of V_{GS}, indicating that the entire area of the channel becomes conductive. I_{on} and I_{off} at $V_{GS} = 0$ V increase with increasing temperature, and the increase in I_{off} is larger than that in I_{on}. Accordingly, I_{on}/I_{off} increases from 5.01×10^9 to 1.35×10^{10} as the temperature increases from 250 to 325 K, and subsequently, it decreases to 3.92×10^8 at 400 K. Nevertheless, our device exhibits outstanding I_{on}/I_{off} ($>10^8$) over a wide temperature range compared to other steep switching devices [11], [12], [13], [14]. Figure 4(b) shows the simulated I_{DS}–V_{GS} transfer curves, which present similar trends to the experimental data. The $V_{Latch-up}$, on/off ratio, and SS values obtained from the I_{DS}–V_{GS} transfer curves at 200–400 K are listed in Table 2.

As for the on/off ratios, there is a difference between the simulation and the experimental results in terms of the inflection temperature; the temperatures are 300 and 325 K for the simulation and the experimental results, respectively. This discrepancy is attributed to the off current that involves unavoidable noise from measurement environments since the on currents on the simulation and the experimental results increase linearly within the same order of 10^{-4}. $V_{latch-up}$ becomes a smaller negative value as the temperature increases from 250 to 400 K, and simultaneously I_{on} and I_{off} increase.

TABLE 2. $V_{\text{Latch-up}}$, on/off ratio, and SS values obtained from I_{DS}–V_{GS} transfer curves at 200–400 K.

Temp. [K]		250	275	300	325	350	375	400
$V_{\text{Latch-up}}$ [V]	Experiment	−0.951	−0.918	−0.881	−0.835	−0.786	−0.721	−0.647
	Simulation	−0.957	−0.956	−0.880	−0.796	−0.729	−0.669	−0.613
I_{on}/I_{off}	Experiment	$5.01\text{x}10^{9}$	$8.63\text{x}10^{9}$	$1.24\text{x}10^{10}$	$1.35\text{x}10^{10}$	$8.44\text{x}10^{9}$	$2.22\text{x}10^{9}$	$3.92\text{x}10^{8}$
	Simulation	$2.30\text{x}10^{9}$	$5.51\text{x}10^{9}$	$9.13\text{x}10^{9}$	$6.62\text{x}10^{9}$	$2.32\text{x}10^{9}$	$6.45\text{x}10^{8}$	$1.70\text{x}10^{8}$
SS [mV/dec]	Experiment	0.124	0.123	0.147	0.135	0.148	0.171	0.173
	Simulation	0.0037	0.0033	0.0036	0.0035	0.0031	0.0033	0.0023

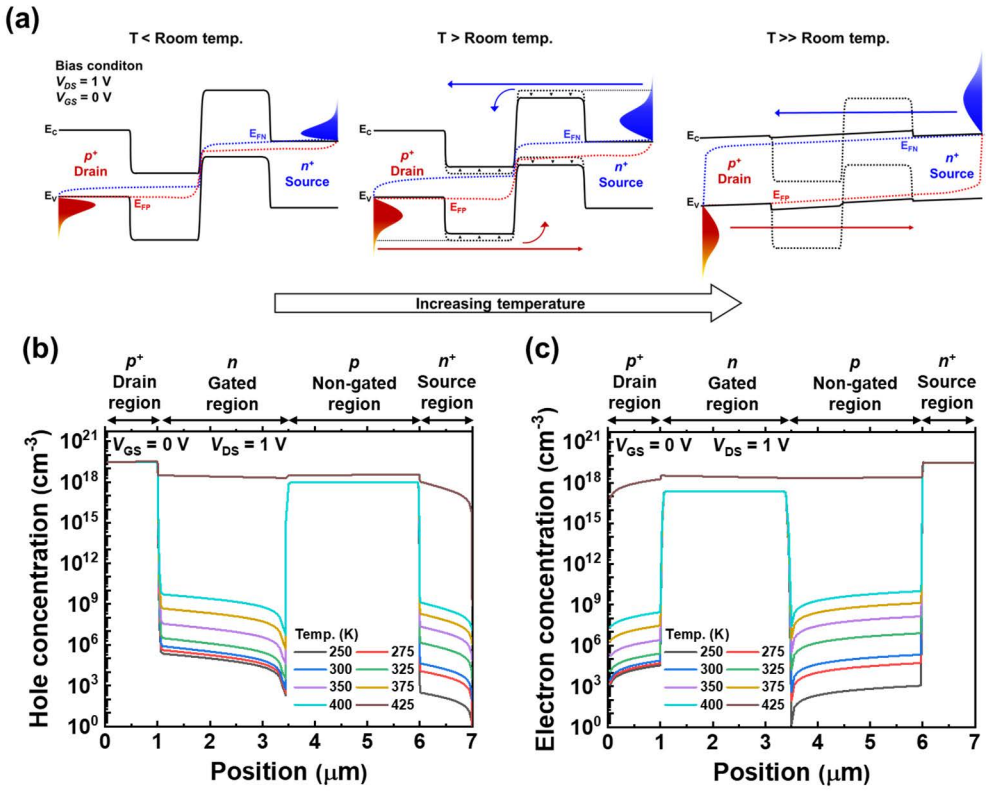

FIGURE 5. (a) Energy band modulation mechanism in p-channel mode FBFET with increasing temperature. (b) Hole and (c) electron concentrations with increasing temperature.

Moreover, our simulation results reveal that the device is turned on regardless of V_{GS} at 425 K. However, the simulated SS values are approximately two orders of magnitude smaller than the experimental results over the entire temperature range. In this study, the SS value is calculated as SS $= [\text{d}(\log 10|I_{DS}|)/\text{d}V_{GS}]^{-1}$, and in the experiments, the minimum step of the V_{GS} sweep cannot be reduced to less than 1 mV owing to the limitation of our measuring equipment. Therefore, the experimental SS values are relatively larger than the simulated ones. The changes in the electrical characteristics—I_{on}, I_{off}, and $V_{latch-up}$—as shown in Figure 4 indicate that temperature increase affects the kinetic energy of the charge carriers and the potential barrier, which blocks the injection of charge carriers into the channel region.

Figure 5(a) shows the energy band modulation mechanism in the *p*-channel mode FBFET in the off state ($V_{DS} = 1$ V, $V_{GS} = 0$ V) with increasing temperature. At temperatures below room temperature, the potential barriers formed in the valence band (the conduction band) are sufficiently high to block the injection of holes (electrons) from the drain (source) region to the channel region. However, as the temperature gradually increases, the quasi-Fermi levels (E_{FN} for electrons and E_{FP} for holes) become closer to the conduction band or the valence band. Therefore, the electron and hole concentrations increase, as shown in Figures 5(b) and (c), and the kinetic energy of the charge carrier increases. The increase in the kinetic energy allows some electrons and holes to have sufficient energy to overcome the potential barrier at the junction between the source (or drain) and channel

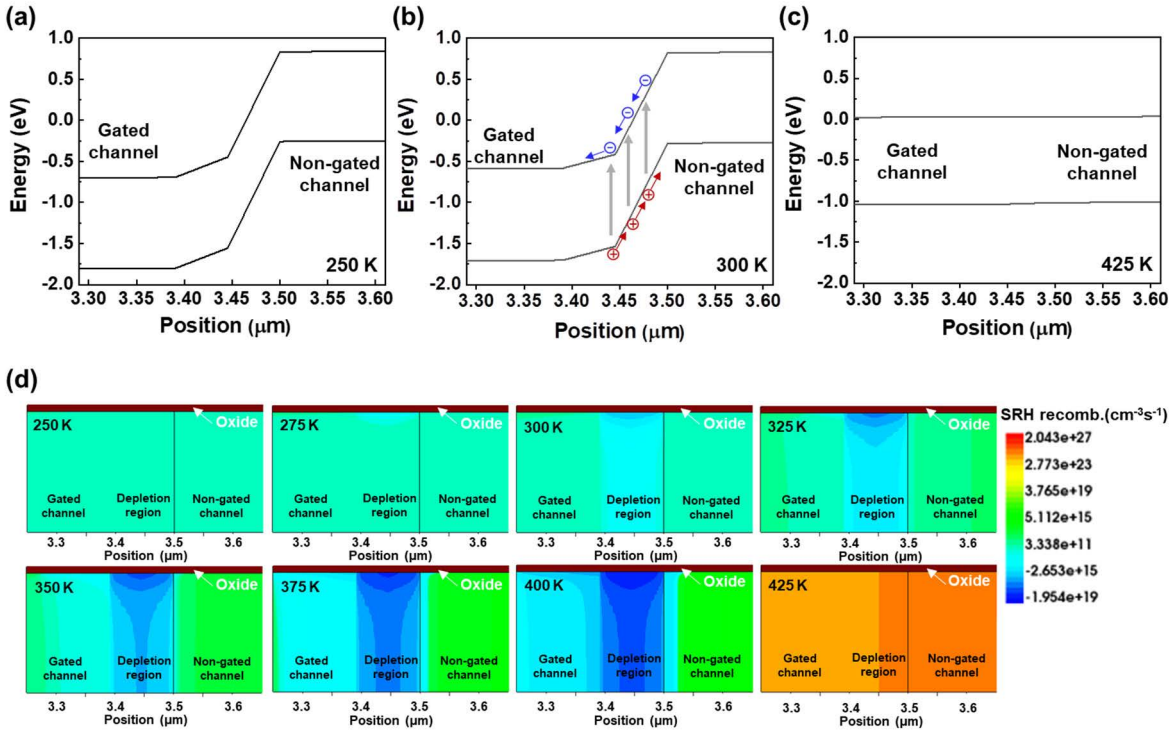

FIGURE 6. Representative energy band diagrams for depletion region at (a) lowest temperature (250 K), (b) room temperature (300 K), and (c) highest temperature (425 K). (d) Simulation results of electron–hole pair generation in depletion region.

regions. Some electrons and holes flow toward the drain and source regions, increasing I_{off}, whereas the others accumulate in the potential well. The accumulation of electrons and holes reduces the height of the potential barrier, which plays a critical role in determining $V_{latch-up}$. As the potential barrier height decreases, a relatively smaller $|V_{GS}|$ value is required to generate the positive feedback loop. Moreover, at a high temperature of 425 K, a thermally induced positive feedback loop is generated by the interaction of the electrons and holes injected into the channel owing to the high thermal energy. Consequently, the *p*-channel mode FBFET is turned on regardless of the V_{GS} sweep, as shown in Figure 4.

In the following, the contribution of electron–hole pair generation to the energy band modulation of the *p*-channel mode FBFET is discussed. The FBFET has a p^+–*n*–*p*-n^+ diode structure, and accordingly, the p–n junction of the channel region becomes a reverse bias condition when a forward bias is applied to the drain. Figure 6 shows the thermal generation of electron–hole pairs in the depletion region of the p–n junction of the channel region at which reverse bias occurs. Representative energy band diagrams for the depletion region at the lowest temperature (250 K), room temperature (300 K), and highest temperature (425 K) are shown in Figures 6 (a)–(c), respectively. Slight energy changes in the conduction and valence bands occur at 250 and 300 K, the potential barrier collapses at 425 K, and the channel becomes conductive. The electron–hole pair generation in the depletion region is driven by thermal energy via the defects in the forbidden band [15], [16]. Based on our simulations, impurity atoms located interstitially or substitutionally in the silicon crystal lattice and interface traps existing between silicon and silicon oxide mainly contribute to the thermal electron–hole pair generation in the depletion region. The simulation results of electron–hole pair generation are shown in Figure 6(d). The generation rate considerably increases from $7.04 \times 10^{10}\,\mathrm{cm^{-3}\cdot s^{-1}}$ to $1.48 \times 10^{19}\,\mathrm{cm^{-3}\cdot s^{-1}}$ as the temperature increases from 250 K to 400 K. The thermally generated electrons and holes drift to the potential wells formed in the conduction and valence bands, respectively, under the electric field in the depletion region These electrons and holes are blocked from moving to the drain and source regions by the potential barrier and accumulate in the potential wells. Consequently, they contribute to the reduction in the potential barrier height and the generation of a thermally induced positive feedback loop.

Figure 7 shows the energy band diagram of the *p*-channel mode FBFET with increasing temperature. The potential barrier formed in the valence band in the gated channel gradually decreases as the temperature increases from 250 to 400 K at intervals of 25 K ($0.85 \rightarrow 0.85 \rightarrow 0.83 \rightarrow 0.82 \rightarrow 0.81 \rightarrow 0.78 \rightarrow 0.72$ eV).

Subsequently, it abruptly decreases to 0.06 eV at the highest temperature of 425 K. Similar to the potential barrier in the valance band, that formed in the conduction band in the non-gated channel first gradually decreases and subsequently abruptly decreases at the highest temperature of 425 K.

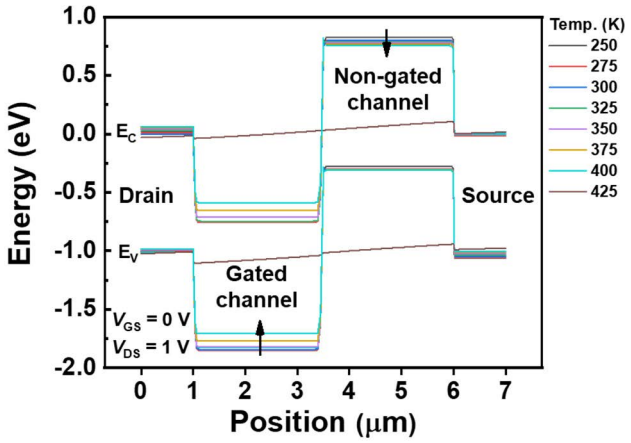

FIGURE 7. Variations in energy bands of p-channel mode FBFET with increasing temperature.

The corresponding values are 0.84 → 0.81 → 0.80 → 0.79 → 0.78 → 0.76 → 0.74 → 0.07 eV. The influence of temperature enables the injection of charge carriers with sufficient energy to overcome the potential barriers and the accumulation of generated electron–hole pairs in the depletion region to reduce the potential barrier height. The reduction in the potential barrier height explains the $V_{\text{latch-up}}$ decrease with increasing temperature. Nevertheless, the potential barrier required for a positive feedback loop is sufficiently maintained and exhibits steep switching characteristics over a wide temperature range of 250–400 K.

IV. CONCLUSION

In this study, the temperature-dependent electrical characteristics of a *p*-channel mode FBFET were investigated by experiments and simulations. At a temperature up to 425 K, the device became turned on, regardless of V_{GS}, owing to the generation of a thermally induced positive feedback loop. However, as the temperature increased from 250 to 400 K, $V_{\text{latch-up}}$ slightly shifted from −0.951 to −0.613 V with a high I_{on}/I_{off} ratio of over 10^8. Moreover, the FBFET exhibited SS values of less than 1 mV/dec. These values were independent of the temperature. Owing to its relatively low SS and high I_{on}/I_{off} ratio with a wide range of temperature stability, the developed FBFET has considerable potential as a low-power high-performance device.

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