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METHODS

A Framework for Sensitivity Analysis of Real-Time Power Hardware-in-the-Loop (PHIL) Systems

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ABSTRACT Power hardware-in-the-loop (PHIL) simulation leverages the advanced real-time emulation based technique to carry out in-depth investigations on novel real-world power components. Power amplifiers, sensors, and signal conversion units based power interfaces (PI) incorporate physical hardware systems and real-time simulation platforms into PHIL setups. However, the employment of any interfacing technique inevitably introduces disturbances such as sensor noise, switching harmonics, or quantization noise to PHIL systems. To facilitate quantitatively analyzing and assessing the impact of external disturbances on PHIL simulation systems, a framework for sensitivity analysis of PHIL setups has been developed in this paper. Detailed modelling principles related to the sensitivity analysis of PHIL systems and the inherent relationship between sensitivity transfer functions and stability criteria are elaborated along with theoretical and experimental validation. Based on this concept, accuracy assessment methods are employed in this framework to quantify generic sensitivity criteria. Moreover, physical passive load and converter-based PHIL setups are applied and experimental results are presented to characterize and demonstrate the applicability of the proposed framework.

INDEX TERMS Power hardware-in-the-loop (PHIL) simulation systems, sensitivity analysis, power interface, system modelling, system theory, control systems, real-time simulation system.

I. INTRODUCTION

PHIL simulation, an advanced and efficient tool incorporating the physical power apparatus and large-scale power network into a real-time testing environment, has been widely utilized to promote the research and development in the power industry [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11]. Owing to the merit of carrying out repeated, non-destructive, and in-depth investigation of the power apparatus and their interactions with the power network, PHIL has been extensively employed for prototyping applications [4], [5], [6], the verification of novel control paradigm [7], the black start testing of grid-forming converter [8], or the dynamic modelling and prototyping of renewable energy systems, such as variable-speed wind turbines [10], solar energy [6], and energy storage resources [5], [11].

PHIL systems are defined as closed-loop systems consisting of a digital real-time simulator (DRTS) interfacing

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with the hardware under test (HUT) through a power interface (PI), which facilitates the conservation of instantaneous power as exists in the real-world system through natural coupling. The PI that is typically comprised by a power amplifier (PA), sensors, signal conversion cards, or filters, inevitably introduces non-ideal characteristics such as time delay, noise, or signal distortion to PHIL simulation. From the perspective of system operation, these non-idealities play a crucial role with respect to PHIL system properties such as stability, accuracy, and sensitivity. In literature, approaches for time-discrete and time-continuous modelling of PHIL systems are given [12], [13], [14], [15], [16], [17], [18], [19]. In this work, the time-continuous modeling is chosen for system analysis including appropriate representations of discretization and sampling effects caused by the digital real-time simulator or non-linearities.

The impact of the non-ideal characteristics and the dynamics stemming from the PI on the PHIL system stability and accuracy has been extensively discussed in literature [20], [21], [22], [23], [24]. Many research efforts have been devoted to improve the stability and accuracy of the PHIL simulation, such as the impedance shifting method [4], multi-rate partitioning interface [19], Bergeron transmission line model based multi-time-step interface [6], Smith-predictor based compensation [23], $\mathcal{H}_\infty$ optimal control based interface [5], the optimal compensation filter design [24], and other advanced methods as summarized in [25]. Detailed modelling principles, block diagrams, stability criteria, and accuracy metrics have been developed for the assessment of system properties such as stability and accuracy of respective approaches.

Apart from the conventional stability and accuracy assessments of the PHIL simulation, the assessment of the impact of external disturbances on the PHIL simulation is an important factor in PHIL setups. Due to the implementation of the non-ideal PI, external disturbances are inevitably injected into the PHIL setup and are mainly stemmed from (i) Offset noise in the measurement units, (ii) Quantization error/noise in the ADC converter, (iii) Sensor measurement noise (typically high-frequency), and (iv) Switching harmonics stemming from high-frequency pulsating modulation.

From an application point of view, a comprehensive sensitivity analysis and assessment is crucial for a high-fidelity and robust PHIL simulation. In contrast to the well-presented framework for stability and accuracy assessment in the literature, no sensitivity analysis framework has been developed within the PHIL community. In this article, a framework for sensitivity analysis of the PHIL setups has been proposed for quantifying the sensitivity criteria. The main contributions of this article are summarized as follows:

1) A framework based on detailed modeling was developed for the sensitivity analysis of PHIL setups using transfer functions describing the dynamic behaviour of forward and feedback paths.
2) The inherent relationship between stability, accuracy and sensitivity was elaborated and verified by the framework and allows for a precise estimation of PHIL system properties prior to experimental testing.
3) Along with the sensitivity analysis criteria, practical methods involving the signal-to-noise (SNR) and the total harmonic distortion plus noise (THD+N) are presented to quantity the sensitivity, which are easily applied to practical experiments.
4) Based on the voltage-type and current-type ITM interfaces, the framework for sensitivity analysis was characterized and verified by experimental PHIL setups at two laboratories, the Dynamic Power Systems Laboratory at the University of Strathclyde and the Electric Energy Systems Laboratory at the NTUA of Athens, demonstrating its applicability for simplified to complex power system and component testing.

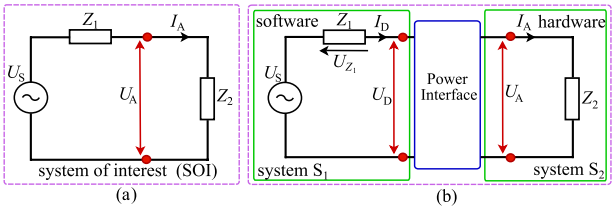

FIGURE 1. Principle topology of (a) the system of interest (SOI) and (b) the corresponding PHIL simulation system.

This article is structured in subsequent manner: following this Introduction, the detailed modelling of the PHIL system is presented in Section II. Section III provides the in-depth details of the sensitivity analysis framework. Analytical assessments of the proposed sensitivity framework are presented in IV, followed by its experimental validation presented in Section V. Section VI concludes this article.

II. STATE-OF-THE-ART INTERFACING TECHNIQUES FOR PHIL SIMULATION SYSTEMS

This section presents the topology of the PHIL system along with its detailed modelling, characteristics and properties.

A. PHIL TOPOLOGY

PHIL simulation combines the physical power component with real-time emulated system into a closed-loop testing configuration that mimics the original system of interest (SOI). Fig. 1 illustrates the SOI and its corresponding PHIL simulation setup. The original SOI is expressed by a lumped voltage divider topology comprising two series-connected Thévenin equivalent circuits S_1 and S_2, respectively. System S_1 comprises a voltage source U_S in series with an equivalent impedance Z_1 and system S_2 comprises an equivalent impedance Z_2. S_1 represents the real-time emulated power network in DRTS referred to as software side and S_2 represents the real-world HUT referred to as hardware side, both of which are coupled through a PI in the PHIL setup.

The PI comprises one or several PA, sensors, analogue-to-digital (ADC) and digital-to-analogue (DAC) conversion cards, and signal processing units such as low-pass filtering blocks for noise mitigation. The configuration of these

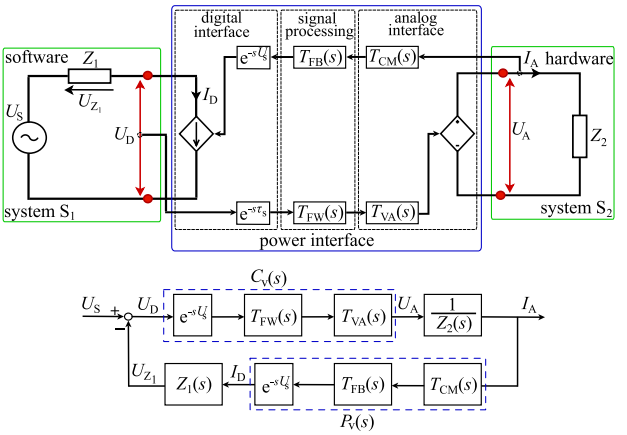

FIGURE 2. Model and block diagram of a PHIL simulation system with applied V-ITM interface.

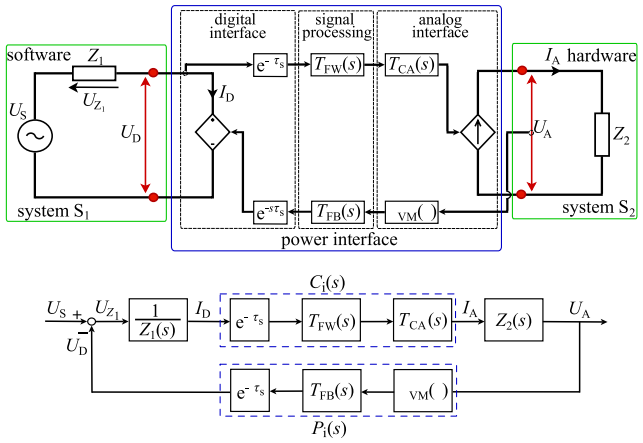

FIGURE 3. Model and block diagram of a PHIL simulation system with applied I-ITM interface.

components and the manner in which the power is transferred between the DRTS and the HUT are defined by the interface algorithms (IAs) [12]. Interface algorithms such as the ideal transformer model (ITM), the damping impedance method (DIM), or the partial circuit duplication (PCD) have been discussed and evaluated in the literature [12], [13], [14]. Among these mentioned interfacing methods, the ITM interface is widely adopted because of its simple implementing structure and shows a good performance with respect to the stability and accuracy properties. This interface will be utilized throughout the paper, even though a similar methodology could be applied to other interface mechanisms as well.

B. ITM INTERFACE MODELLING

The PI bridges the DRTS and physical hardware, whose control and operation is a crucial factor for realizing a robust and high-fidelity PHIL simulation. The characteristics of the PA, sensors, ADC and DAC, and other key components within the PI are key determinants of the stability, accuracy, and sensitivity of PHIL simulation. The PI, along with systems S_1 and S_2, can be expressed by their continuous-time system equivalent. By an approximation of the relevant system nonlinearities, the resulting transfer functions in the Laplace domain can be utilized and applied for theoretical analysis.

As shown in Fig. 2 and Fig. 3, the ITM interface can be decomposed into the digital interface, signal processing unit, and the analog interface. Depending on the type of power amplification and the controllable power sources implemented in the DRTS and hardware side, ITM can be categorized as voltage-type or current-type. Detailed modelling of these ITM interfaces are presented below.

1) VOLTAGE-TYPE ITM (V-ITM) INTERFACE

As presented in Fig. 2, the V-ITM is configured as a voltage source in hardware side and a current source in DRTS side, which are controlled by a voltage-type PA and current sensor, respectively. All key components and interface signals are represented in the form of a single-input-single-output (SISO) closed-loop PHIL system and the respective equivalent block diagram is presented in Fig. 2 (bottom). The open-loop transfer function $F_O^v(s)$ is given by

$$F_O^v(s) = \underbrace{e^{-s\tau_s} T_{FW}(s) T_{VA}(s)}_{C_v(s)} \frac{Z_1(s)}{Z_2(s)} \underbrace{e^{-s\tau_s} T_{FB}(s) T_{CM}(s)}_{P_v(s)}, \quad (1)$$

where $T_{FW}(s)$, $T_{FB}(s)$ represent the signal processing unit in the feed-forward and feed-back path respectively, $T_{VA}(s)$ represents the dynamic behavior of the PA in voltage mode, $T_{CM}(s)$ represents the current measurement unit, and τ_s is the time step size of the DRTS.

2) CURRENT-TYPE ITM (I-ITM) INTERFACE

In contrast to the V-ITM, as shown in Fig. 3, the I-ITM is configured as a current source on the hardware side and a voltage source on the software side, which are controlled by a current-type PA and a voltage sensor signal, respectively.

In analogy to the equivalent SISO closed-loop block diagram as, shown in Fig. 3 (bottom), the open-loop transfer function $F_O^i(s)$ of the I-ITM PHIL setup is given by

$$F_O^i(s) = \underbrace{e^{-s\tau_s} T_{FW}(s) T_{CA}(s)}_{C_i(s)} \frac{Z_2(s)}{Z_1(s)} \underbrace{e^{-s\tau_s} T_{FB}(s) T_{VM}(s)}_{P_i(s)}, \quad (2)$$

where $T_{CA}(s)$ represents the dynamic behavior of the PA in current mode and $T_{VM}(s)$ represents the voltage measurement unit.

C. PHIL SYSTEM CHARACTERISTICS AND PROPERTIES

Inherent time delays within the PHIL setup [15] and the characteristics of the PA [26] play a major role in the stability and accuracy of PHIL setups, and therefore the stability and accuracy of such setups is not guaranteed even upon selection of an appropriate interface. The stability analysis and accuracy assessment are crucial for a PHIL setup prior to its final implementation.

1) STABILITY

Once the open-loop transfer function $F_O(s)$ of the SISO closed-loop system in Fig. 2 or Fig. 3 is obtained, the system stability can be assessed by applying suitable stability criteria such as the Nyquist or the Routh–Hurwitz criterion [28] to the system characteristic equation that is given by

$$1 + F_O(s) = 0. \tag{3}$$

The gain margin (GM) and phase margin (PM) are key factors to determine the closed-loop stability from the open-loop transfer function. Provided that the GM and PM are positive, the PHIL stability is guaranteed if the magnitude and phase responses of the open-loop transfer function $F_O(s)$ satisfy the following criteria

$$\begin{cases} GM = 0 - 20log(\left|F_O(j\omega_{cp})\right|), & GM > 0, \\ PM = \angle F_O(j\omega_{cg}) - (-180°), & PM > 0, \end{cases} \tag{4}$$

where ω_{cg} is the gain crossover frequency at which the magnitude of $F_O(s)$ is 0 dB, ω_{cp} is the phase crossover frequency at which the phase of $F_O(s)$ crosses $-180°$.

2) ACCURACY

Based on the equivalent block diagram and transfer functions of the PHIL system, the accuracy of PHIL simulation can be analyzed and assessed. For instance, the closed-loop transfer function between the analog voltage $U_A(s)$ and the equivalent voltage source $U_S(s)$ in the V-ITM PHIL setup is given by

$$T_C(s) = \frac{U_A(s)}{U_S(s)} = \frac{C_v(s)}{1 + F_O^v(s)}. \tag{5}$$

Assuming the ITM interface presents unity-gain and infinite bandwidth characteristics without any time delay, such that $C_v(s) = P_v(s) = 1$, the PHIL system is equivalent to the original SOI. For an idealized PHIL simulation setup, the ideal closed-loop transfer function $T_{C,id}(s)$ relates system voltages $U_A(s)$ and $U_S(s)$, respectively, resulting in

$$T_{C,id}(s) = \frac{U_A(s)}{U_S(s)} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)}. \tag{6}$$

For a given signal $U_A(s)$, the accuracy can be quantitatively analyzed by employing the relative error $\epsilon(s)$ that quantifies the deviation between the ideal PHIL case and the actual PHIL case. The relative error $\epsilon(s)$ is defined by

$$\epsilon(s) = \left| \frac{T_C(s) - T_{C,id}(s)}{T_{C,id}(s)} \right|. \tag{7}$$

Alternatively, as presented in [5] and [24], the accuracy metrics including the power signal tracking error or the measurement to reference signal error, serve as an useful metrics to quantitatively assess the accuracy of the PHIL setups.

III. FRAMEWORK FOR THE SENSITIVITY ANALYSIS OF PHIL SIMULATION SYSTEMS

This section presents the proposed comprehensive framework for sensitivity analysis. First, the principles of sensitivity analysis are explained followed by the derivation of sensitivity functions for PHIL simulation setups. The relationship between the sensitivity analysis and the stability and accuracy of PHIL setups is then established.

A. MODELLING PRINCIPLES

The sensitivity analysis of PHIL systems requires the derivation of sensitivity functions. A sensitivity function represents the relationship between a disturbance and the signal of interest in frequency domain. Its characteristics may indicate the attenuation or the amplification of the disturbance within the signal of interest for each frequency and its corresponding phase shift. The disturbances in PHIL setups mainly stem from the non-ideal PI, affecting the digital signals U_D and I_D as well as the analogue signals U_A and I_A of the PI. These disturbances are identified within Fig. 4 and Fig. 5, denoted by the symbol δ as a prefix.

B. SENSITIVITY FUNCTIONS FOR PHIL SIMULATION SETUPS

The sensitivity function $S_1(s)$ of signals of interest $U(s)$ or $I(s)$ related to associated local disturbances $\delta U(s)$ or $\delta I(s)$, respectively, is defined as

$$S_1(s) = \begin{cases} \dfrac{U_A(s)}{\delta U_A(s)} = \dfrac{1}{1 + F_O(s)}, \\ \dfrac{U_D(s)}{\delta U_D(s)} = \dfrac{1}{1 + F_O(s)}, \\ \dfrac{I_A(s)}{\delta I_A(s)} = \dfrac{1}{1 + F_O(s)}, \\ \dfrac{I_D(s)}{\delta I_D(s)} = \dfrac{1}{1 + F_O(s)}. \end{cases} \tag{8}$$

where subscripts A and D represent analogue and digital signals, respectively. Sensitivity functions for other disturbances with respect to the signal of interest can be derived in a similar manner. The following two sub-sections present the sensitivity functions for the two types of the ITM interface.

1) V-ITM SENSITIVITY FUNCTIONS

The model and block diagram representation of the V-ITM interface algorithm in Fig. 2 is extended by incorporating the relevant disturbances as shown in Fig. 4. The analogue current I_A fed back from the hardware to the software side represents the signal of interest for V-ITM and is employed for the following analysis. The sensitivity metrics for analyzing the impact of the identified disturbances on the signal of interest I_A are defined as

$$\begin{cases} S_1^v(s) = \dfrac{I_A(s)}{\delta I_A(s)} = \dfrac{1}{1 + F_O^v(s)}, \\ S_2^v(s) = \dfrac{I_A(s)}{\delta U_A(s)} = \dfrac{1/Z_2(s)}{1 + F_O^v(s)}, \\ S_3^v(s) = \dfrac{I_A(s)}{\delta U_D(s)} = \dfrac{C_v(s)/Z_2(s)}{1 + F_O^v(s)}, \\ S_4^v(s) = \dfrac{I_A(s)}{\delta I_D(s)} = \dfrac{-C_v(s)Z_1(s)/Z_2(s)}{1 + F_O^v(s)}. \end{cases} \tag{9}$$

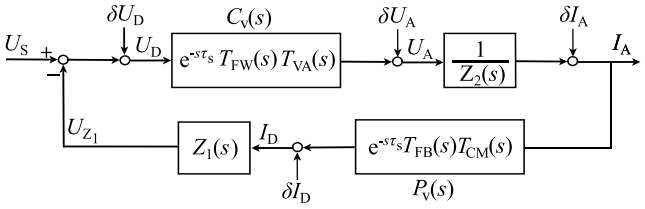

FIGURE 4. Block diagram of PHIL with V-ITM interface.

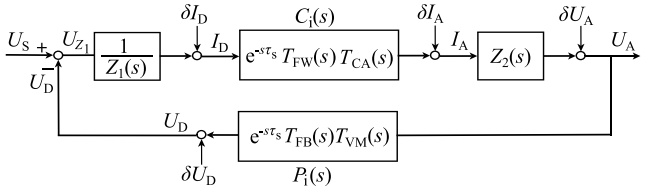

FIGURE 5. Block diagram of PHIL with I-ITM interface.

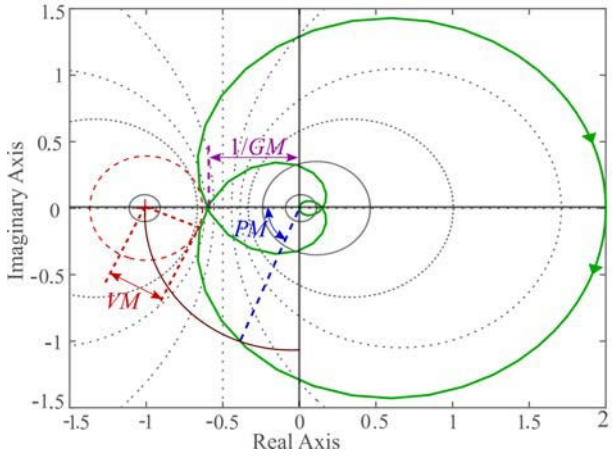

FIGURE 6. Nyquist diagram of an arbitrary open-loop transfer function $F_O(s)$ highlighting gain, phase, and vector margins.

2) I-ITM SENSITIVITY FUNCTIONS

In analogy to III-B1, the model and block diagram representation of the I-ITM interface algorithm in Fig. 3 is extended by including the relevant disturbances as given in Fig. 5. The analogue voltage U_A fed back from the hardware to the software side in the I-ITM represents the signal of interest. The sensitivity metrics for analyzing the impact of the identified disturbances on the voltage U_A can be derived by following the similar manner as (9). On the other hand, the analysis of the impact of the disturbance associated with the signal of interest on all the interface signals within the PHIL setup is also crucial. For the disturbance δU_A, the sensitivity metrics for analyzing its impact on the analogue and digital signals are defined as

$$\begin{cases} S_1^i(s) = \dfrac{U_A(s)}{\delta U_A(s)} = \dfrac{1}{1+F_O^i(s)}, \\ S_2^i(s) = \dfrac{U_D(s)}{\delta U_A(s)} = \dfrac{P_i(s)}{1+F_O^i(s)}, \\ S_3^i(s) = \dfrac{I_D(s)}{\delta U_A(s)} = \dfrac{-P_i(s)/Z_1(s)}{1+F_O^i(s)}, \\ S_4^i(s) = \dfrac{I_A(s)}{\delta U_A(s)} = \dfrac{-C_i(s)P_i(s)/Z_1(s)}{1+F_O^i(s)}. \end{cases} \tag{10}$$

C. SENSITIVITY ANALYSIS AND STABILITY

For a disturbance with frequency ω, the magnitude of the sensitivity function $S_1(j\omega)$ defined in (8) is given by

$$|S_1(j\omega)| = \left| \frac{1}{1+F_O(j\omega)} \right|. \tag{11}$$

For each frequency ω, $|S_1(j\omega)|$ corresponds to the reciprocal of the distance of the Nyquist curve to the Nyquist point (-1, 0) [28]. The shortest distance between the Nyquist curve and the Nyquist point is referred to as the vector margin (VM), as shown in Fig. 6. The magnitude of the sensitivity function at this point is at its maximum value calculated as $|S_1(j\omega)|_{max}$. The greater the value of $|S_1(j\omega)|_{max}$ is, the closer the Nyquist curve is to the Nyquist point. In this case, the PHIL system is less robust.

The maximum magnitude of the sensitivity function given by $|S_1(j\omega)|_{max}$ indicates the robustness of overall PHIL stability and is given by

$$|S_1(j\omega)|_{max} = \left| \frac{1}{1+F_O(j\omega_0)} \right|_{max}, \tag{12}$$

or

$$VM = \frac{1}{|S_1(j\omega)|_{max}}. \tag{13}$$

Fig. 6 illustrates the relationship between the gain margin GM, phase margin PM, and the vector margin VM, with their relationship to guarantee stability being derived from following relations

$$\begin{cases} VM + \dfrac{1}{GM} & \le 1, \\ VM & \le sin(PM). \end{cases} \tag{14}$$

Substituting (13) into (14), the inequalities between the sensitivity function and stability margins are given by

$$\begin{cases} \dfrac{1}{|S_1(j\omega)|} & \le \dfrac{GM-1}{GM}, \quad \forall \omega > 0, \\ \dfrac{1}{|S_1(j\omega)|} & \le sin(PM), \quad \forall \omega > 0. \end{cases} \tag{15}$$

D. SENSITIVITY ANALYSIS AND ACCURACY

The magnitude of the sensitivity function determines the extent to which the external disturbance distorts the output signal and deteriorates the simulation accuracy, while the phase response indicates the corresponding phase shift. Based on the sensitivity metrics in (9), (10), the impact of the external disturbance on the system output can be analyzed and quantified. For accuracy assessment in the continuous-time domain, the following methodologies are employed to quantify how the disturbances distort the PHIL accuracy in this framework:

- THD+N: DFT-based signal decomposition and calculation of the weighted function of the magnitude of signal with the frequency of interest and the aggregated magnitude of signals excluding the frequency of interest given by

$$THD + N = \frac{\sqrt{\sum_{i=2}^{n} U_i^2 + U_{noise}^2}}{U_1} \times 100\%, \quad (16)$$

where U_i is the RMS value of the i-th harmonic voltage, U_{noise} is the RMS value of the noise signal, and U_1 is the RMS value of the voltage signal with fundamental frequency component.

- Signal to noise ratio (SNR): The SNR is calculated by

$$SNR\,(dB) = 10log\Big(\frac{P_s}{P_n}\Big), \quad (17)$$

where P_s is the power of the signal with fundamental frequency component only and P_n is the power of the signal excluding the fundamental frequency component.

IV. ANALYTICAL ASSESSMENT OF THE SENSITIVITY FRAMEWORK

This section presents an analytical assessment of the sensitivity functions related to potential disturbances within the PHIL setup and given outputs of interest. Sensitivity analysis is performed for PHIL systems with V-ITM and I-ITM interfaces.

A. SENSITIVITY ANALYSIS OF V-ITM INTERFACE

Sensitivity properties are evaluated by means of the block diagram representation presented in Fig. 4. The analysis focuses on the impact of disturbances on the analogue current I_A fed back from the PA to the software side, considering the sensitivity transfer functions defined in (9). System impedances $Z_1(s)$, $Z_2(s)$, the line-to neutral voltage $U_{S,LN}$, the fundamental frequency f_0, and related transfer functions for the chosen numerical setup are reported in Table 2. The evaluation of the open-loop transfer function defined in (1) according to the numerical quantities of Table 2 yields to:

$$F_O(s) = \frac{32.58\, e^{-s\,1.03\cdot 10^{-4}}}{s^3\, 2.64\cdot 10^{-13} + s^2\, 8.0\cdot 10^{-7} + s + 2199}. \quad (18)$$

To ensure linearity and thus make the system amenable for analysis, a (1,1) Padé approximation [29] has been chosen to represent the time delays in the transfer function expressions. For an arbitrary delay τ, the associated exponential in the Laplace domain is replaced by a first-order linear function

$$e^{-s\tau} \approx \frac{1 - s\frac{\tau}{2}}{1 + s\frac{\tau}{2}}. \quad (19)$$

Considering this approximation, the Nyquist diagram of $F_O^v(s)$ and Bode diagrams of $F_O^v(s)$ and $S_{2,3,4}^v(s)$ are shown in Fig. 7 and Fig. 8, respectively. From Fig. 7, it is straightforward to determine that the closed-loop system is stable, since the number of encirclement of the Nyquist curve around the $(-1, 0)$ point and the number of positive poles in $F_O^v(s)$ are both equal to zero. From the Nyquist diagram, one can also assess that the system has infinite phase margin, since any rotation of the curve does not change the number of encirclements around $(-1, 0)$. This is confirmed in Fig. 8, where it is shown that the gain of $F_O^v(s)$ is smaller than 1 for all frequencies. The GM is also straightforward to compute and it is equal to 54.6 dB, obtained at a frequency of approximately 2.75 kHz.

To quantify the stability robustness of the system with respect to simultaneous gain and phase variations of the open loop transfer function, the vector margin VM has been computed as the inverse of the maximum magnitude of S_1^v and is equal to 0.9977. This implies robustness of the system, as a combined variation of gain and phase in $F_O^v(s)$ would still require an added gain of $20\log_{10}(1/(1 - VM)) = 52.72$ dB

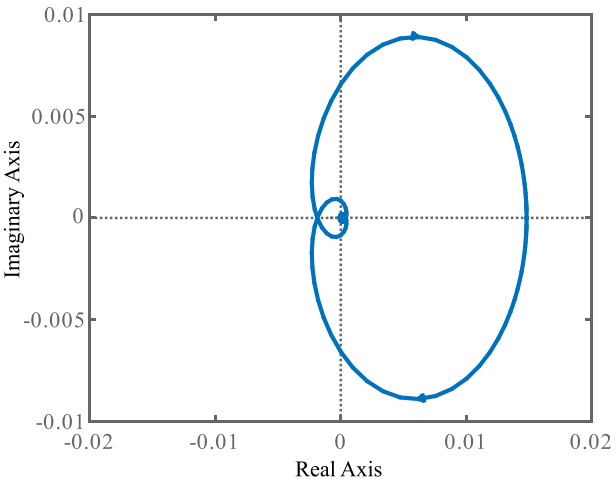

FIGURE 7. Nyquist diagram of the open-loop transfer function $F_O^v(s)$.

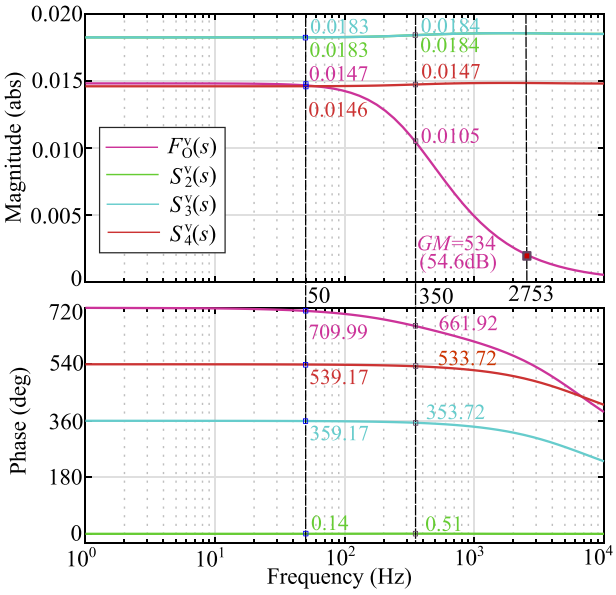

FIGURE 8. Frequency response of the open-loop transfer function $F_O^v(s)$ and sensitivity functions $S_{2,3,4}^v(s)$ in (9).

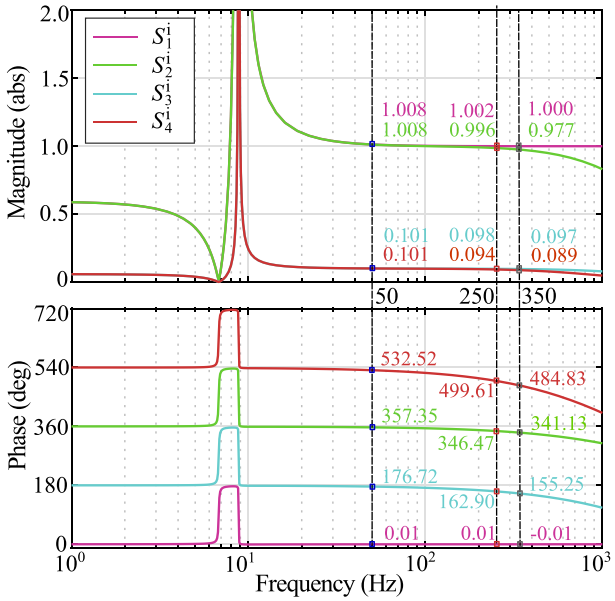

FIGURE 9. Frequency response of sensitivity transfer functions $S^i_{1,2,3,4}(s)$ in (10).

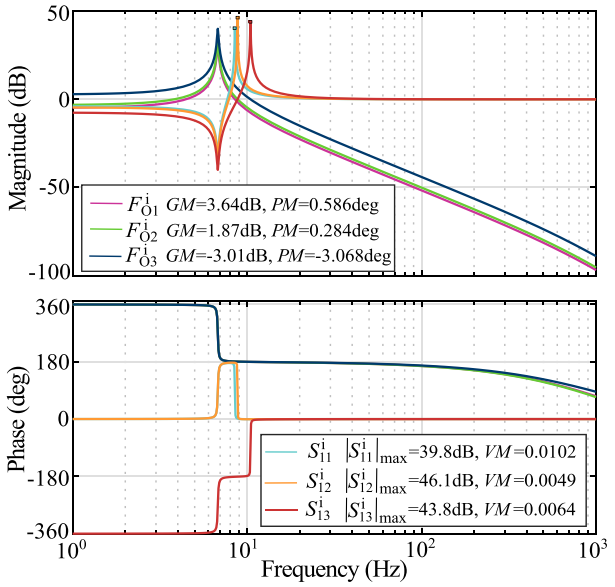

FIGURE 10. Bode diagram of open-loop and sensitivity transfer functions $F^i_{O1,2,3}(s)$, $S^i_{11,12,13}(s)$.

to lead to instability. It is worth noting that this property is strictly related to the ratio Z_1/Z_2. For example, when choosing $Z_1 = 27\,\Omega$ and an impedance ratio of 0.5, gain and vector margins result to 24 dB and 0.92, respectively.

Having analyzed the system stability, the sensitivity of the chosen setup with respect to external disturbances is now quantified. For the chosen V-ITM interface, the analysis has focused on the impact of disturbances δU_D of the voltage U_D on the current I_A that is fed back to the software side of the PHIL simulation setup. For the chosen parameter, the Bode diagram of $S^v_3(s)$, as defined in (9), is represented in light-blue in Fig. 8.

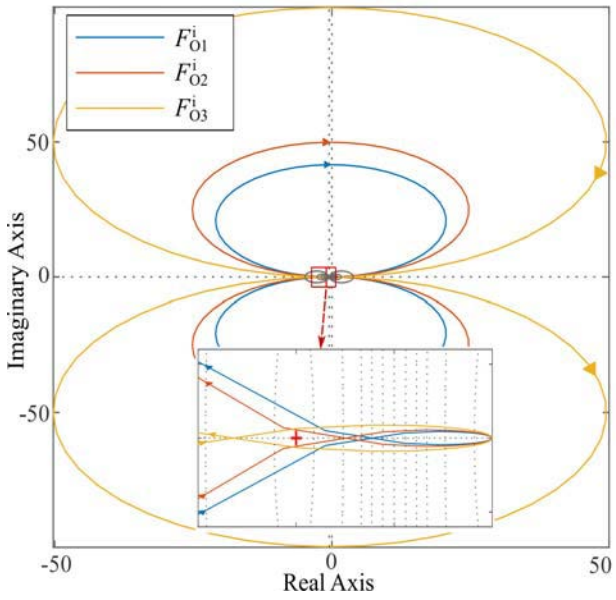

FIGURE 11. Nyquist plot of open-loop transfer functions $F^i_{O1,2,3}(s)$.

TABLE 1. Stability margins of the I-ITM open-loop transfer functions $F^i_{O1,2,3}(s)$.

Transfer Function	*Software Impedance* (Ω)		*GM (abs)*	*PM (deg)*	*VM (abs)*
$F^i_{O1}(s)$	$Z_{11}(s)$	$12 + s4.775e^{-4}$	1.5205	0.586	0.0102
$F^i_{O2}(s)$	$Z_{12}(s)$	$10 + s4.775e^{-4}$	1.2402	0.284	0.0049
$F^i_{O3}(s)$	$Z_{13}(s)$	$5 + s4.775e^{-4}$	0.7071	-3.0680	0.0064

In the present case, disturbances with frequencies up to 10 kHz are attenuated by 34.8 dB representing a gain of approximately 0.0184, with an even more consistent reduction at higher frequencies. The phase shift is negligible up to 350 Hz and then gradually decreases, until reaching −180 degrees at about 10 MHz.

B. SENSITIVITY ANALYSIS OF I-ITM INTERFACE

The stability and sensitivity analysis has also been performed for the I-ITM interface, considering the block diagram in Fig. 5. The parametrization of this PHIL setup is tabulated in Table 3 in Appendix A. The analysis discusses a numerical case representing a realistic scenario and which is consistent with experimental results from Section V-B.

In this case, the sensitivity analysis has focused on the impact of the output voltage disturbance δU_A of the power converter, stemming from the measurement noise and switching of the power converter as HUT, on the analogue and digital interface signals in the PHIL setup. For a given disturbance with frequency ω, the frequency-dependant magnitude and phase response of the analogue and digital signals can be derived from the sensitivity metrics in (10) for further analysis. For the disturbance δU_A, the magnitude and phase

FIGURE 12. Experimental setup of the implemented PHIL simulation system with applied V-ITM interface.

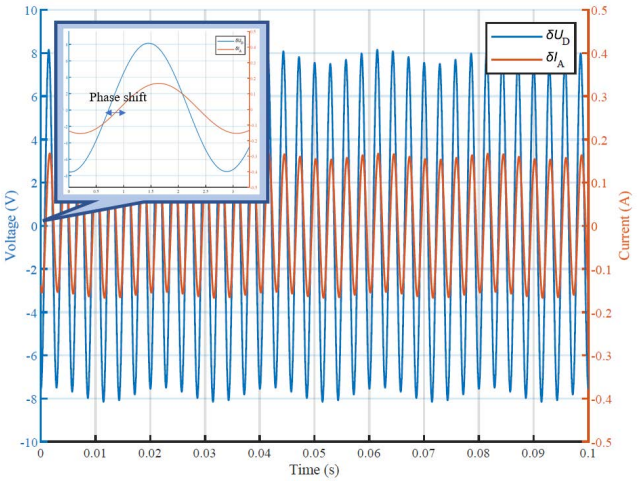

FIGURE 13. Voltage disturbance δU_D and current disturbance δI_A.

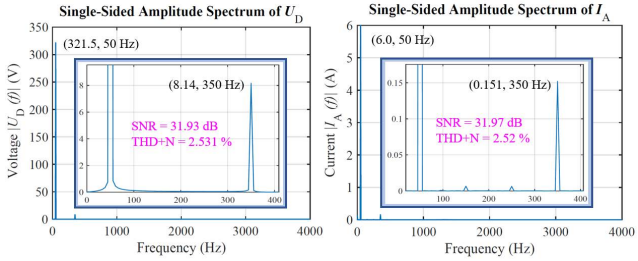

FIGURE 14. Frequency spectrum of perturbed signals U_D and I_A, and SNR and THD+N measurements.

response of the interface signals U_A, U_D, I_A, and I_D over certain frequencies of interest are highlighted in Fig. 9.

For the analytical assessment of the sensitivity and stability criteria defined in Section III-C, a case study involving different software side impedance as given in Table 1 is discussed. Fig. 10 presents the frequency response of the open-loop transfer functions $F^i_{O2,3,4}(s)$ and their corresponding sensitivity functions $S^i_{11,12,13}(s)$, of which the stability margins and the maximum magnitude are given in Table 1. Gain and phase margins of $F^i_{O1}(s)$ and $F^i_{O2}(s)$ as well as the maximum magnitude of the sensitivity functions $S^i_{11}(s)$ and $S^i_{12}(s)$ satisfy the inequality criteria defined in (14), (15). Therefore, these systems are stable which is consistent with the stability status as indicated in the Nyquist plot in Fig. 11. However, the gain and phase margin of $F^i_{O3}(s)$ as well as the maximum magnitude of the sensitivity function $S^i_{13}(s)$ do not satisfy the inequality criteria defined in (14), (15) and therefore, the corresponding PHIL setup is unstable.

V. EXPERIMENTAL ASSESSMENT OF THE SENSITIVITY FRAMEWORK

For the evaluation of the sensitivity framework, two experimental studies were carried out. The first case study considers a PHIL setup with V-ITM interface algorithm while the second utilizes a PHIL setup with I-ITM interface algorithm, both providing a straight comparison to the previously identified sensitivity transfer functions in (9), (10) respectively.

A. EXPERIMENTAL V-ITM PHIL SETUP

The first experiment conducted for the validation of the sensitivity framework concerns a PHIL setup with applied V-ITM interface. The setup comprises a DRTS, a linear-mode PA with a nominal output power of 5 kVA, and a passive load bank. For experimental validation, the characteristics of the setup, both in the simulation and hardware side, were chosen such as to keep the total stochastic behavior and the non-relative factors that might impact the sensitivity analysis to a minimum. Compared with the setup for the analytical evaluation from Table 2, software and hardware impedances remain unchanged allowing for a direct comparison of results.

Theoretical analysis investigates the impact of disturbance δU_D on the feedback current signal I_A. To evaluate the impact in experimental setup, a seventh harmonic (350 Hz) sinusoidal signal has been chosen in the time domain as the disturbance, with peak value of 8.16 V, 2.5% of nominal voltage amplitude. The higher harmonic signal is superimposed in the output digital voltage signal of DRTS and subsequently applied to the amplifier. The output is observed and the impact is experimentally quantified in terms of changes in magnitude and phase of the 7th harmonic current component.

Fig. 13 presents the harmonic content of the voltage δU_D and the current δI_A, while the spectrum, the SNR, and THD+N of the two perturbed signals U_D and I_A are presented in Fig. 14, providing an accurate assessment of the accuracy of the experimental setup. The amplitude of the seventh harmonic component of the current is 0.151 A, and is in compliance with the theoretical analysis as in Fig. 8. The phase of the 7th harmonic component of current lags the 7th harmonic component of the voltage by 22 degrees.

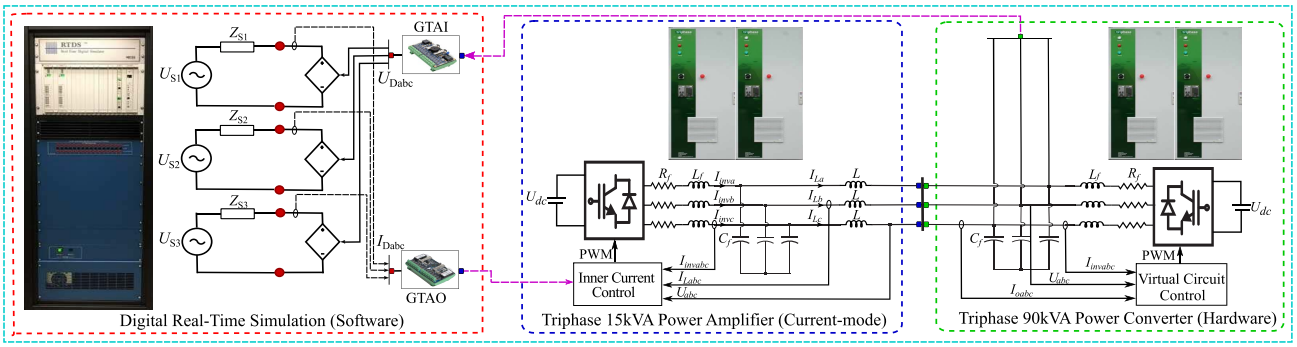

FIGURE 15. Experimental setup of the implemented PHIL simulation system with applied I-ITM interface.

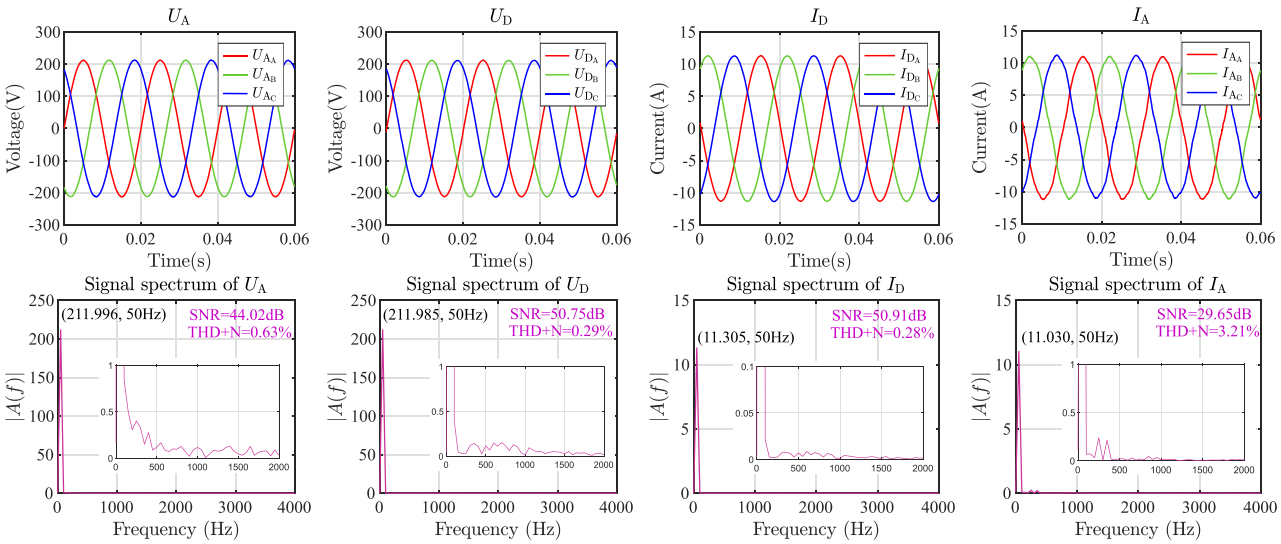

FIGURE 16. Waveforms and corresponding signal spectrum of interface signals without external harmonics injection.

According to the phase bode plot of Fig. 8, the expected phase lag of the current's harmonic component is 6.28 degrees. This discrepancy in phase lag is due to the difference in time delay considered for theoretical analysis compared to the time delays that actually exist within an experimental setup. Theoretical analysis considers that the delay introduced by the DRTS is equal to one time-step. While the time delay is typically considered constant, [15], [27] point out that the introduced time delays can vary significantly within an experimental PHIL setup. More specifically, in [27], it is demonstrated that the delay introduced from the sampling time can vary between 1 and 3 time steps of the DRTS. In the presented case study, the phase difference between 6.28 and 22 degrees equates to 11.9 μs, which relates to approximately 2.38 time steps. This delay deriving from processing inputs and outputs has been verified through DRTS simulation without hardware connection, confirming an identical the phase lag between voltage and current harmonics with the PHIL experiment. While it is expected that the PA introduces an additional phase lag, the 3.1 μs delay introduced by the linear PA is negligible in comparison to the delay of the DRTS.

B. EXPERIMENTAL I-ITM PHIL SETUP

This case study involves incorporating a voltage source back-to-back converter into a PHIL simulation setup by applying the I-ITM interface. Fig. 15 illustrates the setup for this PHIL experimental test. The digital current signal I_D measured from the real-time network model is transmitted to the Triphase 15 kVA (TP15 kVA) current-type PA as a command signal to command the resulting output current I_A. The output terminal of the TP15 kVA is coupled with that of the Triphase 90 kVA (TP90 kVA) power converter with the former sourcing current to the latter. The output voltage U_A of the TP90 kVA is measured and transmitted to the DRTS as the command voltage signal U_D for the controllable voltage source. For the modelling process, the parametrization of each component in this PHIL setup is shown in Table 3.

An equivalent voltage source with a nominal line-to-line (LL) AC voltage $U_{S,LL}$ of 400 V, and the fundamental frequency f_0 of 50 Hz emulates a low-voltage grid. A low X/R ratio grid impedance, as listed in Table 3, emulates a strong grid. The output voltage of the TP90 kVA power converter

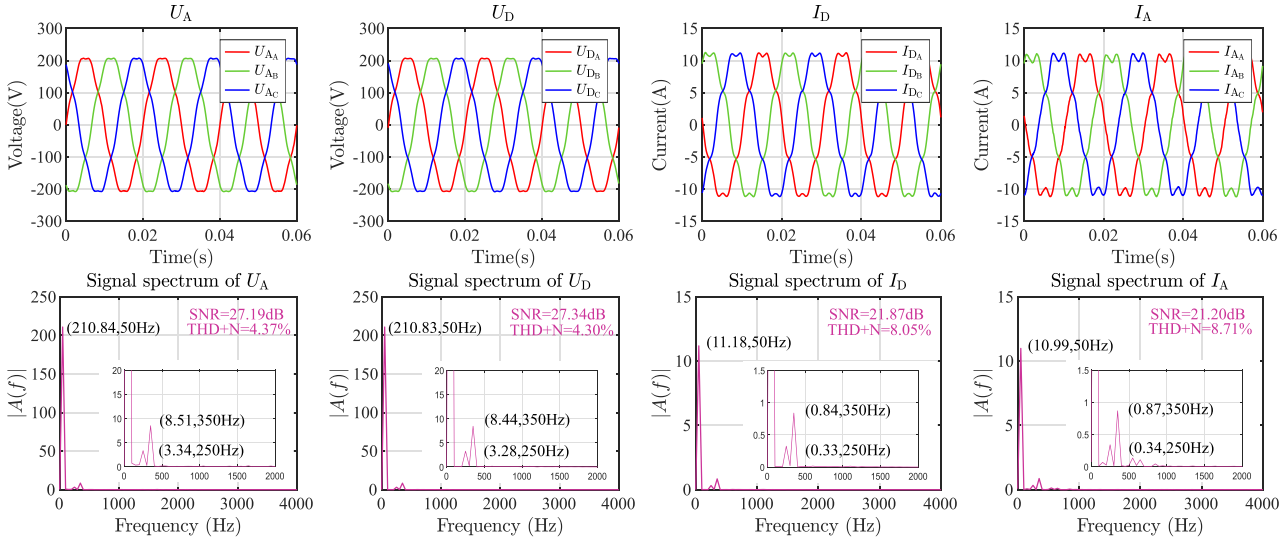

FIGURE 17. Waveforms and corresponding signal spectrum of interface signals with fifth and seventh harmonics injection.

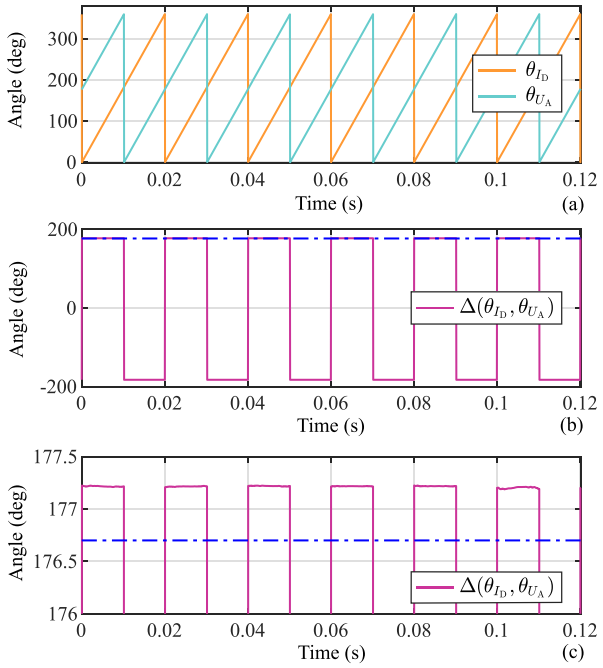

FIGURE 18. I-ITM setup: (a) phase angle of I_D and U_A with fundamental frequency (50 Hz), (b) phase difference between I_D and U_A, (c) zoomed-in version of (b).

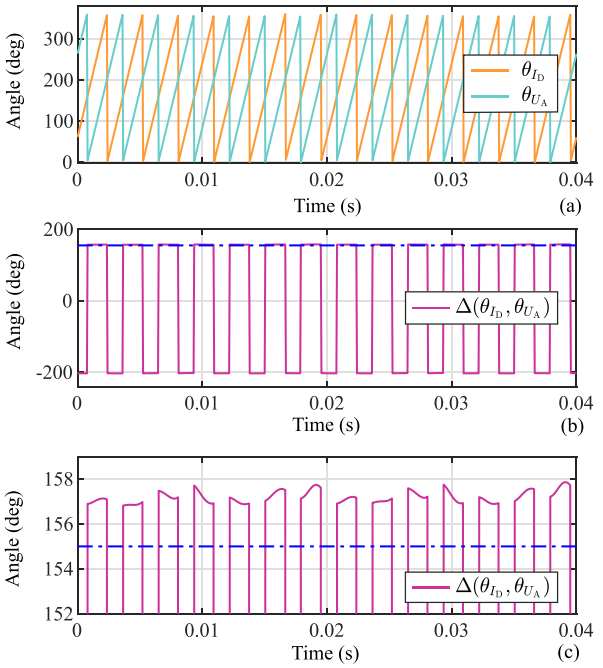

FIGURE 19. I-ITM setup: (a) phase angle of I_D and U_A with seventh harmonic (350 Hz), (b) phase difference between I_D and U_A, (c) zoomed-in version of (b).

was regulated at a LL AC voltage of 260 V, 50 Hz. The digital signals U_D and I_D are recorded with a sampling rate of 20 kHz in DRTS and the analogue signals U_A and I_A are recorded with a sampling rate of 8 kHz by the Triphase datalogger.

1) PHIL SYSTEM WITHOUT EXTERNAL DISTURBANCE INJECTION

Fig. 16 shows waveforms of interface signals of the PHIL setup and their single-sided amplitude spectrum. The analogue signal U_A is distorted by the harmonics and high-frequency noise introduced by the pulsating modulation of the converter. Due to the implementation of a low-pass filter with a cut-off frequency of 1500 Hz, the digital voltage U_D presents a higher SNR and lower THD+N than that of the analogue voltage U_A and is less noisy. The SNR and THD+N of the digital current I_D are approximately equal to that of the digital voltage U_D. However, the amplitude of most frequency components of I_A are greater than that of the reference signal I_D and correspondingly the current I_A presents a lower

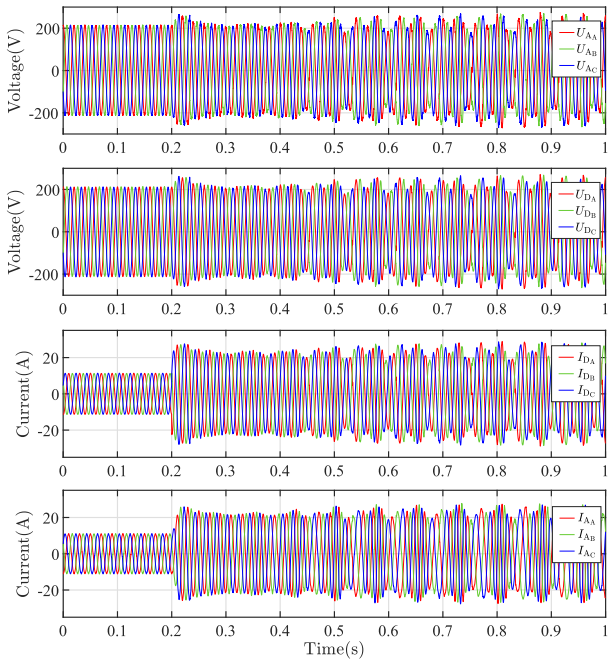

FIGURE 20. Interface signals of the I-ITM PHIL setup with varying grid impedance $Z_{12}(s)$ and $Z_{13}(s)$ as given in Table 1.

SNR and higher THD+N than that of the current I_D. The inherent disturbances stemming from aforementioned signal conversions and high-frequency pulsating modulation at each stage deteriorate the interface signals.

2) PHIL SYSTEM WITH EXTERNAL DISTURBANCE INJECTION

Fig. 17 presents waveforms of interface signals and their single-sided amplitude spectrum. To demonstrate the impact of the disturbance δU_A on the interface signals, the fifth (0.015 p.u.) and seventh (0.04 p.u.) harmonics are injected in the output voltage of the TP90 kVA power converter. All interface signals show lower SNR and higher THD+N than those of the scenario without external harmonics injection. Due to the magnitude attenuation and phase shift of the amplifier, significant discrepancy between the digital current I_D and the analogue current I_A are existent throughout the entire range of frequency of interest as shown in Fig. 17. Apart from the frequencies of interest, the amplitude spectrum of I_A presents higher portion of harmonics than the digital signal which derives from the high-frequency modulation of the converter.

Sensitivity can be assessed through the signal spectrum of interface signals and the phase response of dedicated interface signals over the frequency of interest. As illustrated in the frequency spectrum of Fig. 17, the magnitude responses of the interface signals (i.e., U_D, I_D, I_A) with respect to an externally injected harmonic signal (δU_A) over the frequency of interest are consistent with the magnitude responses of sensitivity metrics (i.e., $S_2^i(s)$, $S_3^i(s)$, $S_4^i(s)$) in Fig. 9. In terms of the phase response assessment of the sensitivity metrics, taking the voltage signal U_A and current signal I_D as examples, the phase shifts of the interface signal I_D against the externally injected voltage signal U_A with a fix harmonic can be directly revealed from their phase response. Fig. 18(a) presents the phase response of I_D and U_A over the fundamental frequency. Based on these phase responses, the phase difference between these two interface signals is calculated and illustrated in Fig. 18(b) and Fig. 18(c). This phase difference slightly deviates from the constant value 176.72 deg (blue dashed line) that corresponds to the phase response of the sensitivity metric ($S_3^i(s)$) at the fundamental frequency in Fig. 9. Furthermore, the phase response of I_D and U_A over the seventh harmonics is presented in Fig. 19(a) along with their phase difference as presented in Fig. 19(b) and Fig. 19(c). Once again, this phase difference deviates from the phase response (155.25 deg) of the sensitivity metric ($S_3^i(s)$) at 350 Hz in Fig. 9. The discrepancy between the experimental phase shift and the phase shift of the analytical sensitivity metric may arise from the the additional time delay stemming from the current or voltage measurement units, and the variable time delay in the power amplifier.

3) PHIL SYSTEM STABILITY EXPERIMENTAL ASSESSMENT

Based on the I-ITM PHIL setup, grid side impedance variations are emulated to verify the stability and sensitivity criteria. Impedances $Z_{12}(s)$ to $Z_{13}(s)$ are modified at $t = 0.2$ s, as given in Table 1, and the interface signals are shown in Fig. 20. After the impedance change, the interface signals present significant oscillations and the PHIL system is unstable. This is consistent with the analytical stability analysis in Section IV-B. As given in Table 1, the stability margin decreases as a result of the grid side impedance decrement. When the grid side impedance witness a variation from $Z_{12}(s)$ to $Z_{13}(s)$, the inequalities between gain margin, phase margin and vector margin defined in (14) and (15) are no longer guaranteed and the system becomes instable.

VI. CONCLUSION

This work presents a comprehensive framework for the purpose of sensitivity analysis for PHIL simulation systems. One major contribution is represented by the introduction of an analytical modelling of PHIL systems with particular reference to potential disturbances causing sensitivity issues regarding interfacing methodologies. Based on modeling principles, sensitivity transfer functions for PHIL setups with voltage-type and current-type interfaces are introduced. The introduced sensitivity functions are of major importance when evaluating robustness or enhanced stability properties of PHIL setups with power interfacing techniques. Based on the generic concept using continuous time-modeling, sensitivity analysis can be performed for PHIL systems.

A second major contribution is given by the analytical and experimental assessment of the proposed sensitivity

TABLE 2. Model parametrization of the PHIL simulation setup with applied V-ITM interface.

Description	*Symbol*	*Unit*	*Value*
Time step size	τ_s	µs	50
Software side voltage source	$U_{S,LN}$	V	230
Fundamental frequency	f_0	Hz	50
Software system impedance	$Z_1(s)$	Ω	0.8
Hardware system impedance	$Z_2(s)$	Ω	54
Voltage-type PA; Equivalent delay and filter as identified in [4]	$T_{VA}(s)$	-	$\frac{e^{-s3.1e^{-6}}}{s^2 2.642e^{-13}+s0.8e^{-6}+1}$
Current measurement	$T_{CM}(s)$	-	1
Forward signal processing	$T_{FW}(s)$	-	1
Feedback low-pass filter	$T_{FB}(s)$	-	$\frac{1}{(1/2\pi 350)s+1}$

TABLE 3. Model parametrization the PHIL simulation setup with applied I-ITM interface.

Description	*Symbol*	*Unit*	*Value*
Time step size	τ_s	µs	50
Software side voltage source	$U_{S,LL}$	V	400
Fundamental frequency	f_0	Hz	50
Software system impedance Emulated grid impedance	$Z_1(s)$	Ω	$10 + s4.775e^{-4}$
Hardware system impedance Converter output impedance [30]	$Z_2(s)$	Ω	$\frac{s5.5e^{-4}+6.842}{s^2 5.5e^{-4}+s3.216e^{-4}+1}$
Current-type PA; Current control transfer function with delay compensation [24]	$T_{CA}(s)$	-	$\frac{1}{(1/2\pi 768)s+1}$
Voltage measurement	$T_{VM}(s)$	-	1
Forward signal processing	$T_{FW}(s)$	-	1
Feedback low-pass filter	$T_{FB}(s)$	-	$\frac{1}{(1/2\pi 1500)s+1}$

framework. By identifying a set of sensitivity transfer functions, analysing resulting Bode diagrams, the sensitivity behaviour and system properties such as stability or accuracy may be determined in a reproducible and accurate way.

Finally, a comparison of results confirms the applicability of the sensitivity framework for PHIL test setups, in practice. The entire sensitivity framework is introduced as a guideline providing valuable information regarding design principles and system analysis, and decision making referring to the choice of interfacing techniques is so supported.

APPENDIX A SETTINGS AND PARAMETRIZATION OF TEST SETUPS FOR THE ANALYTICAL AND EXPERIMENTAL ASSESSMENT

A. V-ITM INTERFACE

System parametrization used for analysis of the V-ITM interface in Section IV-A, and in the corresponding experimental setup in Section V-A are reported in Table 2. The signal processing in the forward path $T_{FW}(s) = 1$ is assumed to be ideal, whereas the impact of the voltage amplifier includes a delay of 3.1 µs characterized as an exponential function in $T_{VA}(s)$. For the feedback loop, the analogue interface is also considered to be ideal with $T_{CM}(s) = 1$, while the effect of the feedback processing is modelled by choosing $T_{FB}(s)$ as a low pass filter with a cut-off frequency of 350 Hz.

B. I-ITM INTERFACE

System parametrization used for analysis of the I-ITM interface in Section IV-B, and in the corresponding experimental setup in Section V-B, is reported in Table 3. For this setup, the time step size and the fundamental frequency are set as 50 µs and 50 Hz, respectively and the line-to-line software side voltage is 400 V. The forward signal processing and the feedback voltage measurement are assumed to be ideal, thus respective transfer functions $T_{FW}(s)$ and $T_{VM}(s)$ are equal to 1. The current-type PA shows a low-pass behaviour with a cut-off frequency of 768 Hz, as highlighted in the table. The cut-off frequency of $T_{FB}(s)$ is 1500 Hz. Complex software and hardware system impedances including grid impedance properties as well as the converter output impedance are shown in Table 3.

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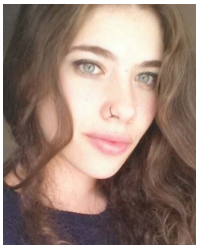

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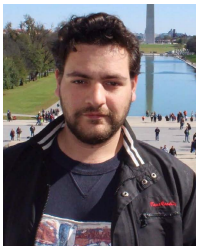

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