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RESEARCH ARTICLE

TCAD Simulation of Single Event Transient in Si Bulk MOSFET at Cryogenic Temperature

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ABSTRACT In this paper, the functional relationship between temperature and single event transient currents caused by heavy-ion striking using TCAD simulation is investigated from 77K to 300 K on 65nm Si bulk n MOSFET. TCAD simulation shows that temperature has a significant influence on the trends of heavy-ions-induced current. The peak value of drain current and collected charge in MOSFET reach the maximum value at 200 K, while the SET fall time decreases monotonously as temperature decrease from 300 K to 77 K at four LET values. The extracted analysis found that the enhancement of bipolar amplification effect is the main reason for the increase of collected charge and broader pulse width at high temperatures. The above conclusions provide a theoretical basis for the wide application of 65nm devices in 77 K-300 K space environment.

INDEX TERMS Heavy ion, single event transient, cryogenic temperatures, TCAD simulation.

I. INTRODUCTION

When high-energy charged particles strike and pass through the sensitive volume of space-borne devices, a large number of ionized electron-hole pairs are created along the ion track. A single-event transient (SET) current is observed as the charges are collected through drift and diffusion (DD) mechanisms [1], [2]. When the collected charge exceeds the critical charge, leading to the variation or disorder of the logic circuits and becomes the source of soft errors [3]. Both simulation and experimental observation indicate that soft-error rates have a strong dependence on the shape of the SET pulse [4], [5]. The parameters that determine the SET pulse after particles strike (drift, diffusion, bipolar effects, etc.) are a strong function of temperature [6]. Any change in operating temperature will alter the sensitivity to SEE. However, the temperature on moon can range from 90K at night, all the way up to 400 K in near solar radiation for example [7]. Therefore, to improve the reliability of electronic devices exposed to extremely harsh environments, the effects of temperature need to be fully concerned. Especially for small size devices, the influence of temperature on a single particle will be further intensified as the reduction of critical charge.

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There have been several experimental reports and simulations studied the temperature dependence of SEE. Truyen *et al.* [8] reported the temperature dependence of SEU for 0.18μm SRAM memory cell, results showed that at a given linear energy transfer (LET) value, heavy-ions-induced current peak decreases when the temperature increases from 218K to 418K and the threshold LET reaches a maximum at 320K. Alles *et al.* [9] demonstrated that over a temperature range from 125°C to 25°C in a SOI SRAM show that increased SEU sensitivity is expected to substantially increase with temperature. Moreover, modeling of the heavy ion-induced current transients in Si bulk devices and SOI floating devices revealed that pulse width and charge collection increases with temperature, which is closely correlated with the enhancement of the bipolar amplification effects [10], [11]. However, to date, there has been little research aimed at the effect of single event transient at extremely low temperature, understanding the response of devices in a wide range of temperature is of great significance in space applications.

In this paper, simulations are performed in the 300K to 77 K temperature range on a 65nm Si bulk NMOSFET at different LET value. The impact of the temperature on the current pulse under heavy-ion irradiations are evaluated. First of all, the investigated device and conditions of simulations

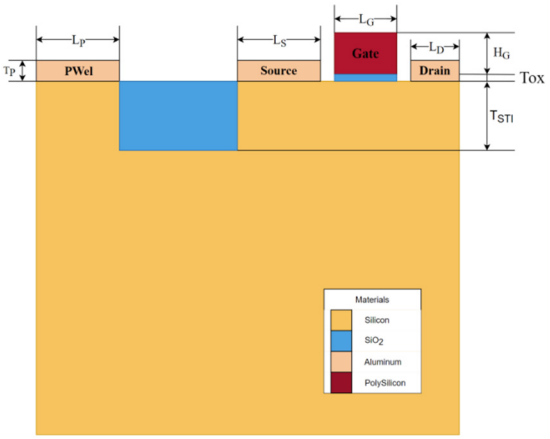

FIGURE 1. Cross-sectional view of a MOSFET considered in this paper.

TABLE 1. Units for magnetic properties.

Parameter name	Symbol	value	Unit
Gate length	L_G	0.035	μm
Drain length	L_D	0.12	μm
Source length	L_S	0.12	μm
Pocket length	L_P	0.2	μm
Gate height	H_G	0.1	μm
STI height	T_{STI}	0.35	μm
Gate oxide thickness	T_{OX}	0.002	μm
Pocket thickness	T_P	0.05	μm
Source/Drain doping	N_{sd}	1×10^{20}	cm^{-3}
LDD doping	N_{ldd}	2.4×10^{19}	cm^{-3}
Channel doping	Nc	7.9×10^{18}	cm^{-3}
Pocket doping	$Npwel$	1×10^{18}	cm^{-3}
Substrate doping	$Nsub$	1×10^{16}	cm^{-3}

will be described. In a second part, the effects of the ion strike on the main electrical parameters inside the structure as well as the physical mechanism will be analyzed. The finding of this paper will be beneficial for the radiation resistance reinforcement of devices under extreme cryogenic temperature environment.

II. DEVICE STRUCTURE AND CONDITIONS OF SIMULATIONS

Due to the good ability of physical insight into the radiation behavior and strong computing power, the Silvaco Technology Computer Aided Design (Silvaco TCAD) device simulator was used to evaluated the SEE. The radiation effect on the simulation can be divided into device simulation and radiation effect simulation. Frist of all, a three-dimensional (3D) structure model was built by Silvaco DevEdit simulator which can accurately define the grid information and doping concentration. Fig. 1 shows the cross-sectional view of the simulated devices. The length and width ratios of the MOSFET is W_L:W_W = 310nm:70nm. And the channel length is 65nm. During the simulation, silicon is used as bulk and substrate material. And drain, pwell, source are made of Aluminum. The physical and technological parameters of the structure in bulk MOSFET are shown in Table 1.

The effect of heavy-ion strike was simulated by Silvaco ATLAS simulation tool from TCAD. Considering the feature size of the device reaches nanometer level, single event upset is easier to be captured and produce soft errors. The classical drift-diffusion transport model (DD model) becomes less accurate to describe the non-local effects, such as velocity overshoot, which would cause premature breakdown of the device. Therefore, the hydrodynamic Model (HD) is more suitable for the device simulated in this paper.

The following models were used in numerical simulations: Shockley-Read-Hall (SRH) and Auger recombination model which takes into account high values of extrinsic doping concentration and temperature. Similarly, Boltzmann statistics is replaced by Fermi-Dirac statistics because of the presence of high doping concentration. The band-gap narrowing effect (BGN), impact ionization, and considering the effect of temperature, doping concentration, electric field and the carrier–carrier scattering model are used [12].

The striking conditions of heavy-ion is for normal incidence. The devices are biased in the OFF state (Vg =0 V), the substrate and source are grounded, and the drain terminal is constantly biased at the positive voltage (Vd = 0.9 V). The track of heavy-ion striking is vertical in the center of drain which is the most sensitive volume of the device. The generation rate produced by a heavy-ion track is modeled as a temporal Gaussian response centered at 50 ps with a characteristic time of 2 ps and an exponential radial distribution of charges with a fixed characteristic radius of 0.05μm. In all 3-D simulations, the LET value is taken constant all along the track. To investigate the effect of temperature on MOSFET SEEs, a charge deposition of 0.01–0.1 pC/μm was chosen, approximately equivalent to LET=1–10 MeV/(mg/cm^2), and the temperature is various from 300K to 77K.

The simulation process is as follows: firstly, the physical model and electrical properties of the device are calculated to obtain the steady-state solution. Afterward, the transient solution is calculated based on the coupled single event model, then the information on current transient, internal carrier mobility, and potential is obtained.

III. RESULTS

Using the established NMOS device model, a single event effect simulation was carried out for four temperature points of 300K, 200K, 125K, and 77K respectively. At each temperature point, the device is respectively struck by 1, 4, 8, and 10 MeV · cm^2/mg heavy-ion. Temperature has a significant effect not only on the shape of the drain current, but also on the magnitude of the drain current. When the temperature decreases from 300K to 77K, the obtained current peak increases and its SET drain current width decreases at a given LET value. What's more, the dropping rate of transient current decreases continuously and forming a current tail at a given LET value and temperature, the whole time to drop

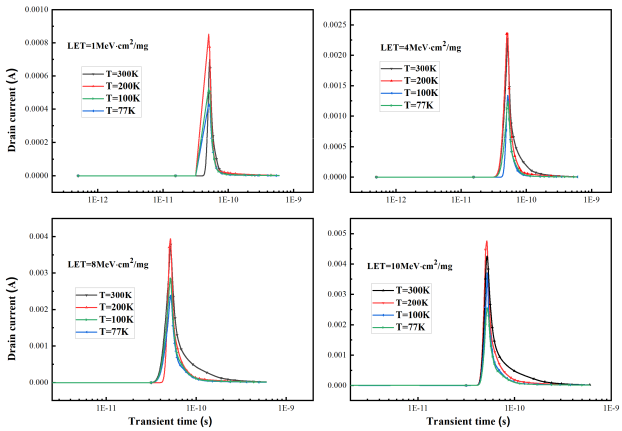

FIGURE 2. Drain current as a function of transient time for (a) LET = 1 MeV · cm^2/mg, (b) LET = 4 MeV · cm^2/mg, (c) LET = 8 MeV · cm^2/mg, (d) LET = 10 MeV · cm^2/mg at four operating temperatures. In the range of 50ps-300ps are plotted.

back to the initial state is much longer than reach to the peak value, which is typical for bulk devices.

According to the previous studying of charge collection, the transient current caused by the single event effect can be divided into two stages. The first stage is the rapid charge collection process, which mainly corresponds to the sharp part in the transient current diagram and lasts for a short time. This is due to the combination of drift charge collection in the depletion region and auxiliary electric field in the funnel region, resulting in a very short time for particles to pass through the device. In a very short time, the generation rate of the electron-hole pair is extremely fast, forming a large transient current. The other stage is the delayed collection process, corresponding to the tail of the transient current change slowly in the figure, where the main role is diffusion motion, lasting for a long time. The temperature dependence of the ''funneling'' current and the diffusion current will be discussed in the next parts.

A. THE DRAIN CURRENT PEAK VERSUS TEMPERATURE

Fig. 3 shows the change of peak transient current as a function of operating temperature at different LET values. It can be seen that the transient peak current of the four LET values has a similar dependence on temperature. The magnitude of peak current first increased and then declined monotonically when temperature decreased from 300 K to 77 K.

The transient peak current is related to carrier mobility, electric field intensity, and LET value, ignoring the contribution of impact ionization in the temperature range, I_0 can be expressed as [13]:

$$I_0 =< \mu E_{field} > LET \tag{1}$$

where μi s the average of electron mobility and E_{field} is the average of the electric field.

At a given LET value, peak current is in direct proportion to the mobility which varies $T^{-\beta}$for electrons [14], [15] at a

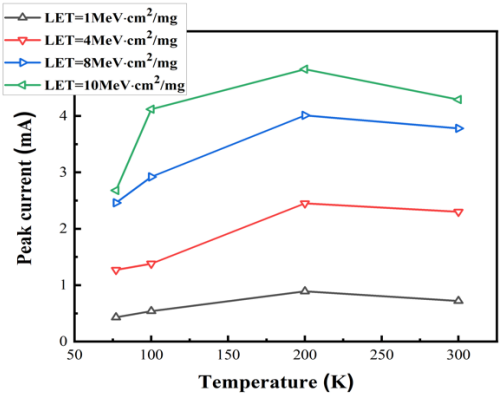

FIGURE 3. Drain current peak I_0 versus temperature for four LETs in the off-state NMOS.

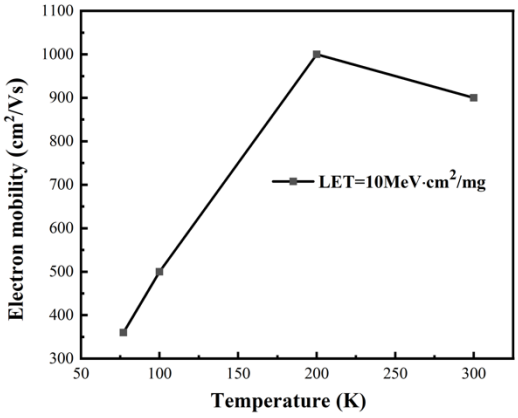

FIGURE 4. Average of electron mobility versus temperature at LET = 10 MeV · cm^2/mg.

given LET and electric field. The average of electron mobility nearby the drain were extracted by a function of temperature at LET = 10 MeV·cm^2/mg in fig.4. It is obvious that electron mobility μ remains the same trend as peak drain current. The maximum electron mobility reaches 1001.5 cm^2/V · s at 200 K.

B. THE DRAIN CURRENT FALL TIME VERSUS TEMPERATURE

The evolution of transient current pulse fall time versus temperature under different LET values are shown in Fig.5. The temperature plays an important role in transient drain current pulse. The fall time is defined as the time from the peak current value to the moment when it first reaches 10μA. Different from the trends of peak drain current, the SET fall time decreases gradually with the reduction of temperature at a given LET value. What' more, the larger LET value is, the faster it decreases. When LET = 10 MeV · cm^2/mg, the fall time changed from 497.13ps at 300 K to 346.08ps at 77 K, decreasing by43.65%.

The mechanism of the change of fall time with temperature is linked to the diffusion process. The relative variation of

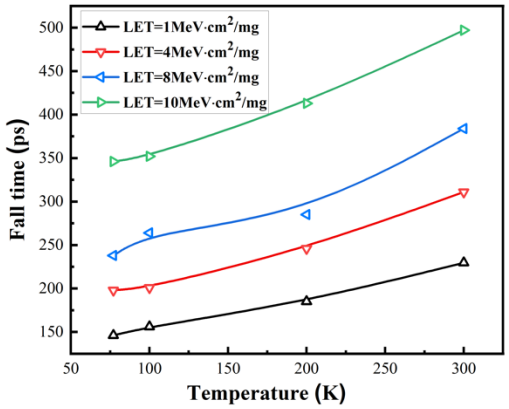

FIGURE 5. Drain current fall time versus temperature for four LETs.

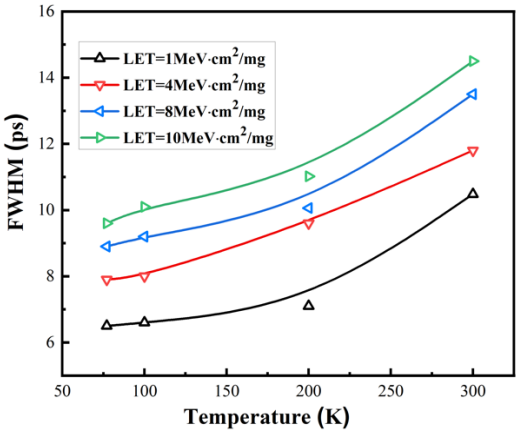

FIGURE 6. Drain current FWHM versus temperature for four LETs.

the diffusion constant D_{iff} is generally used to represent the diffusion capacity of carriers which is related to mobility and temperature as shown by Einstein's relation [16]:

$$\frac{D_{iff}}{\mu} = \frac{k_0 T}{q} \tag{2}$$

where k_0 is Boltzmann constant. The diffusion coefficient D_{iff} is correlated with $T^{-\gamma}$ depending on doping concentration. Therefore, as the temperature decreases, both D_{iff} and μ increase and the diffusion ability of carriers increases, resulting in the diffusion process ending faster. Similar trend was found in p+/n/n+ diodes [14], [15].

Fig.6 extracted the transient drain current full width at half maximum (FWHM) at different temperatures. It can be seen that the current pulse width decreases when temperature drops from 300K to 77K. The change of SET pulse width is dominated by charge collection. In other words, the trends for drain current pulse width versus temperature ought to remain the same as current fall time.

Fig. 7 shows the drain current fall time versus drain voltage for the simulated device at four LET values. As drain voltage decreases, the fall time decreases. The fall time decreases from 602ps to 423ps when drain voltage increases from 0.6V

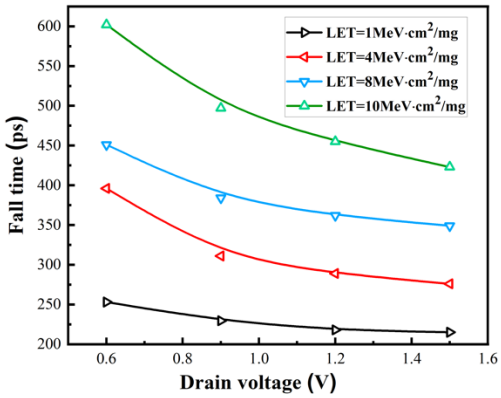

FIGURE 7. Drain current fall time versus drain voltage for four LETs.

to 1.5V at LET $=$ 10 MeV $\cdot$ cm^2/mg. The electric field is weaker at a low bias voltage than at a higher voltage, leading to the electron-hole pairs generated after heavy ion stroke are not easy to separate and the parasitic transistor is difficult to open, thus the pulse current reaches initial state is longer at the low bias. The smaller the drain voltage, the bigger the SET response time will last.

C. THE CHARGE COLLECTION VERSUS TEMPERATURE

Charge collection as a function of temperature under four LET values is plotted in Fig. 8. $Q_{collect}$ is extracted by integrating the drain current over the simulated time. As we can see the collected charge first increases and then decreases when temperature decreases from 300 K to 77 K. The collected charge reaches a maximum value 1.18E-13C at 200 K, increasing by 3.2E-14C compared with 8.60E-14C at 300K when LET $=$ 10 MeV $\cdot$ cm^2/mg.

The amount of charge deposited in the sensitive position of the device and the collection efficiency of the device jointly affect the magnitude of charge collection after a heavy-ion struck.

The effect of temperature on charge deposition is mainly reflected in the effect of temperature on the bandgap. With the increase in temperature, the bandgap width becomes narrower, resulting in more electron-hole pairs under the same condition. Bandgap versus temperature is expressed as [17]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{(T+\beta)} \tag{3}$$

where T is the temperature variable, $E_g(0)$ is the bandgap at 0 K with a default value of 1.17eV, α and β are the material parameters, for silicon, $\alpha = 4.73 \times 10^{-4}$, $\beta = 636$ [18] in general. When the temperature drops from 300K to 77K, the bandgap increases from 1.125eV to 1.166eV under default parameters. Meanwhile, in silicon materials, the average energy consumed for each electron-hole pair ionized can be calculated [19] by equation (4):

$$\varepsilon = 2.2E_g(T) + 0.96E_g^{\frac{3}{2}}(T) \cdot \exp\left(\frac{0.75E_g(T)}{T}\right) \tag{4}$$

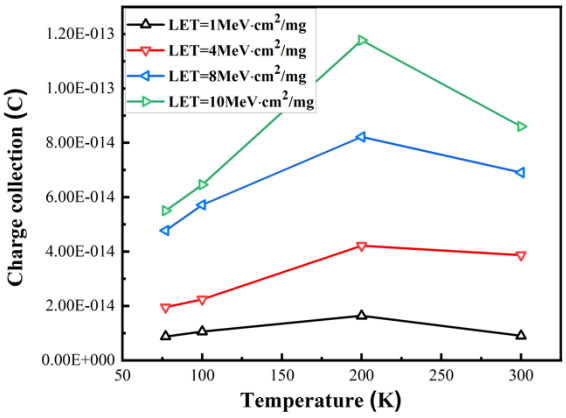

FIGURE 8. Charge collection versus temperature for four LET values.

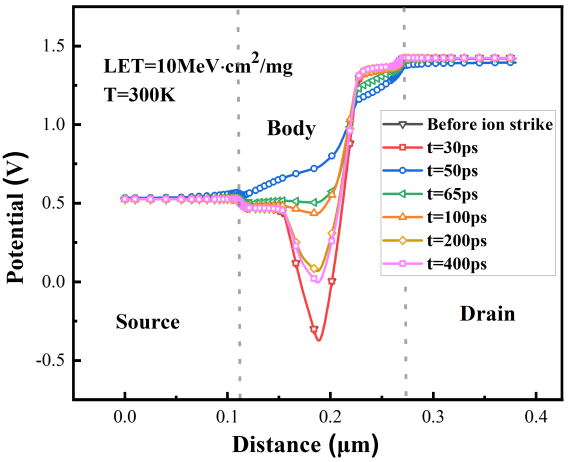

FIGURE 9. 1-D potential profile in a cutline along the x-axis at different time points before and after the ion strike. The LET value is 10 MeV · cm^2/mg and temperature is 300K.

According to equations (3) and (4), increased energy consumed by a generation of the electron-hole pairs from 3.62eV to 3.79eV was found as the temperature decreased from 300K to 77K, and the concentration of the electron-hole pair decreases by 4.49% at the same deposited energy.

Fig. 9 shows the potential variation of the device (from source to drain) in a cutline of 2nm below the Si/SiO_2 interface at different time points before and after ion strike. The LET value is 10 MeV · cm^2/mg and temperature is 300K. The potential is strongly affected by SET. At the moment before ion striking, an equivalent NPN transistor exists among source, body and drain because of a large source to drain barrier. As time goes on, the holes generated by heavy ion are stored in the body region and lead to the increase of body potential as shown at t=50ps. The reduction of source to drain barrier contributes to the opening of parasitic transistor, the additional electrons will flow into the channel, becoming a part of the drain transient current and further increasing the collection charge, which is known as the bipolar amplification effect.

Studies have demonstrated that temperature has a significant effect on the bipolar amplification effect [20], [21]. Enhancement of temperature leads to sever bipolar amplification effect and more collected charge. The lattice scattering effect is a dominant factor that influencing carrier mobility at high temperature, inducing lower carrier mobility and higher parasitic resistance. The increase of the resistance between body contact and bulk region, generating a higher potential and smaller source to drain barrier, therefore bipolar amplification effect is more sever at high temperatures. And the corresponding SET pulse width becomes broader either.

Generally, the diffusion process of carriers is much slower than the drift process. Therefore, the contribution of diffusion process to the total collected charge is mainly reflected in the tail of transient drain current and is very limited by temperature.

As described in Refs. [14], the charge collected by diffusion process Q_{diff} is mainly related to the minority diffusion length L_p, which is decided by the ambipolar diffusion coefficient D^* and minority carrier lifetime τ. Q_{diff} can be expressed as:

$$Q_{diff} = q \cdot LET \cdot \frac{L_p}{w_p} \tag{5}$$

$$L_p = \sqrt{D^* \tau} \tag{6}$$

where q is electron charge and w_p is the minority diffusion width. Both D^* and τ have a strong temperature dependence. At a given LET value, with the increasing of simulated temperature, D^* gradually increases while τdecreases. The overall result is that the L_p is weakly influenced by the temperature, and charge collected by diffusion has little relationship with temperature [22].

The influence of temperature on charge collection is divided into the process of diffusion, drift and bipolar amplification. The effect of temperature on the drift process is related to the change of mobility with temperature. As the temperature increases, the mobility reaches the maximum value at 200K, leading to the increase of collected charge by drift process. However, the collected charge by diffusion is basically unchanged, and the amount of charge collected by bipolar amplification increases gradually with temperature, the total result is that the maximum amount of charge collected at 200K.

IV. CONCLUSION

TCAD simulations of single event transient effects show that a decrease in temperature leads to a decrease in the fall time for a 65nm Si bulk MOSFET at a given LET value. Both peak current and collected charge reach a maximum value at 200 K, suggesting that temperature has a strong dependence on drain transient current. The evolution of electrical parameters may be caused by the increase of electron mobility at cryogenic temperatures. The effect of pulse broadening is attributed to the enhancement of bipolar amplification effect which

is much sever at high temperatures. The above conclusions provide a theoretical basis for the wide application of 65nm devices in 77 K-300 K space environment.

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