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RESEARCH ARTICLE

A Novel Differential to Single-Ended Converter for Ultra-Low-Voltage Inverter-Based OTAs

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ABSTRACT For the design of inverter-based OTAs with differential input and single-ended output, the differential to single-ended (D2S) converter is a key building block. In fact, the performance of the D2S strongly affects the overall common-mode rejection ratio (CMRR) and input common-mode range (ICMR) of the whole OTA. In recent literature, inverter-based OTAs rely on a D2S topology based on an inverter driving another inverter with the input and output tight together which behaves as a "diode" connected device to implement a voltage gain approximately equal to −1. However, since this approach is based on the matching of the inverters, the performance of this D2S results sensitive to PVT variations if the bias point of the inverters is not properly stabilized. In this paper we present a novel topology of inverter-based D2S converter, exploiting an auxiliary, standard-cell-based, error amplifier and a local feedback loop. The proposed D2S, compared to the conventional one, exhibits higher CMRR, improved ICMR and better robustness with respect to PVT variations. We present also an ULV, standard-cell-based OTA, which exploits the proposed D2S converter and shows excellent performance figures of merit with low area footprint.

INDEX TERMS Standard-cell, ultra-low-voltage (ULV), inverter-based, fully synthesizable.

I. INTRODUCTION

The era of the Internet-of-Things (IoT) has paved the way to a plenty of new trends in electronic and communication fields, strongly motivating the whole researchers' community to rethink the way in which electronic circuits are designed [1], [2]. The stringent requirements imposed by portable and wearable devices have driven integrated circuits designers to speed up the design time and to drastically reduce the area usage to cut costs [2]. Furthermore, due to the fact that many IoT circuits require energy harvested architectures [1], [2], the design of Ultra-Low-Voltage (ULV) analog building blocks suitable to operate with supply voltages as low as 0.3V, is becoming more and more attractive.

The Operational Transconductance Amplifier (OTA) is surely one of the most useful analog building blocks in electronic apparatuses, and stands out for its application in several analog circuits such as filters, comparators, analog to digital converters (ADCs), digital to analog converters (DACs), low dropout regulators (LDOs), and so on.

In this ultra-constrained scenario several high performance OTAs which exploit body-driven gate-biased architectures have been presented in the recent literature [3], [4], [5]. In detail, the usage of the body-driven approach has resulted in a plenty of topologies which exhibit state-of-the-art performances, both in terms of small signal and large signal figures of merit, and good robustness with respect to process, supply voltage and temperature (PVT) variations [3], [6], [7]. However, such OTAs have to be designed and routed manually and very often result in huge area occupation, due to the fact that separate wells are mandatory to implement body-driven architectures.

On the other hand, several inverter-based OTAs have been proposed in the literature. The Nauta transconductor has been presented for the first time in 1992 [8] and it has been recently exploited in [9] and [10] to implement fully differential OTAs for high speed applications. However, it has to be noted that most of the inverter-based implementations available in the

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literature, require custom-defined inverters to reach reasonable performance under PVT and mismatch variations. Custom inverters allow degrees of freedom which are not guaranteed for inverter gates taken from standard-cell libraries. In fact, it is very difficult to control the bias point of standard-cell inverters and, as a result, the bandwidth, the power consumption and the phase margin of standard-cell-based OTAs, compared with other not fully standard-cell based architectures, exhibit a greater sensitivity to PVT variations [11]. In order to address these issues, several techniques to properly set node voltages have been proposed [7], and in some cases an improvement in terms of robustness with respect to PVT variations has been observed [11]. Another advantage of custom-defined inverters is that their body terminals are accessible and can be used to implement body-bias strategies which allow to enhance the robustness of such OTAs with respect to PVT variations. A further advantage is that custom inverters can be optimized to center the design point at a given power supply voltage and bias current. However, it has to be noted that the area of custom inverters is typically much larger than the area of inverter gates taken from standard-cell libraries whose area footprint is strongly optimized by IC manufacturers.

With the aim of speeding up the design time and to drastically reduce the area usage of analog building blocks, researchers have recently focused on optimizing and refining novel layout strategies, searching for a way to automate the design flow of analog blocks by using some features, such as the automatic place and route strategies for standard-cell-based circuits, typically adopted in the digital design flow to implement fully-synthesizable comparators [12], [13], [14], [15], ADCs [16], [17], [18], [19], DACs [20], LDOs [21], [22], [23] and OTAs [2], [24], [25], [26], [27].

Recently the digital (DIG) OTA, proposed in [28] has been introduced as a novel approach to design OTAs with minimum area and power consumption. In [25] a standard-cell implementation of the digital OTA suitable for automatic place and route has been proposed showing state-of-the-art performance both in terms of area consumption and figures of merit (FOMs). Though its promising performance, as outlined by authors, DIG-OTAs result sensitive to PVT and mismatch variations and often require some sort of calibration or supply-voltage-adjusting to work properly [25].

In the same context, other approaches exploit digital standard-cells to mimic the behaviour of analog circuits. In fact, the most common practice to design standard-cell-based analog functions is to exploit the inverter gate, taken from a standard-cell library, as a basic analog amplifier. Focusing on the inverter-based implementation of OTAs with differential input and single-ended output, the differential to single-ended (D2S) converter plays a main role [3], [11], [29]; indeed its performance directly affects the overall common-mode rejection ratio (CMRR) and input common-mode range (ICMR) of the whole OTA. In recent literature [29], [30], inverter-based OTAs rely on a D2S topology based on an inverter driving another inverter with the input and output tight together which behaves as a ''diode'' connected device to implement a voltage gain approximately equal to -1. However, since this approach is based on the matching of the inverters, the performance of this D2S results sensitive to PVT variations if the bias point of the inverters is not properly stabilized. To overcome this issue, in [29] a body-bias strategy to set the static output voltage and the bias current of inverters has been proposed; however this approach requires ad-hoc circuits whose supply voltage is larger than the one of the ULV OTA. Recently a similar replica-bias approach to set the output static voltage of the basic amplifier cells has been presented in [31].

In this work we propose a novel topology of inverter-based D2S converter which exploits a local feedback to achieve higher CMRR and better robustness with respect to the previously published inverter-based D2S. An ULV standard-cell-based OTA which exploits the proposed D2S is also presented, showing outstanding performance in terms of performance figures of merit with limited area footprint.

In the following, section II reviews the previously published inverter-based D2S converter and presents for the first time a detailed analysis of its performances. The novel, improved, inverter-based, D2S converter is introduced and analyzed in section III. The design of an ULV, standard-cell-based OTA exploiting the novel D2S converter is presented in section IV, and simulation results are discussed in section V. Finally, a comparison against the state of the art of ULV OTAs, and some conclusions are reported in sections VI and VII respectively.

II. REVIEW OF THE CONVENTIONAL INVERTER-BASED D2S CONVERTER

In the context of analog design, the differential to single-ended conversion is usually carried out in the first stage of the OTA by means of the well known differential pair with current mirror active load. The same kind of differential to single-ended conversion is needed also in inverter-based or standard-cell-based OTAs exhibiting a differential input and a single-ended output. In recent research works dealing with inverter-based analog circuits such as [6], [7], [11], [29], [30], the differential to single-ended conversion is often performed exploiting the circuit topology depicted in Fig. 1. In the following we will refer to the circuit in Fig. 1 as the ''conventional inverter-based D2S'' stage.

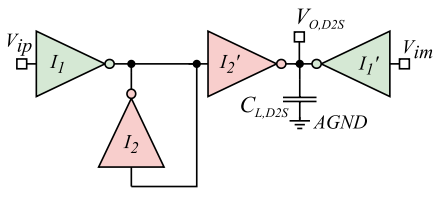

FIGURE 1. Conventional inverter-based D2S [29].

The conventional inverter-based D2S in Fig. 1 mimics the behaviour of a pseudo-differential pair implemented by the

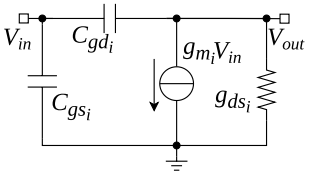

FIGURE 2. Small-signal model of the generic inverter I_i.

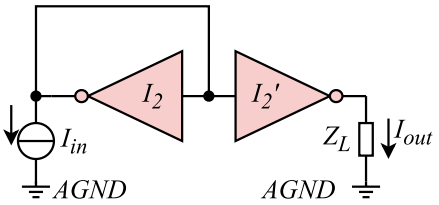

FIGURE 3. Conventional inverter-based current mirror.

inverters I_1 and $I_{1'}$ with a current mirror active load which is implemented by the inverters I_2 and $I_{2'}$. In particular, since I_2 has the input and output tight together, it behaves as a "diode" connected device to mimic the input transistor of a current mirror.

In order to gain insight into the behaviour of this D2S, we express its performance by modelling the generic inverter I_i as a transconductance amplifier whose parameters are described in Fig. 2.

In Fig. 2 g_{m_i} denotes the overall transconductance gain given by both the *PMOS* and *NMOS* transistors which compose the inverter:

$$g_{m_i} = g_{m_{n_i}} + g_{m_{p_i}} \tag{1}$$

and the same notation is used for the output conductance g_{ds_i} and the parasitic capacitances C_{gd_i} and C_{gs_i} of MOS transistors as follows:

$$g_{ds_i} = g_{ds_{n_i}} + g_{ds_{p_i}} \tag{2}$$
$$C_{gd_i} = C_{gd_{n_i}} + C_{gd_{p_i}} \tag{3}$$
$$C_{gs_i} = C_{gs_{n_i}} + C_{gs_{p_i}} \tag{4}$$

Moreover, in the following, we denote with A_{0_i} the intrinsic voltage gain of the conventional inverter g_{m_i}/g_{ds_i}.

A. FREQUENCY RESPONSE

With the above assumptions, the voltage gain frequency response $A_{v_{D2S}}(s)$ of the conventional inverter-based D2S in Fig. 1 can be expressed as follows:

$$A_{v_{D2S}}(s) = \frac{V_{O,D2S}(s)}{V_{ip}(s) - V_{im}(s)} = \frac{A_{v_{D2S_0}}}{1 + s\tau_o} \frac{1 + s\tau_1/2}{1 + s\tau_1} \tag{5}$$

where the dc gain $A_{v_{D2S_0}}$ is:

$$A_{v_{D2S_0}} = \frac{g_{m_1}}{g_{ds_1} + g_{ds_2}} \tag{6}$$

and the time constants τ_o and τ_1 are:

$$\tau_o = \frac{C_{L,D2S} + C_{gd_1} + C_{gd_2}}{g_{ds_2} + g_{ds_1}};$$
$$\tau_1 = \frac{C_{gd_2}\frac{g_{m_2}}{g_{ds_1}+g_{ds_2}} + 2C_{gs_2} + 2C_{gd_1}}{g_{ds_2} + g_{ds_1}} \tag{7}$$

As can be observed in eq. (5) the "diode" connection of I_2 results in a pole-zero doublet very similar to the one which appears in a traditional analog current mirror. Also in the inverter-based D2S, since the pole and the zero in eq. (5) are one octave distant to each other, their effect on the overall frequency response can be neglected.

B. ACCURACY OF THE CURRENT MIRROR

In order to estimate the current gain I_{out}/I_{in} of the current mirror used in the conventional inverter-based D2S, we refer to the circuit configuration shown in Fig. 3, where the input current flowing into the "diode" connected inverter I_2, is mirrored at the output of $I_{2'}$ and flows trough Z_L.

Referring to Fig. 3 the input-output transfer characteristic of the current mirror made up of I_2 and I_2' for $Z_L = 0$ can be easily computed as:

$$\frac{I_{out}}{I_{in}} = \frac{1/g_{ds_2}}{1 + g_{m_2}/g_{ds_2}} \cdot g_{m_{2'}} \tag{8}$$

Eq. (8) clearly shows that the current gain of the conventional inverter-based current mirror tends to unity if the two following conditions are fulfilled:

- $g_{m_2}/g_{ds_2} \gg 1$;
- $g_{m_2} = g_{m_{2'}}$.

It is therefore evident that the conventional current mirror exhibits a limited accuracy due to the relatively small value of the intrinsic voltage gain of inverters in nanometer technologies. An additional effect that further limits the accuracy of the conventional inverter-based current mirror is related to the different static voltages across the two inverters I_2 and I_2' that strongly affect the ability to achieve the second condition: $g_{m_2} = g_{m_{2'}}$. In fact, referring to Fig. 3, the output of the inverter I_2' in short circuit condition (i.e. $Z_L = 0$) is connected to the analog ground equal to $V_{DD}/2$, whereas the static voltage at the input node of the current mirror is dependent on inverters' sizes and is sensitive to mismatches. This effect is similar to the one present in a traditional analog current mirror when the drain source voltages of the input and output transistors of the mirror are not well matched to each other.

C. COMMON-MODE REJECTION

The common-mode rejection ratio CMRR of the conventional inverter-based D2S can be easily computed as follows:

$$CMRR = \frac{g_{m_2}}{g_{ds_1} + g_{ds_2}} \tag{9}$$

From eq. (9) it is evident that the D2S in Fig. 1 exhibits a limited CMRR, which in recent nanometer CMOS technologies is surely lower than 20dB even in typical conditions. If transistor mismatches are taken into account, the CMRR of this stage is further reduced to values which are often not acceptable for high performance ULV OTAs.

D. OFFSET IN UNITY GAIN CONFIGURATION

In order to account for the effect of mismatches on the conventional inverter-based D2S configured as a unity gain buffer (i.e. V_o connected to V_m in Fig. 1), we model the generic inverter I_i as a transconductance amplifier whose output short-circuit current (offset current) can be described as a random variable with mean value μ_i and standard deviation σ_i. Moreover, we assume that when the input of the D2S in unity gain configuration is connected to the analog ground ($AGND = V_{DD}/2$), the current offset can be described with a normal distribution with mean value 0 and $\sigma_i \neq 0$. The block scheme for computing the offset standard deviation σ_v of the conventional inverter-based D2S in unity gain configuration is reported in Fig. 4.

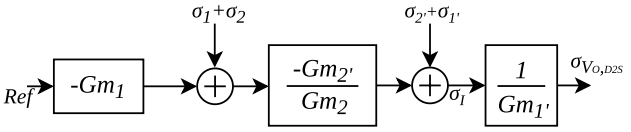

FIGURE 4. Block scheme of the conventional inverter-based D2S for computing the offset standard deviation σ_V.

According to the block scheme in Fig. 4, and noting that the unity gain configuration for the D2S results in a "diode" connection for the inverter $I_{1'}$, the output current offset (whose standard deviation is denoted as σ_I) at the node where V_o is connected to V_m can be multiplied by the factor $1/g_{m_{1'}}$ to compute the output voltage offset (whose standard deviation is denoted as σ_V), obtaining:

$$\sigma_v^2 = \frac{\sigma_1^2 + \sigma_2^2}{g_{m_{1'}}^2 \frac{g_{m_2}^2}{g_{m_{2'}}^2}} + \frac{\sigma_{2'}^2 + \sigma_{1'}^2}{g_{m_{1'}}^2} \tag{10}$$

III. THE PROPOSED INVERTER-BASED D2S

In this section we introduce a novel, inverter-based, D2S converter which exhibits much better CMRR and ICMR than the conventional one, and allows to implement high performance, ULV, standard-cell-based OTAs. The proposed improved inverter-based D2S converter is depicted in Fig. 5. The converter exhibits a symmetrical architecture and is made up of inverters $I_{1,2}$ and $I'_{1,2}$ which are identical to each other. The output of the inverter I_1 is connected to the positive input terminal of an auxiliary differential amplifier A_D, made up of four inverters $I_{3,4}$ and $I'_{3,4}$ which are also assummed identical to each other. The output of the differential amplifier drives the input of the inverters I_2 and I'_2, whereas a reference voltage (equal to $AGND = V_{DD}/2$) is applied to the negative input terminal. The role of the auxiliary amplifier A_D is to boost the CMRR of the conventional D2S converter described in the previous subsection. Indeed, with respect to the conventional D2S converter, the combination of I_2 and A_D alongside with I'_2 acts as an improved current mirror, which, due its higher accuracy, allows to improve the CMRR performance as will be better detailed in the following.

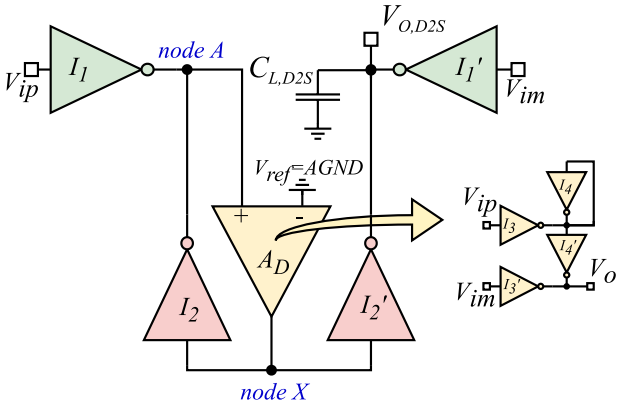

FIGURE 5. Novel inverter-based D2S converter proposed in this work.

A. IMPROVED ACCURACY OF THE CURRENT MIRROR

In order to estimate the current gain I_{out}/I_{in} of the improved current mirror used in the proposed inverter-based D2S, we consider the circuit configuration depicted in Fig. 6, where the input current flows into a "super-diode" device (implemented through the combination of I_2 and A_D), is mirrored at the output of $I_{2'}$ and flows trough Z_L.

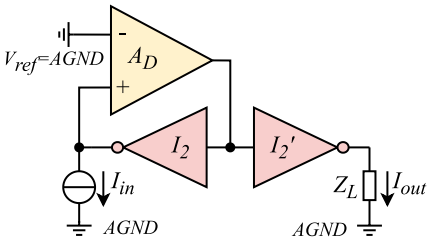

FIGURE 6. Improved inverter-based current mirror exploited in the D2S proposed in this work.

Referring to Fig. 6, the input-output transfer characteristic of the improved current mirror can be written as:

$$\frac{I_{out}}{I_{in}} = \frac{\frac{A_D}{g_{ds_2}}}{1 + \frac{g_{m_2} A_D}{g_{ds_2}}} \cdot g_{m_{2'}} \tag{11}$$

where:

$$A_D = \frac{g_{m_3}}{g_{ds_3} + g_{ds_4}} \tag{12}$$

In this case eq. (12) shows that the current gain of the proposed improved inverter-based current mirror tends to unity if the two following conditions are fulfilled:

- $(g_{m_2}/g_{ds_2}) \cdot A_D \gg 1$;
- $g_{m_2} = g_{m_{2'}}$

It is therefore evident that the proposed current mirror exhibits an improved accuracy with respect to the conventional one, due to the gain provided by the auxiliary differential amplifier. An additional important advantage of the proposed improved current mirror which further improves its accuracy with respect to the conventional inverter-based

current mirror is related to the static voltages across the two inverters I_2 and I_2' that have a strong impact on the possibility to achieve the condition $g_{m_2} = g_{m_{2'}}$. In fact, referring to Fig. 6, the output of the inverter I_2' in short circuit conditions (i. e. $Z_L = 0$) is connected to $AGND = V_{DD}/2$, whereas the static voltage at the input node of the current mirror is forced to *AGND*, due to the feedback loop provided by the auxiliary amplifier A_D. In fact, the auxiliary amplifier A_D has its negative input terminal V_{im} connected to an explicit reference voltage equal to $V_{ref} = AGND = V_{DD}/2$ which represents the reference voltage of the loop. Thanks to the action of the feedback loop the two inverters I_2 and I_2' implementing the current mirror operate with the same input and output voltages, thus maximizing the accuracy of the current mirroring. It is important to note that the feedback loop with an explicit reference voltage sets the output of I_2 at *AGND* in spite of PVT variations and mismatches, thus greatly improving the robustness of the proposed D2S with respect to the conventional one. According to the above considerations the proposed feedback loop enhances the precision of the current mirror, even for large variations of the input common-mode voltage. Indeed, when large common-mode variations occur, the intrinsic gain of the inverters starts to decrease and as a consequence the current mirror error starts to increase. However, the proposed circuit results in a lower current mirror error due to the fact that also under large-signal conditions, it holds:

$$\frac{g_{m_2} \cdot A_D}{g_{ds_2}} \gg g_{m_2}/g_{ds_2} \tag{13}$$

Moreover, due to the benefits of the feedback, the bias point of I_2 and I_2' is steadier with respect to the conventional D2S converter, thus the open-loop gain denoted in eq. (13) remains greater under input common-mode variations as we will better show in the following.

B. FREQUENCY RESPONSE

Referring to the topology of the proposed improved D2S in Fig. 5, and using the same model parameters described in Fig. 2 and used in section II, the frequency response of the differential gain can be written as:

$$A_{v_{D2S}}(s) = \frac{A_{v_{D2S_0}}}{1 + s\tau_o} \frac{1 + s\frac{\tau_A}{2}}{1 + s\tau_A} \tag{14}$$

where the dc gain $A_{v_{D2S_0}}$ is:

$$A_{v_{D2S_0}} = \frac{g_{m_1}}{g_o} \tag{15}$$

considering $g_o = g_{ds_1} + g_{ds_2}$, the time constants τ_A and τ_o are:

$$\tau_A = \frac{C_A}{g_{m_2} A_D}; \qquad \tau_o = \frac{C_o}{g_o} \tag{16}$$

where

$$\begin{aligned} C_A &= C_{gd_2} + C_{gd_3}\frac{g_{m_3}}{g_{m_4}} + C_{gs_3}; \\ C_o &= C_{L,D2S} + C_{gd_1} + C_{gd_2} \end{aligned} \tag{17}$$

and

$$A_D = \frac{g_{m_3}}{g_{ds_3} + g_{ds_4}} \tag{18}$$

As it can be observed form eq. (16), the feedback allows to shift the pole-zero doublet to frequencies greater than the one of conventional D2S (summarized in eq. (5)). Furthermore, as done for eq. (5) we can neglect the effect of the pole-zero doublet given by τ_A and simplify the frequency response as follows:

$$A_{v_{D2S}} = \frac{A_{v_{D2S_0}}}{1 + s\tau_o} \tag{19}$$

Thus, as a first order approximation the proposed D2S exhibits the same frequency response of the conventional one.

C. COMMON-MODE REJECTION

The CMRR of the improved D2S can be easily derived as:

$$CMRR = \frac{g_{m_2}}{g_{ds_1} + g_{ds_2}} \cdot A_D \tag{20}$$

Therefore, by comparing eq. (9) with eq. (20), it is evident that the proposed D2S converter exhibits a CMRR which is higher than the one of the conventional D2S of the factor $A_D \approx \frac{g_{m_3}}{g_{ds_3}+g_{ds_4}}$.

D. OFFSET IN UNITY GAIN CONFIGURATION

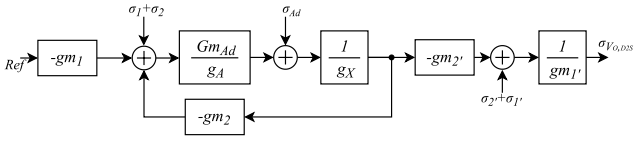

FIGURE 7. Block scheme of the proposed improved inverter-based D2S for computing the offset standard deviation σ_V.

The block scheme for computing the offset standard deviation σ_v of the proposed improved inverter-based D2S in unity gain configuration is reported in Fig. 7. According to the block scheme in Fig.7, and noting that the unity gain configuration for the D2S results in a "diode" connection for the inverter $I_{1'}$, the output current offset (whose standard deviation is denoted as σ_I) at the node where V_o is connected to V_m can be multiplied by the factor $\frac{1}{g_{m1'}}$ to compute the output voltage offset (whose standard deviation is denoted as σ_V), obtaining:

$$\sigma^2_{V_{O,D2S}} = \frac{\sigma_1^2 + \sigma_2^2}{\frac{g^2_{m_2}}{g^2_{m_{2'}}} g^2_{m_{1'}}} + \frac{\sigma^2_{A_D}}{\frac{g^2_{m_{A_D}}}{g^2_A}\frac{g^2_{m_2}}{g^2_{m_{2'}}} g^2_{m_{1'}}} + \frac{\sigma^2_{2'} + \sigma^2_{1'}}{g^2_{m_{1'}}} \tag{21}$$

By comparing eq. (10) and eq. (21) it can be seen how the proposed implementation significantly decrease the offset given by I_2. However the offset of the differential auxiliary amplifier is added to the overall offset, thus resulting in greater standard deviation with respect to conventional D2S converter. Eq. (21) shows that there is a trade-off in designing

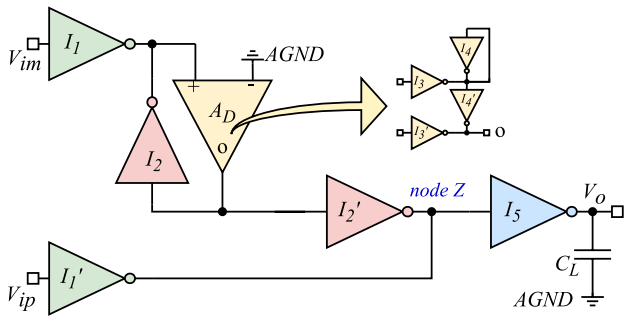

FIGURE 8. Proposed ULV, standard-cell-based OTA.

inverters $I_{3,4,3',4'}$; in fact if these inverters are sized with the minimum area allowed by the standard-cell library the power consumption and area are minimized at the cost of increased offset standard deviation.

IV. STANDARD-CELL-BASED ULV HIGH PERFORMANCE OTA EXPLOITING THE PROPOSED D2S

As an application of the novel D2S converter analyzed in section III, we introduce a novel ULV, standard-cell-based OTA, whose gate level schematic is reported in Fig. 8. As it can be observed, beside the D2S converter, just an addtional inverter stage I_5 is added as the second stage after the D2S. In the following we describe the performance behaviour of the proposed amplifier.

A. FREQUENCY RESPONSE OF THE PROPOSED ULV OTA

The differential gain of the proposed ULV, standard-cell-based OTA can be derived as:

$$A_{v_D}(s) = \frac{A_{v_{D2S_0}}}{1 + s\tau_{o_1}} \frac{A_0}{1 + s\tau_L} \tag{22}$$

where

$$\tau_{o1} = \frac{C_Z}{g_{ds_1} + g_{ds_2}} \tag{23}$$

$$\tau_L = \frac{C_L}{g_{ds_5}} \tag{24}$$

and

$$C_Z = C_{gd_5} \cdot \frac{g_{m_5}}{g_{ds_5}} + C_{gs_5} + C_{gd_1} + C_{gd_2} \tag{25}$$

is the total capacitance at node Z in Fig. 8.

Starting from eq. (22), the phase margin of the OTA can be derived as:

$$m\varphi = 180 - \arctan \tau_{o_1} - \arctan \tau_L \tag{26}$$

According to the above equations, two design strategies to provide frequency compensation of the proposed OTA can be devised:

1) to size the inverter I_5 so that the value of its input capacitance C_{in} results in $\tau_{o_1} \gg \tau_L$ for a given $C_{L_{max}}$;
2) to size the inverter I_5 in order to obatain $\tau_L \gg \tau_{o_1}$ for a given $C_{L_{min}}$.

Since our goal is to design an OTA which is able to drive both on-chip and off-chip capacitive loads, we set the value of the minimum load capacitance $C_{L_{min}}$ to a value which is integrable on-chip and we then size the inverter I_5 so as to attain the required phase margin for such minimum load capacitance.

B. CMRR

Since the topology of the proposed OTA is derived by simply adding the inverter I_5 to the proposed D2S, the CMRR of the OTA is the same obtained by the D2S converter and is expressed by eq. (20).

C. LARGE-SIGNAL PERFORMANCE

The positive and negative slew rate (SR_+ and SR_-) are set by the output capacitance C_L and the maximum output current $I_{5,max}$ of the inverter I_5 during the low-to-high and high-to-low transitions respectively. An expression of SR_+ and SR_- can be derived as follows:

$$\begin{aligned} SR_+ &= \frac{I_{d0_p}}{C_L} \exp\left(\frac{V_{DD} - |V_{th_p}|}{n_p U_t}\right) \\ SR_- &= \frac{I_{d0_n}}{C_L} \exp\left(\frac{V_{DD} - V_{th_n}}{n_n U_t}\right) \end{aligned} \tag{27}$$

Therefore the SR is set by the values of $V_{th_{n,p}}$ and $I_{d0_{n,p}}$ in the adopted CMOS technology.

V. SIMULATION RESULTS

Both the proposed D2S converter in Fig. 5 and the ULV standard-cell-based OTA in Fig. 8 have been designed and simulated within the Cadence environment by using the standard-cell library of a commercial 130nm CMOS process from STMicroelectronics. Referring to the D2S converter in Fig. 5, the inverters $I_{3,4,3',4'}$ have been implemented with the minimum sized standard-cell (IVx2), whereas inverters $I_{1,2,1',2'}$ have been implemented with the IVx160 standard-cells (i.e. with 80 times larger transistors). Then considering the ULV standard-cell-based OTA in Fig. 8, $I_{3,4,3',4'}$ have been implemented with IVx2, $I_{1,2,1',2'}$ with IVx160, and I_5 with the IVx20 standard-cell. Since our goal was to design an OTA able to drive both on-chip and off-chip capacitive loads, we have set the value of the minimum load capacitance $C_{L_{min}}$ at 2 pF and sized the inverter I_5 so as to attain a phase margin greater than 52° for such loading condition.

A. SIMULATIONS OF THE PROPOSED IMPROVED INVERTER-BASED D2S

In this subsection we compare the conventional inverter-based D2S against the proposed improved inverter-based D2S from a simulation perspective, where all the inverters are taken from the same standard-cell library. The histogram of the common-mode rejection ratio *CMRR* for both the conventional and the proposed D2S is reported in Fig. 9 after 200 Monte Carlo mismatch simulations. Fig. 9 shows that the *CMRR* of the proposed D2S exhibits a larger standard deviation with respect to the conventional

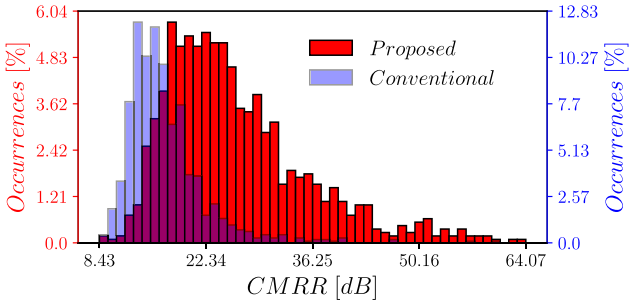

FIGURE 9. Common-mode rejection ratio *CMRR* of the proposed (red) and conventional (blue) inverter-based D2S.

D2S. However it has to be pointed out that the improved D2S exhibits a much higher average value of *CMRR* and therefore, if we set a specification for the minimum value of *CMRR*, such as for example $|CMRR| > 20$ *dB*, the proposed D2S allows to achieve a dramatically improved yield (in the range of 75%) with respect to the conventional one (which exhibits a yeld limited to about 15%).

To further compare the performance of the conventional and the improved D2S converters we have evaluated the differential gain A_{v_D}, the common-mode gain A_{v_C}, the output offset voltage *Offset* and the power consumption P_D in the five process corners. As it can be observed in Tab. 1, the crossed corners FS and SF significantly affect the output DC voltage of the conventional D2S, resulting in a relatively large offset. The performances of the improved D2S converter in the five process corners are summarized in Tab. 2. As it can be observed in Tab. 2, the *Offset* is lower than 1.29 *mV* also in crossed corners due to the action of the feedback loop which forces *node A* in Fig. 5 to *AGND*. If compared to the conventional D2S converter, the enhanced D2S converter exhibits a worst case offset voltage, which is about six times lower than the one of conventional D2S.

TABLE 1. Performance of the conventional D2S VS corner variations.

	A_{v_D} [dB]	A_{v_C} [dB]	$Offset\,[mV]$	P_D [μW]
TYP	13.87	-1.49	-0.87	5.81
FF	12.17	-1.75	-1.75	12.58
SS	15.41	-1.26	-0.78	2.99
FS	14.03	0.22	-7.83	6.5
SF	13.38	-0.67	6.18	6.17

TABLE 2. Performance of the improved D2S converter VS corner variations.

	A_{v_D} [dB]	A_{v_C} [dB]	Offset $[mV]$	P_D [μW]
TYP	14.42	-12.94	0.92	5.93
FF	12.77	-11.08	1.29	12.87
SS	15.91	-14.58	0.65	3.06
FS	14.57	-9.51	0.87	7.37
SF	13.9	-12.19	1.27	6.56

Tab. 2 also confirms that the enhanced D2S converter provides lower A_{v_C} and the higher CMRR across the different corners.

B. SIMULATIONS OF THE PROPOSED ULV, STANDARD-CELL-BASED OTA EXPLOITING THE IMPROVED D2S

1) SIMULATIONS IN NOMINAL CONDITIONS

The frequency response of the differential gain (magnitude and phase) of the proposed standard-cell-based OTA is depicted in Fig. 10, showing a differential gain of about 35 *dB* with a phase margin $m\varphi \cong 60\,deg$. The simulated differential gain results to be about equal to the gain of the D2S with a cascaded inverter: $A_{v_D}(0) \approx A_0^2/2 \approx 35\ dB$, as expected from the theoretical analysis in section III. The frequency response of the common-mode gain of the proposed standard-cell-based OTA is depicted in Fig. 11. Considering a differential gain of about 35 *dB*, the CMRR at DC results to be about 27 *dB*, in very good agreement with the theoretical analysis in section III.

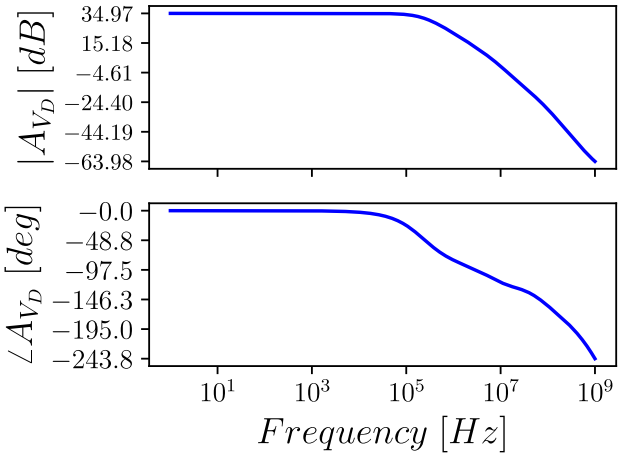

FIGURE 10. Frequency response of the differential gain of the proposed standard-cell-based OTA.

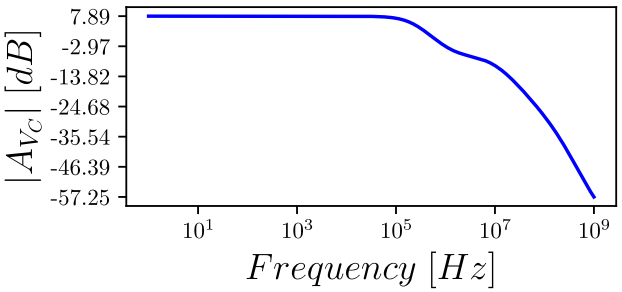

FIGURE 11. Common-mode gain of the proposed standard-cell-based OTA.

The OTA has then been tested in closed-loop, non-inverting, unity gain configuration and the frequency response is reported depicted in Fig. 12.

The time domain response to a full-swing input pulse is shown in Fig. 13, highlighting the rail-to-rail characteristics due to the enhanced D2S. The total harmonic distortion vs a sinusoidal waveform of frequency 1 *MHz* whose amplitude varies around 10% and 100% of the V_{DD} is reported in Fig. 14.

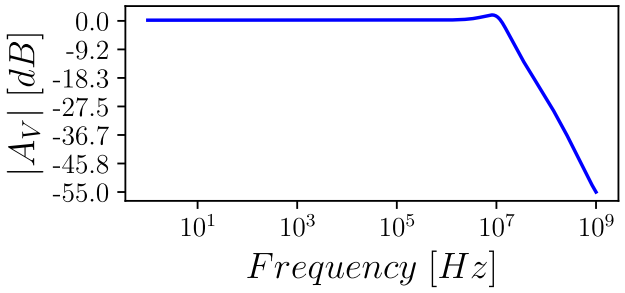

FIGURE 12. Frequency response in unity gain configuration.

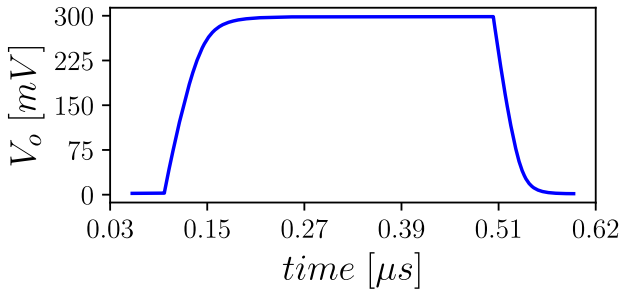

FIGURE 13. Transient response in unity gain configuration with a rail-to-rail input signal.

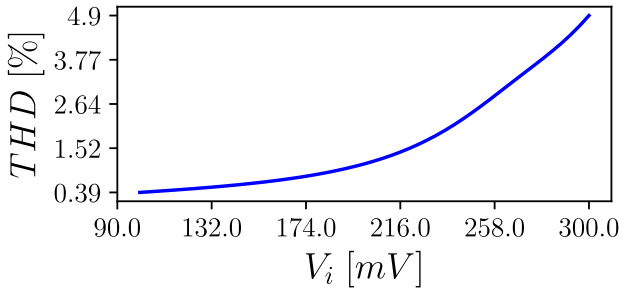

FIGURE 14. Total Harmonic Distortion under different input signal amplitudes.

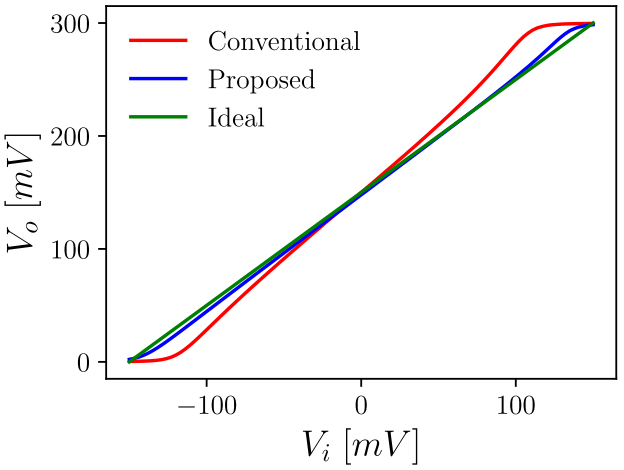

FIGURE 15. Dc voltage transfer characteristic of the OTA with the conventional (red), proposed (blue) and ideal (green) D2S.

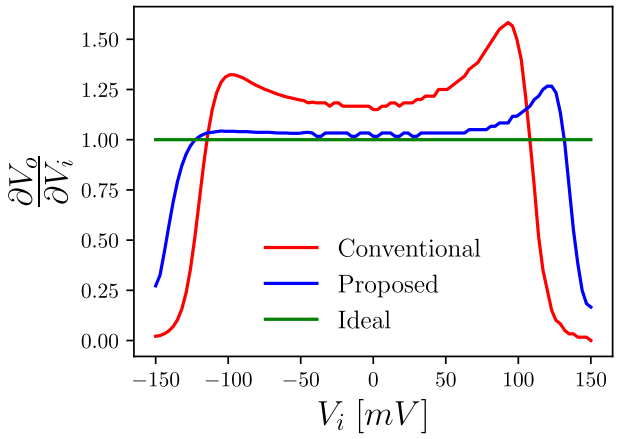

FIGURE 16. Voltage gain in unity gain configuration vs. input signal amplitude.

To better assess the advantages provided by the proposed improved D2S also in terms of input common-mode range (ICMR) we have simulated the dc voltage transfer characteristic of the OTA with both the conventional and the proposed D2S and results are reported in Fig. 15. Fig. 16 reports the voltage gain (derivative of the dc voltage transfer characteristic) as a function of the input common-mode voltage, further highlighting how the proposed improved D2S allows to enlarge the ICMR and to greatly improve the accuracy of the OTA configured as a voltage buffer (i.e. closed-loop voltage much closer to the ideal value of 0 *dB*). As outlined in Sec. III-A, the proposed D2S enhances the input common-mode range, thanks to the local feedback provided at *node A*. As expected, when a small-signal stimulates the non inverting buffer, the conventional D2S and the proposed one are both valuable solutions, though the proposed one attains better accuracy. On the other hand, when large signals stimulate the non inverting buffer, the conventional D2S drastically reduces its accuracy and, with respect to the proposed one, results in lower input common-mode range. This behaviour is due to the fact that no reference voltage is provided in the conventional D2S architecture and thus, under large common-mode input signals, the diode-connected inverter (I_2) works with a static voltage which strongly differs from the one of I_2', thus the accuracy of the differential to single-ended conversion is drastically reduced with respect to the proposed D2S. On the other hand, in the proposed D2S, the local feedback sets the *node A* at the reference voltage ($V_{ref} = AGND$), even for large commone-mode variations, and provides a better accuracy and a larger input common-mode range.

2) SIMULATIONS IN THE DIFFERENT PVT CONDITIONS

The robustness of the architecture has been investigated with respect to process, supply voltage and temperature (PVT) variations and results of the analysis are summarized in Tables 3-4. As it can be observed in Table 3, both the differential and the common-mode gains are stable with respect to different corners, as well as the offset and the phase margin,

TABLE 3. Performance of the proposed OTA in the different process corners.

	TT	FF	SS	FS	SF
A_{V_D} [dB]	34.97	31.19	37.9	34.86	34.1
A_{V_C} [dB]	7.89	8.19	7.66	9.88	6.53
GBW [MHz]	12.69	27.64	8.18	12.36	11.81
$m\varphi$ [deg]	62.56	66.35	58.63	64.93	64.58
P_D [μW]	6.10	13.2	3.15	7.07	6.63
$Offset$ [mV]	2.13	3.49	1.61	6.95	2.54
SR_p [V/μs]	4.54	7.34	2.83	2.72	7.25
SR_m [V/μs]	6.82	11.87	4.26	10.62	3.94
THD [%]	3.38	3.02	4.31	3.45	3.56

which results to be always greater than 58.63 [*deg*]. Otherwise, as expected, the power consumption results to be sensitive to process variations due to the fact that the current of each inverter is not controlled and depends on the threshold voltages $V_{th_{n,p}}$ of MOS transistors, which vary with process. Due to the fact that the quiescent current is not well defined, the transconductances g_{m_i} vary with the quiescent current and, as a consequense, the *GBW* results sensitive to process variations. Since slew rate performance depends on the maximum current of the inverter I_5 which, once again, depends on the threshold voltages $V_{th_{n,p}}$ according to eq. 27, the positive and negative slew rates are also process dependent. The

TABLE 4. Performance of the proposed OTA in the different supply voltage and temperature conditions.

	Voltage Variations		Temperature Variations	
T [°C]	27	27	0	80
V_{DD} [mV]	270	330	300	300
A_{V_D} [dB]	34.03	35.7	35.86	33.17
A_{V_C} [dB]	7.91	7.87	8.24	7.68
GBW [MHz]	8.30	18.88	7.97	24.64
$m\varphi$ [deg]	63.75	61.63	61.71	64.27
P_D [μW]	3.67	9.90	3.33	15.38
$Offset$ [mV]	2.26	2.08	2.16	2.06
SR_p [V/μs]	2.58	7.50	3.25	7.12
SR_m [V/μs]	3.85	11.31	5.41	9.21
THD [%]	4.59	2.67	4.66	2.36

proposed architecture has been tested also under voltage and temperature variations and it appears clear from results in Tab. 4, that both temperature and supply voltage variations, affecting the bias conditions of each inverter, have an impact on the *GBW*, the P_D and the $SR_{p,m}$. However, it has to be noted that the proposed D2S is able to work in all the different operating conditions. The output offset is always lower than 2.3 *mV* and the differential gain, the common-mode gain and the phase margin are robust with respect to PVT variations.

These results confirm that ULV standard-cell-based amplifiers, even if allow to minimize silicon area and are suitable for automatic place and route, exhibit more sensitivity to PVT variations with respect to ULV full-custom designed amplifiers. ULV full-custom designed amplifiers, especially the body-driven ones, on the other hand exhibit heavy drawbacks in terms of area footprint, design time and effort for the layout step.

TABLE 5. Performance of the proposed OTA under mismatch variations.

	Typical	Mean	Std
A_{V_D} [dB]	34.97	34.85	0.34
A_{V_C} [dB]	7.89	10.99	8.26
GBW [MHz]	12.69	12.96	1.33
$m\varphi$ [deg]	62.56	63.2	1.84
P_D [μW]	6.10	6.25	0.14
$Offset$ [mV]	2.13	2.62	8.91
SR_p [V/μs]	4.54	4.55	0.48
SR_m [V/μs]	6.82	6.86	0.89

TABLE 6. Main performance parameters of the proposed OTA for different V_{DD} values.

V_{DD} [V]	0.2	0.3	0.45	0.6	0.75	0.9	1
C_{load} [pF]	2	2	2	2	2	2	2
A_{V_D} [dB]	30.18	34.97	37.57	38.54	37.86	36.31	35.24
A_{V_C} [dB]	5.25	7.89	7.63	7.59	7.92	7.95	7.87
GBW [MHz]	2.6	12.69	77.32	299.5	636	873.4	960
$m\varphi$ [deg]	68.23	62.56	59.12	57.93	59.08	61.15	62.43
P_D [μW]	0.99	6.10	56.07	338.3	1.32k	3.47k	5.66k
$Offset$ [mV]	3.20	2.13	2.08	2.32	3.13	4.75	6.21
SR_p [V/μs]	0.60	4.54	30.24	75.19	130.7	194.8	239.9
SR_m [V/μs]	0.78	6.82	47.08	122.8	213.6	317.5	391.8

3) MISMATCH MONTE CARLO SIMULATIONS

The proposed amplifier has been tested under mismatch variations and results of the analysis are reported in Tab. 5. As it can be observed, the common-mode gain shows a certain sensitivity to mismatch variations due to the fact that matching between g_{m_2} and $g_{m_{2'}}$ strongly affects the overall *CMRR* (see eq. (8)). However, as outlined in Fig. 9, both the mean value and the standard deviation result greater than the one showed by the conventional D2S, and this allows to attain better CMRR with a greater yield if compared with the conventional D2S.

In addition, as outlined from Tab. 5, the GBW, the phase margin, the P_D and also the $SR_{p,m}$ result in very good agreement with typical simulations. The offset, which is one of the main drawbacks of fully synthesizable OTAs results to be in line with literature [3], [7], [30], [32] and, if compared with the same OTA which exploits the conventional D2S appears to be comparable, in spite of having adopted minimum sized standard cells for the error amplifier A_D. Indeed, under mismatch variations, the same architecture with conventional D2S shows an offset whose mean value is comparable with the one presented in Tab. 5, but the standard deviation results slightly higher (9.81 mV) than the one of the proposed (8.91 mV). This result is not obvious, since as outlined in Section III-D a further mismatch contribution was added. However, the effect of the negative feedback is to impose the reference voltage to the internal *node A* of the OTA, thus under mismatch variations the internal nodes of the OTA result to be better biased than the one in which the conventional D2S is exploited. Moreover, when the non inverting buffer is closed, the contribution of σ_{A_D} to the $\sigma_{V_{O,D2S}}$ can be neglected, since is attenuated by the overall A_{V_D} gain.

TABLE 7. Comparison table.

	This Work†	[11]†	[32]†	[5]†	[28]‡	[4]‡	[6]†	[30]†
Year	2022	2022	2022	2022	2021	2020	2020	2020
Technology $[\mu m]$	0.13	0.13	0.13	0.13	0.18	0.18	0.18	0.18
V_{DD} $[V]$	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
DC_{gain} $[dB]$	34.97	28.3	52.92	38.07	30	98.1	39	51
C_L $[pF]$	2	1.5	50	50	150	30	10	10
GBW $[kHz]$	12.69k	15.42k	35.16	24.14	0.25	3.1	0.9	0.27
$m\varphi$ $[deg]$	62.56	54	52.40	60.15	90	54.2	90	90
SR_+ $[\frac{V}{ms}]$	4.54k	9.08k	18.61	20.02	-	14	-	-
SR_- $[\frac{V}{ms}]$	6.82k	9.08k	11.51	8.44	-	4.2	-	-
SR_{avg} $[\frac{V}{ms}]$	5.68k	9.08k	15.06	14.23	0.085	9.1	-	-
$CMRR$ $[dB]$	27.08	41.07	42.11	54.88	41	60	30	37
$Power$ $[nW]$	6.10k	4.41k	21.89	59.88	2.4	13	0.60	0.50
$Mode$	STD CELL	STD CELL	BD	BD	DIGITAL	BD	GD	GD
$Area$ $[\mu m^2]$	217.85	164	5.2k	2.7k	982	9.84k	472	727
$FOM_{S,A}$ $[\frac{MHz \cdot pF}{mW \cdot \mu m^2}]$	19.10	32.01	15.44	7.47	16.18	0.73	31.77	7.43
$FOM_{L,A}$ $[\frac{V \cdot pF}{\mu s \cdot mW \cdot \mu m^2}]$	8.54	18.84	6.62	4.4	5.50	2.13	-	-
$FOM_{L_{wc},A}$ $[\frac{V \cdot pF}{\mu s \cdot mW \cdot \mu m^2}]$	6.84	18.84	5.06	2.61	-	0.98	-	-

† Simulated; ‡Measured .

C. SCALABLE PERFORMANCE UNDER SUPPLY VOLTAGE VARIATIONS

In order to investigate the possibility of scaling the performance with the supply voltage, the proposed OTA has been simulated also under different supply voltages ranging from 0.2V to 1V. Main performance parameters for the different V_{DD} values are reported in Tab. 6. It has to be remarked that, as expected, the small signal and large signal performances improve with higher V_{DD}, with a corresponding increase of the power consumption. An important feature of the proposed OTA which is evident from Tab. 6 is that, even if the load capacitance is left unchanged at 2pF for all the simulated supply voltage values, the phase margin of the OTA remains almost constant. This is due to the fact that the poles ratio is given by:

$$\frac{\tau_L}{\tau_{o_1}} = \frac{C_L}{C_Z} \frac{g_{ds_5}}{g_{ds_1} + g_{ds_2}} \tag{28}$$

Since both C_Z and the ratio $g_{ds_5}/(g_{ds_1}+g_{ds_2})$ are very weakly dependent on the supply voltage, the poles ratio remains unaltered under different V_{DD} values and the phase margin doesn't change significantly according to eq. (26).

D. AUTOMATED LAYOUT FLOW

The schematic of the OTA in Fig. 8 has been described in structural Verilog language by instantiating the x2 and x160 inverters taken from the standard-cell library and the obtained Verilog netlist is reported in the APPENDIX. The Verilog netlist has been imported in the Cadence Innovus environment, together with all the technology files needed in the conventional place and route flow usually adopted for digital circuits. A conventional place and route flow (without timing constraints) including design import, floorplanning, place, and routing has then been carried out exploiting the same scripts conventionally adopted to implement digital circuits as in [29]. The automatically generated layout is depicted in Fig. 17 and has resulted in an Area consumption of about 217.86 μm^2 (Width=22.15 μm, Length=9.84 μm).

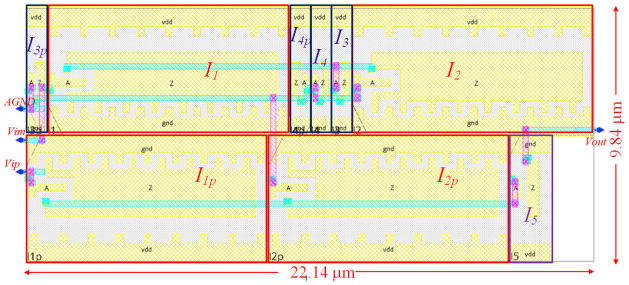

FIGURE 17. Layout of the proposed standard-cell OTA generated by the place and route tool.

VI. COMPARISON

The proposed OTA exploiting the improved D2S has been compared with other ULV high performance OTAs from the literature. The small-signal and large-signal figures of merit (FOM_S and FOM_L) are the most common metrics exploited to compare OTAs. However, these metrics do not take into account the Area contribution of the OTA, so in [28] the area-normalized $FOM_{S,A}$ and $FOM_{L,A}$ have been proposed. These two FOMs are defined as follows:

$$FOM_{S,A} = \frac{GBW \cdot C_L}{P_D \cdot Area}; \qquad FOM_{L,A} = \frac{SR_{avg} \cdot C_L}{P_D \cdot Area} \tag{29}$$

The performance of the most performant ULV OTAs (i.e. operating down to 0.3V of supply voltage) with respect to Area-normalized FOMs have been depicted in Tab. 7. As it can be observed, just [11] results in lower area footprint and higher $FOM_{S,A}$, $FOM_{L,A}$. It has to be noted that also the DIGITAL OTA, presented in [2] results in low area-consumption and good trade-off between performance and area consumption. Moreover, among the full custom OTAs, despite its high

area usage (about 25 times greater than the one proposed), also [32] shows very good values of the area normalized FOMs.

VII. CONCLUSION

In this paper we have proposed a novel topology of inverter-based D2S converter based on an auxiliary standard-cell-based local feedback loop which allows to improve the accuracy of the current mirror performing the differential to single-ended conversion. Simulation results have shown that the proposed D2S, compared to the conventional one, exhibits higher CMRR, improved ICMR and better robustness with respect to PVT variations. An ULV standard-cell-based OTA which exploits the proposed D2S has also been presented, showing excellent performance in terms of both area usage and performance figures of merit. Mismatch Monte Carlo simulations performed on the proposed ULV OTA have demonstrated good performance of the OTA under mismatch variations in spite of the adoption of minimum sized inverters for the A_D block. This confirms the effectiveness of the proposed approach which, at a very low cost (in the range of 2%) in terms of increased area and power consumption, results in greatly improved CMRR, ICMR and robustness.

APPENDIX

The netlist of the architecture depicted in Fig. 8 is as follow:

```
module d2sota ( AGND, Vim, Vip, Vout );

inout  AGND, Vim, Vip, Vout;

IV_X20_PB0_L I5 ( .Z(Vout), .A(net4));
IV_X160_PB0_L I1p ( .Z(net4), .A(Vip));
IV_X160_PB0_L I2p ( .Z(net4), .A(net2));
IV_X160_PB0_L I1 ( .Z(net1), .A(Vim));
IV_X160_PB0_L I2 ( .Z(net1), .A(net2));
IV_X2_PB0_L I3p ( .Z(net2), .A(AGND));
IV_X2_PB0_L I3 ( .Z(net3), .A(net1));
IV_X2_PB0_L I4p ( .Z(net2), .A(net3));
IV_X2_PB0_L I4 ( .Z(net3), .A(net3));

endmodule
```

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