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RESEARCH ARTICLE

Novel Observations and Physical Insights on PSIJ Behavior in CMOS Chain-of-Inverters

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ABSTRACT This paper presents novel observations and physical insights on jitter in a chain of CMOS inverters. It is demonstrated that at the final output of the inverter chain, power supply induced jitter does not necessarily increase with the number of inverter stages. The presented investigation is validated by comparing the results using a semianalytical method with SPICE based simulations. The proposed observations are also validated using measurement results obtained by two measurement setups.

INDEX TERMS CMOS inverter, chain of inverters, delay-line, jitter, power supply induced jitter.

I. INTRODUCTION

This paper presents an extension of the work presented in [1] by introducing novel observations and physical insights on power supply induced jitter (PSIJ) in a CMOS chain-of-inverters. The chains of CMOS inverters have various applications in VLSI systems such as delay lines or as clock networks, etc. [2], [3], [4]. Chain-of-inverters are also used in I/O drivers for driving on-chip and off-chip loads. For driving higher capacitive loads, tapered buffers are used [5] where chain-of-inverters are designed with the geometric progression size for subsequent inverter stages. The delay of these chains is very sensitive with respect to power supply variations [6]. Power supply noise (PSN) causes time interval error (TIE) which in turn contributes to PSIJ [7], [8], [9], [10], [11], [12], [13]. Due to narrow timing margins and very low supply voltages, PSIJ is one of the critical performance parameters that significantly impacts the overall timing budget in present high-speed systems. There are many studies available in the literature for the analysis of TIE and PSIJ in CMOS chain-of-inverters [13]. This paper presents a novel investigation on nature of PSIJ in CMOS chain-of-inverters.

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A. RELATIONSHIP BETWEEN NOISE AND JITTER

In a CMOS inverter, noise can propagate to its output through power supply, ground and input terminals. The noise at output propagating through different paths depend on the transfer functions of the respective paths [14]. Due to the total noise response, the transition edge (rising/falling) of the output signal may deviate from nominal position, known as time interval error (TIE). An efficient technique for estimation of TIE is presented in [15], using the slope of the output response. In this method, TIE is estimated from the total noise response at the mid-point of the rising/falling edge by dividing it by the signal slope at the same point. The expression for the TIE (or instantaneous jitter, represented by J_r) for a particular bit is given as:

$$\text{TIE} = J_r = \frac{v_{r_n}(t_m)}{\alpha_{t_m}} \tag{1}$$

where, $v_{r_n}(t_m)$ is the magnitude of noise response at the mid-point (t_m) of rising/falling edge of the output response (calculated using the noise transfer function) and α_{t_m} is the slope of the signal at t_m. By calculating TIE for a large number of bits using (1), the PSIJ can be estimated as:

$$\text{PSIJ} = J_{P-P} = \max(J_r) - \min(J_r) \tag{2}$$

Here, J_{P-P} corresponds to the peak-to-peak jitter. The above expressions for PSIJ estimation [1], [15] are further adopted

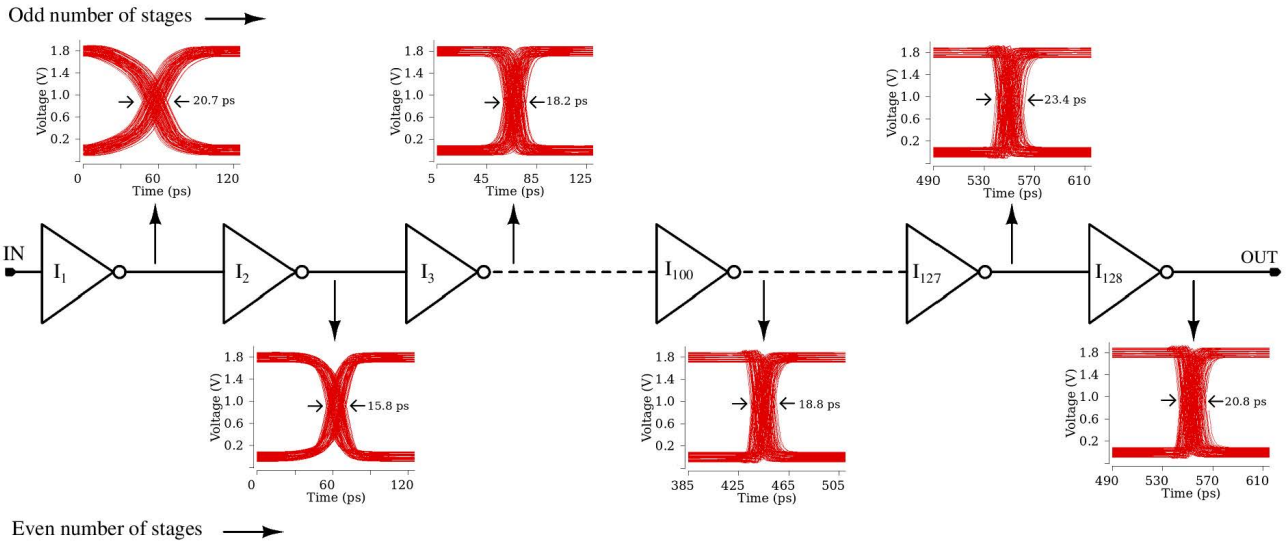

FIGURE 1. Eye crossing at the output of chain-of-inverters with different number of stages in the presence of multiple noise sources.

to obtain physical insights into the behavior and impact of power supply noise on timing deviations, and are detailed in the following sections.

II. NOVEL OBSERVATIONS ON THE BEHAVIOR OF PSIJ

Fig. 1 shows a CMOS inverter based delay-line frequently used in clock networks of digital systems. The number of inverter stages in the chain may vary based on the amount of delay required by the system.

In the example used in Fig. 1, 128 inverter stages are used and the figure shows the simulated eye-crossings at the output of various number of stages in the presence of power supply as well as ground noise sources. The inverters are designed in 55 nm triple-gate oxide BiCMOS technology of STMicroelectronics with a supply voltage of 1.8 V. For simulation purposes, different sinusoidal signals with frequencies ranging from 200 MHz to 800 MHz are used as noise sources. A signal with data rate of 1 Gbps is applied at the input. The simulation was done using industry standard EDA tools. *In Fig. 1, it can be observed from the eye-diagrams that, PSIJ is not increasing monotonically along the number of stages, instead it tends to decrease at the output of even number of stages and increase at the output of odd number of stages.*

III. PHYSICAL INSIGHTS

The phenomenon of the behavior of peak-to-peak jitter values in the eye-diagrams of Fig. 1, can be explained by a simple example having a chain of three inverters as shown in Fig. 2. In Fig. 2, the noise sources $v_{n_s}(t)$, $v_{n_g}(t)$ and $v_{n_d}(t)$ correspond to the deterministic noise sources at different terminals representing supply noise, ground noise and data noise, respectively.

Consider the rising edge of a data signal at the input of a chain-of-inverters in the presence of noise. The

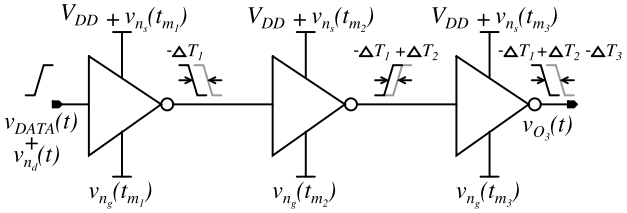

FIGURE 2. A rising edge of input signal and the corresponding rising/falling edge of output signals in the presence of multiple noise sources in a chain-of-inverters. Here the black lines at the output of inverters represents the ideal waveform and the grey line represents the deviated waveform in the presence of noise sources.

corresponding signal transitions (rising/falling) at the output of each stage are shown in Fig. 2. At the output of the first stage, the slope ($\alpha_{t_{m_1}}$) is negative (due to the falling edge) at the mid-point (t_{m_1}). Hence, if the total noise response ($v_{o_1}(t_{m_1})$) is positive, then the TIE (J_{r_1}) will be negative and is represented by ΔT_1, given by:

$$\Delta T_1 = \frac{v_{o_1}(t_{m_1})}{\alpha_{t_{m_1}}}. \tag{3}$$

After the propagation delay of inverter ($t_{m_2} - t_{m_1}$), the output of second inverter reaches mid-point (t_{m_2}) of rising edge. If the noise frequency is not very high, the phase of total noise response ($v_{o_2}(t_{m_2})$) will also be approximately same as the phase of $v_{o_1}(t_{m_1})$. Also, note that, for this stage, the TIE due to power supply and ground noise will be positive (due to positive slope). Correspondingly, the total TIE at the rising edge of the second inverter output can be estimated as [16]:

$$J_{r_2} = -\Delta T_1 + \Delta T_2 \tag{4}$$

where $\Delta T_2 = \frac{v_{o_2}(t_{m_2})}{\alpha_{t_{m_2}}}$. From (4), it can be seen that the magnitude of total TIE is reduced at the output of second

TABLE 1. TIE at different stages.

Inverter Stage	Signal Slope	Total TIE at the output of the stage
Stage - 1	Negative	$-\Delta T_1$
Stage - 2	Positive	$-\Delta T_1 + \Delta T_2$
Stage - 3	Negative	$-\Delta T_1 + \Delta T_2 - \Delta T_3$

stage. Similarly, at the output of the third stage, note that the phase of total noise response ($v_{o_3}(t_{m_3})$) at the mid-point (t_{m_3}) is approximately same as that of phase of $v_{o_2}(t_{m_2})$. Also, the TIE due to power supply and ground noise will be negative (due to negative slope). Consequently, the total TIE at the rising edge of third inverter output can be expressed as:

$$J_{r_3} = -\Delta T_1 + \Delta T_2 - \Delta T_3; \qquad \Delta T_3 = \frac{v_{o_3}(t_{m_3})}{\alpha_{t_{m_3}}}. \tag{5}$$

As is obvious from (5), the magnitude of the total TIE is increased at the output of third stage compared to the one at the output of 2nd stage. Table 1 shows the sign of slopes and the corresponding TIE at the output of each stage.

A. TAPERED BUFFERS AND DELAY LINES

For the case of tapered buffers also, a similar pattern follows as the magnitudes of transfer functions remain approximately constant in spite of scaling of inverter sizes (both nMOS and pMOS). This is because the numerator and denominator of the transfer functions (refer to (47) of [1]) scale proportionally with respect to the size of MOSFET. Also, the transfer functions scale based on the biasing conditions.

It is to be noted that, in delay lines, after initial few stages, the slope of the noise response approximately remains same, and also the biasing conditions at the mid-points ($t_{m_1}, t_{m_2}, t_{m_3}$, etc.) (refer to Fig. 9 of [1]). In other words, the rise/fall times after a few stages in a long chain of inverters do not depend much on the rise/fall time of the input at the first stage.

Hence, it can be concluded that the incremental/decremental TIE (ΔT) at the output of each stage of a chain-of-inverters will be approximately same (assuming that the frequency of noise is very low compared to the propagation delay of an inverter). This is observed in Fig. 1, where there is not much change in jitter values between the output of first stage inverter and 128th stage inverter, in spite of a large number of stages in between.

IV. RESULTS AND DISCUSSION

A. SIMULATION RESULTS

Four Examples are considered in this section to validate the novel observations and physical insights presented in this paper. First example presented here corresponds to the Example-5 of [1] which considers a delay line having 10 equal sized inverters with data rate of 240Mbps and the noise sources at data input, supply and ground, having frequencies of 233 MHz, 1 GHz and 500 MHz, respectively. The amplitudes for all the noise sources are same but different phases are used. Fig. 3(a) (which corresponds to the Fig. 14(a) of [1]) shows the jitter at the output of every stage using the conventional SPICE simulation and the proposed estimation. As can be seen from the graph, after the initial three stages, the peak-to-peak jitter remains approximately constant for all odd stages (also true for even number of stages) confirming the novel observations. To further verify the validity of the presented observations, three more experiments are performed in the similar way using tapered buffer circuit with stage ratio of 2, and with different types of noise sources (e.g., sawtooth noise). Here, the saw-tooth noise is generated by superimposing multiple sine waves. In all three new examples presented here, the inverter chain is designed in 55 nm CMOS technology and the input data rate to the inverter chain is 1 Gbps. The peak-to-peak amplitude of the noise is restricted to $\frac{V_{DD}}{10}$ so that the bias conditions don't change. Corresponding results are presented in Fig 3 (b), (c) and (d). It can be observed from the plots, after the first few initial stages, that the incremental and decremental PSIJ at the output of odd and even number of stages, respectively, remain approximately the constant. Hence, after few initial stages, the peak-to-peak jitter remains approximately constant for all odd (and even) number of stages. These results confirm the novel observations made in this paper, that the PSIJ after initial few stages remains more or less the same due to the cancellation of TIE from odd and even stages.

B. IMPACT OF ON-CHIP INTERCONNECTS ON THE PROPOSED OBSERVATIONS

The proposed observations are also correct in different technologies/foundries, including the effects of interconnects in presence of supply fluctuations. For the purpose of validation, the length of the segment (or the metal wire) between two inverters is roughly in the range of 1 μm for 180 nm technology or below technology nodes. The maximum noise considered in work is 1 GHz, the wavelength of which will be equal to 30 cm. Thus, for this comparatively small electrical length of 1 μm, the phase of noise will not change significantly. Noise at lower frequencies will have even larger wavelengths. The interconnect RC values can be minimal compared to the total node capacitance and resistance of the transistors at the output of each inverter. Hence the effect of interconnects on the charging and discharging of node capacitance will be negligible. Because of this, the effect of interconnects on TIE will also be negligible. For the purpose of validation, a chain of 10 inverters is designed in CMOS 180 nm technology node of Lfoundry and simulated with and without interconnects between every consecutive stage. Fig. 4 shows the comparison between both the cases, which assures the validity of the proposed claim in the presence of on-chip interconnects. It is worth to note that if the total electrical length of the inverter chain is very small compared to the wavelength of the noise, the phase of noise will not change significantly from the input to output stage. Hence the rule presented in this work will hold irrespective of the distance

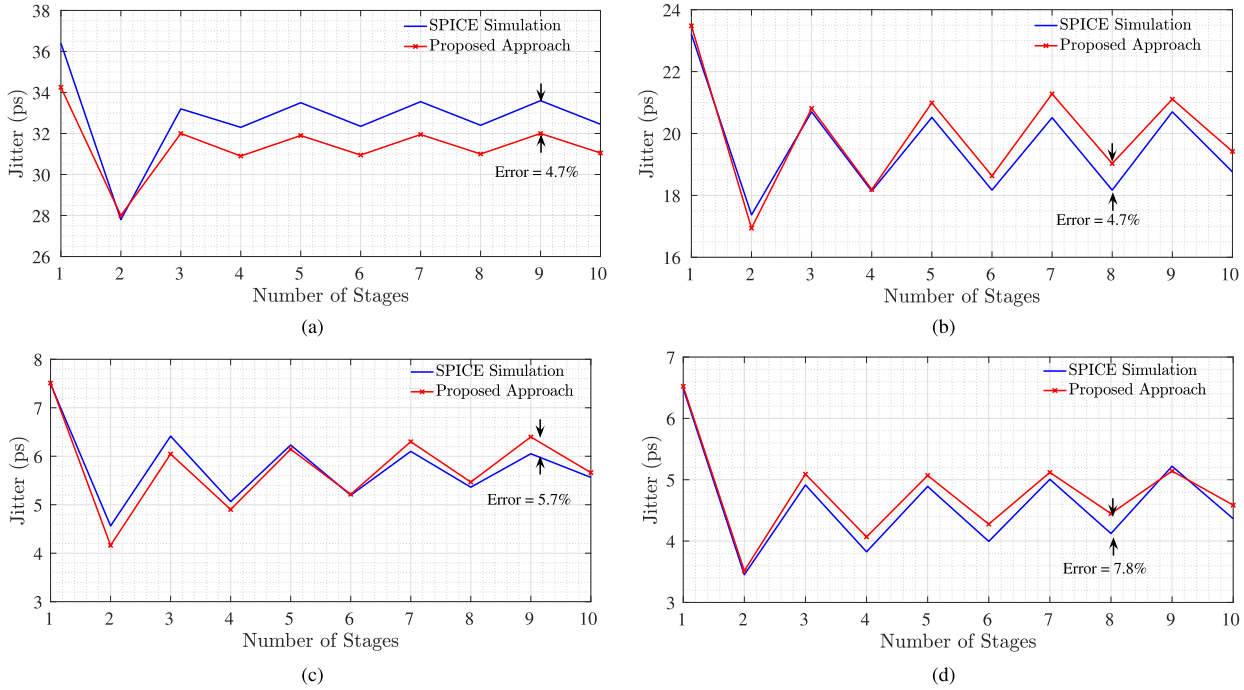

FIGURE 3. Comparison of jitter estimation using simulation and proposed approach for inverter chains with different number of stages: (a) Delay-line with three different sinusoidal signals as noise sources at power supply, input and ground [1], (b) Tapered buffer with three different sinusoidal signals as noise sources at supply, input and ground. (c) Tapered buffer with one sawtooth wave as noise source at supply. (d) Tapered buffer with sawtooth wave as noise at ground.

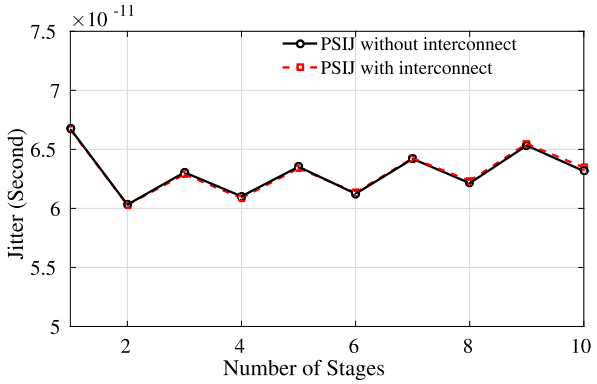

FIGURE 4. Comparison between PSIJ values at the output of each stage in a chain-of-inverters with and without RC interconnects.

between inverters if the frequency of the noise is not very high.

C. MEASUREMENT RESULTS

In this section, measurement based validation of the proposed concepts is presented. For this purpose, two measurement setups are used. These setups were designed in two different laboratories.

1) MEASUREMENT SETUP-1

Fig. 5(a) shows a block diagram of the first measurement setup for the estimation of PSIJ in the presence of PSN. The setup consists of a device under test (DUT), an arbitrary function generator (AFG) (AFG1062 by Tektronix) for the input waveform generation, an Oscilloscope (MSOS104A by Keysight) for the measurement of PSIJ. A series combination of DC supply and PSN Source is used for providing the power supply voltage (V_{DD}) with small ac fluctuations to the DUT. For the PSN source, a single-tone sinusoidal signal is generated using the same AFG. A prototype with ten CMOS inverter stages has been designed using the CD74HCT04E integrated circuit (IC) (vendor: Texas Instruments). This is accomplished using two CD74HCT04E ICs as each of the ICs contains only six independent CMOS inverters. An equal length for interconnects is considered for connection between any two stages. A photograph of the complete measurement setup is given in Fig. 5(b).

In this experiment, a 1 V single-tone sinusoidal signal having a frequency of 5.213 MHz is applied on top of the V_{DD}. The data rate of the input signal is 6 Mbps and is varied from 0 V to V_{DD}, where V_{DD} is 5 V. For the PSIJ measurement, an eye diagram is plotted using a mixed-signal oscilloscope (MSO) with and without supply fluctuations. The difference between the two gives the PSIJ. A photograph of the complete measurement setup is depicted in Fig. 5(b). The measurement results of PSIJ with respect to the number of stages is shown in Fig. 6. The behaviour of the PSIJ in Fig. 6 also confirms the validity of the proposed observations.

2) MEASUREMENT SETUP-2

For additional validation, a second measurement setup, this time with different modules with similar type of connections as in setup-1 is setup. Here, two M74HC04B1 ICs (vendor: STMicroelectronics) were used and the Oscilloscope model

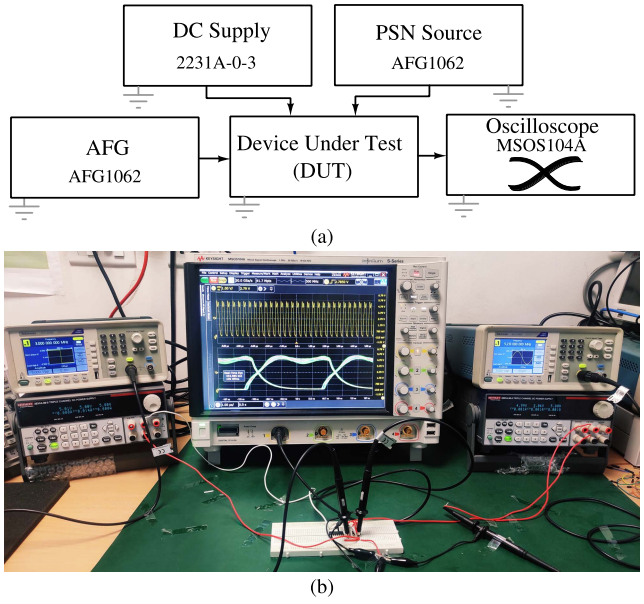

FIGURE 5. Measurement setup: (a) Block diagram and (b) Photograph.

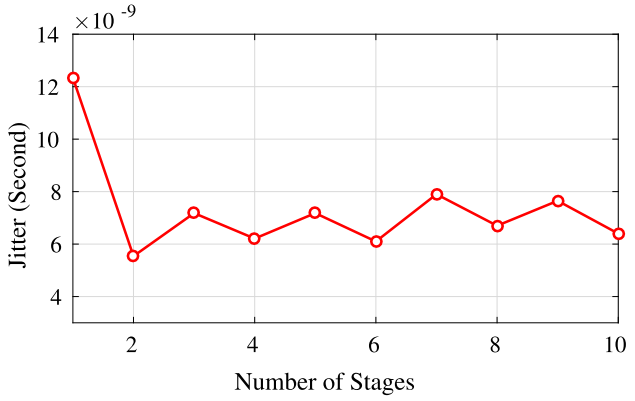

FIGURE 6. Jitter for a 10 stage inverter chain using measurement Setup-1.

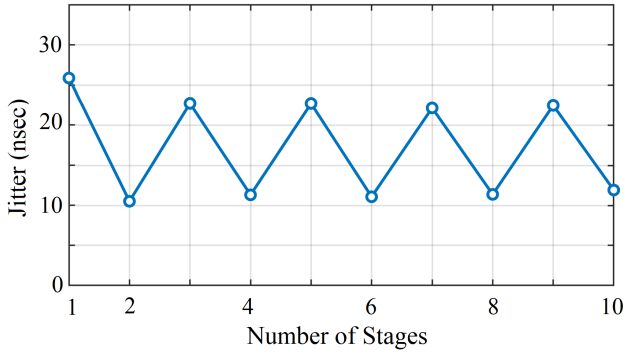

FIGURE 7. Jitter for a 10 stage inverter chain using measurement Setup-2.

MSOX4054A (Keysight) was used. The function generator used was DDS30 (Aplab). In this case, the data rate used was 3 Mbps. All other input parameters were same (e.g. noise amplitude, frequency, etc.) as in measurement setup-1. The measurement results of PSIJ with respect to the number of stages is shown in Fig. 7.

It is evident that results obtained from both the measurements converge and support the proposed observations and theory developed in this paper.

V. CONCLUSION

Novel investigations and physical insights for time interval error as well as power supply induced jitter in a chain of CMOS inverters due to the effect of power supply noise are presented in this paper. It is demonstrated using several simulation as well as measurement results that PSIJ is not necessarily higher in a chain of inverters having higher number of stages.

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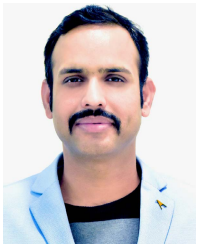

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