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RESEARCH ARTICLE

A-Si TFT Integrated Gate Driver Workable at −40 °C Using Bootstrapped Carry Signal

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ABSTRACT A thin-film transistors (TFTs) integrated gate driver which can work well at low temperature down to −40 °C is proposed and demonstrated. The carry signal (C_N) of the driver, being generated through the voltage bootstrapping approach using a C_N-connected capacitor, is used to pre-charge the following stage of the driver. As the rising and falling time of C_N is much shorter than that of the gate driving signal G_N, the bootstrapping voltage is increased and voltage loss of the pre-charge transistor can be much reduced, to avoid the driver's malfunction at low temperature. This structure further benefits maintaining the driving speed over long operation time at high temperature. On the other hand, the G_N, instead of C_N, is used to reset the gate driver to suppress the voltage feed-through effects. One single stage of the driver consists of 11 TFTs and 2 capacitors, driven by 4 clock signals with the duty ratio of 25%. An a-Si:H TFTs implemented single stage circuit of the driver occupies an area of 250 μm×1099 μm. Measurements show that the output voltage magnitude can be maintained well when temperature varies from −40 °C to 80 °C. Moreover, the rising-time and falling-time increase of the output pulse are both less than 3 μs after 240 hours of the accelerated high temperature aging operations.

INDEX TERMS A-Si TFT, gate driver circuit, reliability, low temperature.

I. INTRODUCTION

Nowadays gate driver integration using thin-film transistors(TFTs) has been a mainstream in high-end active matrix displays due to the merits of decreased peripheral driver chips, narrower display bezel with simplified module process, and reduced manufacturing cost [1], [2], [3], [4]. However, implementations of TFTs integrated gate-driver for higher resolution display with large panel size become increasingly challenging [5], [6], [7]. This is because the effective addressing time of gate-lines is limited and pixel charging ratio is insufficient due to the increase of loading resistance and capacitance at gate driver's output electrodes [8]. In addition, at lower temperature, the effective gate addressing time is further reduced due to the serious degradation of circuit speed, and even malfunction of gate driver circuit, especially for vehicle or mobile displays [9]. On the other hand, at high temperature, there are reliability issues after gate drivers experience long operation time.

Up to date, hydrogenated amorphous silicon (a-Si:H) TFTs are still playing important roles in the flat panel display industry, thanks to the mature manufacturing process, low fabrication cost, and good electrical uniformity over large substrate area, [11], [12], [13]. However, the workable temperature range for a-Si:H TFT based gate driver is a critical issue as the speed and stability are seriously degraded at low and high temperature, respectively [14], [15]. This is because there is conduction current decrease at lower temperature, while the threshold voltage shift with fast speed for long operation time at high temperature, [16], [17], [18]. Therefore, new circuit schematic with increased circuit speed is of great importance, to extend applications of a-Si:H TFT circuits in vehicle and mobile display panels.

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For conventional schematic, buffer TFTs with large width-to-length ratio (W/L>10^4), which occupies significant layout areas, are used to reduce the rising and falling time of the gate driver, especially for low temperature operations. However, due to the limited bezel area of display module, it is still difficult to meet the timing requirements by only increasing W/L of the buffer transistor for high resolution displays [19], [20], [21], [22], [23]. Furthermore, buffer transistor with too large W/L also leads to additional parasitic capacitance, which increases voltage feed-through effect and dynamic power consumptions. Liu *et al.* demonstrated a low temperature workable gate driver [12], with an additional carrying signal i.e. C_N, which is in the same phase with the gate driving node, to control the shift register components. Lin *et al.* proposed increasing the over-drive voltage (i.e. Vgs-Vth) of the buffer transistor with multiple-voltage-bootstrapping approaches, which benefits decreased rising and falling time while maintaining small buffer transistor [13]. However, this method requires additional transistors and capacitors, which consumes additional layout area. Hence, new circuit topologies are still needed to improve the driver's transient performance for wider temperature range and better stability.

This paper proposes a new integrated gate driver circuit with separated C_N and G_N nodes, while the C_N node is connected to a bootstrapping capacitor. In section II, the circuit structure and operating details are described. In section III, measurements of transient response at low temperature with different schematics will be compared. Following that, reliability measurement results with long time are discussed in section IV.

II. THE PROPOSED GATE DRIVER

Fig. 1 shows the proposed gate driver with the block diagram and the timing diagram. For the n-th single gate driver stage, ST1 and ST2 are two start signals, which are from the starting pulse (C0 and G0) for the first stage, and from C(n-1) and G(n-1), the output signals of stage (n-1) for the rest stages. Meanwhile, RST is the resetting signal, which is from RST1 and RST2 for stage (N-1, N), and from G(n+2), the output signal of stage (n+2) for the rest stages. Here, 2≤n≤(N-2), while N presents the total row of display matrix. Four non-overlapping clocks (i.e. CK1 to CK4) are used with the duty ratio of 25%, and the high/low levels are V_H/V_L, respectively. Because of the reduced clock frequency, compared with conventional schemes, the proposed gate driver renders lower power consumption and shorter stress time due to the reduction of clock's duty ratio [7], [14].

Fig. 2 demonstrates structure of the proposed gate driver, (a) schematic of the single stage, and (b) the timing diagram. For a single stage gate driver, 11 TFTs and 2 capacitors are employed, which consists of input TFTs (T1 and T2), driving TFT (T3a and T3b), and low-level-holding TFTs (T4 to T10). The gate electrode of T1 is connected to C_{N-1}, which plays the role of the start signal (i.e. ST) for pre-charging period, while the drain of T1 is connect with G_{N-1}. The gate

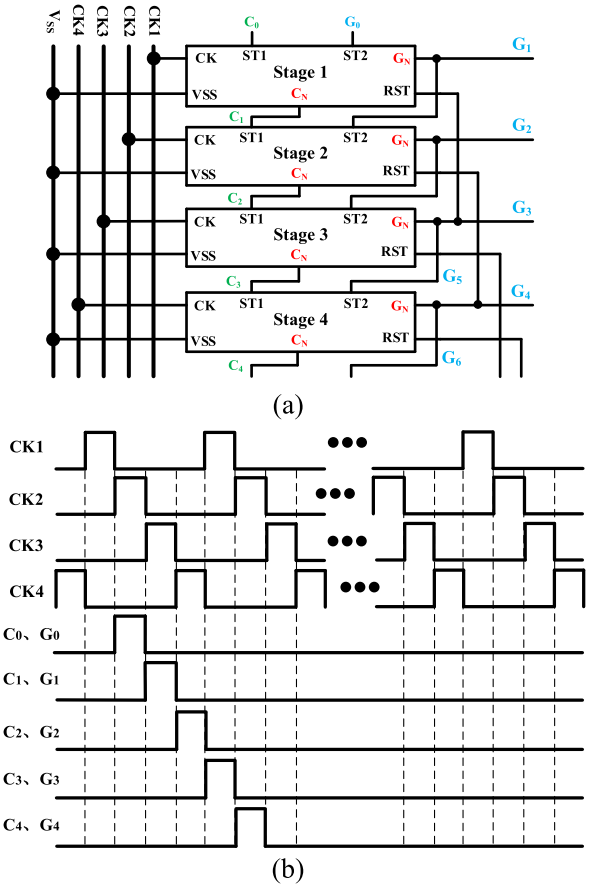

FIGURE 1. The proposed gate driver, with (a) the block diagram and (b) the timing chart.

electrode of T2, is connected to G_{N+2}, namely the reset signal (i.e. RST) for the pulling-down period. For the conventional gate driver circuits, RST is usually connected with C_{N+2} or C_{N+1}.

For a complete display frame, there are four successive operation periods, viz. (1) the pre-charging period, (2) the bootstrapping period, (3) the pulling-down period, and (4) the low-level-holding period. The operating principles will be described in details as follows.

A. PRE-CHARGING PERIOD (P1)

In the P1 period, T1 is turned on as both C_{N-1} and G_{N-1} are with V_H. Then through T1, charges are accumulated at the Q node, until the level of Q node reaches V_H - V_{TH1} by the end of P1 period, where V_{TH1} is the threshold voltage of T1. Consequently, the driving TFTs (T3a and T3b) are turned on in prior to the bootstrapping period. As the level of CLK is V_L, C_N and G_N are expected to maintain with the low voltage level. In addition, T5 and T7 are turned on to pull down the gate electrode of T6 and Q_B. Then T8, T9 and T10 are turned off, and the possible charge loss of Q node can be mitigated.

B. BOOTSTRAPPING PERIOD (P2)

In P2 period, node Q is floating as T1 is turned off due to the falling of C_{N-1} and G_{N-1} from V_H to V_L. In addition,

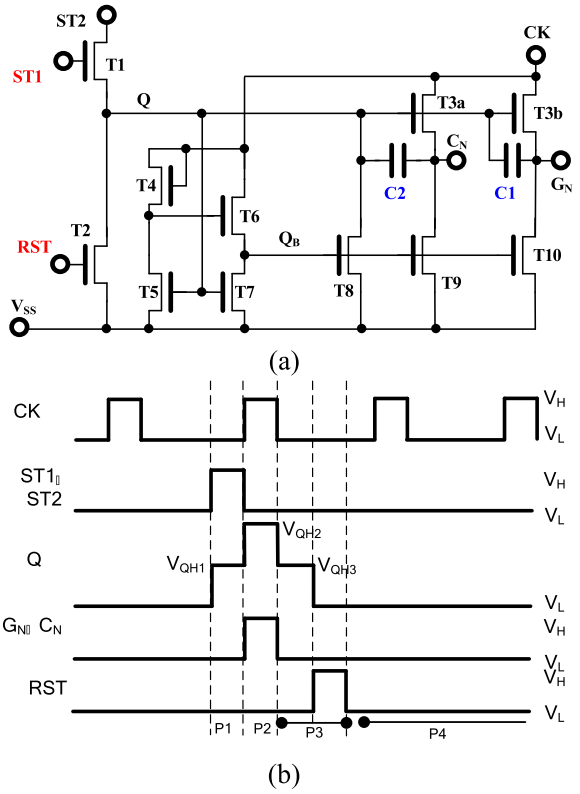

FIGURE 2. Schematic of the proposed single stage gate driver, with (a) the circuit structure and (b) the timing chart.

the other TFTs associating with Q node are also turned off. Meanwhile T3a and T3b are maintained turning on, following the rising of CK from V_L to V_H, then both the level of G_N and C_N are pulled up through T3a and T3b, respectively. According to the charge conservation law, the level of Q node can be bootstrapped to V_{QH2}, which helps keeping T3a and T3b with high conductance. Here, the value of C2 is much larger than C1 (C2>C1), thus the bootstrapping voltage of node Q can approximately be expressed by

$$V_{QH2} - V_{QH1} = \frac{C2}{C_Q}\left(V_{C_N} - V_L\right). \tag{1}$$

On the other hand, the bootstrapping capacitor is connected to G_N for conventional designs [3], [12], [14], and then the bootstrapping voltage of node Q can be expressed by

$$V_{QH2} - V_{QH1} = \frac{C1}{C_Q}\left(V_{G_N} - V_L\right). \tag{2}$$

For the initial stage of the P2 period, the level of C_N is obviously higher than G_N because of the decrease of loading capacitance. Consequently, the bootstrapping voltage for the proposed driver circuit can be increased compared with that of conventional schematics. Thus, we don't need to increase both C1 and C2, which are layout-area consuming. Instead, a larger C2 is preferred for higher voltage bootstrapping level and faster circuit speed, while the sum of C1 and C2 can be kept the same.

TABLE 1. Parameters of the proposed single stage gate drive.

Design parameter	Value
V_H	20 V
V_L	-10 V
L	5 μm
(W) $_{T1, T2, T8, T9}$	400 μm
$(W)_{T3a}$	800 μm
$(W)_{T3b}$	3000 μm
$(W)_{T4, T7}$	100 μm
$(W)_{T5,T6}$	200 μm
$(W)_{T10}$	500 μm
C1	0.5 pF
C2	2.0 pF

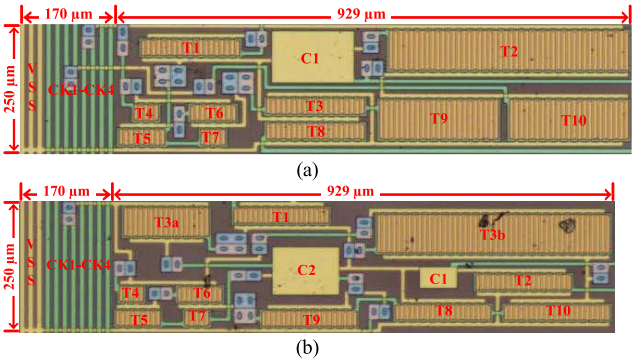

FIGURE 3. The optical image of the fabricated single stage gate driver, with (a) the conventional structure and (b) the proposed structure.

C. PULLING-DOWN PERIOD (P3)

In the first half of P3 period, due to the bootstrapping principal [21] again, the level of Q node is pulled down to V_{QH3}. As node Q is still floating, the value of V_{QH3} is approximately equaling to V_{QH1}. This means, T3a and T3b are maintained on and can be reused to discharge C_N and G_N, respectively.

While in the second half of P3 period, the level of G_{N+2} and C_{N+2} are raised up. Then charges of node Q can be removed and T3a and T3b are turned off in prior to the secondary CK pulse to suppress the possible feedthrough voltage.

D. LOW-LEVEL-HOLDING PERIOD (P4)

In the P4 period, node Q_B can be charged with V_H through T6 following the rising of CK from V_L to V_H. Then, T8, T9 and T10 are turned on to maintain the low level of node Q, C_N and G_N, respectively. On the other hand, if the level of CK is turned to V_L, node Q_B is discharged through T6, and then T8, T9 and T10 are turned off. For the presented gate driver circuit, the duty ratio of low-level-holding transistors can be reduced to 25%. As being avoided from stressing of constant direct voltage, the low-level-holding transistors will have improved stability with reduced V_{TH} shift (ΔV_{TH}).

III. TEMPERATURE MEASUREMENT RESULTS

The proposed gate driver is manufactured with the standard 5-mask a-Si:H TFT process. That is to say, both the gate driver and the display pixel array were implemented using a-Si:H TFT process. The channel length of all TFTs is 5 μm.

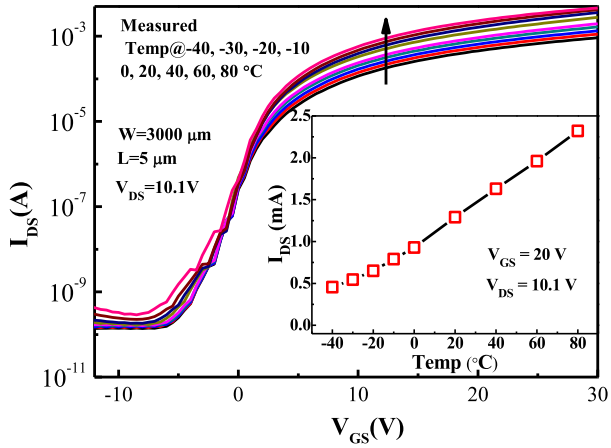

FIGURE 4. The measured transfer characteristics of the a-Si:H TFT with W/L = 3000 μm/5 μm for different operation temperature, while the inset shows the I_{DS} versus temperature with V_{GS} of 20 V and V_{DS} of 10.1 V.

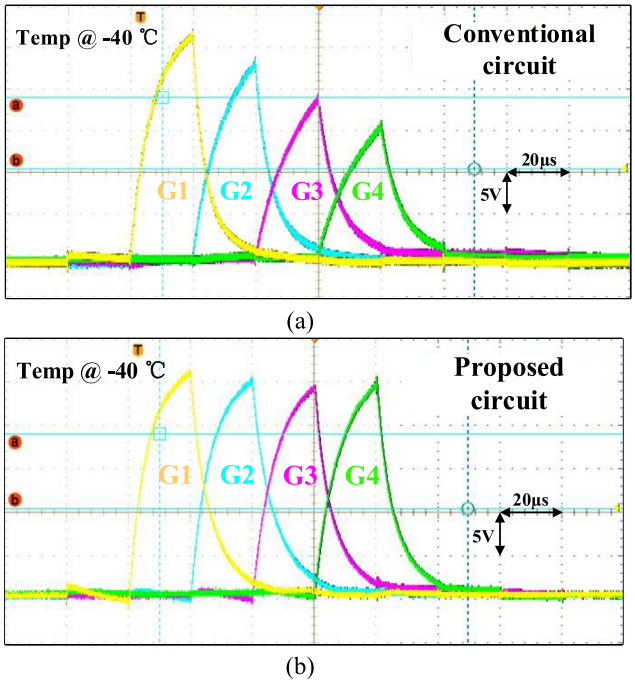

FIGURE 5. Comparison of the measured transient waveforms with the temperature of −40 °C, for (a) the conventional driver circuit and (b) the proposed driver circuit.

The overlap between gate-to-source electrodes and gate-to-drain electrodes is 3 μm. Then the parasitic gate-to-drain capacitance (i.e. C_{GD0}) and gate-to-source capacitance (i.e. C_{GS0}) are approximately 9×10^{-10} Fm^{-1}. Using the well-known linear extrapolation method, the fabricated a-Si:H TFTs has a threshold voltage of 1.3 V, and an equivalent filed-effective mobility of 0.65 $cm^2.V^{-1}s^{-1}$, and a sub-threshold swing of 0.96 V/dec. The geometrical and electrical parameters of the proposed driver circuit are listed in Table 1.

Fig. 3 shows the optical image of the fabricated gate driver with a single stage, using the conventional circuit structure (a) [3], and the proposed structure (b). For fair comparison, the sum of used capacitor area is kept the same, while both these two schematics have a layout area of 250 μm × 1099 μm for the single stage, including all the clock and Vss lines. During the transient response measurements, all the output electrodes of every gate driver stage are serially connected with the loading resistance and capacitance of 4.7 kΩ and 300 pF, respectively, to mimic the actual vehicle display panels with high resolutions.

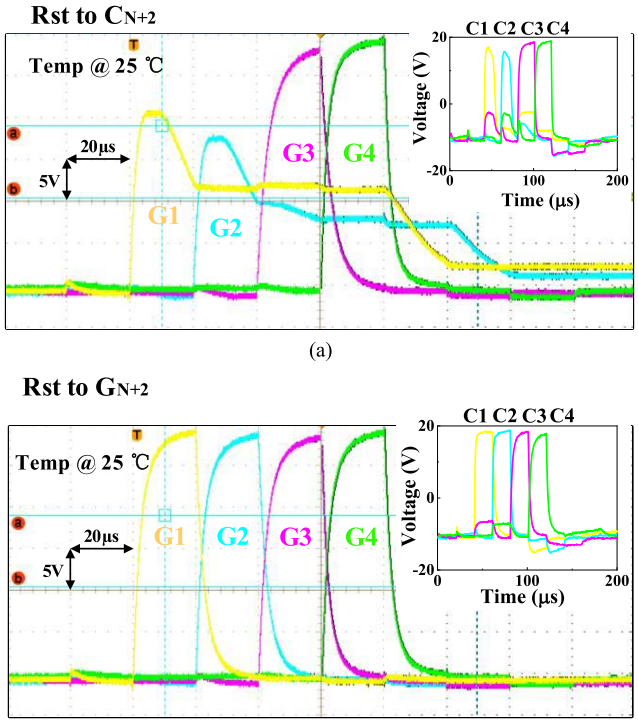

FIGURE 6. Transient response measurements of the gate driver, (a) the measured G1-G4 waveforms for RST connected with C_{N+2}, while the inset shows the measured C1-C4 waveforms and (b) the measured G1-G4 for RST connected with G_{N+2}, while the inset shows the measured C1-C4 waveforms.

Fig. 4 demonstrates the measured conduction current (I_{DS}) versus gate-to-source voltage (V_{GS}) of a-Si:H TFT with temperature variations from −40 °C to 80 °C. And the inset shows the evolution of I_{DS} with the temperature increases for V_{GS} of 20 V and V_{DS} of 10.1 V. It is observed that I_{DS} is decreased to 0.5 mA at −40 °C, which is only about one third of that at 20 °C. The on-current decrease at low temperature can be attributed to the reduction of the effective field mobility and increase of the threshold voltage, which were explained and modelled in [24] and [25].

The gate driver samples were cooled down using a closed incubator, while being connected to the external timing and voltage sources through flexible printed circuit (FPC). Fig. 5 illustrates the measured transient response of the conventional [3] and the proposed gate driver with 4 cascaded stages at low temperature. It is observed that the conventional gate driver fails to generate consecutive scanning pulses at the temperature of −40°C. While the proposed gate still functions well with the high voltage level above 15V from G1 to G4, although the rising and falling time are increased to 14.1 μs and 17.8 μs, respectively.

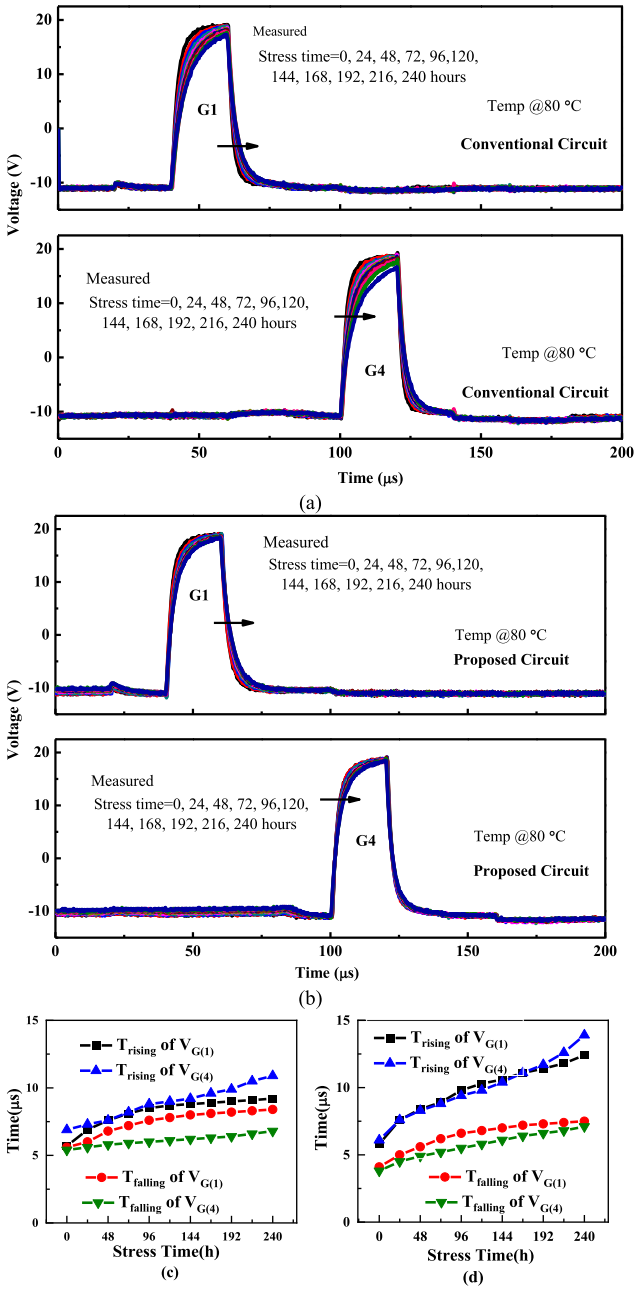

FIGURE 7. Waveforms comparison of G1 to G4 for the reliability measurements with 80 °C (a) the measured G1, G4 of the conventional gate driver, (b) extracted T_{rise} and T_{fall} of G1, G4, of the conventional gate driver, (c) the measured G1, G4 of the proposed gate driver, and (d) extracted T_{rise} and T_{fall} of G1, G4, of the proposed gate driver.

IV. RELIABILITY MEASUREMENT RESULTS

Fig. 6 (a) and (b) demonstrates the comparison of the measured G_N with RST terminal connected with C_{N+2} and G_{N+2} respectively, while the insets show the related C_N waveforms, and these measurements were conducted with room temperature. It is observed that the proposed gate driver circuit can output consecutive uniform C_N and G_N voltage pulses, with rising time and falling time of 4 μs and 4 μs, respectively. On the contrary, there are obvious amplitude loss and falling time increase in G1 and G2 waveforms with RST connected with C_{N+2}. These serious distortions in the waveforms of G1 and G2 are caused by the ripple waveforms of C3 and C4, which are sensitive to voltage feed-through effects due to smaller loading capacitance of carry signals.Aging measurements for the conventional [3] and the proposed gate drivers were conducted and compared at the high temperature of 80 °C. To accelerate the aging test, the frame period time is reduced to 620 μs, while the conventional frame period time is 16 ms. Fig. 7 (a) and (b) show the transient response of the conventional and the proposed gate driver, respectively. While Fig.7 (c) and (d) presents the extracted rising and falling time for the conventional and the proposed gate driver, respectively. After aging test of 240 hours, the magnitude of output waveforms of the conventional gate driver is decreased by 5 V, and rising and falling time are increased by 7.5 μs, and 3 μs, respectively. While for the proposed circuit, there is almost no voltage magnitude loss and both the increasing of rising and falling time are less than 3 μs. This can be attributed to the better driving ability of the proposed driver circuit, as the over-drive voltage of T3a and T3b is increased as shown in eq. (1) and (2). These differences become obvious when Vth shift of T3a and T3b are large after long operating time.

TABLE 2. Performances comparison among the proposed and other related work.

Parameters	Ref [3]	Ref [12]	Ref [14]	This work
TFT & Cap	10T-1C	8T-2C	20T	11T-2C
Clock number	4	12	4	4
Reliability	200 hours @80°C	NA	1500 hours @ 60°C	> 240 hours @80°C
Min. temperature	-20°C (meas.)	-40℃ (simu.)	NA	-40°C (meas.)
RC loading	4 kΩ, 300 pF	5.9 kΩ, 118 pF	NA	4 kΩ, 300 pF
Layout area of single stage	250×1099 μm^2	126×2410 μm^2	270×6420 μm^2	250×1099 μm^2
Power consumption per single stage	1.41 mW	NA	1.5 mW	1.75 mW

Table 2 lists the performances comparison among this work and other related one, in terms of circuit structure, signal numbers, and reliability. With a compact circuit topology, the proposed gate driver is effective to suppress the driving ability degradations over long operation time. The presented gate driver is also promising to be implemented using oxide TFTs, then driving ability of the integrated gate driver can be further improved for high-resolution and high frame-rate displays.

V. CONCLUSION

A TFT integrated gate driver using voltage bootstrapped carrying signal (C_N) was demonstrated to increase the driving ability for wilder operating temperature. Operating principles of the proposed gate driver were detailed. Transient

response and reliability performances over long operating time were measured using cascaded gate driver samples, which were fabricated by standard a-Si:H TFT process. It was demonstrated that voltage amplitude of the output pulses can be maintained with temperature variations from -40 °C to 80 °C, while the conventional gate driver malfunctions at -40 °C. Compared with conventional schemes, the proposed gate driver shows much reduced rising and falling time over 240 hours stressing measurements at 80 °C. Therefore, this presented gate driver circuit is promising for high-end vehicle and mobile displays with wide range of temperature.

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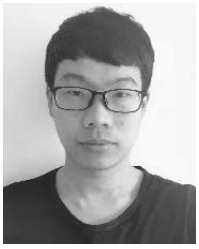

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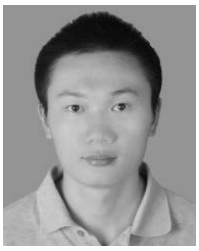

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