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RESEARCH ARTICLE

Conduction Performance Evaluation of Silicon and SiC Power Semiconductors for Solid-State DC Breakers

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ABSTRACT The main obstacle for the further development and commercialization of solid-state DC circuit breakers is the high ON-state power losses caused by the active power semiconductor devices. This paper presents an experimental evaluation of the electrical ON-state performance among several commercial high-power semiconductor device technologies rated at $1200V$ and $1700V$ at elevated temperatures. In addition, the potential of reducing ON-state losses by applying the maximum gate voltage, namely overdriving, has been assessed. It is shown that under nominal gate voltages, the normally-ON silicon carbide junction-field-effect transistor exhibits the lowest ON-state losses for both voltage classes, as well as at both temperatures. By using the overdriving concept, the ON-state voltage of silicon insulated-gate bipolar transistors has been minimized up to 10%. In addition to that, both the silicon carbide metal-oxide-semiconductor field effect transistors and normally-ON junction-field-effect transistors experience voltage reduction up to 16% and 33% respectively when overdriving, at elevated junction temperatures.

INDEX TERMS DC circuit breakers, losses, power semiconductor devices.

I. INTRODUCTION

Nowdays the direct-current (DC) distribution power grids have gained momentum over the alternating-current (AC) counterparts [1], [2]. DC grids will ease the interconnections of decentralized renewable electrical energy sources and utility-scale battery storage systems, as well as electrification of charging infrastructure. However, the lack of high performance protection equipment against DC short-circuit faults is currently a showstopper for the development of such grids [3], [4]. Until now, various circuit breaker (CB) concepts for medium- and high-voltage DC grids have been demonstrated [5]. These CBs can be classified to mechanical, solid-state and hybrid breakers. The solid-state CB clears faults shorter than the other two concepts, and it requires less maintenance [3]. On the other hand, solid-state CBs exhibit the lowest efficiency due to the high conduction losses caused in the utilized high-power semiconductor devices.

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Solid-state DC CBs might employ either fully controlled or semi-controlled active semiconductor devices [5]. The latter CB type utilizes mostly thyristors. Among others, Z-source [6], [7], T-source [8], and coupled-inductors-based breakers [9] employ semi-controlled devices. Under a fault, these CBs do not rely on an external triggering scheme and hence they are more sensitive to extensive load current variations, which might accidentally trigger the CB. On the other hand, CBs based on fully controlled semiconductor devices, namely interrupting CBs, seem to be more reliable in terms of their triggering process under faults and especially in DC applications that require short fault-clearance times and triggering current accuracy. This is the reason that the focus of this paper is the fully controlled semiconductor devices utilised in interrupting CBs, and not at the thyristor-based CBs, which necessitate additional power circuitry for forcing the fault current to zero. A typical structure of an interrupting solid-state DC circuit breaker is shown in Fig. 1. It comprises a current limiting inductor, L_s, high-power semiconductor devices, as well as voltage clamping circuits and energy absorption circuits [10]. In addition, auxiliary circuits for

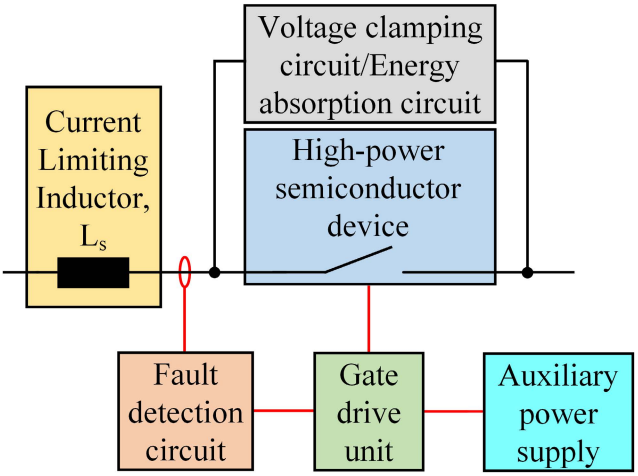

FIGURE 1. Block diagram demonstrating the main components of a typical interrupting solid-state DC circuit breaker.

fault detection and for supplying the required power to the gate of the semiconductor devices are also required.

Active power semiconductors utilized in interrupting solid-state CBs must exhibit three characteristics [11]. Firstly, their voltage ratings must be such to withstand transient overvoltages and to block the DC grid voltage safely during the fault-clearing process. Secondly, they should be able to turn-off the fault current with the minimum thermal stress. Last but not least, the high-power semiconductor devices employed in solid-state CBs must exhibit low conduction losses. This paper investigates the last criterion which is currently the obstacle in further development and commercialization of solid-state CBs. This becomes crucial considering that during the major part of a CB's lifetime, the breaker operates in the current-conduction mode, which eventually generates conduction power losses.

The use of voltage clamping circuits in a solid-state DC CB (as shown in Fig. 1), such as snubber circuits, enables soft switching operation at a cost of long fault clearance times [10]. These times might be significantly longer (e.g., several tens of microseconds) than the turn-OFF times of the active devices, which can be below $1\mu s$. Although the switching performance of a power semiconductor device is critical in switch-mode applications, this characteristic is less significant in solid-state breakers. The reason is that the active device used in such a breaker, switches less frequently compared to a switch-mode converter. Therefore, the switching performance of active power semiconductors in solid-state breakers in terms of switching losses and switching speed becomes less crucial compared to switch-mode applications.

Several high-power semiconductor devices have been investigated as candidates in interrupting solid-state DC CBs [5]. For high-voltage and high-power CB designs, the most popular bipolar Silicon-based technologies are insulated gate bipolar transistors (IGBTs) [12], integrated gate commutated thyristors (IGCTs) [13] or bi-mode insulated gate transistors (BIGT) [11]. On the contrary, at low-voltage DC grids (e.g., microgrids), unipolar semiconductors, such as Silicon-based metal-oxide semiconductor field effect transistors (MOSFETs) [14] and junction field effect transistors (JFETs) [15], [16] can also be used. With the advent of Silicon Carbide (SiC) semiconductors [16], [17], unipolar MOSFETs and JFETs can also be designed and fabricated with blocking voltages higher than $1kV$. The switching performance of these power semiconductor technologies in solid-state CBs during the fault-clearing process has been extensively investigated. From these studies, it is revealed that the existing semiconductors technology and their design principles used in switch-mode power converters can be adopted in the design of solid-state CBs. However, the operating capabilities of the existing semiconductors materials and power devices technologies in terms of reduced conduction power losses in interrupting solid-state CBs have not been assessed.

A way to reduce conduction power losses in a solid-state CB, is to decrease the ON-state voltage drop by increasing the chip area of the devices for a given current. However, this method imposes a larger investment cost and possibly a more complicated gate-driver design. On the contrary, a slight increase of the gate voltage, namely overdriving operation, can potentially lead to lower ON-state voltage drop, and thus, lower conduction power losses. Overdriving of the gates becomes possible in solid-state CBs, because there is no need for continuous and high-frequency switching operation, which might excite extensive transient overvoltages across the gate terminal. During a turn-OFF operation, the overdrive operation would not affect the anticipated negative overvoltage across the gate terminal. On the other hand, during a turn-ON operation, the gate overvoltage will be added to the overdrive voltage level. In order to avoid such a condition, a high gate resistance can be used and thus, the gate overvoltage will be minimized. An additional solution to deal with the turn-ON overvoltage challenge, is to apply initially the nominal gate voltage to avoid gate overvoltages, and only after the switching transient reached steady state, overdrive operation can be enabled until the next breaking operation.

The contribution of this paper is on evaluating the conducting performance of existing Silicon and SiC power semiconductor device technologies with voltage ratings in the range of $1200 - 1700V$. Such devices are suitable for operation in interrupting medium-power solid-state CBs in DC grid voltages of $700 - 1100V$. The evaluated criterion is the conduction power losses of each technology and voltage class at room temperature (i.e. 25^oC) and at elevated junction temperatures. Additionally, the conducting performance of the devices under overdriving operation with higher gate voltages than the nominal values is investigated, aiming to minimize the conduction power losses.

The paper structure is as follows. Section II presents an overview of high-power semiconductor devices suitable for solid-state CBs. The comparative evaluation of the high-power semiconductors at room temperature is shown in Section III. Section IV presents the results by applying the maximum gate voltage while Section V shows the

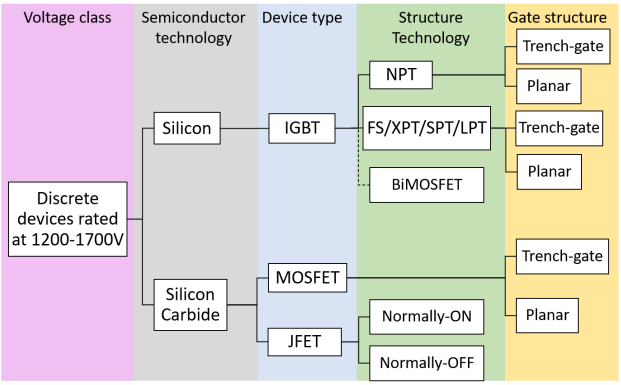

FIGURE 2. Commercially available high-power semiconductor devices suitable for solid-state DC breakers rated in the range of 1200 – 1700*V*.

performance of the power devices under overdriving at elevated junction temperatures. Lastly, a discussion part and the conclusions are found in Sections VI and VII.

II. OVERVIEW OF HIGH-POWER SEMICONDUCTOR DEVICES RATED IN THE VOLTAGE RANGE 1200-1700V

Power semiconductor devices are categorized into uncontrolled (i.e. diodes), semi-controlled such as thyristors and fully controlled devices (e.g., IGBTs and MOSFETs). However, only devices from the last category can be utilized in a typical interrupting solid-state DC breaker [5]. The presented investigations have been performed on fully controlled Silicon and SiC devices in the voltage class of $1200 - 1700V$, which are suitable for low- to medium-voltage DC solid-state CBs. These devices are classified to bipolar (e.g., IGBTs) or unipolar devices (e.g., MOSFETs and JFETs) based on the type of charge carriers causing current flow. For each device type, the design structures of both main body and gate area of the devices lead to different design generations and therefore, several devices are emerged. An overview of the various high-power semiconductor devices that are suitable for interrupting solid-state breakers with a rated voltage in the range of $1200 - 1700V$ can be seen in Fig. 2.

These power semiconductor devices have been designed for operation in switch-mode power converters. This means that a design trade-off between switching speed and ON-state power losses exists. On the other hand, in solid-state CBs, high-power semiconductor devices should be optimized for achieving low ON-state losses, while the switching performance would not be of high importance. Therefore, the solution is either to design devices with minimized ON-state losses at a cost of lower switching speeds or to utilize the existing technology at its operating limits in terms of ON-state losses.

A. INSULATED GATE BIPOLAR TRANSISTORS

IGBTs have gained momentum over other high-power semiconductor devices utilized in high-power converters due to their voltage-controlled gate and ruggedness at high blocking voltages [18]. Punch-Through (PT) IGBTs are fabricated by

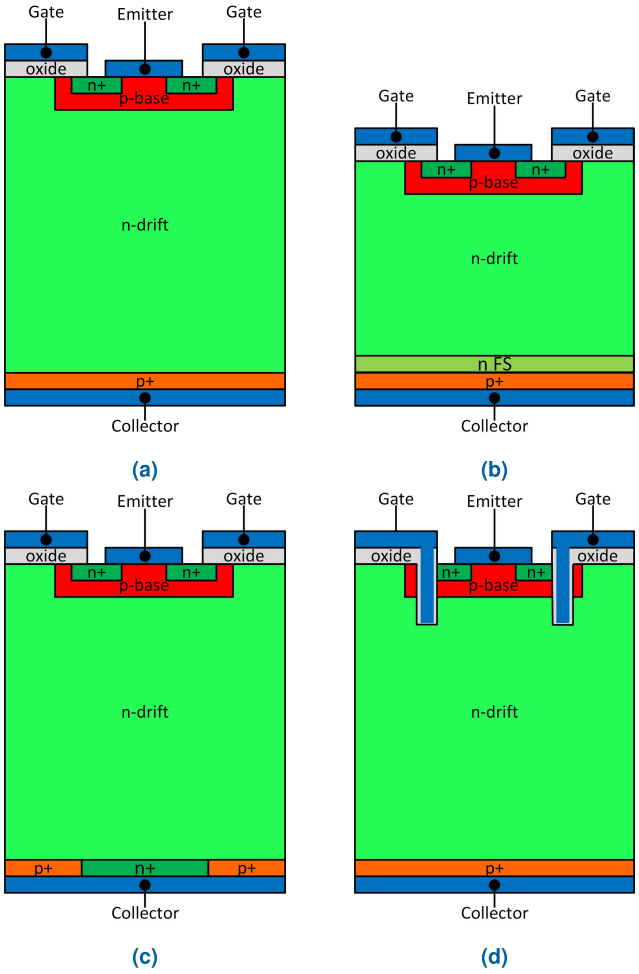

FIGURE 3. Typical IGBT structures: (a) NPT IGBT, (b) FS/XPT/SPT/LPT IGBT, (c) BiMOSFET and (d) NPT IGBT with trench-gate.

creating an n-epitaxial drift layer and a thin high-doped n+ buffer layer on top of a thick high-doped p+ substrate. They are designed for low blocking voltages, and hence, they will not be investigated further in this paper. Non-Punch-Through (NPT) IGBTs (Fig. 3) have a thinner p+ substrate, a thicker n-epitaxial drift layer and they lack the n+ buffer layer compared to PT designs. NPT IGBTs exhibit higher blocking voltages due to the thick drift layer, achieving lower switching losses, as well as higher switching robustness [18]. However, the thick drift layer causes high ON-state losses and thus IGBT designs such as the soft-punch-through (SPT), light-punch-through (LPT), field-stop (FS) or extreme light-punch-through (XPT) have been developed. All these IGBT names imply the same fabrication technology, which differs from the previous PT and NPT structures as follows. A thin n- buffer layer has been added beneath a thinner n-epitaxial drift layer compared to NPT structure, while the p-substrate remains similar to the NPT technology. Fig. 3b illustrates a typical structure of a FS/XPT/SPT/LPT IGBT [18]. In this way, the electric field in the drift region is distributed in a trapezoidal way, and thus the forward voltage drop decreases. Last but not least, a Bipolar Metal-Oxide Semiconductor Field Effect

Transistor (BiMOSFET) has been manufactured maintaining the typical structure of the NPT IGBT, but introducing an n+ collector-short pattern as shown in Fig. 3c [19]. BiMOSFETs are found with rated voltages of $1600 - 3600V$.

The fabrication of trench-gate IGBTs aims at lowering the forward voltage drop by having a different design of the gate layer compared to planar-gate IGBTs [20]. The presented IGBT structures, i.e. NPT, FS/XPT/SPT/LPT can be designed with either a planar or a trench gate technology. A typical structure of a NPT IGBT with trench gate can be seen in Fig. 3d. However, commercial NPT IGBTs with trench gate are only rated up to 1200V. Additionally, even if SiC-based IGBTs have been fabricated, the manufacturing technology of such devices is currently not mature enough and hence, they are not commercially available [21]. Besides, other design challenges of SiC IGBTs are the presently highly resistive p-substrate required for fabricating SiC n-IGBTs, the low channel mobility of SiC p-IGBTs, the poor characteristics of the SiC/SiO_2 interface and finally, the lack of high-voltage packaging technology suitable to encapsulate SiC IGBTs rated at $12 - 15kV$ and beyond. These devices will not be further investigated in this study due to the lack of a commercial SiC IGBT device.

B. SILICON CARBIDE METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS

SiC MOSFETs are the most suitable unipolar SiC active device to replace Silicon IGBTs in power converters [17]. This is mainly due to the voltage-controlled gate, which -in many design cases- eases the direct replacement of Silicon IGBTs with SiC MOSFETs. The structure of SiC MOSFETs is similar to the PT IGBT's structure, with the main difference of not having the p+ substrate. Similar to IGBTs technology, SiC MOSFETs can be fabricated having either a planar- or a trench-gate structure (Fig. 4) for the investigated blocking voltage range of $1200 - 1700V$ [22]. Trench SiC MOSFETs are fabricated with a view of minimizing the ON-state resistance, as well as to reduce the switching energy compared to the planar SiC MOSFET designs. By introducing small structure changes, different semiconductor companies develop different generations for either planar or trench SiC MOSFETs.

C. SILICON CARBIDE JUNCTION FIELD EFFECT TRANSISTORS

The last potential switch candidate for solid-state CBs is the SiC JFET [23]. SiC JFETs can either be designed as enhancement mode (i.e., normally-OFF) or depletion mode (i.e., normally-ON) devices [24]. Currently available SiC JFETs exhibit blocking voltages in the range of $1200 - 1700V$. Additionally, the absence of gate oxide layer in SiC JFETs makes this technology more reliable for long-term and high-temperature operation compared to SiC MOSFET technology [24]. A typical JFET structure can be observed in Fig. 5. The enhancement mode JFETs are normally-OFF devices and require a significant amount of

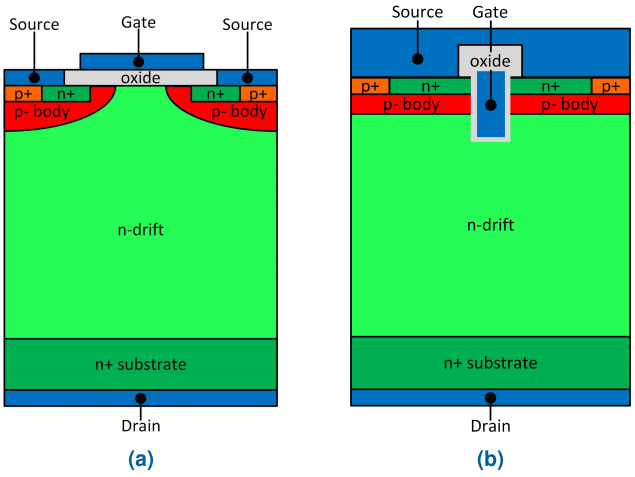

FIGURE 4. Typical SiC MOSFET structures with: (a) a planar-gate and (b) a trench-gate.

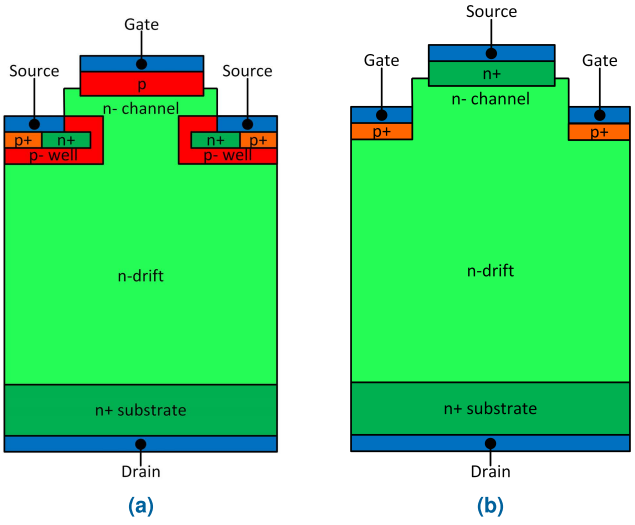

FIGURE 5. Typical SiC JFET structures: (a) Depletion mode (normally-ON) and (b) enhancement mode (normally-OFF).

gate current when they conduct, which eventually causes excessive gate driver losses [16]. Thus, normally-OFF SiC JFETs will not be further examined in this paper. On the other hand, the depletion mode JFETs are normally-ON devices and thus, they do not require gate supply in order to remain in the ON-state. These devices can be found even at higher voltages, i.e. $1700V$. Normally-ON SiC JFET has been considered as a suitable device for solid-state DC CBs designs due to its normally-ON characteristics, since the active switches in solid-state CBs, operate in the current conduction mode for most of their operational lifetime.

III. COMPARATIVE EVALUATION AT NOMINAL GATE VOLTAGE

The first set of measurements of the ON-state conduction characteristics has been performed by operating nine different power semiconductor devices rated at $1200V$ at their nominal gate voltages. The characteristics and the prices of these

TABLE 1. Characteristics and prices of the investigated 1200V-class power semiconductor devices.

Semiconductor device	Structure technology	Gate structure	Current rating at $T_c = 25^oC$	Symbol	Manufacturer	Model	Packaging technology	Price [$/A] (www.mouser.com)
Si IGBT	NPT	Planar	60A	D_1	Littelfuse, IXYS	IXDH30N120D1	TO-247 AD	0.175
Si IGBT	NPT	Trench	50A	D_2	ONsemi/Fairchild	FGA25N120ANTD	TO-3P	0.077
Si IGBT	XPT	Planar	84A	D_3	Littelfuse, IXYS	IXA55I1200HJ	ISOPLUS 247	0.184
Si IGBT	FS	Trench	50A	D_{4a}	Infineon	IHW25N120E1	TO-247	0.072
Si IGBT	FS	Trench	50A	D_{4b}	ROHM Semiconductor	RGS50TSX2DHR	TO-247N	0.183
SiC MOSFET	-	Planar	63A	D_{5a}	Wolfspeed, Cree	C3M0032120K	TO-247	0.351
SiC MOSFET	-	Planar	65A	D_{5b}	STMicroelectronics	SCT50N120	HiP-247	0.514
SiC MOSFET	-	Trench	55A	D_6	ROHM Semiconductor	SCT3040KLHR	TO-247	0.901
SiC JFET	Normally-ON	-	63A	D_7	UnitedSiC	UJ3N120035K3S	TO-247	0.393

TABLE 2. Characteristics and prices of the investigated 1700V-class power semiconductor devices.

Semiconductor device	Structure technology	Gate structure	Current rating at $T_c = 25^oC$	Symbol	Manufacturer	Model	Packaging technology	Price [$/A] (www.mouser.com)
Si IGBT	NPT	Planar	50A	D_8	Littelfuse, IXYS	IXGH24N170	TO-247	0.378
Si IGBT	XPT	Planar	58A	D_9	Littelfuse, IXYS	IXYH24N170CV1	TO-247 AD	0.263
Si IGBT	BiMOSFET	Planar	60A	D_{10}	Littelfuse, IXYS	IXBH24N170	TO-247	0.413
SiC MOSFET	-	Planar	40A	D_{11}	Wolfspeed, Cree	C2M0080170P	TO-247 Plus	0.891
SiC MOSFET	-	Trench	3.7A	D_{12}	ROHM Semiconductor	SCT2H12NZ	TO-3PFM	1.622
SiC JFET	Normally-ON	-	273A	D_{13}	UnitedSiC	UF3N170006X3S	TO-264	0.238*

* purchased from UnitedSiC

devices are summarized in Table 1. The prices (USD per Ampere, $/A) have been taken from the distributor website, www.mouser.com, for a purchase of single devices. In addition, six devices rated at 1700V have also been evaluated in terms of ON-state conduction performance. The characteristics along with the prices of these devices are shown in Table 2.

For measuring the current-voltage (IV) characteristics of these power devices at room temperature, the B1505A Power Device Analyzer/Curve Tracer from Keysight Technologies has been used. In order to achieve a fair assessment and comparison among the various devices, the current axes in the IV characteristics have been normalized with respect to the rated current of each individual device. A total number of five samples from each device has been examined for all the case studies. The following plots present the average values from the five samples.

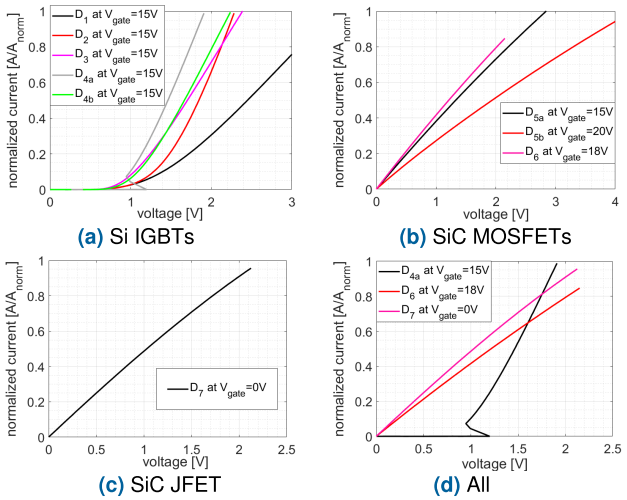

FIGURE 6. IV characteristics at nominal gate voltages for all the investigated 1200V high-power semiconductor devices at room temperature.

A. HIGH-POWER SEMICONDUCTOR DEVICES RATED AT 1200V

As seen from Table 1, five Silicon IGBTs, three SiC MOSFETs and one normally-ON SiC JFETs are considered, where their current ratings are also depicted. The reason that two FS Silicon IGBTs with trench-gate are included in the investigations, is the different manufacturers. Similar to this, two SiC MOSFETs with planar-gate from different manufacturers are also examined.

The IV characteristics at room temperature (25^oC) of all investigated high-power semiconductor devices rated at 1200V are shown in Fig. 6. The gate voltages have been set to the nominal values based on the datasheet of each device. In particular, the gate voltage was set at 15V for all IGBTs ($D_{1,2,3,4a,4b}$) and one SiC MOSFET (D_{5a}), at 20V and 18V for the other two SiC MOSFETs (D_{5b} and D_6 respectively), and at 0V for the normally-ON SiC JFET (D_7).

From Fig. 6a, it is observed that the FS Silicon IGBTs, D_{4a}, exhibits the lowest voltage drop for almost the entire normalized current range compared to the other IGBT technologies under investigation. Additionally, Fig. 6d shows the IV characteristics of the three best semiconductor technologies in terms of the lowest voltage drop. It can be concluded that the normally-ON SiC JFET achieves the lowest conduction losses among all the investigated devices for a normalized

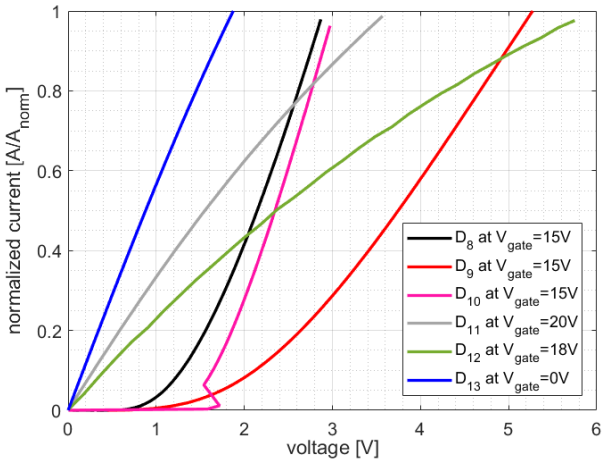

FIGURE 7. IV characteristics of high-power semiconductor devices rated at 1700V at room temperature (25^oC) under nominal gate voltages.

current range of up to 80%. Beyond that point, the FS Silicon IGBT seems to achieve the best performance compared to the other counterparts in terms of minimizing the voltage drop. The reason for this is the conductivity modulation, which becomes the dominant forward conduction mechanism at high current densities in IGBTs.

B. HIGH-POWER SEMICONDUCTOR DEVICES RATED AT 1700V

The group of investigated high-power semiconductor devices rated at 1700V (Table 2) contains three Silicon IGBTs, two SiC MOSFETs and one normally-ON SiC JFET. The absence of Silicon IGBT with trench-cell rated at 1700V is due to the fact that this device is not commercial yet.

The normalized IV characteristics of all investigated high-power semiconductor devices rated at 1700V by applying the nominal gate voltages at room temperature (25^oC) are depicted in Fig. 7. Similar to the previous case at 1200V, the gate voltages were set according to devices' datasheets and they are as follows: 15V for all IGBTs ($D_{8,9,10}$), 20V and 18V for the two SiC MOSFETs (D_{11} and D_{12} respectively), and zero gate voltage for the normally-ON SiC JFET (D_{13}).

It can be seen that the normally-ON SiC JFET (blue line in Fig. 7) exhibits the lowest voltage drop in the entire investigated current range. Besides that, the SiC MOSFETs seem to achieve better conductive performance compared to Silicon IGBTs under a certain normalized current. Similar to the previous case at 1200V, the NPT and BiMOSFET designs of Silicon IGBTs minimize the voltage drop at current levels close to their nominal values, being more efficient than SiC MOSFETs.

IV. COMPARATIVE EVALUATION AT MAXIMUM GATE VOLTAGE

When overdrive operation is used, the forward voltage drop decreases due to the higher carrier injection into the channel. This is valid for all investigated power device technologies. However, the gate voltage cannot be significantly higher than the nominal value of the gate voltage, which is usually specified by the manufacturer. The maximum gate voltage is limited by the thickness and characteristics of the gate-oxide layer in IGBTs and MOSFETs and by the gate current in JFETs. The maximum gate voltage is defined as the voltage that can be applied continuously to the gate of each device ensuring long-term reliability. This gate voltage limit is usually given in the datasheet of each high-power semiconductor device. If the gate voltage exceeds the maximum limit in IGBTs and MOSFETs, it is likely that the gate oxide will degrade due to the tunneling effect loosing its dielectric properties. In JFETs, a positive gate voltage higher than the maximum value will cause an excessive continuous gate current flowing through the gate-source pn junction, causing additional gate driver losses.

This Section presents the results of the anticipated ON-state voltage drop of the power semiconductor devices under investigation, when the maximum gate voltage is applied (i.e., overdrive operation). Overdrive operation can be useful for minimizing the conduction power losses of power semiconductors employed in solid-state CBs. The absence of continuous switching operation in CBs can lead to reduced overvoltages in the gate voltages due to the lack of high-speed switching. Therefore, the device can be driven at higher gate voltages compared to switching mode applications, as it happens in power converters.

A. HIGH-POWER SEMICONDUCTOR DEVICES RATED AT 1200V

The same devices shown in Table 1 have also been considered in this section. For the Silicon IGBTs, the maximum gate voltage was set to 20V (for $D_{1,2,3,4a,4b}$), while for the SiC MOSFETs the gate voltage was equal to 18V (D_{5a}) and 22V (D_{5b} and D_6), and lastly, a gate voltage of 2V was applied to the normally-ON SiC JFET (D_7). The maximum gate voltages have been set according to the maximum values of the gate voltages defined in the devices' datasheets.

The impact of driving the devices with the maximum gate voltage on the ON-state voltage drop at room temperature (25^oC) can be seen in Fig. 8. In case of SiC MOSFET with planar gate structure, D_{5b}, the ON-state voltage decreases significantly at elevated currents when applying the maximum gate voltage. Similarly, the normally-ON SiC JFET exhibits better performance when a higher gate voltage is applied compared to the zero gate voltage. On the other hand, the Silicon IGBTs seem to improve their performance under maximum gate voltages but not significantly. In particular, at 80% of normalized current, the reduction of the ON-state voltage by applying overdriving for every investigated device is as follows: 8.7% in D_1, 3.3% in D_2, 5.7% in D_3, 4.6% in D_{4a}, 6.5% in D_{4b}, 10% in D_{5a}, 14.5% in D_{5b}, 15% in D_6 and 17% in D_7.

The results for all the investigated high-power semiconductor devices when the maximum gate voltage is applied can be seen in Fig. 9. Unlike to the case with nominal gate voltages shown in Fig. 6d, it can be seen in Fig. 9d that the SiC JFET

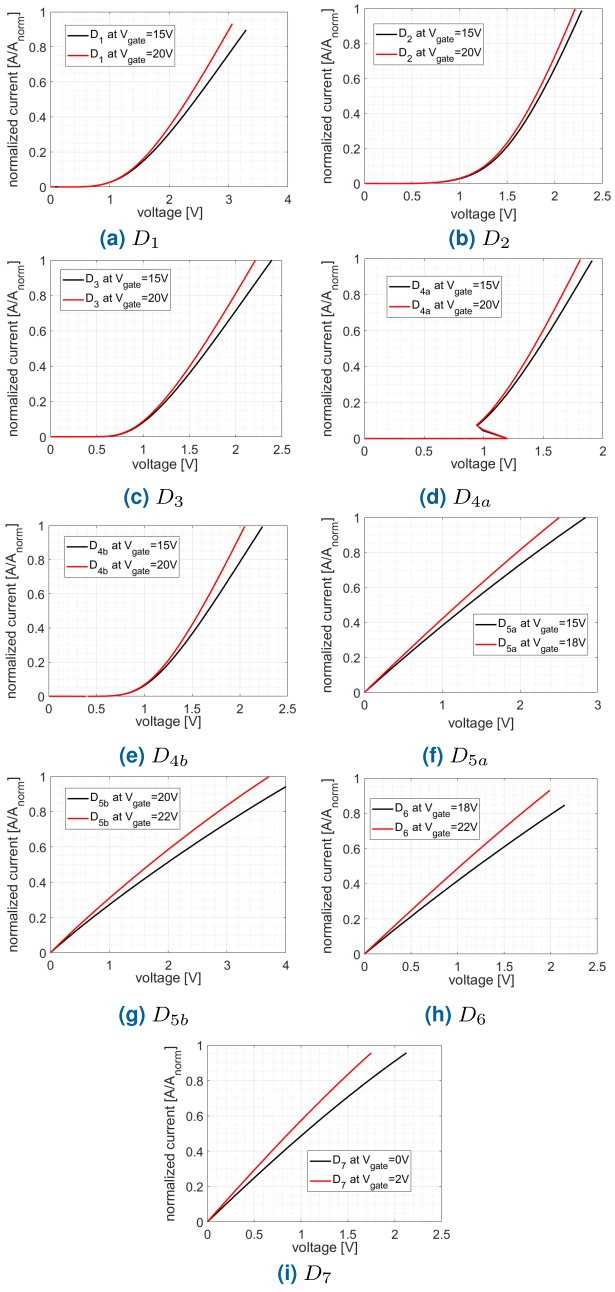

FIGURE 8. IV characteristic at nominal and maximum gate voltages for all investigated 1200V-class high-power semiconductor devices.

(D_7) minimizes the voltage drop for the entire normalized current range.

B. HIGH-POWER SEMICONDUCTOR DEVICES RATED AT 1700V

The ON-state voltage drop of the devices shown in Table 2 has been investigated by applying overdriving. The maximum gate voltages were set according to the datasheet of each semiconductor. In particular, the gate voltage has been set to 20V for all Silicon IGBTs, 22V for the two SiC MOSFETs, while for the normally-ON SiC JFET, the gate-source voltage was set to 2V.

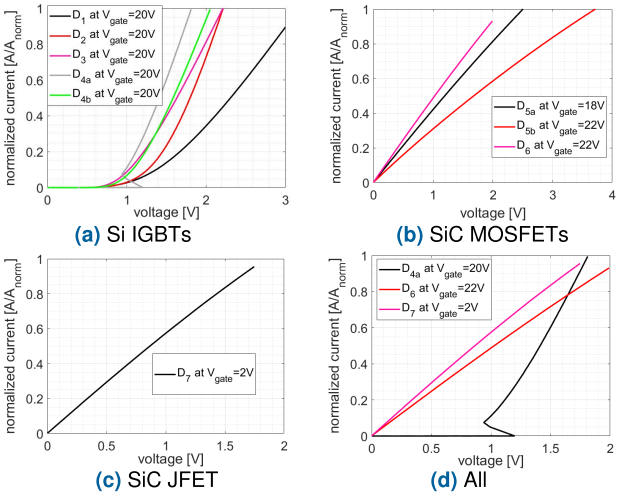

FIGURE 9. IV characteristic at maximum gate voltages for all investigated 1200V-class high-power semiconductor devices.

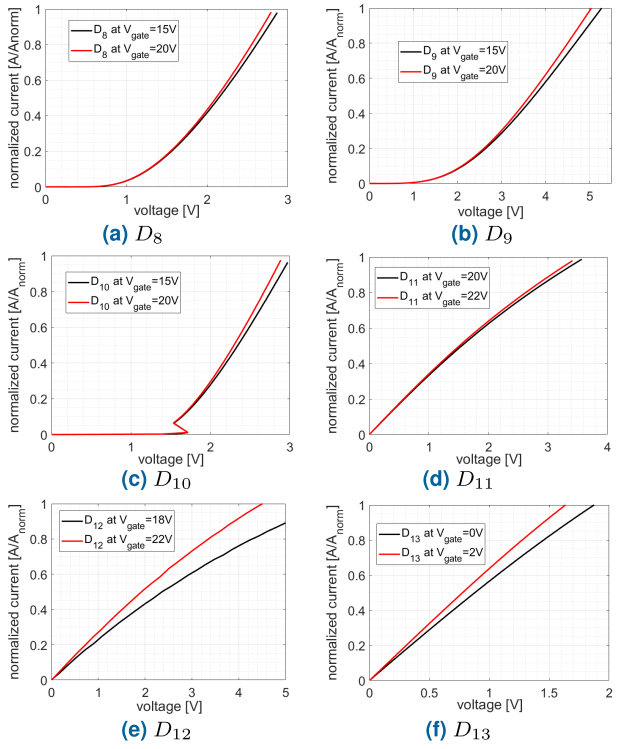

FIGURE 10. Characteristic IV at nominal and maximum gate voltages for all the investigated 1700V high-power semiconductor devices.

The voltage drop gain when utilizing overdrive at room temperature (25^oC) can be seen in Fig. 10. Similar to the 1200V-class switches, the gain is low for Silicon IGBTs, while in SiC MOSFET with trench-cell, the voltage is reduced significantly by applying the maximum gate voltage. In particular, at 80% of normalized current, the ON-state voltage drop reduction using overdriving operation for every investigated device is as follows: 2.3% in D_8, 4.2% in D_9, 2.9% in D_{10}, 3.7% in D_{11}, 20% in D_{12} and lastly, 11.7% in D_{13}. A comparative graph is depicted in Fig. 11, where the superiority of normally-ON SiC JFET remains clear in

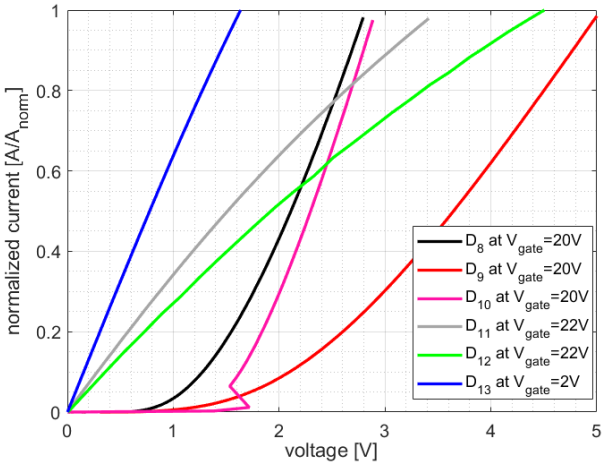

FIGURE 11. IV characteristic at maximum gate voltages for all investigated 1700*V*-class high-power semiconductor devices.

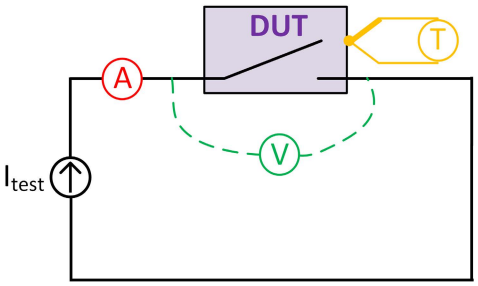

FIGURE 12. Schematic diagram of the test circuit for measuring the ON-state voltage drop across the DUT, and the DUT's case temperature for various I_{test}.

terms of ON-state voltage drop minimization compared to the other semiconductors technologies when the maximum gate voltage is applied.

V. OVERDRIVE OPERATION AT HIGH TEMPERATURES

This Section presents the impact of overdriving operation of the high-power semiconductor devices under investigation on the anticipated reduction of the conduction power losses at elevated junction temperature. For this purpose, a DC test circuit was constructed in the lab. The simplified schematic diagram of the test setup is shown in Fig. 12. The test circuit consists of a DC power source (ETSystem LAB/HP/E2020) that supplies the direct current (I_{test}), and a high-resolution voltmeter (Fluke 8842A) for measuring the ON-state voltage drop of the device under test (DUT). Lastly, a K-type thermocouple (Amprobe TMD-50) was also connected for measuring the case temperature of the DUTs. The DUTs have been mounted on a aluminium heatsink with a fan (Fischer Elektronik, LA 21/200 24V).

A. HIGH-POWER SEMICONDUCTOR DEVICES RATED AT 1200V

The conduction power loss percentage reduction for all DUTs rated at 1200*V* when applying the maximum gate voltages at various test currents, I_{test}, can be seen in Fig. 14. The losses are calculated based on the measured voltage drop

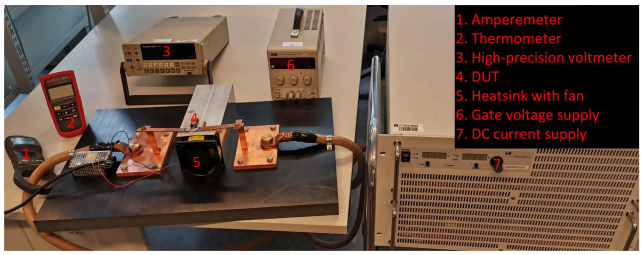

FIGURE 13. Photo of the experimental test setup.

across the DUT and the I_{test} for both cases, i.e., when applying nominal and maximum gate voltages. It is observed that the loss reduction becomes more significant at higher currents for almost all DUTs. It should also be mentioned that for all devices, the maximum test current has been set at different values in order potential thermal runaways to be avoided by keeping the same cooling system in all investigations. This implies that if higher test currents are required in a specific device, then a better cooling system would be required. However, as mentioned above, the use of a fixed cooling system for all the investigations has been chosen in order to provide the same thermal resistance for all tests. In case of IGBT-based devices ($D_{1,2,3,4a,4b}$), Fig. 14a indicates that the reduction of loss is proportional to the test current, while in case of SiC MOSFETs ($D_{5a,5b,6}$ in Fig. 14b), the loss reduction does not follow the same pattern. The reason for the latter is the high temperature dependence of the ON-state resistance of SiC MOSFETs. When the current through the MOSFET-based devices increases, the device temperature as well as the ON-state resistance rise leading to even higher conduction losses. In case of IGBT-based devices, the ON-state resistance contributes less to the conduction losses compared to MOSFET-based counterparts, and thus the previous phenomenon has less impact on the losses. Lastly, the normally-ON SiC JFET (D_7) achieves the highest conduction loss minimization by overdriving for the whole examined current range at elevated junction temperatures.

Table 3 shows the numerical results for the conduction losses, as well as the estimated junction temperatures (T_j) for the maximum DC test current in case of applying either nominal or maximum gate voltages. The junction temperature is calculated taking into account the losses, the junction-to-case thermal resistance of each device found in datasheet and the case temperature which is measured using the thermocouple.

The reduction of the ON-state losses is clear for all DUTs. In particular, the two FS trench IGBTs ($D_{4a,b}$) managed to carry a current of approximately 80% of their nominal value at room temperature (I_{nom}), achieving a loss reduction of around 10%. A similar reduction can also be observed for D_1, while the last two IGBTs devices ($D_{2,3}$) achieved lower reductions. Furthermore, the two planar-based SiC MOSFETs ($D_{5a,b}$) could not handle higher currents than 36% of their nominal values, achieving however, a significant loss reduction of around 10% when a maximum gate voltage was applied. Similar to IGBTs, in SiC MOSFETs with trench-cell

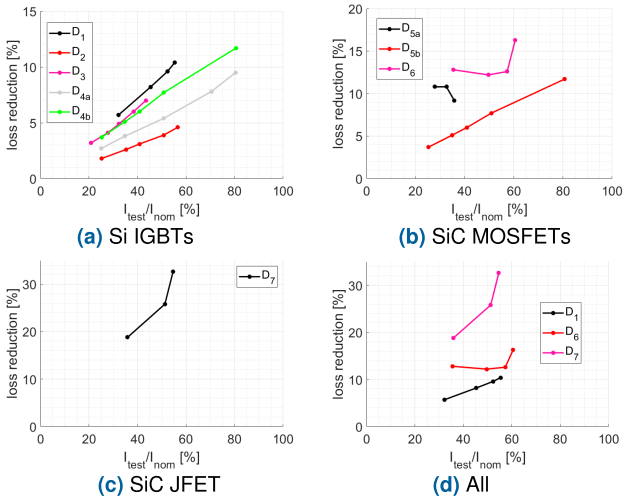

FIGURE 14. ON-state loss reduction when applying maximum gate voltages at elevated junction temperatures for all DUTs rated at 1200*V* and at various I_{test}.

(D_6), a higher test current has been used leading to a 16% reduction of the conduction losses. Lastly, the most significant impact of overdriving can be seen in normally-ON SiC JFETs (D_7). The drain-source voltage dropped by 33% when the gate voltage was set to $2V$ at 55% of nominal current.

In the same table, the junction temperatures of the DUTs are also shown. From this table, a significant reduction of T_j when a maximum gate voltage is applied can be seen for all devices. In particular, T_j decreases up to 10% for the IGBTs (e.g., D_{4b}), 12% for the SiC MOSFET (e.g., D_6) and lastly, a 22% junction temperature decrease can be observed in case of normally-ON SiC JFET. The anticipated reduction of T_j will soften the cooling requirements (i.e., lighter and smaller heatsinks).

B. HIGH-POWER SEMICONDUCTOR DEVICES RATED AT 1700V

The impact of overdriving the high-power semiconductor devices rated at $1700V$ at elevated junction temperatures on the ON-state loss reduction is shown in Fig. 15. One observation is that the percentage of the maximum DC test current over the nominal current has been generally kept lower compared to the devices rated at $1200V$. This happened due to the thicker chips required in these devices in order to withstand higher voltages. The latter means that the ON-state resistance becomes higher, leading to higher ON-state losses and eventually to increased junction temperatures for a given heatsink design. The trend in IGBT technology remains similar to the devices at the voltage class of $1200V$, i.e. the loss reduction increases proportional to the test current, while in SiC MOSFETs, this is less clear due to the high dependence of the ON-state resistance on the temperature increase. Lastly, the normally-ON SiC JFET experiences higher loss reduction at higher test currents similar to the corresponding device rated at $1200V$.

TABLE 3. Impact of the overdrive on the conduction loss and junction temperature of the DUTs rated at 1200*V* and at maximum DC test current.

Device test	V_{gate} $[V]$	I_{test} $[A]$	I_{test}/I_{nom} [%]	losses $[W]$	T_j $[^oC]$
D_1	15	33.2	55	103.1	136.5
	20	33.2	55	92.4	124.4
D_2	15	28.3	57	63.2	112.7
	20	28.3	57	60.3	108.5
D_3	15	36.5	44	69.5	119.8
	20	36.5	44	64.6	113.4
D_{4a}	15	40.2	80	90.5	113
	20	40.2	80	81.9	105.3
D_{4b}	15	40.3	80	119.5	120.1
	20	40.3	80	105.5	108.4
D_{5a}	15	22.5	36	32.7	85.4
	18	22.5	36	29.7	80.2
D_{5b}	20	23.2	36	47.6	100.9
	22	23.2	36	42	91.4
D_6	18	33.3	61	88.6	105
	22	33.3	61	74.2	92.4
D_7	0	34.4	55	76.2	88.8
	2	34.4	55	51.4	68.9

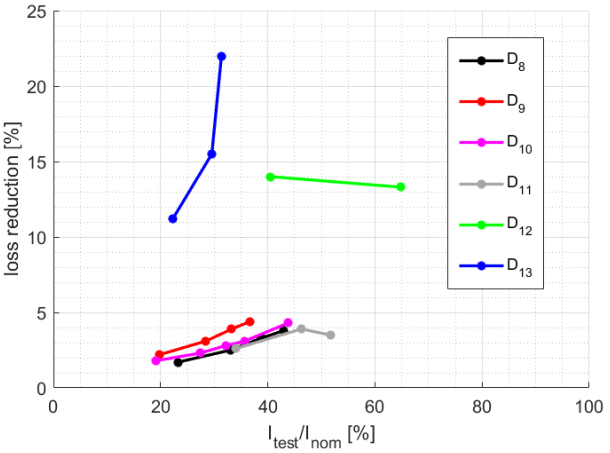

FIGURE 15. ON-state loss reduction when applying maximum gate voltages at elevated junction temperatures for all the investigated 1700*V* high-power semiconductor devices at various I_{test}.

Table 4 shows the numerical results for the conduction losses and junction temperatures when the gate voltage is set to nominal and maximum values for the maximum DC test current case. The reduction of the ON-state losses for all IGBTs is around 4%. The same percentage reduction is also obtained for the planar SiC MOSFET (D_{11}). On the other hand, the SiC MOSFET with trench-cell achieved a loss reduction of 13.3% when a maximum gate voltage was applied. Lastly, the conduction losses reduced by 22% when the gate-source voltage of the normally-ON SiC JFET was set to $2V$. Similar results can be seen for the reduction of the junction temperatures when applying maximum gate voltages. For both IGBTs and SiC MOSFETs, the junction temperature drops slightly, while in normally-ON SiC JFET case, T_j decreases more than 16%.

TABLE 4. Impact of the overdrive on the conduction loss and junction temperature of the investigated high-power semiconductor devices rated at 1700V at maximum DC test current.

Device test	V_{gate} $[V]$	I_{test} $[A]$	I_{test}/I_{nom} [%]	losses $[W]$	T_j $[^oC]$
D_8	15	21.5	43	56.6	128.3
	20	21.5	43	54.4	124
D_9	15	21.3	37	103	136
	20	21.3	37	98.6	131.6
D_{10}	15	26.3	44	77.7	137.8
	20	26.3	44	74.4	133.2
D_{11}	20	20.7	52	46.7	88.7
	22	20.7	52	45	86.4
D_{12}	18	2.4	65	10.5	80.5
	22	2.4	65	9.1	73.4
D_{13}	0	85.6	31	97.7	83.8
	2	85.6	31	76.2	70

VI. DISCUSSION

A. SAFE OPERATING AREA AND RELIABILITY OF SEMICONDUCTOR DEVICES UNDER OVERDRIVE OPERATION

The focus of this study is the conduction performance evaluation of various Silicon and SiC semiconductor devices employed in solid-state DC CBs. Besides, the overall performance evaluation of a breaker also needs to consider the limitations of the Safe Operating Area (SOA) of the semiconductor devices, especially in terms of the expected overvoltage during turn-off. This issues has been extensively investigated for both Silicon and SiC devices employed in switching-mode power converters. Similar performance is anticipated when the devices are utilized either in such converters or in breaker configurations. However, the impact of the overdrive operation on the SOA limitations needs to be discussed further.

The overdrive operation can keep the same SOA as under nominal drive operation by actively adjusting the gate voltage. In particular, once the line current reaches a value higher than the nominal current but lower than the threshold tripping current of the CB, the gate voltage decreases from the maximum value to the nominal gate voltage value. If the line current keeps rising and reaches the threshold value, then a normal turn-off process can be initiated. In this way, the limitations of the SOA of the overdriven semiconductor device, as well as its capability to turn-off, remain the same as in the case of a normal drive operation.

An additional significant aspect during the overdrive operation is the impact of the slightly higher gate voltage on the anticipated long-term stability and ageing of the gate oxide. In this study, the maximum allowable gate voltage for DC operation according to the devices' datasheet has been utilized for all devices under study in overdrive operation. This is definitely a crucial aspect of over-driving the power semiconductors and it is wise to investigate the long-term and also high-temperature performance of the gate oxide layers of the DUTs used in this paper. Device parameters behavior such as the threshold voltage shift, gate leakage current, as well as device on-state voltage and leakage current should be assessed in the future.

B. DISCUSSION OF RESULTS

One of the most crucial design and operating challenges of solid-state DC circuit breakers is the high conduction losses caused by the continuous current flow through the active power semiconductor devices. Based on the presented comparative performance in terms of conduction power losses, it is clear that each device technology outperforms the rest for a specific range of currents. In particular, in case of $1200V$-class devices, the normally-ON SiC JFET (D_7) achieved to minimize the ON-state losses in the current range 0-80% of nominal current when nominal gate voltages are applied compared to the other active devices at room temperature. Beyond that point and until 100% of nominal current, the FS Silicon IGBT with trench-cell (D_{4a}) managed to reduce the ON-state losses at the minimum compared to the rest of DUTs. The main reason is the presence of conductivity modulation in IGBTs, which becomes more dominant at elevated currents. Besides that, the normally-ON SiC JFET (D_{13}) has achieved the lowest conduction losses among the $1700V$-class devices for the entire current range (0-100%) when nominal gate voltages are applied to the gates and at room case temperature.

Additionally, the impact of overdriving the gates of the devices on the anticipated ON-state voltage drop and at room temperature has also been examined. The voltage drop is significantly reduced at currents close to the nominal values in case of SiC MOSFETs and SiC JFETs, while it is less affected in Silicon IGBTs. In particular, the ON-state voltage is decreased up to 20% for SiC MOSFET with trench-cell (D_{12}), and up to 17% for the normally-ON SiC JFET (D_7). The last observation reveals the the superior performance of SiC JFETs in the entire normalized current range (0-100%) in both voltage classes.

Furthermore, the reduction of the ON-state losses by utilizing overdriving in the DUTs at elevated junction temperatures has also been investigated. From the experimental alanysis, a significant reduction of conduction power losses is observed in several $1200V$-class semiconductor technologies. In particular, for the IGBT-based devices, the reduction can be as high as 12% at almost 80% of their nominal current (D_{4b}). On the other hand, in SiC MOSFET-based semiconductors, the improvement can be even higher than IGBTs, that is a loss reduction of up to 16% at 60% of the nominal current (D_6). Lastly, the most significant conduction loss reduction that has been observed is a 33% reduction at 55% nominal current in case of normally-ON SiC JFET (D_7). The loss reduction becomes generally lower when $1700V$-class devices are examined, but a similar trend with the $1200V$ counterparts is observed. The normally-ON SiC JFET (D_{13}) achieved the highest loss reduction, which is as high as 22% at approximately 30% of the nominal current.

Based on the findings presented in this paper, it is apparent that the observations made have flow-on effects on designing high-power solid-state CBs. The straight-forward way to design a low-loss solid-state breaker with higher-current capabilities is to choose the best performing semiconductor technology for the given current and increase the chip area of the active devices. However, in case of solid-state CBs operating with a wide range of load currents, a combination of different device technologies and materials would be more suitable solution for achieving the lowest possible ON-state power losses for the entire range of currents.

C. COST COMPARISON

From the cost aspect, the SiC MOSFETs with trench gate exhibit the highest cost per devices' rated Ampere in both investigated voltage classes. On the other hand, this cost drops significantly in case of Silicon IGBT-based devices. In particular, in the $1200V$-class, the trench gate Silicon IGBTs have the lowest cost among all investigated semiconductor technologies. Additionally, the cost of the normally-ON SiC JFET rated at $1200V$-class (D_7) is higher than the corresponding cost of Silicon IGBT-based devices, and it is in the same price range as the SiC MOSFETs with planar gate technology. However, with the market penetration of SiC power semiconductors technology, their price per rated Ampere will drop further. In addition to the device cost, one should also consider the drop in the total system cost when SiC devices are employed [25]. In the case of high-efficiency solid-state DC breakers, the required cooling requirements are softened. Thus, the cost related to installation and operation (e.g., liquid circulation) of the cooling system is also reduced.

D. FUTURE PERSPECTIVES OF SiC SEMICONDUCTOR DEVICES IN CBs

Due to advantageous material properties of SiC compared to Silicon, SiC dies can be designed having higher blocking voltages. This softens the design complexity of SiC-based medium and high-voltage DC solid-state breakers, because the required number of series-connected single devices to withstand a high DC blocking voltage decreases. Besides, the design complexity of auxiliary circuits, such as gate drivers and snubber circuits for equalizing transient voltages is softened.

On the other hand, there are still several design challenges of SiC devices when employed in solid-state DC breakers. Such issues are related to the high-temperature reliability of the SiC/SiO_2 interface at the oxide layer of SiC MOSFETs and IGBTs, the high cost of the manufacturing process and the increased thermal management requirements due to both the small SiC die sizes and the high-temperature operating capability of those devices [17]. In addition, the use of high-voltage SiC devices, i.e. beyond $6.5kV$, necessitates the development of novel packaging technologies capable to operate under both high-temperature and high-voltage conditions.

In this paper, the conducting performance of Silicon IGBTs, SiC MOSFETs and SiC JFETs rated at $1.2\ kV$ and $1.7\ kV$ has been assessed. However, the higher allowed blocking voltages of SiC devices enable the design of unipolar devices (e.g., SiC MOSFETs) with voltage ratings of $3.3\ kV$ [26], [27], $6.5\ kV$ [28] or even up to $10kV$ [29]. SiC MOSFETs rated at $3.3\ kV$ and $6.5\ kV$ have been researched extensively, and thus these devices could replace the existing Silicon IGBTs in a wide range of power electronic applications, including solid-state DC breakers enabling lower losses. However, the forward voltage drop of SiC MOSFETs becomes unacceptable for voltage levels higher than $10kV$ [17]. Beyond this voltage level, the synthesis of the advantageous SiC characteristics with bipolar device structures, such as SiC IGBTs, becomes more beneficial. Research efforts to design and fabricate high-voltage SiC IGBTs have been made [30], [31]. The main research focus of those devices concern high-voltage designs of $12 - 15kV$ and beyond (e.g., $20kV$). This means that the design of the future medium and high-voltage DC solid-state breakers will be eased by the development of such high-voltage SiC IGBTs due to the lower design complexity as mentioned previously. However, several design challenges need to be tackled such as the immature fabrication technology of SiC IGBTs and the reliability issues of the SiC/SiO_2 interface, before the establishment of SiC IGBTs as potential device candidates for various high-voltage and high-power applications, such as solid-state breakers.

VII. CONCLUSION

This paper presented a comparative evaluation of the conductive electrical and thermal performance of various active power device technologies for solid-state CBs. The ON-state voltage drop and associated conduction power losses were assessed under normal and overdriving operation for $1200V$ and $1700V$-class semiconductor devices at two different temperature conditions. Both Silicon and SiC, as well as, bipolar and unipolar devices have been considered. It has been shown that by utilizing overdriving, the most significant reduction of power losses occurs for SiC JFET. In particular, the overdrive of a $1200V$ normally-ON SiC JFET caused a 33% reduction of the conduction losses at elevated junction temperatures. Similarly, the ON-state losses reduced by 22% in case of a $1700V$ normally-ON SiC JFET at high junction temperature when a maximum gate voltage was applied.

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