IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 26 July 2022, accepted 22 August 2022, date of publication 31 August 2022, date of current version 13 September 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3203190

RESEARCH ARTICLE

A W-Band Amplifier With a New Wide-Band Interstage Matching Technique Using Self-Resonance of a Microstrip-Coupled Line

SUNWOO LEE[1], WANSIK KIM[2], SOSU KIM[3], MIN-SU KIM[4], AND JUNGHYUN KIM[1], (Member, IEEE)

[1]Department of Electrical and Electronic Engineering, Hanyang University, Ansan 15588, Republic of Korea
[2]LIGNex1, Yongin 16911, Republic of Korea
[3]Agency for Defense Development, Daejeon 16911, Republic of Korea
[4]Department of Information and Electronic Engineering, Mokpo National University, Muan 58554, Republic of Korea

Corresponding author: Min-Su Kim (msmy970@mnu.ac.kr) and Junghyun Kim (Junhkim@hanyang.ac.kr)

This work was supported by the Agency for Defense Development under Contract UC170028FD.

ABSTRACT A new interstage matching technique is presented for design of a wide-band multi-stage amplifier using commercial 60 nm GaN-on-silicon technology in the W-band. The proposed interstage matching network is designed as a two-pole conjugated impedance matching approach for wideband characteristics using low-characteristic impedance transmission lines and an optimized microstrip-coupled line. In particular, the microstrip-coupled line provides strong resonance at the desired frequency, enabling optimal conjugate impedance matching of both edge and intermediate frequencies simultaneously. The implemented W-band three-stage amplifier using the proposed interstage matching technique exhibited a small-signal gain above 14.1 dB from 75 to 103 GHz. Also, the output power between 92-100 GHz was greater than 25 dBm, and the maximum output power at 96 GHz was 25.8 dBm. The W-band amplifier was designed with an area of 2 mm × 1.2 mm.

INDEX TERMS Amplifier, W-band, GaN-on-silicon, interstage matching technique, low-characteristic impedance transmission line, microstrip-coupled line.

I. INTRODUCTION

The W-band of 75-110 GHz has a small propagation loss compared to other millimeter-wave frequency bands due to low absorption in atmospheric environments such as water vapor and oxygen [1]. Therefore, it is widely applied to satellite communication, automotive sensors, frequency modulated continuous wave (FMCW) radar, and point-to-multipoint or multi-gigabit-per-second data rates wireless communication networks that require high data rates and fast communication systems [2], [3], [4]. However, path loss due to high-frequency characteristics is an issue. For this reason, multi-stage amplifiers of various structures for high gain and output power have been designed and reported using various processes, such as CMOS, GaAs pHEMT, GaN HEMT, InP HBT, and SiGe HBT [5], [6], [7], [8], [9], [10], [11].

Recently, the gallium nitride (GaN) High Electron Mobility Transistor (HEMT) process has been widely used in high-output power amplifiers due to its wide bandgap voltage characteristics and is being applied to various applications for millimeter-wave frequencies. Silicon carbide-based GaN HEMTs show excellent performance not only in high power amplifiers but also in amplifiers for high robustness and low noise, but it is still difficult to utilize them in many applications due to high process costs and low integration [12], [13], [14], [15]. On the other hand, silicon-based GaN HEMTs are being applied to various mm-waves because they can be integrated with other circuits using a Si-based process and have relatively low process costs [16], [17].

Since the wideband characteristics of amplifiers are advantageous for integrating various circuits using Si-based

The associate editor coordinating the review of this manuscript and approving it for publication was Vittorio Camarchia.

processes, many wideband technologies are being studied to improve the bandwidth of amplifiers such as balanced amplifiers [5], [6], [7] and distributed amplifiers [8], [9], [10], [11]. The balanced amplifier uses a wideband coupler or transformer to match the input and output impedances, making it possible to design an amplifier with excellent frequency characteristics. However, the transformer or coupler must have a high Q because it has a large signal loss itself, and it is difficult to implement them in a process such as that of an III-V compound with a limited number of metal layers.

A well-known distributed amplifier is reported to have excellent wide-band characteristics, but multi-stage transistors are required for high gain and output power, which increases the complexity of the configuration with large DC power consumption and chip size. Since all of these wide-band structures of amplifiers require multiple-stages in the W-band due to the limited gain of a transistor, an interstage matching circuit is a very important factor in designing a wide-band amplifier.

This paper presents a new wide-band interstage matching technique using self-resonance of a microstrip-coupled line (MCL) for optimal design of a W-band multi-stage amplifier using a GaN HEMT on Si process. In section II, the interstage matching method using transmission lines with a low-characteristic impedance, which is generally used in the W-band, is presented, and the proposed interstage matching using self-resonance of the microstrip-coupled line is analyzed and compared. The fabricated W-band three-stage amplifier is reported in section III along with measurement results, while the conclusions are given in Section IV.

II. DESIGN OF THE W-BAND MULTISTAGE AMPLIFIER

A. CONSIDERATION OF THE W-BAND AMPLIFIER DESIGN

In this work, a W-band amplifier MMIC was designed using the commercially available 60 nm GaN HEMT on Si process. This process has a typical cutoff frequency (f_t) of 150 GHz, a maximum oscillation frequency (f_{max}) of 190 GHz, and a gate-drain breakdown voltage of 25 V [18]. Figure 1 presents the simulated maximum available gain/maximum stable gain (MAG/MSG) as a function of frequency for the 4 × 25 μm HEMT with drain voltages (V_{DS}) of 10 V and gate voltages (V_{GS}) of −1 V. Due to limited gain around 5-7 dB available from a single transistor at the W-band, the W-band amplifier typically consists of multiple stages to obtain the sufficient gain required by the system.

Figure 2(a) shows a block diagram of the W-band multi-stage amplifier. The W-band multi-stage amplifier consists of an input matching network (IMN), an output matching network (OMN), and interstage matching networks (ISMN). Since numerous ISMNs influence the overall gain and bandwidth characteristics of the multi-stage amplifier, efficient design of interstage matching is important. Figure 2(b) shows the output impedance of the previous transistor (Z_{ISMN_out}) and the conjugated input impedance of the next stage transistor ($Z^*_{ISMN\_in}$) of a 4×25 μm HEMT in an ISMN from 70 GHz

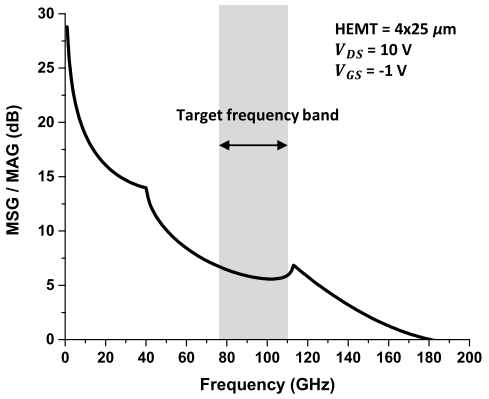


FIGURE 1. Simulated MAG/MSG as a function of the frequency for a 4 × 25 μm HEMT biased at V_{DS} = 10 V and V_{GS} = −1 V.

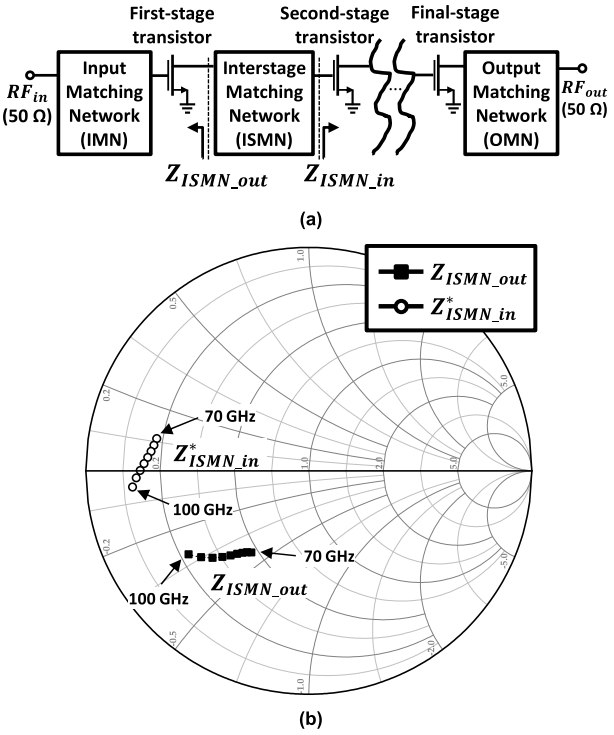


FIGURE 2. (a) Block diagram of the W-band multi-stage amplifier and (b) the simulated output impedance (Z_{ISMN_out}) and conjugated input impedance ($Z^*_{ISMN\_in}$) of the 4 × 25 μm HEMT for an interstage matching network from 70 GHz to 100 GHz on a 50 Ω normalized Smith chart.

to 100 GHz on a 50 Ω normalized Smith chart. In general, the ISMNs are designed for achieving conjugate matching ($Z_{ISMN\_out} = Z^*_{ISMN\_in}$). However, it is difficult to realize optimum and wide-band interstage matching due to the change in $Z^*_{ISMN\_in}$ of reactance in the W-band from capacitive to inductive.

Conceptually, if the ISMN provides complete conjugate matching at two frequency points (f_L, f_H), it forms a two-pole characteristic. Figure 3(a) shows the schematic of the ISMN for the two-pole interstage matching. Z_{ISMN_out} can be simply modeled as a resistor (R_{ds}) in parallel with a capacitor (C_{ds}), while Z_{ISMN_in} is modeled as a resistor (R_{gs}) in series with a capacitor (C_{gs}). This typical ISMN consists of microstrip lines (TL_1, TL_2) and an MIM capacitor for DC blocking.

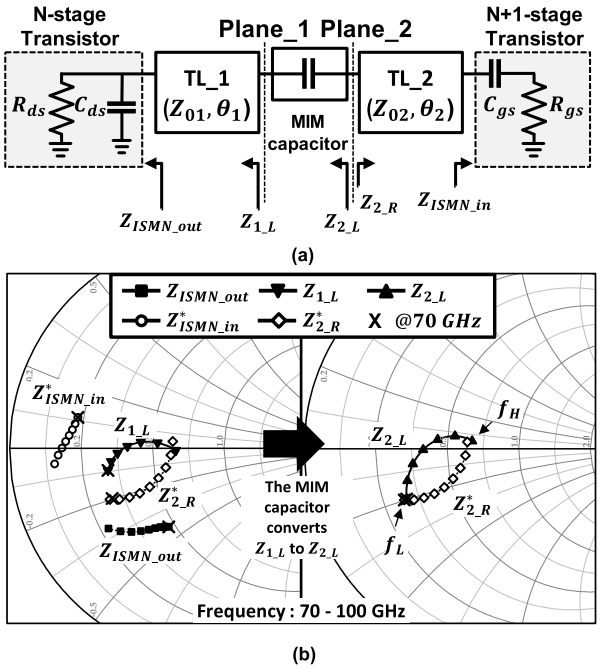


FIGURE 3. The two-pole ISMN using the MIM capacitor: (a) schematic and (b) impedance transformation trajectories from 70 GHz to 100 GHz on a 50 Ω normalized Smith chart.

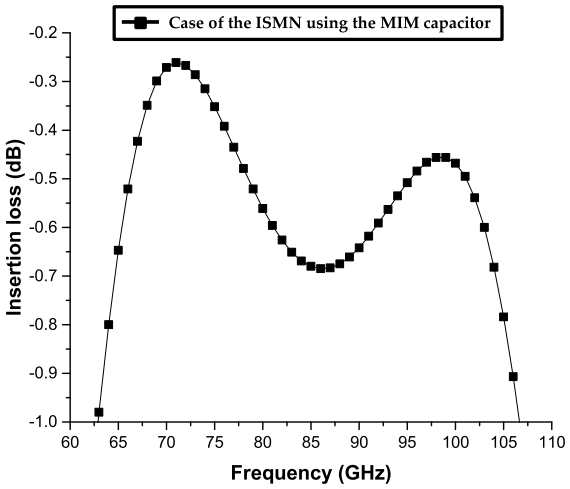


FIGURE 4. Simulated insertion loss of the two-pole ISMN using the MIM capacitor frequency response.

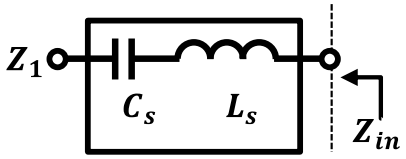


FIGURE 5. Simple equivalent circuit for the DC-block component with self-resonance.

Here, the microstrip lines can be used as complex impedance transformers despite their simple structure [19].

In Fig. 3(a), the characteristic impedance of the TL_1 is Z_{01}, whereas that of TL_2 is Z_{02}. The electrical lengths of TL_1 and TL_2 are θ_1 and θ_2, respectively. The θ_1, θ_2, Z_{01}, and Z_{02} are main design parameters. Figure 3(b) presents the impedance transformation trajectories of the ISMN using microstrip lines and the MIM capacitor from 70 GHz to 100 GHz. The impedances at Plane_1 and Plane_2 toward the left are Z_{1_L} and Z_{2_L} respectively, while the impedance at Plane_2 toward the right is Z_{2_R}. The TL_1 and TL_2 are designed to have a low characteristic impedance due to Z_{ISMN_out} and Z_{ISMN_in} being in the low-impedance area in the Smith chart, as shown in Fig. 2(b). Typical interstage matching is realized using microstrip lines and an MIM capacitor. TL_1 converts $ZISMN\_out$ to Z_{1_L}, whereas TL_2 converts $Z^*_{ISMN\_in}$ to $Z^*_{2\_R}$, TL_1 and TL_2 are connected by the MIM capacitor that separates the drain bias of the N-stage and the gate bias of the N+1-stage. The MIM capacitor with a self-resonance of 85 GHz is designed to have a size of 18 μm×18 μm and converts Z_{1_L} to Z_{2_L}. The conjugate matching ($Z_{2\_L} = Z^*_{2\_R}$) at Plane_2 is achieved at f_L and f_H by the microstrip lines and the MIM capacitor.

The simulated insertion loss for the ISMN using microstrip lines and the MIM capacitor is shown in Figure 4. Although the ISMN using the MIM capacitor provided perfect conjugate matching at f_L and f_H, a deeper notch in the insertion loss due to impedance mismatch can be observed at the mid-band frequency between f_L and f_H. For a wide-band matching characteristic, the mismatch in the mid-band frequency between two matched frequencies cannot be excessive.

B. DESIGN OF A PROPOSED INTERSTAGE MATCHING NETWORK USING SELF-RESONANCE OF A MICROSTRIP-COUPLED LINE

To achieve a wide-band frequency response of interstage matching with a reduced loss notch in the mid-band frequency between the two matched frequencies, an ISMN using self-resonance of a microstrip-coupled line was proposed in this paper. In general, a DC-blocking component with self-resonance, such as an MIM capacitor and MCL, can be modeled as a series L-C resonant circuit as shown in Fi. 5. The simple equivalent circuit of the DC-blocking component with self-resonance is composed of an equivalent series capacitance (C_s) and an equivalent series inductance (L_s). The input impedance (Z_{in}) of the equivalent circuit terminated at an arbitrary impedance (Z_1) and the self-resonance frequency (SRF) can be written as follows.

$$Z_{in}(j\omega) = Z_1(j\omega) + L_s \frac{\left(j\omega + \frac{1}{\sqrt{L_s C_s}}\right)\left(j\omega - \frac{1}{\sqrt{L_s C_s}}\right)}{j\omega} \quad (1)$$

$$f_{SRF} = \frac{1}{2\pi\sqrt{L_s C_s}} \quad (2)$$

As seen in equation (1), if the DC-blocking component with SRF has sufficient L_s, the pole can be added by self-resonance. Also, equation (2) shows that the SRF is determined by the values of C_s and L_s. The MIM capacitor increases the size for a large value of L_s to add resonance, which also increases C_s, making it difficult to form the desired SRF. On the other hand, an MCL forms a small value of C_s and a sufficiently large value of L_s simultaneously,

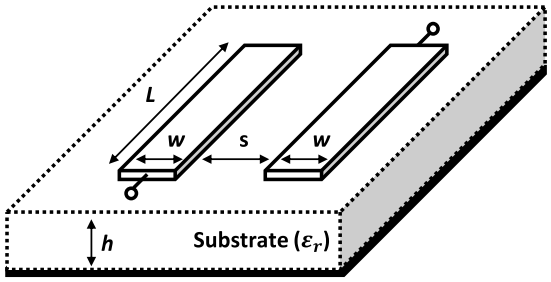


FIGURE 6. Pictorial representation of a microstrip-coupled line cross-sectional geometry.

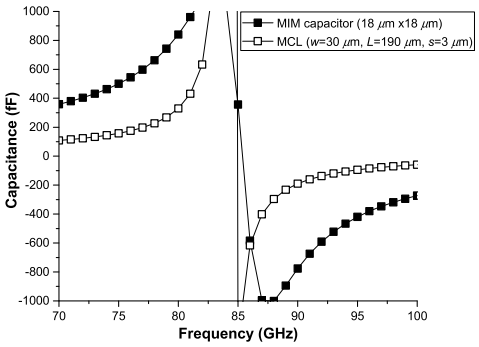


FIGURE 7. Comparison of the simulated capacitance of the MCL and MIM capacitor as a function of frequency.

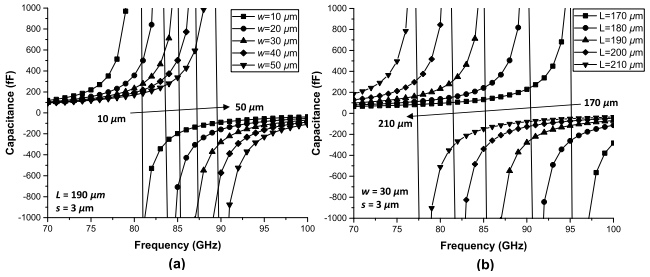
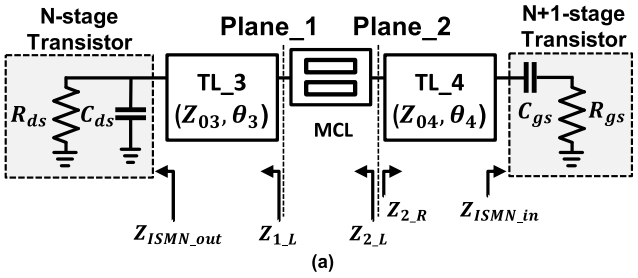


FIGURE 8. Simulated capacitance of the MCL versus frequency: (a) various widths of the microstrip lines with a fixed length of 190 μm and (b) various lengths of the microstrip lines with a fixed width of 30 μm.

so it is easy to achieve the desired SRF. The cross-sectional geometry of the MCL used as the DC-blocking component such as an MIM capacitor is illustrated in Fig. 6. The MCL has the advantage of being able to obtain the desired C_s and SRF by adjusting the width (w) and length (L) of two parallel microstrip lines on the Si substrate with a thickness h of 100 μm and loss tangent of 0.015.

Figure 7 shows the simulated capacitance of the MCL and the MIM capacitor versus frequency in the rage of 70 to 100 GHz. For fair comparison, the DC-blocking components were chosen to have a similar SRF of 85 GHz to the MCL ($w = 30\,\mu$m, $L = 190\,\mu$m, $s = 3\,\mu$m) and the MIM capacitor (18 μm$\times$18 μm). It appears that the MCL forms a smaller capacitance than the MIM capacitor at frequencies below the SRF such as 70 GHz but has a larger negative capacitance, namely a larger inductance, at frequencies above the SRF, such as 100 GHz. As predicted by equations (1) and (2), it is expected that the MCL with a smaller C_s and larger L_s than the MIM capacitor can add strong resonance at the desired



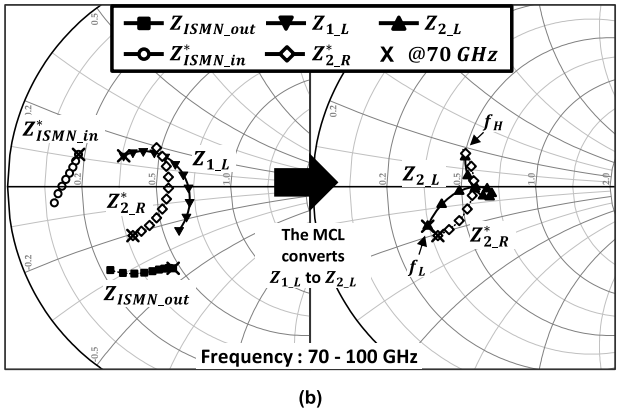


FIGURE 9. The ISMN using the MCL (w=30 μm, L=190 μm, s=3 μm): (a) schematic, and (b) impedance transformation trajectories from 70 GHz to 100 GHz on a 50 Ω normalized Smith chart.

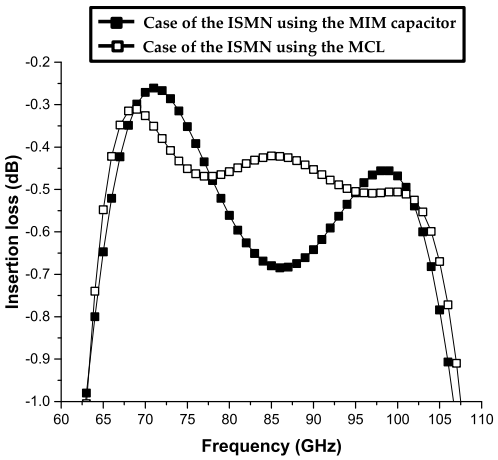


FIGURE 10. Simulated insertion loss of the ISMN frequency response with various DC-blocking components.

frequency. From these analyses, the MCL is recommended as a DC-blocking component when the ISMN is necessary for the resonant to alleviate the mid-band notch between the two matched frequencies.

Figure 8(a) shows the simulated capacitance of the MCL for various widths of microstrip lines with a fixed length of 190 μm in the frequency range from 70 to 100 GHz. Figure 8(b) shows the simulated capacitance of the MCL according to the length of the microstrip lines with a fixed width of 30 μm in the frequency range from 70 to 100 GHz. The MCL can easily be controlled to cause self-resonance at the desired frequency by adjusting the geometric structures such as the width and length of the microstrip line. As a result,

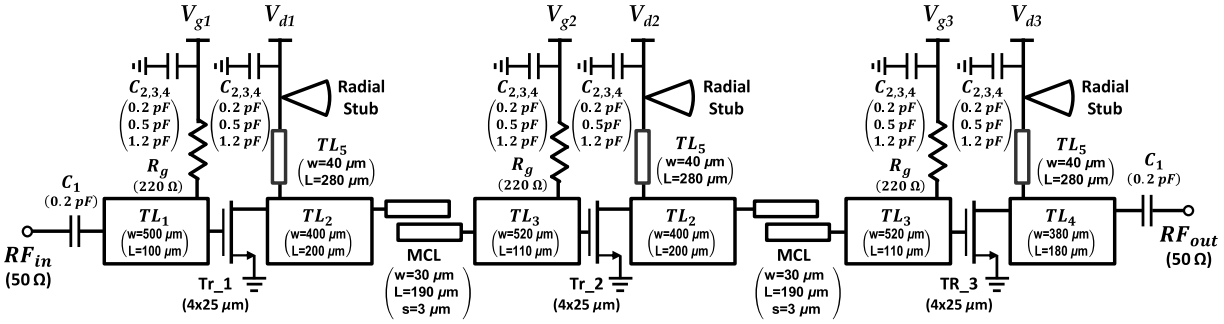


FIGURE 11. Simplified schematic of the W-band multi-stage amplifier with the proposed ISMN using the MCL.

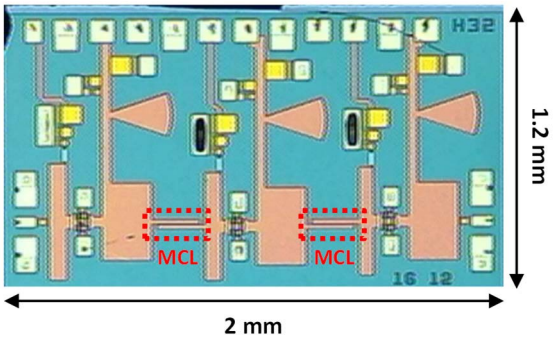


FIGURE 12. Photograph of the fabricated W-band amplifier MMIC.

compared to an MIM capacitor, the proposed ISMN using an MCL can easily form the desired SRF depending on the size of a transistor, which is advantageous for wide matching in various cases.

Figure 9(a) shows the schematic of the ISMN using self-resonance of the MCL, and Fig. 9(b) presents the impedance transformation trajectories of the ISMN using the MCL from 70 GHz to 100 GHz. Unlike the MIM capacitor, the reactance of the MCL significantly affects matching, so TL_3 and TL_4 have different characteristic impedance and electrical lengths from TL_1 and TL_2. TL_3 converts Z_{ISMN_out} to Z_{1_L}, while TL_3 converts $Z^*_{ISMN\_in}$ to $Z^*_{2\_R}$.

Also, TL_3 and TL_4 were connected by the MCL designed to have self-resonance at 85 GHz. When the MCL converts Z_{1_L} to Z_{2_L}, it operates as a series capacitor with a small capacitance below the SRF of the MCL. On the other hand, it operates as a series inductor with large inductance above the SRF of the MCL. Namely, due to self-resonance of the MCL, the impedance trajectory of Z_{2_L} intersects the impedance trajectory of $Z^*_{2\_R}$ in the mid-band frequency between f_L and f_H at Plane_2.

The frequency response of the simulated insertion loss of the two ISMNs is compared in Fig. 10. Although both cases form two similar matched frequencies and bandwidths, the ISMN using self-resonance of the MCL shows a flatter frequency response with smaller mismatched loss in the mid-band frequency between two matched frequencies compared to the ISMN using the MIM capacitor.

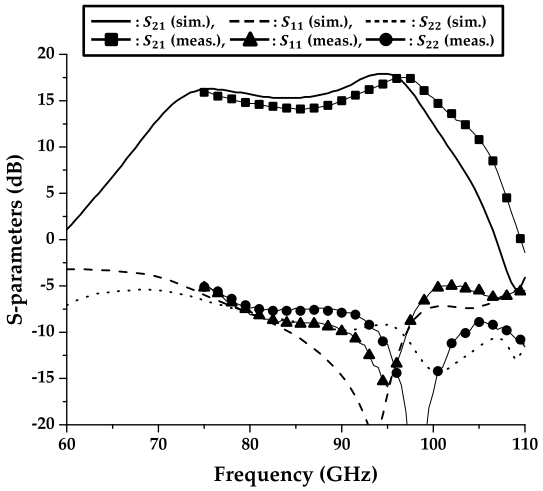


FIGURE 13. On-wafer measured and simulated S-parameters of a W-band amplifier MMIC biased with $V_g = -1$ V and $V_d = 10$ V.

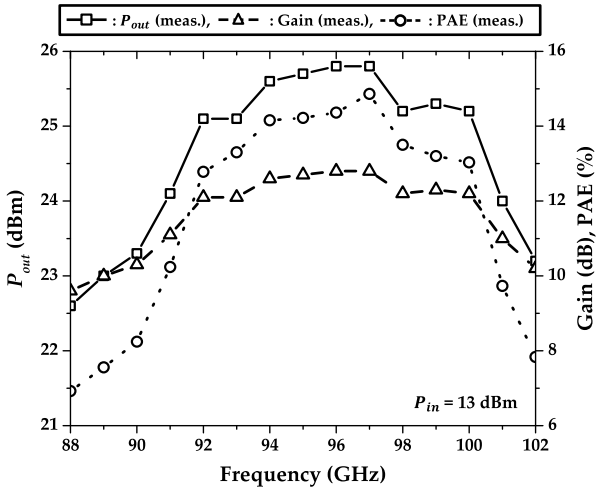


FIGURE 14. On-wafer measured and simulated P_{out}, gain, and PAE-frequency responses of W-band amplifier MMIC biased with $V_g = -1$ V and $V_d = 10$ V.

III. IMPLEMENTATION AND MEASUREMENT RESULTS

A. IMPLEMENTATION OF THE W-BAND MULTISTAGE AMPLIFIER

The simplified schematic of the W-band multi-stage amplifier with the proposed ISMN using the MCL is shown in Fig. 11. The amplifier consists of a three-stage cascade with

TABLE 1. State-of-the-art W-band GAN amplifier MMICS

Ref.	Process	Topology	Bandwidth (GHz)	$\|S_{21}\|$ (dB)	P_{out} (dBm)	Size (mm^2)
[12]	150 nm GaN HEMT on SiC	CS, 3-stage, 5-way combining	75-100	12-16	34	14.85
[13]	80 nm GaN HEMT on SiC	CS, 2-stage, 2-way combining	77.8-89	15.9-18.9	30.6	3.6
[14]	100 nm GaN HEMT on SiC	CS, 4-stage, 2-way combining	75-110	13-28	27	12.75
[15]	100 nm GaN HEMT on SiC	CS, 4-stage, No combining	86-98	20	-	-
[16]	50 nm GaN HEMT on Si	CS, 2-stage, No combining	80-95	7-10	18.3	2.53
[17]	100 nm GaN HEMT on Si	CS, 3-stage, No combining	78.5-90	14.5-17	10.5	4.2
This work	60 nm GaN HEMT on Si	CS, 3-stage, No combining	75-103	14.1-17.5	25.8	2.4

4×25 μm transistors of a common source structure (Tr_1, 2, 3). The IMN and OMN are composed of broad microstrip lines with low characteristic impedance (TL_1, TL_4) and the MIM capacitor (C_1) for DC blocking. Also, the IMN and OMN provide 50 Ω matching of the high end of the band and gain roll-off at the low end of the band. The ISMNs are implemented by the proposed interstage matching technique using the MCL and broad microstrip lines (TL_2, TL_3). The gate and drain bias circuits are simply designed using a resistor (R_g) and quarter-wave short-circuited stubs with an additional radial stub attached to the broad microstrip lines. Also, there were several bypass capacitors ($C_{2,3,4}$) to improve the low-frequency stability. A W-band three-stage amplifier was implemented in commercial 60 nm GaN-on-silicon HEMT technology. Figure 12 shows a photograph of the fabricated W-band amplifier MMIC. The chip dimensions are 2 mm $\times$ 1.2 mm including RF and DC pads.

B. MEASUREMENT RESULTS

The on-wafer S-parameter measurement of the fabricated W-band amplifier MMIC was performed using an R&S ZVA50 vector network analyzer extended by R&S ZVA-Z110 frequency converters. Due to the operating frequency range of the frequency converters, the small signal measurement was limited between 75 GHz and 110 GHz. The measured S-parameters compared to the simulation results are depicted in Figure 13. The W-band three-stage amplifier with a gate voltage (V_g) of -1 V and drain voltage (V_d) of 10 V provides a small-signal gain greater than 14.1 dB from 75 to 103GHz and reaches a peak of 17.5 dB at a frequency of 96 GHz. The agreement between the measured and simulated results is good in the W-band.

The on-wafer continuous-wave (CW) large-signal performance of the W-band amplifier MMIC was measured with Keysight W8486A power sensors for input and output power sensing. An R&S SMF 100A signal generator extended by an R&S SMZ110 frequency multiplier and a SAGE Millimeter SBP drive amplifier module was utilized to apply a sufficient input power at the MMIC. Losses of probe tips and waveguide components such as a coupler, bend, and straight were compensated in the measured results. Figure 14 presents the measured output power (P_{out}), gain, and power-added efficiency (PAE)-frequency responses of the W-band three-stage amplifier with a constant input power of 13 dBm. The output power and PAE between 92 and 100 GHz were above 25 dBm and 13% over the gain of 12 dB, respectively. The maximum P_{out} of 25.8 dBm was achieved at a frequency of 96 GHz.

The measured results of the W-band amplifier MMIC are summarized and compared to state-of-art W-band amplifiers using the GaN-on-SiC and GaN-on-Si processes, with results shown in Table 1. Our W-band three-stage amplifier MMIC had a wider gain bandwidth than most W-band GaN amplifier MMICs except that in a previous study [14]. However, the previous MMIC [14] showed a peak gain of 28 dB and a minimum gain of 13 dB, with a gain deviation of 15 dB. Our measured results show a similar bandwidth to a previous result [12] but with a relatively small gain deviation of 3.4 dB. Although our MMIC does not combine to increase the output, it shows a wide bandwidth and small gain variation.

IV. CONCLUSION

A wide-band interstage matching technique composed of low-characteristic impedance transmission lines and an MCL was proposed and successfully applied for design of the W-band three-stage amplifier and fabricated in a commercial 60 nm GaN-on-silicon technology. The W-band amplifier shows a small-signal gain above 14.1 dB from 75 to 103 GHz and a saturated output power above 25 dBm from 92 GHz to 100 GHz. The proposed wide-band matching technique is expected to be useful for wideband amplifier designs, specifically for millimeter-wave applications where low-characteristic impedance transmission lines and MCLs have been favorably utilized as practical dimensions.

REFERENCES

[1] M. Marcus and B. Pattan, "Millimeter wave propagation; spectrum management implications," *IEEE Microw. Mag.*, vol. 6, no. 2, pp. 54–62, Jun. 2005.

[2] J. Hasch, E. Topak, R. Schnabel, T. Zwick, R. Weigel, and C. Waldschmidt, "Millimeter-wave technology for automotive radar sensors in the 77 GHz frequency band," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 845–860, Sep. 2012.

[3] D. Bleh, M. Rösch, M. Kuri, A. Dyck, A. Tessmann, A. Leuther, S. Wagner, B. Weismann-Thaden, H. P. Stulz, M. Zink, and M. Rießle, "W-band time-domain multiplexing FMCW MIMO radar for far-field 3-D imaging," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 9, pp. 3474–3484, Sep. 2017.

[4] C. Paoloni, F. Magne, F. Andre, X. Begaud, V. Krozer, M. Marilier, A. Ramirez, J. R. R. Carrasco, R. Vilar, and R. Zimmerman, "TWEETHER future generation W-band backhaul and access network technology," in *Proc. Eur. Conf. Netw. Commun. (EuCNC)*, Jun. 2017, pp. 1–5.

[5] P. Pahl, S. Diebold, D. Schwantuschke, S. Wagner, R. Lozar, R. Quay, I. Kallfass, and T. Zwick, "A 65–100 GHz impedance transforming hybrid coupler for a V-/W-band AlGaN/GaN MMIC," in *Proc. Eur. Microw. Conf.*, Oct. 2013, pp. 412–415.
[6] J. Kim, S. Lee, S. Lee, W. Kim, H. Kwon, Y. Kwon, and J. Jeong, "W-band power amplifier using broadband impedance-transforming coupled line couplers," *Microw. Opt. Technol. Lett.*, vol. 57, no. 4, pp. 803–806, Apr. 2015.
[7] Z. J. Hou, Y. Yang, L. Chiu, X. Zhu, E. Dutkiewicz, J. C. Vardaxoglou, and Q. Xue, "A W-band balanced power amplifier using broadside coupled strip-line coupler in SiGe BiCMOS 0.13-μm technology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 7, pp. 2139–2150, Jul. 2018.
[8] D. F. Brown, A. Kurdoghlian, R. Grabar, D. Santos, J. Magadia, H. Fung, J. Tai, I. Khalaf, and M. Micovic, "Broadband GaN DHFET traveling wave amplifiers with up to 120 GHz bandwidth," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2016, pp. 1–4.
[9] C. Zech, S. Diebold, S. Wagner, M. Schlechtweg, A. Leuther, O. Ambacher, and I. Kallfass, "An ultra-broadband low-noise traveling-wave amplifier based on 50 nm InGaAsmHEMT technology," in *Proc. 7th German Microw. Conf.*, Mar. 2012, pp. 1–4.
[10] N. L. K. Nguyen, D. P. Nguyen, A. N. Stameroff, and A.-V. Pham, "A 1–160-GHz InP distributed amplifier using 3-D interdigital capacitors," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 5, pp. 492–495, May 2020.
[11] M. Vigilante and P. Reynaert, "On the design of wideband transformer-based fourth order matching networks for *E*-band receivers in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2071–2082, Aug. 2017.
[12] J. M. Schellenberg, "A 2-W W-band GaN traveling-wave amplifier with 25-GHz bandwidth," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2833–2840, Sep. 2015.
[13] Y. Niida, Y. Kamada, T. Ohki, S. Ozaki, K. Makiyama, Y. Minoura, N. Okamoto, M. Sato, K. Joshin, and K. Watanabe, "3.6 W/mm high power density W-band InAlGaN/GaN HEMT MMIC power amplifier," in *Proc. IEEE Topical Conf. Power Modeling Wireless Radio Appl. (PAWR)*, Jan. 2016, pp. 24–26.
[14] M. Ćwikliński, "Full W-band GaN power amplifier MMICs using a novel type of broadband radial stub," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5664–5675, Dec. 2018.
[15] S. Lardizabal, K. C. Hwang, J. Kotce, A. Brown, and A. Fung, "Wideband W-band GAN LNA MMIC with state-of-the-art noise figure," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2016, pp. 1–4.
[16] D. Marti, L. Lugani, J.-F. Carlin, M. Malinverni, N. Grandjean, and C. R. Bolognesi, "W-band MMIC amplifiers based on AlInN/GaN HEMTs grown on silicon," *IEEE Electron Device Lett.*, vol. 37, no. 8, pp. 1025–1028, Aug. 2016.
[17] X. Tong, P. Zheng, and L. Zhang, "Low-noise amplifiers using 100-nm gate length GaN-on-silicon process in W-Band," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 10, pp. 957–960, Oct. 2020.
[18] S. Colangeli, W. Ciccognani, P. E. Longhi, L. Pace, J. Poulain, R. Leblanc, and E. Limiti, "Linear characterization and modeling of GaN-on-Si HEMT technologies with 100 nm and 60 nm gate lengths," *Electronics*, vol. 10, no. 2, p. 134, Jan. 2021.
[19] H. R. Ahn, "Complex impedance transformers consisting of only transmission-line sections," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 7, pp. 2073–2084, Jul. 2012.

SUNWOO LEE was born in Ulsan, South Korea, in 1989. He received the B.S. degree in electronic system engineering from Hanyang University, Ansan, South Korea, in 2015, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering. His current research interests include mm-Wave low-noise amplifier and power amplifier integrated circuit (IC) design.

WANSIK KIM received the B.S., M.S., and Ph.D. degrees in electrical and electronics engineering from Konkuk University, Seoul, South Korea, in 1991, 1993, and 2005, respectively. In 1999, he joined the Institute for Advanced Engineering, Yongin, South Korea, where he was involved in the development of millimeter-wave transceiver systems for FMCW radar. Since 2005, he has been with the Radar Research and Development Center, LIG Nex1 Company Ltd., South Korea, where he is currently involved in the development of transceiver systems for FMCW radar. His research interest includes integrated circuits and systems from X-band to millimeter-wave.

SOSU KIM received the B.S. and M.S. degrees in electronics engineering from Kyungbuk University, Deagu, South Korea, in 1993 and 1996, respectively, and the Ph.D. degree in radio engineering from Chungnam University, Daejeon, South Korea, in 2014. He is currently the Principal Researcher and the Team Leader of the Agency for Defense Development. His research interest includes microwave seeker system development.

MIN-SU KIM was born in Seoul, South Korea, in 1978. He received the B.S. degree in electronic engineering from Incheon University, Incheon, South Korea, in 2005, and the M.S. and Ph.D. degrees in information and communication engineering from Sungkyunkwan University, Suwon, South Korea, in 2008 and 2012, respectively.

From 2012 to 2015, he was with Samsung Electronics, System-LSI Business, Giheung, South Korea, where he designed receiver circuits for transceivers in mobile terminals. From 2015 to 2018, he was with Broadcom Inc., where he designed low-noise power amplifiers for various LNA-PAMiD. Since March 2022, he has been with the Department of Information and Electronic Engineering, Mokpo National University, Muan, South Korea, where he is currently an Assistant Professor. His research interests include low-noise amplifier design, power amplifier design, RF integrated circuit (IC) design, and mm-Wave IC design for RF systems.

JUNGHYUN KIM (Member, IEEE) was born in Busan, South Korea. He received the Ph.D. degree in electrical engineering from Seoul National University, Seoul, South Korea, in 2005. In 2000, he was a Student Co-Founder with WavICs, a power amplifier design company, which is now fully owned by Broadcom, where he invented the switchless stage-bypass power amplifier architecture called CoolPAM. From 2005 to 2007, he was with the Wireless Semiconductor Division, Avago Technologies, as a Group Manager of the Integrated Circuit Design Group. In 2007, he joined the Division of Electrical Engineering, Hanyang University, Ansan, South Korea, as a Faculty Member, where he is currently a Professor. From 2007 to 2018, he was the External Director with Broadcom. He holds more than 60 U.S. patents on power-amplifier technology and RF integrated circuits. His current research interests include monolithic microwave integrated circuit design for mobile communication and millimeter-wave systems, the thermal packaging analysis of high-power devices, and intermodulation and noise analysis of nonlinear circuits.