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APPLIED RESEARCH

A 0.6 V 4 GS/s −56.4 dB THD Voltage-to-Time Converter in 28 nm CMOS

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ABSTRACT A 0.6 V voltage-to-time converter (VTC) has been presented in this work for the emerging energy-efficient time-domain circuits and systems. The proposed VTC supports a rail-to-rail input by leveraging shrink sampling with two cascaded voltage sampling and charge sharing switches, breaking the tradeoff between linearity and input range of the traditional VTC and enabling low voltage operation. The charging current source is adjustable to calibrate the VTC gain variation. In addition, a 4-bit tunable delay buffer is inserted at the output stage to calibrate the VTC time offset, enhancing the PVT performance. By resizing the push-pull inverters' PMOS/NMOS size ratio in the output buffer chain, the jitter contribution from buffers has been reduced. It also recovers the signal's pulse width consumed during the voltage-time conversion, facilitating the time signal processing following VTC. Designed and fabricated in 28 nm CMOS, the prototype VTC occupies a 0.0012 mm^2 active area. Measurement results show that the VTC can run up to 4 GHz at a 0.6 V power supply, achieving −56.4 dB total harmonic distortion (THD) with Nyquist input and consuming 2.1 mW.

INDEX TERMS Analog-to-digital converter (ADC), energy-efficient, shrink sampling, time-domain signal processing, low-voltage, voltage-to-time converter (VTC).

I. INTRODUCTION

TIME-domain signal processing has emerged as an energy-efficient solution for various applications, such as high-speed data converters, intelligent hardware acceleration, high-speed wireline communication, and the next-generation phased-array system [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29]. It benefits from the scaling of CMOS technology due to the digital form that the relative position of the rising/falling edge is concerned and processed. Fig. 1 shows the primary difference between voltage-domain and time-domain signal processing: the absolute voltage level does not influence the latter, which features the voltage scalability and technology-oriented inherence of the time-domain processing. As a result, reducing supply voltage can be a practical approach to increasing the energy efficiency of the time-domain systems. While lowering the power supply is intractable for voltage signal processing due to the limited voltage headroom and worse signal-to-noise ratio (SNR). Although, lowering voltage levels may also worsen the time-domain circuit's jitter performance due to the increased noise contribution from MOS transistors (decreased V_{GS}-V_{TH}). The noise deterioration can be alleviated by designing a sharp slope of the concerned edge, which diminishes the noise-to-jitter transformation, resulting in higher SNR of the time signals [26]. On the other hand, the time-domain signal stores the information utilizing the absolute arriving time of the transition edges whose value is continuous, the same as the analog signal. Therefore, it shows higher coding efficiency than digital signal processing (DSP) as a long digital bit-stream is needed for DSP with a specific resolution.

There are various time-domain circuit blocks developed for a wide range of applications. Voltage-to-time converter (VTC) is one of the critical blocks in time-domain

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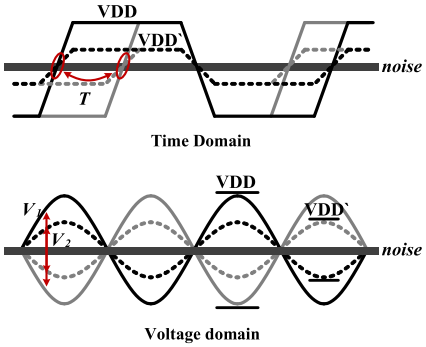

FIGURE 1. Time-domain signals and voltage-domain signals.

circuits and systems for signal quantization and conversions, such as time-domain ADC, time-domain wireline transceiver, time-domain in-memory computing, time-domain DC-DC, and all-digital PLL [1], [2], [3], [4], [5]. In analogy to an analog-to-digital converter (ADC), the ubiquitous circuit which converts the analog signal into a digital signal for subsequent processing, VTC converts the input analog voltage into a time difference other than the digital one. ADC has been explored and investigated profoundly for years of research and industry implementation. While as the analog front-end for time-domain signal processing, VTC is still in the nascent stage [27]. Compared to ADC, VTC is more area-efficient and energy-efficient because the signal conversion is still in the analog domains. It is also more feasible to achieve a wide bandwidth because only a small input sampling capacitor is requested for the conversion [18]. VTC transfers the voltage domain signal represented by its amplitude (Y-axis) to the time domain signal represented by the rising/falling edge sequence (X-axis). It is a pulse-width-modulation (PWM) circuit with the input controlling the pulse width essentially. Then, a voltage-controlled delay line (VCDL) can be regarded as a VTC, but its linearity is poor such that it is not suitable for implementation as an independent VTC in general.

The most straightforward voltage-time (V-T) conversion directly controls the charging/discharging current through the input voltage (variable-slope VTC). This simple method results in a high-speed structure but an inferior linearity performance due to the nonlinear voltage-current controlling of the MOS transistor, as shown in Fig. 2(a). On the other side, one can set up the different initial voltages based on sampling the input voltage and charge/discharge the node with a constant slope to generate the different ramp edges, as shown in Fig. 2(b) (constant-slope VTC). This method achieves better linearity due to precise sampling and constant charging. A sensing comparator with a specific threshold voltage V_{TH} should be deployed to sense the different transition edges in both types, accomplishing the V-T conversion. It results in a limited input voltage range to guarantee the linearity of the conversion. Since the linearity of the time-domain systems is confined by the front-end VTC [20], reducing the supply voltage of the VTC to increase the energy efficiency

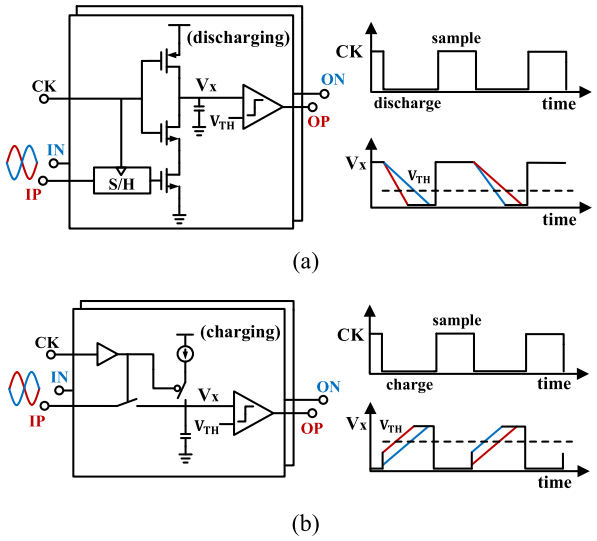

FIGURE 2. (a) Variable-slope VTC and (b) constant-slope VTC.

may be infeasible due to the deteriorated linearity. Lowering input amplitude also worsens the SNR of the signal and reduces the system's dynamic range, which is unpreferred in most cases. As a result, conventional VTC is not suitable for voltage scaling. It prevents the time-domain signal processing system from a low-voltage supply for energy-efficiency improvement if VTC is implemented as the conversion front-end. In addition, the VTC gain, defined by the output time difference over the input voltage (ps/V), varies at different process-voltage-temperature (PVT) corners, posing difficulty for the subsequent time-domain processing. Hence, besides the worse linearity performance with voltage scaling, the PVT sensitivity also weakens the robustness of time-domain processing when VTC is deployed. For high-speed scenarios, the linearity performance and the PVT robustness of VTC are deteriorating further, especially for low power supply.

Aiming to break the input range/linearity tradeoff mentioned and to carry out a robust PVT performance with high energy efficiency, we propose a 0.6 V 4 GS/s −56.4 dB total harmonic distortion (THD) VTC in this work (Fig. 4), which features:

1) Two cascaded switches are implemented as the sample and hold front with inverse clock polarity, setting up an initial step voltage below the threshold of the sensing comparator. Both switches are configured with the bootstrapped structure, supporting a rail-to-rail input with the step voltage proportion to the input signal because of the charge sharing. This unique sampling scheme enables the VTC to work at low supply voltage by breaking the tradeoff between input amplitude and VTC linearity, supporting a better SNR input signal.

2) The bias voltage of the PMOS current source is tunable, and the 3-bit coarse tuning charging path is configured, contributing to adjusting the charging speed during the V-T transition and calibrating the gain variation under different PVT. In addition, a 4-bit tunable delay line is also inserted in the buffer chain after the V-T conversion to calibrate the VTC

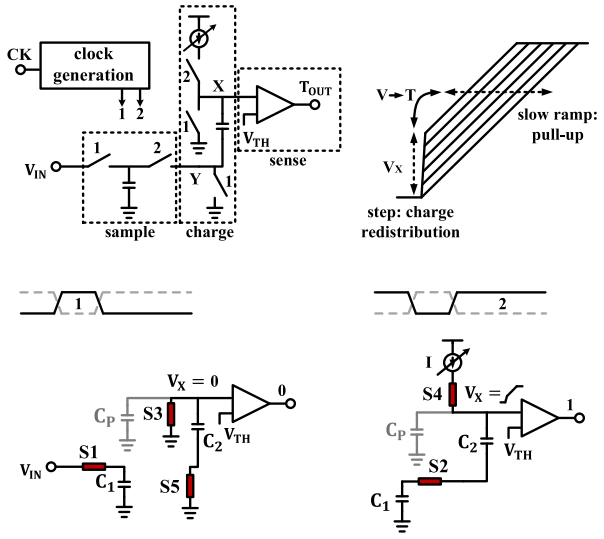

FIGURE 3. The behavioral model of the proposed VTC.

offset, facilitating the implementation of the proposed VTC in time-domain signal processing systems.

3) The PMOS/NMOS size ratio of the push-pull inverters in the buffer chain is optimized to sharpen the rising edge (interested edge), reducing the jitter contribution from the buffer chains and recovering the pulse width consumed during the V-T conversion.

The rest of this article is organized as below: section II elaborates on the details of the architecture and circuit blocks of the proposed VTC, and section III verifies the design consideration with both simulation and measurement. Finally, section IV concludes our work.

II. VTC DESIGN CONSIDERATIONS

A. VTC REVIEWS

VTCs are categorized into two types: variable-slope VTCs and constant-slope VTCs. Figure 2(a) shows the first type of VTC, in which the signal directly inputs to the gate of the current source transistor, controlling the current magnitude and leading to a different charging/discharging speed. It is also regarded as the current-starved-based VTC [9]. A 5 GHz current-starved inverter-based VTC has been reported in [8], which achieves high speed with a simple structure since no sampling switch is required. However, this VTC is limited to 4-bit resolution due to the large nonlinearity from voltage-current controlling of the MOS transistor. The full-scale input is also below 100 mV peak-to-peak. To overcome the linearity issue and limited input range caused by the transistor's charging characteristic, reference [19] proposed a two-step-transition inverter-based VTC achieving −52.5 dB THD with a 0.6 V V_{pp} input at 1 GHz. The analog input NMOS transistor is branched off from the driving pull-down path and released from the voltage headroom, realizing a wider but still limited input range. Reference [20] reported a differential compensated VTC to optimize the linearity performance by alleviating the third harmonic distortion of the

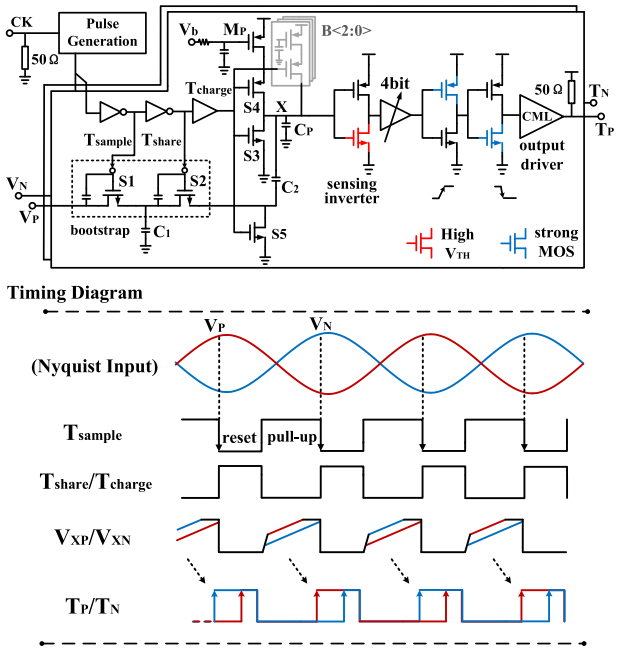

FIGURE 4. The detailed circuits and corresponding timing diagram of the proposed VTC.

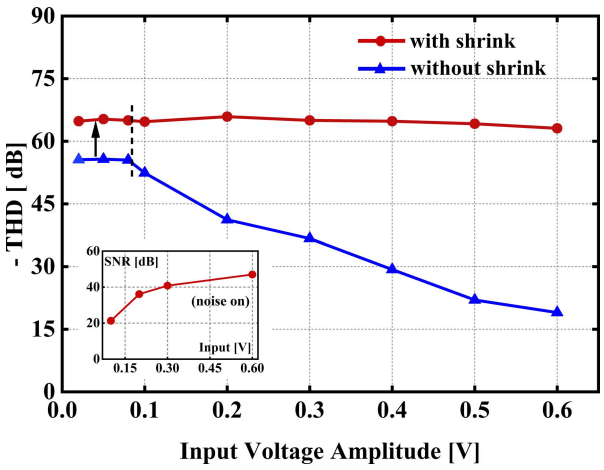

FIGURE 5. The simulated THD (noise off) of the proposed VTC with/without shrink sampling at 4GS/s 0.6V supply with Nyquist input. The embedded figure shows the SNR (noise on) at different input voltage with shrink sampling.

discharging current with another constant discharging pair. It achieves −57 dB THD in 1 GS/s with 0.4 V V_{pp} input at 1 V supply. However, the compensation will be less efficient when working frequency increases, resulting in poor linearity performance [21].

Recently, the VTC deployed in time-domain ADC (TDADC) depends more frequently on the second type structure, shown in Fig. 2(b) [27]. Although the specific circuit topology may vary case by case, they all generate the time difference through a constant current to pull up/pull down the transition node, which is set up with a different initial voltage. Since the initial voltage setup at the beginning of the charging/discharging process is based on the sampled input,

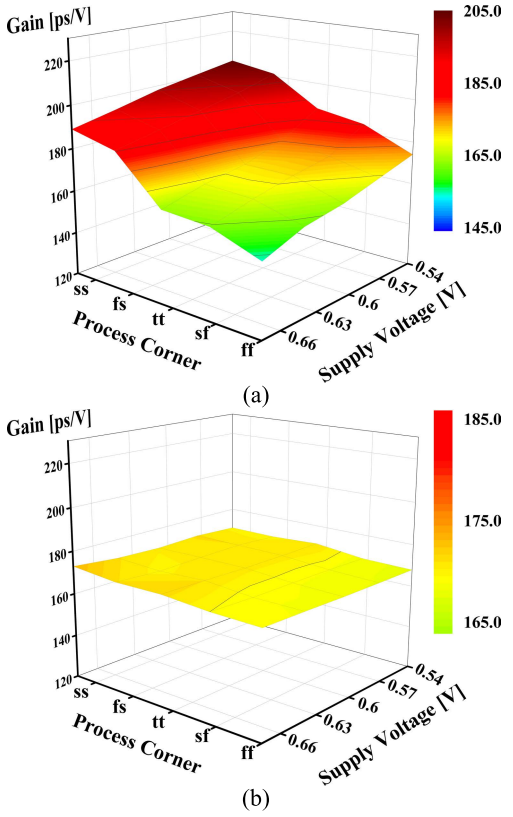

FIGURE 6. (a) Gain variation without charging current calibration, (b) gain variation with charging current calibration, at different PVT corners.

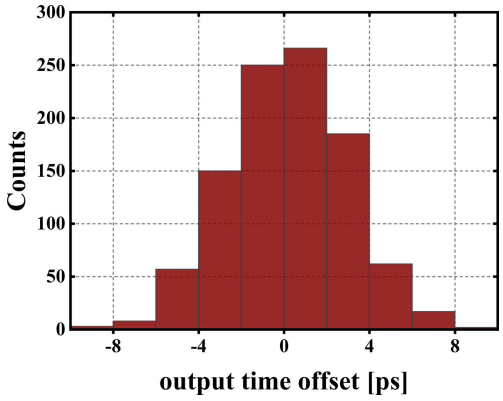

FIGURE 7. The simulated output time offset of the proposed VTC.

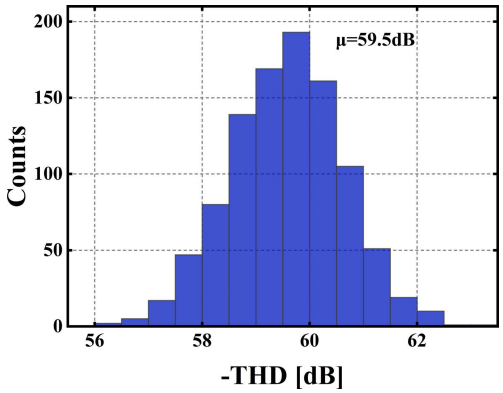

FIGURE 8. The simulated THD of the proposed VTC.

a linear voltage-time conversion can be achieved as long as the threshold voltage of the following sensing comparator is larger than the initial voltage. A 2 GS/s constant-slope VTC achieving −50 dB THD is proposed in [22]. As a buffer front-end of the TDADC, the VTC features a simple structure and large bandwidth due to the small input capacitance. However, maintaining the constant discharging current in [22] would be arduous if a low supply voltage is implemented, resulting in worse linearity. Reference [18] proposed a constant discharging VTC using the bootstrapped switch to generate the initial voltage, which achieves −52dB THD at 2.5 GHz frequency with 450 mV V_{pp} input. However, this VTC is not suitable for the low power supply due to the transistors stacked in the discharging path, and the gain variation of VTC remains unresolved. Recent work in [23] reported a 10-bit TDADC, but the spurious-free dynamic range (SFDR) is only 53 dB for a 1 MHz sinusoidal input. Its linearity performance is unsatisfactory for a 10-bit design, mainly limited by the VTC implemented. The VTC in [23] deploys the widely used integrate-and-fire (I&F) circuitry in spiking neuron emulation to achieve the voltage-time conversion. The gain of the VTC is tunable to cover the PVT variation, but the linearity is non-optimized as the lack of consideration of high-order nonlinearities in I&F.

B. CIRCUIT BLOCKS OF THE PROPOSED VTC

Our work is also based on the constant-slope structure, with a novel V-T conversion scheme, which supports the rail-to-rail input and enables simple gain and offset calibration. The simplified architecture of the proposed VTC is shown in Fig. 3, which consists of the clock generation, the cascaded sampling switches, the charging path, and the sensing comparator. Clocks 1 and 2 with inverse phases derived from the clock generation block fulfill the conversion by controlling the corresponding switches and seaming the sampling and charging processes. The voltage at transition node X will step (sharp ramp) first, followed by a slow ramp (pulled up by the charge current source) when clock 2 turns on. The waveform of node X at the V-T conversion period with different input voltage is shown in the upper-right of Fig. 3. Due to the different initial step voltage established by the sample switches, different charging times generate through the same current source.

To illustrate the working principle intuitively, we divide the conversion behavior into two processes, as shown at the bottom of Fig. 3. When clock 1 is VDD and clock 2 is ground, switches S1, S3, and S5 turn on while switches S2 and S4 turn off. At this moment, the input voltage is tracked and sampled by capacitor C_1. Furthermore, both plates of the capacitor C_2 are reset to the ground by the switches S3 and S4. VTC now achieves the tracking and resetting, establishing the precondition for the following voltage step and pull-up. When clock 2 is VDD and clock one is ground, switches S2 and S4

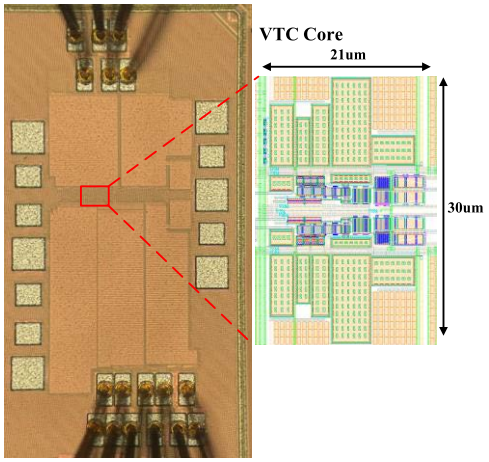

FIGURE 9. VTC chip microphotograph.

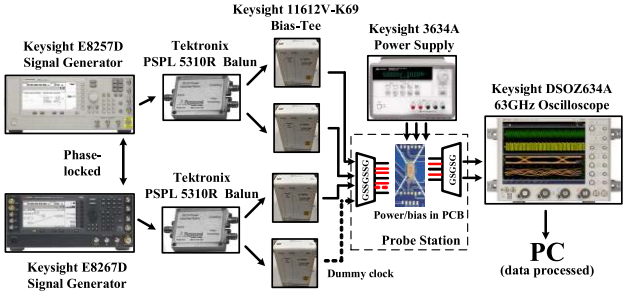

FIGURE 10. The high-speed measurement platform for VTC.

turn on and switch S1, S3, and S5 turn off. Capacitor C_1 stores the charge sampled at the moment when S1 goes off. At the same time, the voltage at node Y (bottom plate of capacitor C_2) changes immediately due to the charge redistribution between C_1 and C_2, assuming the turn-on resistance of S2 is small. The voltage at node X (top plate of the capacitor C_2) also steps instantaneously accordingly because of the charge conservation law (the charge provided by the limited current source flowing into node X is negligible at this instance). Afterward, the voltage at node X is pulled up to VDD by the current source, generating a slow ramp. The followed sensing comparator senses these ramps and produces sequential waveforms with different transition edges, completing the V-T conversion.

Assuming the parasitic capacitance at node X is C_P, and the source current is I, the conversion gain of the VTC can be derived. When clock 2 is VDD, the charge sampled at the capacitor C_1 now shares between C_1 and equivalent capacitance looking into the bottom plate of C_2. Because of the charge conservation, we have the step voltage:

$$V_X = \alpha V_{IN} \tag{1}$$

where:

$$\alpha = \frac{C_1 C_2}{C_1 (C_2 + C_P) + C_2 C_P} \tag{2}$$

Coefficient α is defined as the shrink sampling ratio. After the voltage step, the slow ramp will be pulled up to VDD by the current source. The slope of the slow ramp is the charging speed:

$$\frac{dV}{dt} = \frac{I}{C_{eq}} \tag{3}$$

where:

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} + C_P \tag{4}$$

From (1) and (3), the conversion gain is:

$$A_{V-T} = \alpha \frac{C_{eq}}{I} \tag{5}$$

All the switches in this simplified model are assumed to be ideal with near-zero on-resistance. According to (5), we can achieve the requested conversion gain by choosing the proper capacitance C_1, C_2, and the charging current I. In addition, the cascaded sample switches are implemented to achieve a shrink sampling, enabling the VTC to support a rail-to-rail input by setting the initial voltage lower than the threshold voltage of the sensing comparator, as presented in Fig. 3. This unique feature is vital for the VTC to work at a low power supply, which increases the signal SNR by broadening the input full-scale. This shrink sampling is essentially a passive voltage divider without contributing additional noise, as switch S2 shares a constant charge between C_1 and C_2 (free from the clock jitter of S2).

The schematic of the VTC circuits, along with the corresponding timing diagram, are presented in Fig. 4. A pulse generation block is implemented to transfer the input sinewave into a ∼60 ps width (low level) sampling clock, which will drive all the switches in the VTC core. A pseudo-differential structure is deployed to compress the common mode noise and reduce even-order harmonics. The cascaded switches in the sampling part are both implemented using bootstrap to support the rail-to-rail input and stabilize the on-resistance of the MOS switch during charge sharing when S2 is on. The driving clock polarity of each switch is presented in the timing diagram, which contributes to achieving the sample/reset and voltage step/pull-up for V-T conversion. A 4-bit digital controlled delay buffer is inserted after the sensing inverter with a 500 fs tunable step, which is utilized to calibrate the output time offset of the VTC in the case of the varied PVT. The current source implemented with a PMOS transistor M_p has a tunable gate bias voltage to adjust the charging current. In addition, the tunable bias voltage V_b, which controls the source current, is used for calibrating the gain variation of the VTC. Noise from the gate bias of M_p contributes little to the noise-to-jitter transformation in the V-T conversion as M_p is biased in the linear region (large W/L size), and plenty of decoupling capacitors have also been configured to V_b. In addition, a 3-bit digital controlled (B2-B0) charging path is branched off the main path, enhancing the robustness of the conversion by coarsely tuning the VTC gain.

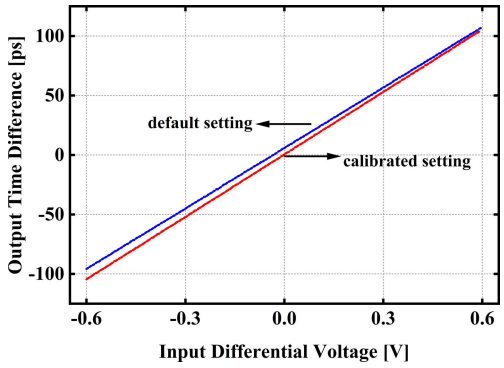

FIGURE 11. Measured conversion curve of the proposed VTC at 0.6V power supply w (red)/wo (blue) offset/gain calibration.

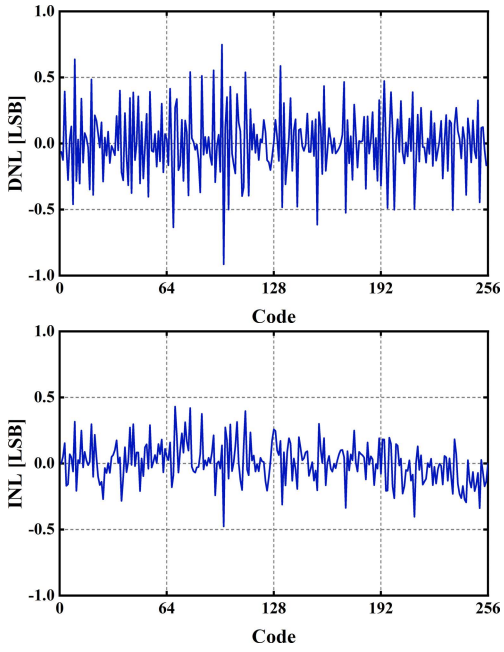

FIGURE 12. Measured VTC's DNL/INL. The input voltage is quantized at the 8bit resolution.

Capacitors C_1 and C_P in the VTC circuit diagram are implemented using the MOM cap provided by the foundry without concerning the absolute value. C_1 is chosen around 60fF to achieve a sizeable analog bandwidth (∼4 GHz), while C_2 and C_P are chosen based on the specified VTC gain. Since a slow rising slope is generated when executing the V-T transition at node X, the pulse width may decrease much after conversion resulting in the incomplete pulse waveform, possibly failing to drive the subsequent buffers. The transistors labeled in blue in Fig. 4 are chosen as a strong MOS in the push-pull inverter to recover the waveform appropriately, which also reduces the jitter contribution from buffers of the rising edges with the sharpened slope. Lastly, for the direct measurement of the high-speed VTC using an oscilloscope, a single-ended current-mode logic (CML) driver is implemented in the last stage as the output interface (DC coupling). The simulation results show that the CML stage does not influence linearity.

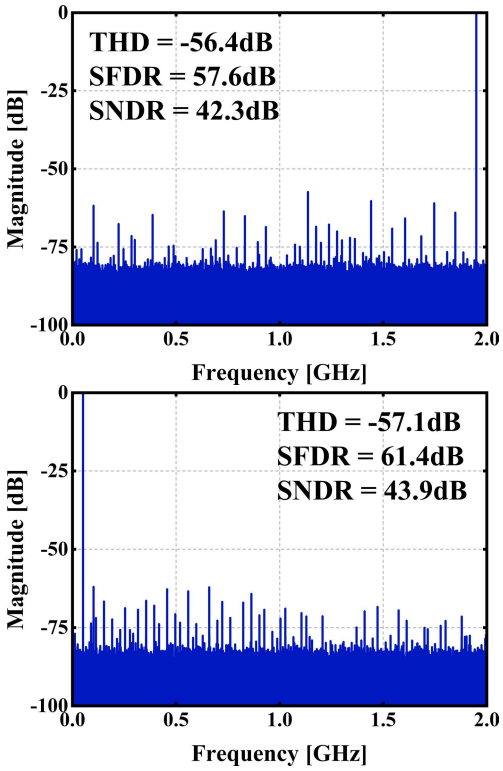

FIGURE 13. Measured VTC output spectrum at 0.6V, 4GS/s with Nyquist (1.9492GHz) and low (50.78MHz) input frequency.

In addition, the jitter amplification of the output CML drivers (loaded with a 50 Ω resistor in simulation) is designed to be near 1 to evaluate the VTC noise performance fairly. The output time signal with different rising edges is non-differential, and the layout of the two signal paths is isolated strictly. Their power/ground connections are located at the far end after passing through enough decoupling capacitors. It reduces the coupling and interference from the other path and maintains the SNR of the time-domain signals.

Note that a push-pull inverter with a high threshold voltage (V_{th}) NMOS is deployed as the sensing comparator. It enables the high-speed sensing of the ramp signals at node X at the low supply voltage. In addition, the high V_{th} NMOS is also utilized for broadening the linearity range. As a large voltage step (smaller shrink ratio) is usually preferred for obtaining the high conversion gain (wide output time range), a prominent nonlinearity may induce if the maximum step voltage exceeds the V_{th} of the NMOS. Therefore, a high V_{th} NMOS is selected to increase the VTC output range without sacrificing linearity. Although the V_{th} varies across the PVT, we can guarantee the linearity by leaving enough margin between the V_{th} and the step voltage amplitude.

C. LINEARITY ANALYSIS

As indicated by (5), the VTC will be entirely linear if a constant current is implemented. However, the transient current is impossible to keep constant during the charging process (the output resistance of an actual current

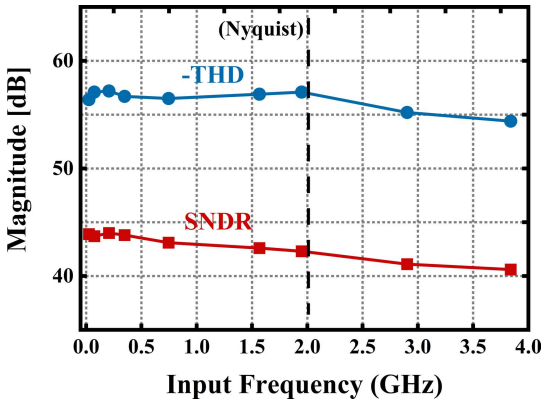

FIGURE 14. Measured THD and SNDR of the VTC with different input frequencies at 0.6V 4GS/s.

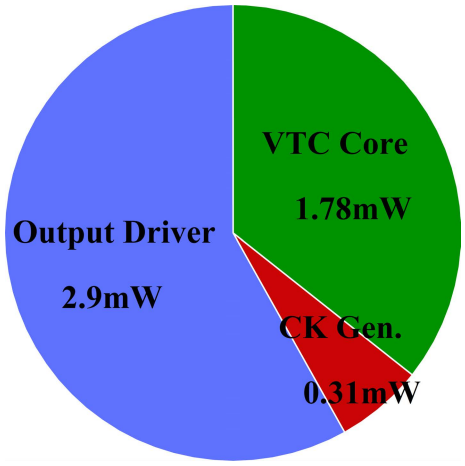

FIGURE 15. Measured power breakdown of the VTC blocks.

source is finite), inevitably leading to some nonlinearity. Since an actual PMOS is deployed as the charging current source in the proposed VTC, the charging current I can be obtained utilizing the square-law function of a MOS transistor:

$$I(t) = K(1 + \lambda(V_{DD} - V_x(t))) \tag{6}$$

K is a constant and λ is the channel-length modulation coefficient. Then, the transient voltage $V_x(t)$ at node X is:

$$V_x(t) = \left(\alpha V_{IN} - \frac{1 + \lambda V_{DD}}{\lambda}\right) e^{-\frac{K\lambda}{C_{eq}}t} + \frac{1 + \lambda V_{DD}}{\lambda} \tag{7}$$

where αV_{IN} is the initial step voltage setup during the charge sharing. The sensing inverter will output the time signal if $V_x(t)$ exceeds V_{TH}. So, take:

$$V_x(T_x) = V_{TH} \tag{8}$$

We have:

$$T_x = -\frac{C_{eq}}{K\lambda} \ln\left(\frac{V_{TH} - \frac{1+\lambda V_{DD}}{\lambda}}{\alpha V_{IN} - \frac{1+\lambda V_{DD}}{\lambda}}\right) \tag{9}$$

Equation (9) shows the non-linear relation between the sensing time T_x and the input voltage V_{IN}. As a result, a small input amplitude is preferred for better linearity, which explains the linearity/input range tradeoff of the constant-slope VTC. The linearity/input range tradeoff has been eliminated with the shrink sampling in the proposed VTC (as identified by the ratio α in (9)). With a delicate choice of the shrink sampling ratio α and the V_{TH} of the sensing inverter, a good linearity performance can be obtained considering a large conversion gain.

Excessively reducing the shrink ratio α will increase the linearity significantly. However, the output time range will be reduced simultaneously and be overwhelmed by the jitter, which makes the extensive shrinking impractical and meaningless. In addition, shrink sampling features passive scaling does not improve the VTC dynamic range as the input-referred SNR remains the same (embedded in Fig. 5). Nevertheless, it is enlightening to implement the proposed shrink sampling with a tunable ratio α (e.g., adjusting capacitor C_2) in the V-T conversion front-end, which will broaden the VTC application scenarios with the configurable full-scale input range. Above all, the simulated results in Fig. 5 show that the VTC deploying the shrink sampling achieves better linearity than the one without input shrinking (both are implemented with the same structure, but capacitor C_2 is removed for the VTC without input shrinking). It indicates that a non-linearity compensation scheme exists between the voltage sampling/charge redistribution (V_{IN}-V_X) and voltage pull-up (V_X-Time). However, further quantitative analysis is necessary for thoroughly exploring the compensation mechanism in future work.

III. SIMULATION AND MEASUREMENT RESULTS

To verify the PVT performance with the straightforward gain/offset calibration proposed, comprehensive post-layout simulations have been conducted before the chip fabrication. Fig. 6 shows the gain variation before/after coarse charging path tuning and fine bias voltage V_b tuning, which illustrates the effectiveness of the proposed gain calibration. A stable conversion gain is critical for system robustness in most applications with time-domain processing. Furthermore, the VTC output time offset due to the process (random) and layout (systematic) mismatches can be reduced with the inserted tunable delay buffer after the sensing inverter, as shown in Fig. 7 with the Monto-Carlo simulations. The 3σ of the time offset ranges from -8.7 ps to 9.1 ps, which is covered by the $+$-8 ps tunable range of the delay buffer.

The THD variation due to process (global & local) and layout mismatch is also simulated and presented in Fig. 8. Since enough margin between the sensing buffer V_{th} and the step voltage amplitude has been allocated, the VTC dynamic performance is steady as a slight THD variation ($3\sigma = 3.13$ dB) is shown. In addition to the spice simulations, the proposed VTC is fabricated utilizing commercial 28 nm CMOS and verified with actual measurements. The chip microphotograph in Fig. 9 occupies a compact 0.0012 mm^2

TABLE 1. Performance comparison.

	09 EuMC [28][a]	16 ESSCIRC [19][a]	19 MJ [29][a]	19 JSSC [24][b]	20 JSSC [18][b]	**This work[a]**
Technology (nm)	90	28	65	65	65	**28**
VDD (V)	1	1	1.2	1	1	**0.6**
Input Range (V_{pp})	0.1	0.6	0.6	0.4	0.45	**0.6**
Output Range (ps)	53.3	128	2340	~100	352	**210**
Conversion Speed (GS/s)	5	1	0.5	1	2.5	**4**
THD (dB)	~-25	-52.5	-68	-57	-53	**-56.4**
Power (mW)	3.6	0.18	0.48	~0.54	1.7	**2.1**

[a] Measurement
[b] Simulation

active area, including the clock pulse generation and output drivers (the VTC core is only 21 um × 30 um). The measurement platform is configured as shown in Fig. 10. The high-frequency clock and input signals are generated with the low-noise Keysight E8257D/ E8267D signal generators and fed into the DUT through the GSSGSSG RF probe. The high-speed output time signals are captured directly by the high-performance Keysight DSOZ634A oscilloscope (63 GHz bandwidth), and the transient waveforms captured are used for post-data processing.

The voltage-to-time conversion characteristic curves are measured first with a pair of slow ramp voltage signals as the input. Compared to the conversion curve without calibration, as presented in Fig. 11, the proposed calibration removed the time offset, and the conversion gain is adjusted to be ∼175 ps/V. Therefore, a linear conversion curve is obtained, and the output full-scale reaches +/−105 ps, providing an adequate time range for the following signal processing. In addition, the differential and integral nonlinearity (DNL and INL) are calculated with the full-scale ramp input quantized at an 8bit resolution [19]. This measurement is similar to the DAC since the output time signal is essentially continuous analog. As a result, Fig. 12 shows that the DNL/INL was suppressed within +0.75/−0.92 LSB and +0.43/−0.48 LSB.

Fig. 13 shows the FFT spectrums with both low-frequency input and Nyquist input. The Nyquist THD reaches −56.4 dB, which results in a good agreement between the measurement and simulation of the proposed VTC. The dynamic performance with different input frequencies at 4 GS/s is also measured in Fig. 14, exhibiting stable linearity across the working band. The SNDR is more than 42 dB in the Nyquist zone, demonstrating a low noise V-T conversion. The power breakdown of the VTC blocks is drawn in Fig. 15. The VTC core only dissipates 35.7% percent of the overall prototype power, considering the power-consuming CML output drivers for probe testing. Finally, the performance of the proposed VTC is summarized and compared to the state-of-the-art (VTC only) in Table 1. Our work achieves the first VTC to work up to 4 GS/s with only a 0.6 V power supply, presenting excellent linearity and high energy efficiency.

IV. CONCLUSION

This work presented a 0.6 V energy-efficient and high-linear VTC in 28 nm CMOS. It deployed novel shrink sampling switches to achieve concurrent voltage sampling and charge sharing, resulting in precise voltage-time conversion. In addition, adjustable charging current source and tunable delay line have been implemented to calibrate the VTC gain variation and offset. As a result, the proposed VTC can support a rail-to-rail differential input with the compact structure, breaking the linearity and input range tradeoff. Measurement results show that the VTC realized −56.4 dB Nyquist THD in 4 GS/s, supporting the rail-to-rail input with only a 0.6 V power supply, which provides an excellent front-end solution for the emerging time-domain circuits and systems.

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