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RESEARCH ARTICLE

Solar PV Fed DC Microgrid: Applications, Converter Selection, Design and Testing

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ABSTRACT In this research article, major applications which use solar PV fed DC microgrid for either their routine operation or gain additional advantages over existing electrical power architecture are elaborated. The role of power converters in interfacing the input with the required output is highlighted. The advantages of solar PV fed DC microgrid are demonstrated by designing and testing a non-isolated high gain high power (HGHP) DC-DC converter to meet the DC distribution voltage level. The proposed converter is synthesized by using hybrid combination of three-phase interleaved boost converter (IBC) with voltage lift technique along with coupled inductors (CIs) and voltage multiplier cell (VMC). The proposed concept is practically demonstrated and the adopted design techniques are validated using simulation and experimentation. The proposed converter with 60V/1.1kV, 100kHz and 3kW rating operates at 92.3% full-load efficiency under practical conditions. Due to the gain extension techniques adopted, the switches used in the proposed converter are subjected to a voltage stress which is only 36% of the output voltage. Due to interleaving technique, the input current ripple and the current stress on the switches are only 15% and 33% of the input current respectively. Key performance parameters of this converter are thoroughly investigated and benchmarked with some state-of-the art converters to appreciate the salient features of the presented converter. The ability to yield higher voltage gain at safe duty ratio, high power handling capacity, low voltage and current stresses on the power switches are the main advantages of the proposed converter.

INDEX TERMS DC-DC power converters, distributed power generation, power conversion, power electronics, renewable energy sources.

I. INTRODUCTION

In recent times, DC microgrids are emerging as efficient means of distributing and utilizing the electrical energy obtained from renewable energy sources like photovoltaic (PV) systems, wind energy conversion systems (WECS) and fuel cells [1], [2], [3], [4]. In addition to the well-known electrical distribution systems, DC microgrids are advantageously used in some key applications like aircrafts [5], [6], [7], [8], ship board power supplies [9], [10], [11], charging stations for electric vehicles (EVs) [12], [13], [14], [15], DC homes [16], [17], buildings [18] and data centres [19]. The enormous advantages of renewable energy fed DC microgrids in plethora of applications continue to enthuse professionals and researchers.

The voltage and power levels of the accessories employed within all the above-mentioned applications are different as depicted in Fig. 1(a). The basic types of power electronic converters and their derivatives along with the voltage and power levels are also clearly portrayed. Interestingly, these varieties of power electronic converters play the intermediate voltage level matching role to perfection and are an integral part of the modern-day applications [20], [21], [22], [23]. Fig. 1(b) illustrates the role of high gain DC-DC converters in the applications discussed so far. Obviously, except the three voltage levels (highlighted in red) all the other voltage and power levels are met using the intermediate high gain power electronic converter. This research work focusses on presenting a case study involving the synthesis, design and

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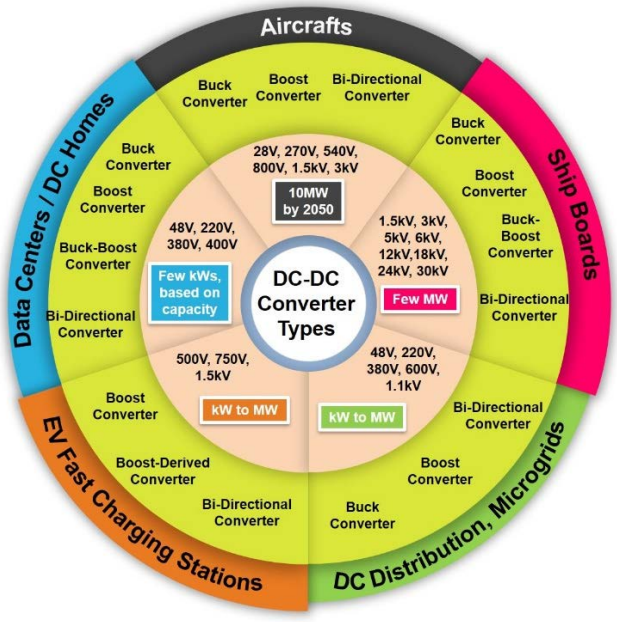


(a)

(b)

FIGURE 1. (a) Types of DC-DC power converters used in some applications. (b) Schematic diagram to illustrate the role of high gain DC-DC converters in various applications.

testing of a high gain high power (HGHP) converter interface for a solar PV fed DC microgrid application.

Recently, due to drastic drift towards utilizing renewable energy sources (RES), there is an impending requirement for step-up converters to integrate the RES to the utility grid and/or other loads. Conventional boost converter (CBC) and some of its basic derivatives like quadratic and cascaded boost converters are unsuitable for high gain high power (HGHP) applications due to some inherent drawbacks like (i) extreme duty ratio operation of switches, (ii) diode reverse recovery problem, (iii) higher voltage stress on the power switches and (iv) degraded efficiency [24], [25].

Generally, the voltage gain obtained from boost-derived converters is enhanced by employing additional gain extension mechanisms [26], [27], [28]. Some converters employ active-passive inductor cells [29], switched inductor cells [30], [31], switched capacitor networks [32], [33], [34], [35] and charge-pump cells [36], [37] to accomplish high voltage gain. Nevertheless, voltage balancing in the capacitors and higher component count are the main tricky issues in such converters.

Coupled inductors (CIs) are effortlessly used to enhance the voltage gain of a power converter; adjusting the turns ratio value accomplishes the task of meeting the high voltage conversion ratio requirement [38]. In [39], [40], [41], and [42], CIs are employed along with gain extension cells which are connected at the secondary side of the CIs to further enhance the overall voltage conversion ratio of the converter [43]. Moreover, by replacing the discrete energy storage inductor with a CI and arranging in an interleaved fashion, the power handling capability is also enhanced besides fulfilling the voltage gain requirement [44].

Though CI based converters offer higher voltage gain the winding leakage inductance causes voltage spikes and results in increased voltage stress on the power switches. Converters employing multi-winding CIs [45], [46] and dual CIs [47] also provide the required higher voltage conversion ratios. However, such converters are rarely used due to the complexity involved in designing and manufacturing the required magnetic components.

In PV applications, ripple-free input current is preferred for easier implementation of maximum power point tracking (MPPT) algorithms. Hence, conscious effort is made to reduce the current ripple at the input. Interleaving technique is widely adopted to cancel the input current ripples and are employed in [39], [40], [41] and [44], [48], and [49].

In the proposed HGHP converter, high voltage gain value is achieved by employing hybrid combinations of interleaving technique along with CIs, voltage-lift and voltage multiplier cells (VMCs). The paper is arranged as follows: Section 1 introduces the proposed converter by thoroughly reviewing the existing literature. In Section 2, the circuit is described followed by the operating principle in Section 3. The detailed analysis and the design equations are derived in Section 4. The experimental results and their inferences are discussed in Section 5 while the comparative features are detailed in Sections 6 and 7. The concluding remarks are outlined in Section 8 followed by the references.

II. CIRCUIT DESCRIPTION OF THE PROPOSED HGHP CONVERTER

Fig. 2 shows the circuit diagram of the proposed HGHP converter. Stage 1 of the converter is synthesized from a conventional three phase IBC comprising of switches Z_1, Z_2 and Z_3 along with the primary windings of CIs (L_{1P}, L_{2P} and L_{3P}) which serve as the energy storage inductors. Voltage lift technique is incorporated using C_{lift} and D_{lift} to enhance the voltage gain of Stage 1. Intermediate diode D_{IBC} is used to prevent the secondary windings from discharging the stored energy. The three secondary windings of the CIs (L_{1S}, L_{2S} and L_{3S}) are connected to one VMC network comprising of

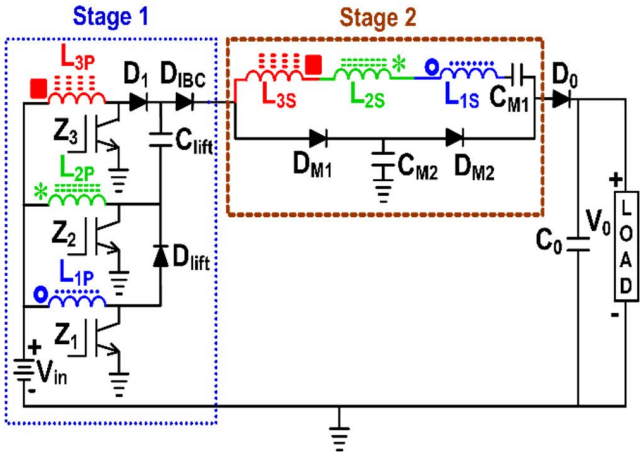


FIGURE 2. Circuit diagram of the proposed HGHP converter.

D_{M1}, D_{M2}, C_{M1} and C_{M2} to extend the voltage gain of the proposed HGHP. Diode D_0 and C_0 act as the conventional boost rectifier diode and the output capacitor. The operating principle is detailed subsequently.

III. OPERATING PRINCIPLE

The working principle of the proposed HGHP converter is elaborated based on the following valid assumptions: (i) all the semiconductor devices are ideal, (ii) the proposed HGHP converter operates in continuous conduction mode (CCM) and (iii) all the three switches Z_1, Z_2 and Z_3 are turned ON for a brief time interval to initially charge the primary inductors L_{1P}, L_{2P} and L_{3P}. The operation of the proposed HGHP converter is explained using six modes in one switching cycle. Figs. 3(a)-(f) show the equivalent circuit of the proposed converter in each mode.

A. MODE 1: $(t_0 - t_1)$

At t_0, switch Z_1 is turned OFF and the switches Z_2 and Z_3 are maintained in ON state. Consequently, the current flowing through the primary winding L_{1P} starts to linearly decrease. The energy stored in L_{1P} is transferred to C_{Lift} and Stage 2 through D_{Lift} and D_{IBC}. Current through D_{lift} is same as the current through L_{1P} and is represented by (1).

$$i_{L_{1P}} = i_{D_{lift}}(t) = n\left(i_{D_{M1}}(t) + i_{C_{M2}}(t)\right) \tag{1}$$

The potential developed across C_{lift} forward biases diode D_{M1} and helps in charging the multiplier capacitor C_{M2}. When C_{M2} is completely charged, D_{M1} turns OFF. Energy stored in C_{M2} starts to be transferred to C_{M1} and the load through D_{M2} and D_0. Current through C_{M1} is given by

$$i_{C_{M1}}(t) = \frac{1}{n^2 L_{py}}\left(nV_{L_{1P}} - v_{C_{M1}}\right) \times t \tag{2}$$

where $L_{py} = L_{1P} + L_{2P} + L_{3P}$ and n is the turns ratio of CIs. Mode 1 ends when the current through L_{2P} reaches its maximum value $I_{L_{2P,\max}}$ at time $t = t_1$.

B. MODE 2: $(t_1 - t_2)$

In this mode, Z_2 is turned OFF while Z_1 and Z_3 are maintained in their respective OFF and ON states. The diode D_{lift} continues to remain in the forward biased condition.

Since Z_2 is turned OFF, the stored energy in L_{2P} is also transferred to C_{Lift} and Stage 2 through C_{lift} and D_{IBC}. As Z_3 is conducting, D_1 remains in the reverse biased state. The current flowing through Z_3 is expressed as

$$i_{L_{3P}} = i_{Z_3}(t) = n\left(i_{C_{M1}}(t) + i_{D_{M1}}(t)\right) \tag{3}$$

In Stage 2, diode D_{M1} is forward biased and enables C_{M2} to charge to its maximum value. As Z_1 is OFF, the energy stored in L_{1P} continues to be transferred to the rest of the circuit (as mentioned in Mode 1) till its current reaches the minimum value$I_{L_{1P,\min}}$ and marks the end of Mode 2 at time $t = t_2$. At the end of Mode 2, using volt-second balance concept, the voltage across C_{lift} is derived and given by (4).

$$V_{C_{lift}}{}^{(i)} = \frac{1}{1-D}V_{in} \tag{4}$$

where D is the duty ratio at which the switches are operated.

C. MODE 3: $(t_2 - t_3)$

Mode 3 starts at t_2 when Z_1 is turned ON while switches Z_2 and Z_3 are maintained in their OFF and ON states respectively. The diodes D_{lift} and D_1 are reverse biased due to the operating states of the switches. Since Z_2 is OFF, current through L_{2P} continues to decrease while the current through energy stored in L_{1P} and L_{3P} increases. In Stage 2, the energy stored in C_{M2} is transferred to C_{M1} and the load through D_{M2} and D_0. Current through C_{M2} is expressed through (5).

$$i_{C_{M2}}(t) = \frac{V_0 - (V_{C_1} + nV_{L_{1P}} + V_{C_{M2}})}{n^2 L_{py}} \times t \tag{5}$$

Mode 3 ends when the current through L_{3P} reaches its maximum value $I_{L_{3P,\max}}$ at time $t = t_3$.

D. MODE 4: $(t_3 - t_4)$

Mode commences when Z_3 is turned OFF to enable the energy transfer process of L_{3P}. Diodes D_1 and D_{IBC} are forward biased and participate in the energy transfer process. Switches Z_1 and Z_2 are retained in their ON and OFF states respectively. Hence, diode D_{lift} is in reverse biased condition. Current through Z_1 is given by

$$i_{Z_1}(t) = ni_{D_0}(t) = \frac{V_0 - (V_{C_1} + nV_{L_{1P}} + V_{C_{M2}})}{n^2 L_{py}} \times t \tag{6}$$

In Stage 2, after C_{M2} is fully charged, its stored energy is transferred to C_{M1} through D_{M2}. Mode 3 comes to an end at time $t = t_4$ when current through L_{2P} reaches its minimum value $I_{L_{2P,\min}}$.

At the instant t_4, voltage across C_{lift} is obtained from basic principles and given by (7).

$$V_{C_{lift}}{}^{(ii)} = \frac{2}{1-D}V_{in} \tag{7}$$

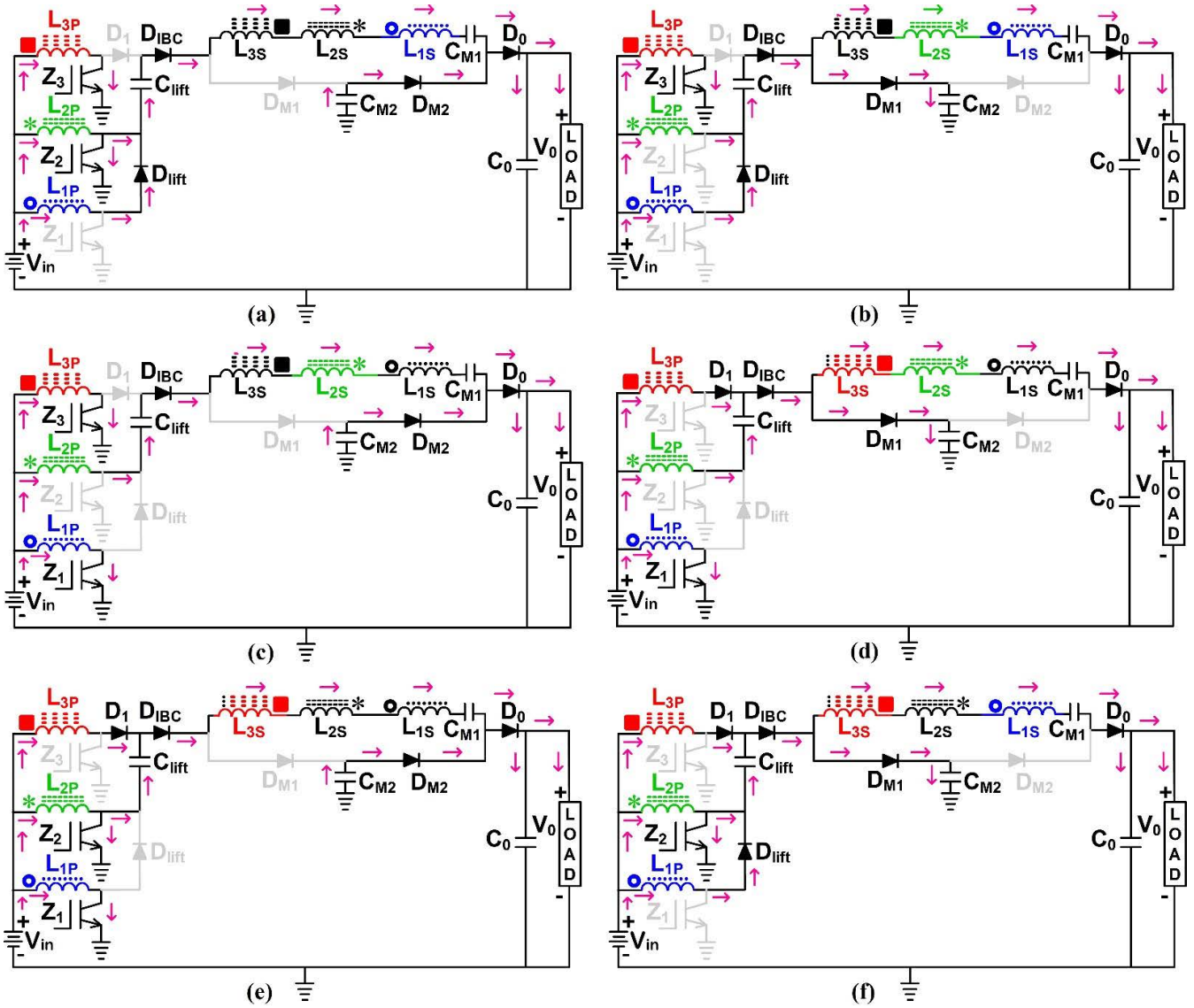


FIGURE 3. Equivalent circuit of the proposed HGHP converter during various operating modes (a) Mode 1 ($t_0 - t_1$), (b) Mode 2 ($t_1 - t_2$), (c) Mode 3 ($t_2 - t_3$), (d) Mode 4 ($t_3 - t_4$), (e) Mode 5 ($t_4 - t_5$) and (f) Mode 6 ($t_5 - t_6$). In Modes 2, 4 and 6, charging of CM2 is shown for additional clarity.

E. MODE 5: ($t_4 - t_5$)

At the beginning of Mode 5, Z_2 is turned ON while Z_1 and Z_3 are maintained in ON and OFF states respectively. Consequently, current through L_{1P} and L_{2P} raises linearly while the stored energy in L_{3P} is transferred to Stage 2. In the multiplier network, C_{M2} charges for some time and discharges its stored energy to C_{M1} and the load. Current through L_{2P} is given by

$$i_{L_{2P}}(t) = i_{Z_1}(t) + i_{C_{lift}}(t) \tag{8}$$

At time t = t_5, the current through L_{1P} reaches its maximum value and marks the end of Mode 3.

F. MODE 6: ($t_5 - t_6$)

Mode 6 begins at the instant t_5 when Z_1 is turned OFF. The other two switches Z_2 and Z_3 are maintained in their respective ON and OFF states. Primary winding L_{2P} continues to store energy while L_{1P} and L_{3P} transfer their stored energies to Stage 2 and load through the diodes D_1, D_{IBC} and D_0. Capacitor C_{M2} starts charging through D_{M1} and transfers its stored energy to C_{M1} as soon as it is completely charged. Mode 6 ends at time t= t_6 when the current through L_{3P} reaches its minimum value. The current through D_0 is given by (9).

$$i_{D_0}(t) = \frac{3V_{in} + V_{C_{M2}}(1-D) - V_0(1-D)}{n^2 L_{py}(1-D)} \times t \tag{9}$$

At the time instant t = t_6, C_{lift} is completely charged to a value which is given by (10) based on the basic principles.

$$V_{C_{lift}}{}^{(iii)} = \frac{3}{1-D} V_{in} \tag{10}$$

At the end of Mode 6, one switching cycle is complete and next cycle commences when the switch Z_3 is gated ON again.

Fig. 4 shows the characteristic waveforms of the proposed HGHP converter.

IV. STEADY-STATE ANALYSIS AND DESIGN DETAILS

In this section, the voltage gain of the proposed converter and other design equations are derived from basic principles.

A. STEADY-STATE ANALYSIS AND DESIGN DETAILS

All the components of the proposed converter participate in stepping up V_{in}. The magnitude of voltage gain obtained from Stage 1is given by (11).

$$M_{Stage\ 1} = \frac{V_{Stage\ 1}}{V_{in}} = \frac{3}{1-D} \tag{11}$$

Voltage gain obtained from Stage 1 is extended in Stage 2 by the secondary windings of CIs and the VMC network. Based on the connection of the secondary windings, Stage 2 voltage gain is given by (12).

$$M_{Stage\ 2} = \frac{V_{Stage\ 2}}{V_{in}} = \frac{2n}{1-D} \tag{12}$$

where n is the turns ratio of CIs.

By summing up (11) and (12), total ideal voltage gain (M) of the proposed HGHP converter is obtained and given by (13).

$$M = \frac{V_0}{V_{in}} = \frac{3+2n}{1-D} \tag{13}$$

Practically, as the CIs are subjected to leakages, by considering 'k' as the average value of coupling coefficient of 3 CIs, the expression for realistic voltage gain is given by

$$M = \frac{V_0}{V_{in}} = \frac{3+2nk}{1-D} \tag{14}$$

B. VOLTAGE STRESS ON POWER SWITCHES AND DIODES

Voltage stress experienced by the power switches Z_1 and Z_2 is equal to the potential across C_{lift}. Therefore, voltage stress impressed across them is given by (15).

$$V_{Z_1} = V_{Z_2} = \frac{V_0}{1+\frac{2}{3}nk} \tag{15}$$

Due to asymmetry caused by C_{lift}, Z_3 experiences a relatively lower voltage stress which is expressed by (16).

$$V_{Z_3} = \frac{V_0}{3+2nk} \tag{16}$$

When Z_1 conducts, D_{lift} is reverse biased while D_1 remains reverse biased when Z_3conducts. Therefore, D_1 blocks a voltage level obtained across Stage 1 given by (15) while voltage stress on D_{lift} is given by (16). From the operating principle, voltage stress on D_{M1}, D_{M2} and D_0 is given by (17) and (18).

$$V_{D_{M1}} = V_{C_{M2}} - \frac{V_0}{1+\frac{2}{3}nk} \tag{17}$$

$$V_{D_{M2}} = V_{D_0} = V_0 - V_{C_{M2}} \tag{18}$$

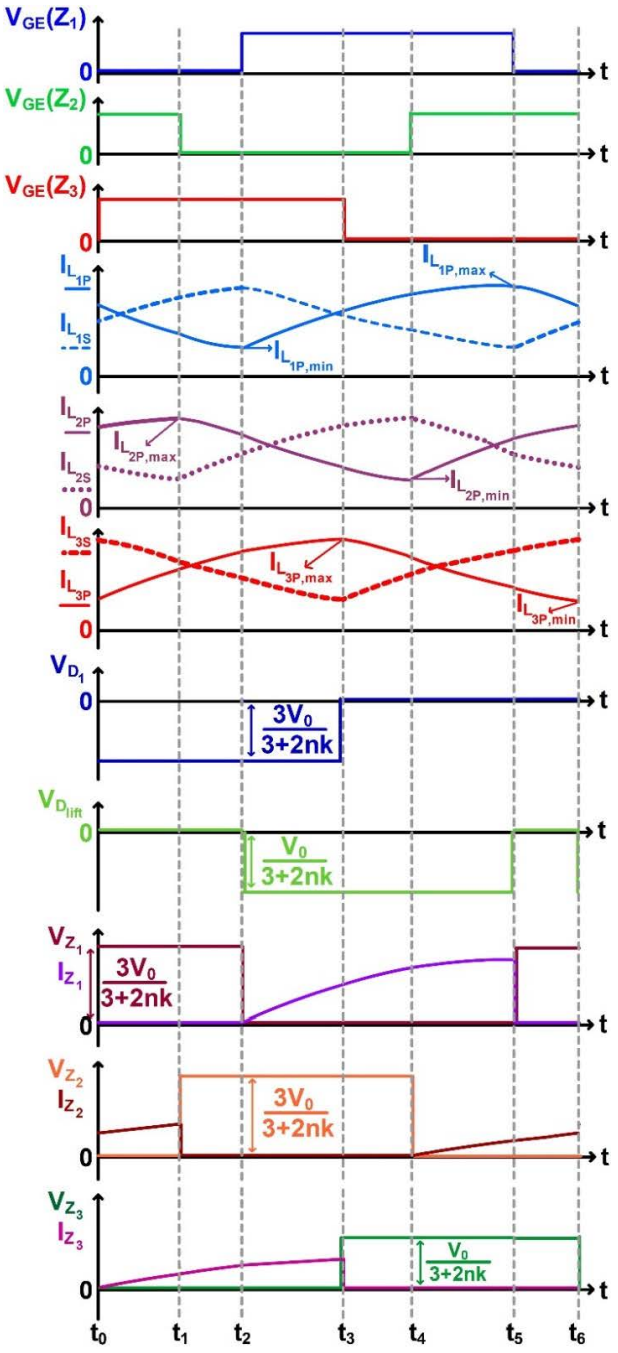


FIGURE 4. Characteristic waveform of the proposed HGHP converter.

The voltage stress on the semiconductor devices is inversely proportional to n and k of the CIs. Therefore, to minimize the voltage stress across the switches and diodes, a careful choice of n is essential. In addition, the CIs are tightly wound to ensure that the value of k is closer to 1 and voltage stress on the semiconductor devices is reduced. The practical value of k is determined to be 0.88. Fig. 5 shows the operating point of the proposed HGHP converter. By operating the switches at $D = 0.55$ and using CIs with $n = 3$, the required voltage gain is obtained when $k = 0.88$.

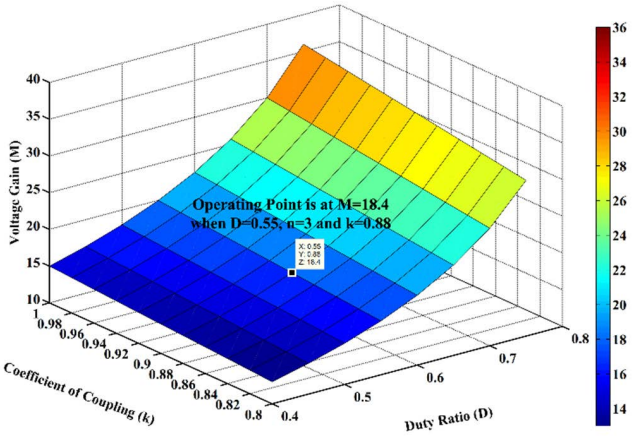


FIGURE 5. Plot of variation in voltage gain (M) versus duty ratio (D) for various values of k when turns ratio n=3 and the operating point.

C. CURRENT STRESS ON POWER SWITCHES AND DIODES

From input-output power balance principle of an ideal power converter, the average input current (I_{in}) is derived as in (19).

$$I_{in} = \frac{3+2nk}{1-D} I_0 \tag{19}$$

Total input current is shared by the three interleaved phases present in the Stage 1. Current through Z_1 is greater than Z_2 and Z_3 due to the asymmetry in Stage 1 caused by C_{lift}. Current through Z_1 is given by (20). Switches Z_2 and Z_3 carry equal current given by (21).

$$I_{Z_1} = \frac{6+4nk}{3(1-D)} I_0 = \frac{2}{3} I_{in} \tag{20}$$

$$I_{Z_2} = I_{Z_3} = \frac{3+2nk}{6(1-D)} I_0 = \frac{1}{6} I_{in} \tag{21}$$

Correlating the conducting intervals of D_{lift}-Z_1 and D_1-Z_3 combinations, current through D_{lift} and D_1 is derived and given by (22) and (23).

$$I_{D_{lift}} = \frac{9+6nk}{5(1-D)} I_0 = \frac{3}{5} I_{in} \tag{22}$$

$$I_{D_1} = \frac{9+6nk}{20(1-D)} I_0 = \frac{3}{20} I_{in} \tag{23}$$

D. DESIGN OF CAPACITORS

The value of C_{M1}, C_{M2}, C_{lift} and C_0 depends on energy transferred through them individually and the voltage ripple across each capacitor. Therefore, the rating of each capacitor is obtained from (24) by substituting the voltage impressed across each capacitor and the individual ripple voltage.

$$C_x = \frac{P_x D}{V_x f_s \Delta v_x} \tag{24}$$

where x is the individual capacitors C_{M1}, C_{M2}, C_{lift} and C_0. From the operating principle and the location, the voltage rating of the capacitors is expressed through (25) – (27).

$$V_{C_{lift}} = \frac{3}{1-D} V_{in} \tag{25}$$

$$V_{C_{M1}} = \frac{nk}{1-D} V_{in} \tag{26}$$

$$V_{C_{M2}} = V_{C_0} = \frac{3+2nk}{1-D} V_{in} \tag{27}$$

E. DESIGN OF COUPLED INDUCTORS

Design of CIs is important as continuous input current with low ripple content is preferred for PV application. Considering the input current ripple (ΔI_{in}), appropriate value of primary inductance (L_{py}) is obtained and given by (28).

$$L_{py} = \frac{3DV_{in}}{f_s \Delta I_{in}} \tag{28}$$

Generally, tight coupling between the primary and secondary windings of the CIs is preferred and its practical coupling coefficient value ($k_{practical}$) is determined from (29).

$$k_{practical} = \sqrt{1 - \frac{L_S}{L_0}} \tag{29}$$

where L_0 and L_S are the inductance values measured across primary winding (of an individual CI) when secondary winding is open and short circuited respectively. In the proposed converter, average value is denoted as 'k'.

F. SELCTION OF TURNS-RATIO

Voltage gain of the converter is predominantly determined from the values of turns ratio (n) and duty ratio (D). The turns ratio of the converter is determined from (30).

$$n = \frac{V_0(1-D)}{2kV_{in}} - \frac{3}{2k} = \frac{M(1-D)-3}{2k} \tag{30}$$

To meet the high voltage gain requirement, increasing the turns-ratio increases the size of the CIs, whereas lesser value of n translates to operating the switches at larger duty ratio values. As sufficient energy needs to be stored across the CIs and transferred to the load, a nominal duty-ratio value of $D = 0.55$ is practically chosen for the proposed HGHP application. For the proposed converter, based on the specifications provided in Table 1, the value of n is computed as $n = 3$.

V. HARDWARE RESULTS AND DISCUSSION

Table 1 provides the converter specifications considered for simulation and experimentation. From (16), the inductor value of primary and secondary windings of CIs is determined to be 18μH and 162μH respectively. The individual multiplier and clamping capacitor (C_1, C_{M1}, C_{M2} and C_{lift}) values are chosen to be 4.7μF. The voltage ratings of the capacitors are chosen depending on their location in the power circuit. TMS320F28027 Piccolo digital signal processor (DSP) is used for generating the required gate pulses. A signal conditioning unit is employed to interface the gate pulses obtained from DSP and the SCALE driver boards (2AP043512) which are used for isolating and driving the power IGBTs. Tektronix TPS2024B digital storage oscilloscope (DSO) and standard accessories like P5210 high voltage probe and A622 current probes are used to capture the key waveforms.

Fig. 6 shows the waveforms obtained from the DSO and correspond to gate pulses applied to the power switches present in the designed converter and the voltage obtained across the output terminals. Gate pulses with a moderate duty ratio ($D = 0.55$) and 120° phase delay between the three interleaved legs provide the required output voltage which is in accordance with the value predicted using (14). The output voltage is fairly constant with negligible ripple content.

The practical voltage stress experienced by the switches Z_1 and Z_3 with respect to the output voltage is depicted through Figs. 7(a) and (b). The turn ON and turn OFF instants of the power switches are in perfect agreement with their respective gate pulses. Further, as majority of the gain extension occurs at Stage 2, the voltage stress magnitude of Z_1 and Z_3 is reduced and in close agreement with (15) and (16).

The voltage spikes impressed on the switches are due to the leakage inductance of the CIs. However, as most of the stored energy is recycled at Stage 2 through the elements present in VMC network, the magnitude of the spikes is much reduced and not alarming.

To replicate the dynamic performance of the HGHP converter when fed from a PV input, the voltage applied to the converter is varied from 48 V to 72 V (80% to 120% of the rated input voltage) while maintaining a constant load.

Fig. 8(a) illustrates the variations in the output voltage. The variation in output voltage is very less. From theoretical computations, the duty ratio variation is between 0.6386 and 0.458 to maintain a constant output voltage. At input voltage levels higher than the specified value, the efficiency is expected to be slightly higher due to marginally lower input current magnitude which causes reduced losses.

To obtain the converter performance when load varies, results are obtained through simulation and experimentation. The output voltage variation of the proposed converter for 75%, 100% and 125% of full load with constant input voltage during experimentation is shown in Fig. 8(b). The output voltage is fairly constant under over-load conditions mainly due to the energy storage elements which act as energy buffer during load variations. During light load condition, due to marginal higher voltage level obtained at Stage 1 and Stage 2, the output voltage also slightly increases.

To appreciate the ripple free input current behaviour, simulated waveforms for current through primary windings of the CIs L_{1P}, L_{2P}, L_{3P} and the total input current are shown in Fig. 9(a). Obviously, due to interleaving technique, the total input current is shared among the three interleaved phases.

Further, since voltage lift technique is employed, the current through the three primary windings of the CIs are slightly non-uniform; asymmetry is caused due to the introduction of C_{lift} between the interleaved phases of Stage 1 in the proposed HGHP converter. By properly designing the CIs, the rise and fall of current through the CI primary windings is ensured while maintaining continuous conduction mode. Additionally, due to the interleaving technique being employed in Stage 1, the input current waveform contains very low ripple.

TABLE 1. Specifications of the proposed HGHP converter.

Parameter	Value
input voltage (V_{in})	60 V
output voltage (v_o)	1.1 kV
output power (p_o)	3 kW
switching frequency (f)	100 kHz
duty ratio (d)	0.55
turns ratio (n)	3.0
coupling coefficient (k)	0.88
primary winding inductance (l_{1p}, l_{2p}, l_{3p})	18 µH
current rating of l_{1p}, l_{2p}, l_{3p} respectively	45 A, 15 A, 15 A
input current ripple (Δi_{in})	15% of I_{in}
output voltage ripple (Δv_0)	5% of V_0

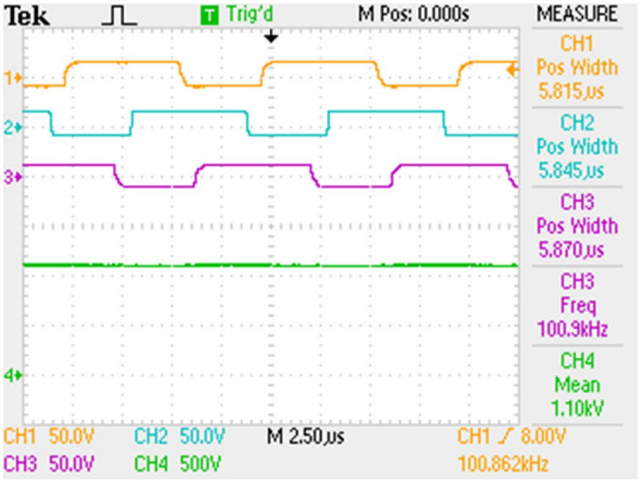
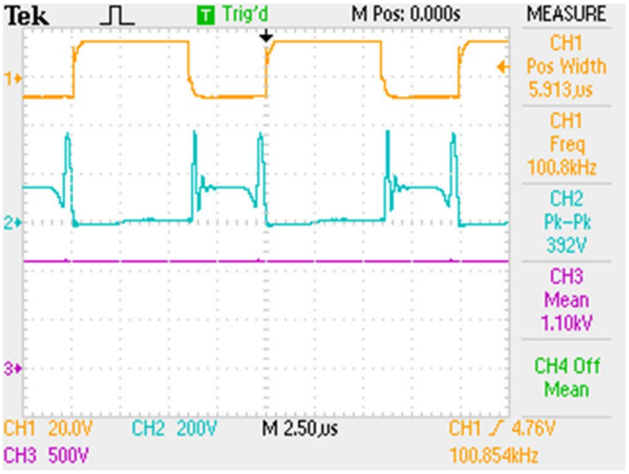


FIGURE 6. Oscilloscope waveforms to practically validate the voltage gain capability of the proposed HGHP converter; gate pulse applied to Z_1, Z_2, Z_3 (CH1, CH2, CH3) and V_0 (CH4).

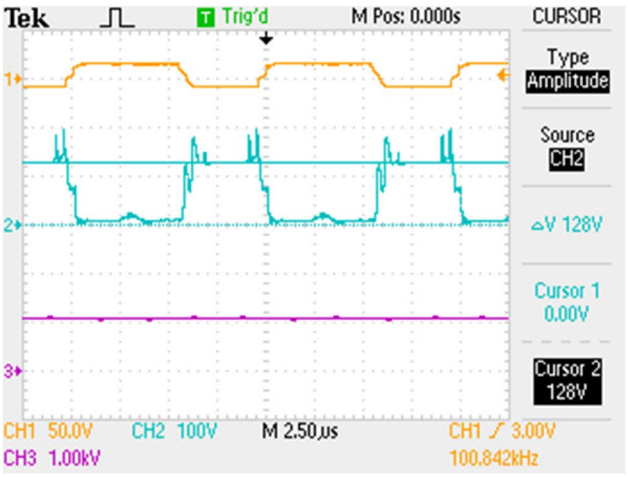
Fig. 9(b) shows the current stress on the power switches plotted along with total input current. The shape of the current through the power switches Z_1, Z_2 and Z_3 are in agreement with the current flowing through the respective primary windings. Since any two switches simultaneously conduct for a small duration of the duty cycle, the shape of the current waveforms slightly deviates from their respective inductor currents.

Because of the inherent current sharing mechanism due to interleaving, the individual switch current magnitude is much lesser when compared to the total input current magnitude. However, due to structural asymmetry, the current sharing is not uniform. Nevertheless, the current sharing pattern is in perfect agreement with (20) and (21) and does not affect the converter performance.

Fig. 10(a) shows the voltage and current waveforms captured at the input and output terminals when the converter delivers rated power (3 kW) to the load. Output voltage and the input current waveforms confirm the voltage gain and power handling ability of the proposed HGHP converter. Furthermore, the ripple magnitudes of I_{in} and V_0 are very low and confirm the design of passive elements. Fig. 10(b) show

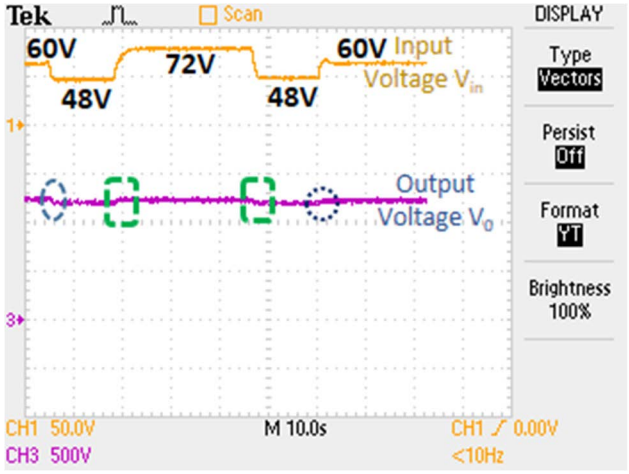


(a)

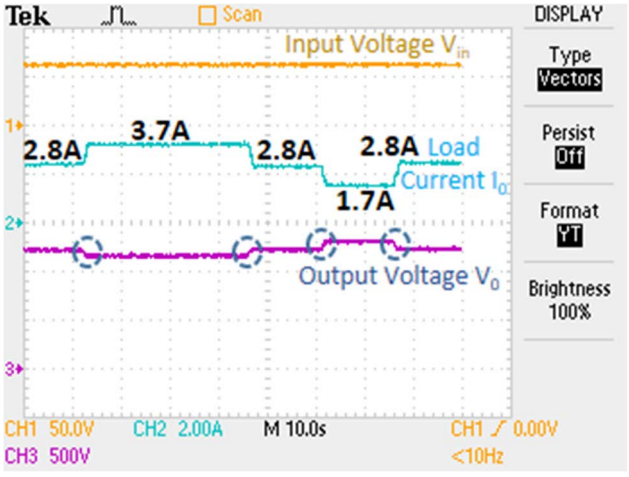


(b)

FIGURE 7. Experimental waveforms depicting the voltage stress on the switches employed in the proposed HGHP converter (a) Gate pulse applied to Z_1 (CH1), voltage stress on Z_1 (CH2) and output voltage (CH3), (b)Gate pulse provided to Z_3 (CH1), voltage stress on Z_3 (CH2) and output voltage (CH3).



(a)



(b)

FIGURE 8. Experimental results to study the dynamic performance of the proposed HGHP converter, (a) variation of output voltage when input voltage varies from 48V to 72V, (b) variation of output voltage when load varies from 75% to 125% of full load condition while maintaining a constant input voltage.

the output voltage and efficiency profiles under various load conditions during simulation and experimentation.

The converter operates at a maximum efficiency of 92.3% under rated load condition. The output voltage of the converter varies by 2.67% of rated value when the load is increased to 125% of the rated load. The total power loss occurring in the converter is estimated using the expressions presented in [26] and [40]. The power loss distribution profile of the proposed HGHP converter is developed and presented in Fig. 11.

Fig. 12 shows the top angle photograph of the experimented converter. Devices with SOT227 package are employed. Heat sinks are located at the back side of the board. The converter dimensions are 0.30 m × 0.22 m × 0.065 m (length × breadth × height). Table 2 provides the details of components that are used to fabricate and test the proposed converter. Fig. 13 shows the photograph of the experimental setup.

The suitability of the proposed HGHP converter to implement maximum power point tracking (MPPT) algorithm is demonstrated through Fig. 14. The variation in duty ratio is obtained using

$$D_{MPP} = 1 - (3 + 2nk)\sqrt{\frac{R_{Conv-MPP}}{R_L}} \tag{31}$$

where D_{MPP} is the duty ratio required to track maximum power point, $R_{Conv\text{-}MPP}$ is the equivalent resistance seen by the source at maximum power point and R_L is the load resistance.

When the solar irradiation undergoes variations, the input power available from the PV source also changes. Due to the implementation of MPPT algorithm, the output power

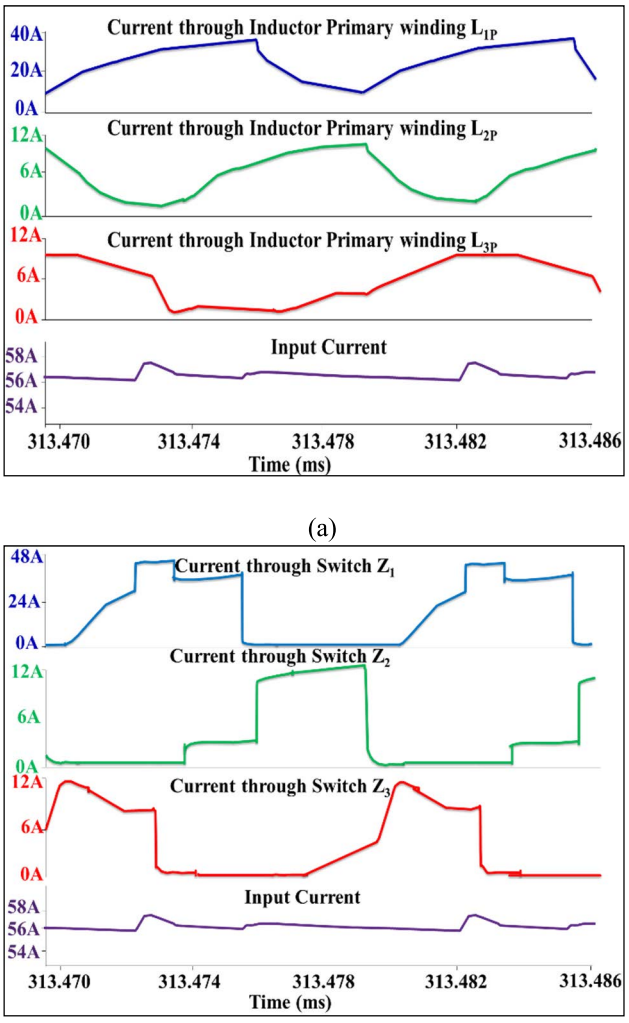


FIGURE 9. Simulated results demonstrating (a) current through L_{1P}, L_{2P}, L_{3P} and I_{in}, (b) current through Z_1, Z_2, Z_3 and I_{in}.

TABLE 2. Component details of the proposed HGHP converter.

Components used	Part Number (Key specifications)
switches Z_1, Z_2, Z_3	IXGN72N60C3H1 (600 V, 52 A, 2.5 V)
voltage lift diode D_{lift}	DSEP2x91-03A-ND (300 V, 90 A, 1.54 V)
diode D_1	DSEI2x101-12A (1.2 kV, 91 A, 1.87 V)
diodes D_{IBC}, D_0	DSS2x41-01A-ND (100 V, 40 A, 0.7 V)
Diodes D_{M1}, D_{M2}	MDD56-16N1B-ND (1.6 kV, 71 A, 1.14 V)
Capacitors C_{lift}, C_{M2}	FFB56L0475K (4.7 µF, 1.1 kV)
Capacitor C_{M1}	B32524Q3475K000 (4.7 µF, 250 V)
Output capacitor C_0	UNL15W4P7K-F (4.7 µF, 1.5 kV)
Heat Sinks	BDN18-6CB/A01

follows the input power variation. Thus, the proposed HGHP converter is capable of extracting maximum power from the input PV source and delivering the same to the load when irradiation varies.

By implementing a simple closed-loop control, the output voltage of the proposed HGHP converter is regulated.

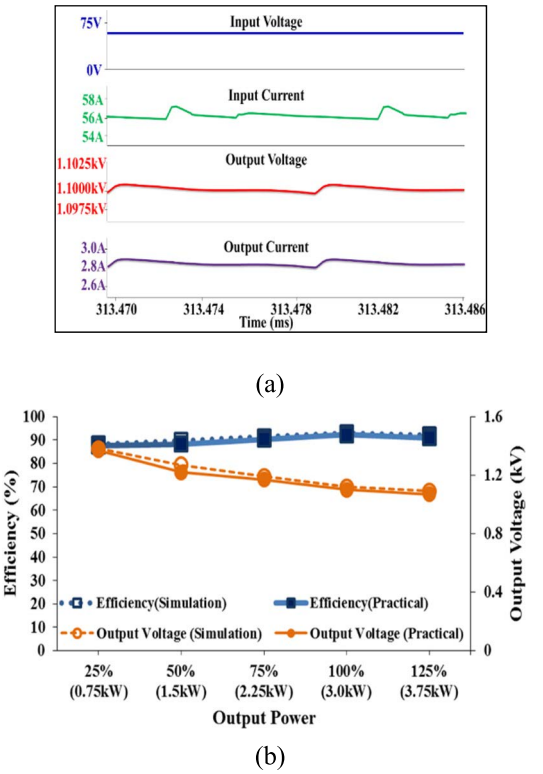


FIGURE 10. Efficiency characteristics of the proposed HGHP converter (a) simulation results to obtain the efficiency under full-load condition, (b) efficiency curve and output voltage variation under simulation and experimentation.

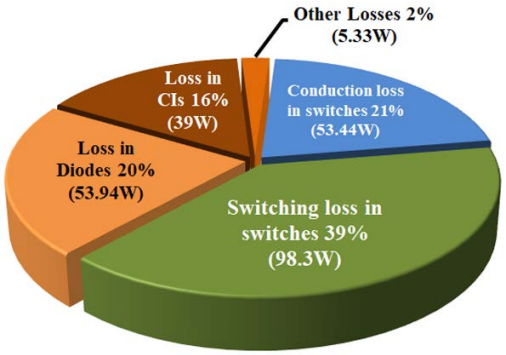


FIGURE 11. Loss distribution profile of the proposed HGHP converter.

Fig. 15 depicts the load regulation characteristics of the proposed HGHP converter. The proposed HGHP converter is capable of regulating the load voltage when the load current swings from the rated value of 2.8 A to a maximum value of 3.85 A.

VI. PERFORMANCE BENCHMARKING

To highlight the salient features of the proposed HGHP converter, some of its main attributes are benchmarked with few state-of-the art high gain converters. The comparison summary is presented in Table 3 and the salient features are elaborated.

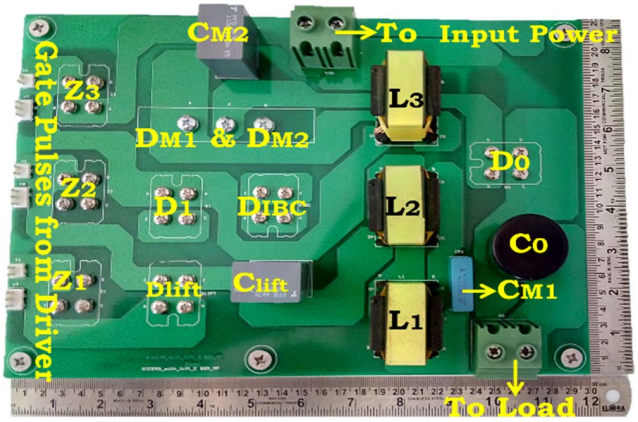


FIGURE 12. Photograph illustrating the top view of the experimented converter.

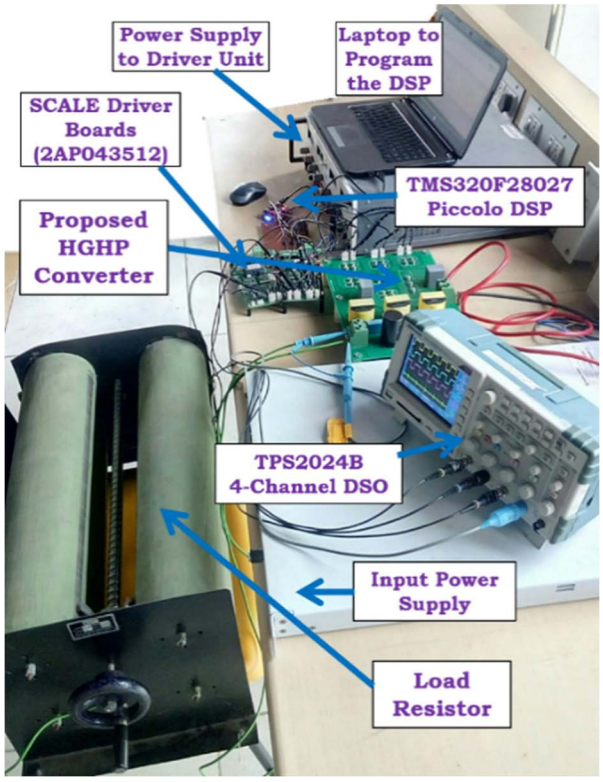


FIGURE 13. Photograph showing the experimental setup used to test the proposed HGHP converter.

A. VOLTAGE GAIN AND POWER LEVEL

All the converters considered for comparison provide a minimum voltage gain of 10 at safe duty ratio values except [27] in which the duty ratio is slightly higher at 0.742. However, their power delivering capabilities are significantly lower when compared to the proposed HGHP converter. The converter presented in [40] offers the second highest voltage gain value of 15.83. However, the converter's power rating is only 100 W. The converter described in [37] offers the lowest voltage gain value in the vicinity of 10 with low power handling capability.

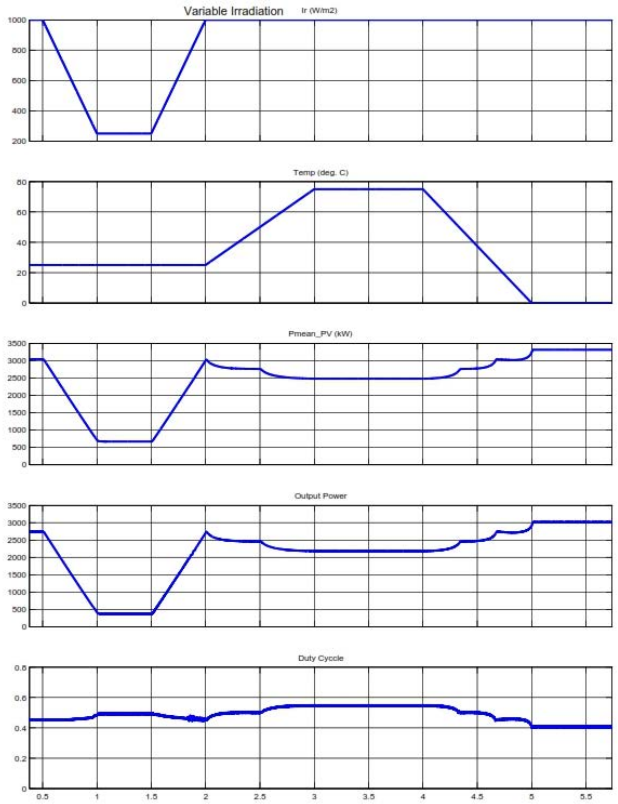


FIGURE 14. Behaviour of the proposed HGHP converter when MPPT is implemented.

The converter detailed in Andrade *et al.* [35] yields a good voltage gain of 13.33 at 200 W power level. The proposed HGHP converter yields the second highest voltage gain value of 18.33 at a significantly higher power level of 3 kW. The highest power level is mainly due to the employment of CI based three-phase IBC in Stage 1. In some of the other converters that are compared, despite using CIs, the technique employed for achieving high gain is responsible for their reduced power handling capability.

B. TOTAL COMPONENT COUNT (TCC) AND M/TCC

The converter discussed in [36] uses the maximum number of components (20) to obtain a voltage gain of 13.33 resulting in the second lowest *M*/TCC value of 0.66. The converter described in [27] uses only 10 components to yield a high voltage gain value of 12.5; its *M/TCC* value translates to 1.25. However, the switches are operated at a high duty ratio value of 0.742. The converter elaborated in [40] uses 14 components to offer a reasonably higher voltage gain value of 15.83 at a duty ratio value of 0.65. Hence, its *M/TCC* value translates to 1.13 which is the third highest among the converters that are compared. The converter detailed in [37] and the proposed HGHP converter use 16 components each. Despite using 4 magnetic elements, the converter in [37] offers only a voltage gain of 10.33 while the proposed HGHP converter yields the second highest voltage gain value of 18.33 by adopting only 3 CIs. The proposed HGHP converter

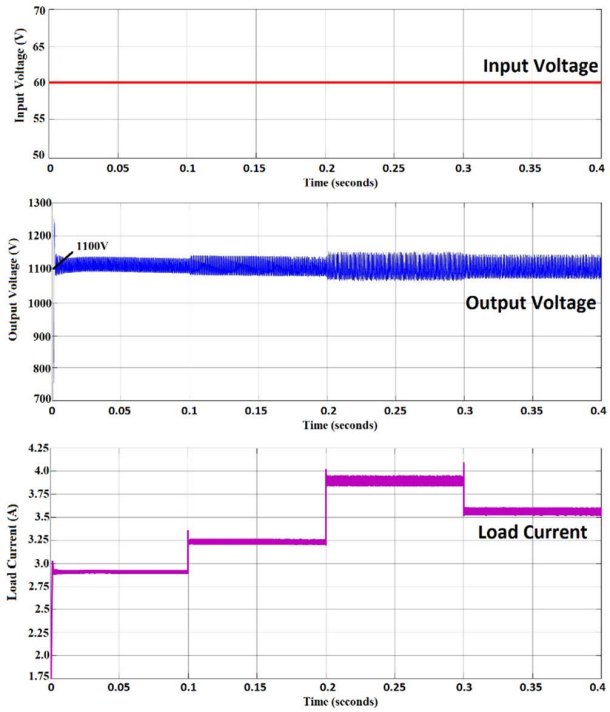


FIGURE 15. Load regulation characteristics of the proposed HGHP converter under closed-loop condition.

outshines the other converters when observed from the perspective of excellent power handling capability and *M*/*TCC* value.

C. VOLTAGE STRESS ON THE SWITCHES

Generally, low voltage stress on the switches is preferred for high voltage gain applications. The location of the switches and the techniques that are employed to achieve the required high voltage conversion ratio determine the voltage stress on the switches. Despite providing the second highest voltage gain value, the converter presented in [40] is subjected to the highest voltage stress value (50% of V_0) mainly due to the interleaved quadratic boost converter structure which is adopted.

The converter described in [37] provides a voltage gain of 10.33 only. The switches employed in the converter block the voltage developed across the charge-pump capacitors. Resultantly, the switches experience a high voltage stress (45% of V_0). For the converter presented in [27], the high voltage gain value is mainly due to the high duty ratio value. Consequently, the switches are subjected to a voltage stress which is close to one-third of V_0. The converter presented in [36] employs hybrid combinations of gain extension techniques. In the process, many components are employed and the switch is also judiciously located closer to the input. Resultantly, the switch is subjected to the least voltage stress value of just 15% of V_0. The proposed HGHP converter employs 3-phase IBC structure in Stage 1 and VMC based gain extension mechanism is adopted at the secondary side of the CIs. As majority of the voltage gain occurs at the secondary side, the switches are subjected to a reduced voltage stress level of about 36% of V_0.

D. CURRENT RIPPLE

Among the converters compared in Table 3, the converter discussed in [40] and the proposed converter employ interleaving mechanism. Resultantly, the input current ripple is low (12.9% and 15%) respectively. The converters described in [27], [36], and [37] rely only on the energy storage inductor

TABLE 3. Comparison of the proposed HGHP converter with some state-of-the art converters.

Attributes	Converters presented in references				Proposed HGHP Converter
	[27]	[36]	[37]	[40]	
Voltage gain (M)	12.5	13.33	10.33	15.83	18.33
Power rating (P_0) (kW)	0.2	0.2	0.3	0.1	3
Duty ratio (D)	0.742	0.51	0.58	0.65	0.55
No. of Magnetic components	3	2	4	2	3
Turns ratio CIs (n)	NA	2.11	NA	2.73	3
No. of switches	2	1	2	2	3
No. of diodes	2	8	4	6	6
Total component count (TCC)	10	20	16	14	16
M/TCC	1.25	0.66	0.64	1.13	1.145
Switch stress (% of V_0)	31	15.3	45.4	50	35.63
Current ripple (% of I_{in})	30	57.75	43	12.9	15
Efficiency (%)	93	94	94.3	92.49	92.3

TABLE 4. Comparison of the proposed HGHP converter with some CI based high gain converters.

Attributes	Converters presented in references				Proposed HGHP Converter
	[26]	[45]	[46]	[47]	
Voltage gain (M)	18.33	14.92	20	13.33	18.33
Power rating (P_0) (kW)	3	0.216	0.4	1	3
Magnetic components	3 CI	1 - 3 winding CI	2 - 3 winding CI	2 dual CI	3 CI
Turns ratio CIs (n)	2	2,1	1	1.33	3
TCC	24	12	14	11	16
M/TCC	0.76	1.24	1.42	1.2	1.145
P_o/M	0.163	0.014	0.02	0.075	0.163
P_o/TCC	0.125	0.018	0.028	0.091	0.187
Switch stress (% of V_0)	36	14	12.5	25	35.63
Current ripple (% of I_{in})	10	36.3	15	20	15
Efficiency (%)	92.6	94	94.05	93.6	92.3

which is located at the input side for reducing the ripple current. Consequently, depending on the duty ratio values, the ripple current magnitudes are also higher. In fact, in [36], the converter operates in discontinuous conduction mode (DCM) for some duration.

E. EFFICIENCY

All the converters compared in Table 3 operate at good efficiency values ranging from 92.3% to 94.3%. In fact, the efficiency values of all the converters are very close to each other. Since the voltage stress across the switches employed in all the converters compared in Table 3 is only about one-third of the output voltage, the converters are capable of operating at reasonably good efficiency values. Nevertheless, considering the voltage gain and power handling capability, the efficiency value of the proposed HGHP converter is appreciable.

VII. CI BASED CONVERTERS VERSUS THE PROPOSED HGHP CONVERTER

The power rating of the converters compared in Table 3 are very low compared to the proposed HGHP converter. In order to ensure a fairer comparison and justify the superior features of the proposed HGHP converter, some CI based high gain converters which yield a minimum voltage gain of 13 are compared. Table 4 summarizes the attributes that are compared.

Generally, in non-isolated high gain DC-DC converters, higher voltage gain is achieved by using (i) coupled inductors with appropriate turns ratio and (ii) higher number of passive components. All the converters that are compared utilize one or more coupled inductors. The converter presented in [47] employs two dual CIs; no gain extension cells are included. Since the converter uses only 11 components and CI with $n = 1.33$, its M/TCC is slightly greater than the proposed HGHP converter. However, its P_0/M and P_0/TCC are lesser than the proposed HGHP converter despite operating at 1 kW power level.

The converter described in [46] uses two three winding coupled inductors in their topology to achieve an excellent voltage gain value of 20. The converter has few advantageous features like (i) unity turns ratio, (ii) less component count (14) and (iii) low voltage stress on the switches. However, owing to its low power handling capability of 400 W, its P_0/M and P_0/TCC ratios are very less compared to proposed converter.

The converter presented in [45] offers a good voltage gain of 14.92 using only 12 components with the least voltage stress on the switch. However, due to the lower power rating of about 216W, the P_0/M and P_0/TCC ratios of the converter becomes negligible.

Both the proposed HGHP converter and the one presented in [26] offer the same voltage gain and operate at the same power levels; their P_0/M ratio values are the highest and equal to 0.163. However, in [26], to achieve a high voltage gain and higher power handling capacity, combination of CIs and voltage extension cells are employed. Consequently, the TCC value is the highest in [26] which results in a relatively lower M/TCC and P_0/TCC ratio values as compared to the proposed HGHP converter.

The switches of all the converters compared in Table 4 are subjected to a low voltage stress value only. Significantly, the switches employed in [45] and [46] suffer from the least and second least voltage stress values; the use of voltage gain extension mechanism and the power levels result in low voltage stress values. The converters employed in [45] and [47] use only the energy storage inductors for limiting the input current ripple. The other converters compared in Table 4 use interleaving technique which results in reducing the input current ripple to a large extent. Since all the converters employ switches which are subjected to reduced voltage stress levels, the efficiency values of all the converters are very close to

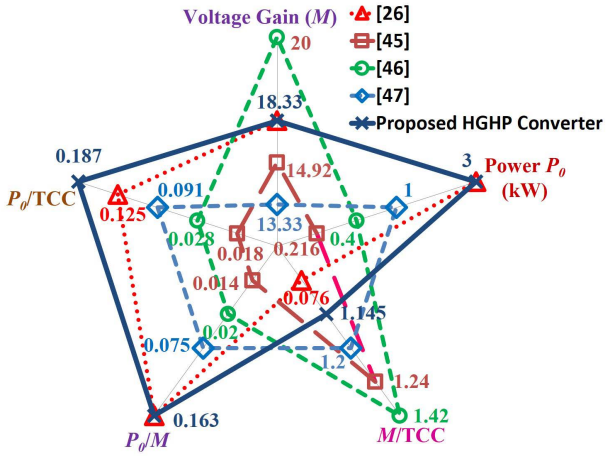


FIGURE 16. Radial chart to demonstrate the superior features of the proposed HGHP when compared to some state-of-the art converters.

each other and vary within a narrow range from 92.3% to 94.05%. Fig. 16 provides a graphical illustration of the some of the salient features of the proposed HGHP converter and some CI based state-of-the art high gain converters.

In the proposed HGHP converter, though the component count is on the higher side, CIs with appropriate turns ratio are employed to handle a reasonably large power (3kW) output. Moreover, the switches are also subjected to reduced voltage stress levels only. Hence, the proposed HGHP converter is more advantageous for deployment in sustainable energy applications as compared to the other converters.

VIII. CONCLUSION

In this paper, the key role of power electronic converters in some solar PV fed DC microgrid applications was highlighted. A high-gain high-power DC-DC converter was selected, synthesised, designed and practically tested considering a 1.1 kV DC distribution line. The proposed converter was tested from a 60 V DC input and yielded 1.1 kV to 3 kW load at 92.3% efficiency. A high voltage conversion ratio of 18.33 at high power level of 3 kW was practically realized. The high voltage gain with higher power handling ability was achieved by hybrid combination of interleaved structure which used coupled inductors, voltage lift capacitor and VMC network. The power switches and diodes experienced lower current and voltage stress due to interleaving and the type of voltage gain extension techniques adopted. The maximum voltage and current stress levels were just 36% and 33% of the output voltage and input current respectively. Due to the gain extension achieved by the CIs and VMC network, the stored energy in the leakage inductance was partially recycled and this resulted in reducing the voltage stress on the semiconductor devices. Due to interleaving technique, the input current ripple was only 15% of the total current magnitude. Experimental results obtained under dynamic conditions at the input and output side prove the versatility of the developed converter. The desirable and salient features of this converter prove to be a good candidate topology for DC microgrid and renewable energy applications.

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