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RESEARCH ARTICLE

Analyzing the Characteristics of Faults in a Transmission Line and High Voltage Capacitor Banks in a 115-kV-Power System Using Discrete Wavelet Transform

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ABSTRACT The protection of conventional high voltage capacitor banks relies on an unbalance relay. However, investigating the faults requires time and human resources. To address this issue, the characteristics of system parameters were analysed in this study by performing simulations using the power systems computer-aided design software. The simulations were modelled based on a 115-kV-system of the Electricity Generating Authority of Thailand. The case studies involved faults in the transmission line, a single capacitor bank, and a back-to-back connected capacitor bank. Additionally, the influence of other factors on the system parameters was investigated, including the varying fault phase, location, and inception angles. Moreover, the discrete wavelet transform (DWT) was applied to analyse the system parameters comprehensively. The results indicate that the characteristics of system parameters in the case of faults occurring in a transmission line are unique when compared to those in the case of faults occurring in a capacitor bank. Furthermore, the discrepancy between the system parameters in the case of faults occurring in a single capacitor bank and two capacitor banks connected in a back-to-back topology was solved by applying DWT. Therefore, the study findings can aid in improving the efficiency of power systems and ensure their protection.

INDEX TERMS Discrete wavelet transforms, high voltage capacitor bank, fault location, power system transients, transmission lines.

I. INTRODUCTION

The increasing demand for electrical power required the expansion of power system networks to provide sufficient power to all areas. The expanding network transferred the electrical power from one substation to others via transmission lines. Consequently, the increasing number of substations rendered the protection of power systems complex. Additionally, the power quality was a major concern during electrical power transmission. Therefore, a high voltage capacitor bank was installed in substations to improve the power quality.

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Typically, a capacitor bank is protected by an unbalance relay and operated based on an unbalanced current detected at an unbalance detection point installed on the neutral line of the capacitor. The neutral current is nearly zero when the system is operated under normal conditions. Therefore, the value recorded by the unbalance detection point is close to zero when a high voltage capacitor bank is operated normally. However, the capacitance of the faulty capacitor unit decreases when a fault occurs within the high voltage capacitor bank, which in turn increases the unbalanced current. If the fault is not eliminated efficiently by the unbalance relay, other related equipment may be damaged, reducing the reliability of the power system.

According to the unbalance relay data recorded from 2016 to 2019 by the Electricity Generating Authority of

Thailand (EGAT), the unbalance relay located at 115 kV is tripped most frequently [1], [2]. Fig. 1 depicts the tripped data recorded in 2020, wherein unbalance relays installed in 115-kV-substations tripped frequently; such events were recorded 81 times. As the unbalance relay can operate in 'alarm' or 'trip' mode without determining the cause of the fault, maintenance workers should manually identify the cause of the unbalance relay being tripped. The results of manual investigations indicate that only 31% of the tripped events were caused by the fault occurring at the capacitor unit. Furthermore, 25% of the tripped events were attributed to the fault occurring in other parts of the power system without the capacitor bank, and 44% of the events remained to be verified.

Based on the maintenance process, the workers identified two procedures for determining the cause of the fault: (1) a visual inspection to observe the structure and insulation of the high voltage capacitor bank, and (2) verifying the fault phase by measuring the impedance per phase and comparing it with that from a previous annual audit. The fault in the capacitor bank was confirmed when the comparison of the impedance per phase was higher than 1%. By contrast, when the comparison of the impedance was lower than 1%, the capacitor unit was not identified as the source of the fault, and the unbalance relay was considered to trip owing to the occurrence of faults in other parts. The tripped unbalance relays negatively affect the power system in terms of reliability. Moreover, the absence of capacitor banks results in poor power quality. In terms of the economy, the organisation wastes wages and human resources to investigate unnecessary incidents. Therefore, improving the unbalance relay and identifying the accurate causes of faults can ensure that the power systems are well-protected.

the voltage and current, to detect faults in the transformer. Similarly, the current [5], [6], [7] was effectively diagnosed when faults occurred in the synchronous motor and distribution system. The investigation of a fault occurring in transmission systems focused on both fault classification and location identification using the aforementioned fundamental factors. The methods commonly used to locate a fault involve the application of the travelling wave [7] and wavelet transform [8], [9], [10], [11], [12].

Although studies have successfully classified and identified faults in various parts of the power system, faults occurring in high voltage capacitor banks are not investigated sufficiently. This is because capacitor banks in a power system occupy a smaller portion of the total power system compared to other equipment. Nevertheless, studies on capacitor banks have predominantly focused on the influence of inrush current and its limitations [13], [14], [15], [16], [17], which can improve the power system design by determining the optimum location and size of capacitor banks [18], [19], [20].

To summarise the existing research [21], [22], the characteristics of fundamental system parameters in transient and recovery states were effectively analysed to verify the occurrence of faults. Additionally, applying the parameter of neutral and mathematic techniques to analyse the fault enhanced the process of fault detection [23], [24], [25]. However, case studies failed to focus on all sections of the power system where faults can occur.

To further analyse the faults occurring in capacitor banks and solve the problem of EGAT in terms of trips caused by the error in the unbalance relay, this study investigated the characteristics of system parameters during fault occurrence using the neutral current unbalance protection method [26]. Three scenarios of fault occurrence, namely the faults in a transmission line, a single capacitor bank, and two capacitor banks (back-to-back connection) were used for the case study, which was simulated using the power systems computer-aided design (PSCAD) program. The objective of this study is to distinguish the cause of the fault based on the unique features of system parameters when the fault occurs. The discrete wavelet transform (DWT) was applied for improved analytical efficiency.

The highlights of the proposed method can be summarised as follows:

- The system simulated in the PSCAD program was based on the actual system of EGAT.
- Unlike existing studies [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], the case study analysed faults occurring in both the transmission section and substation equipment (capacitor bank).
- The signals were observed considering both fundamental system parameters and mathematical techniques (DWT).
- The unique feature of considering a single capacitor bank and back-to-back connected capacitor banks for fault detection addresses the drawbacks of existing

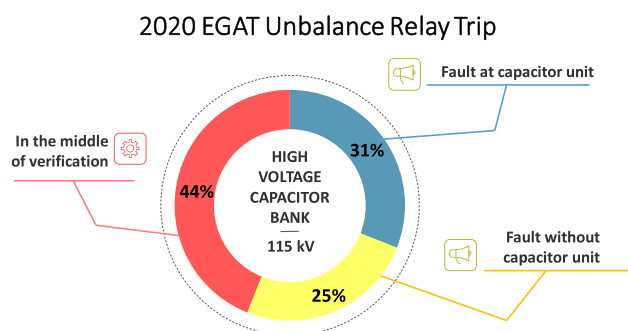


FIGURE 1. Maintenance processes to address an unbalance relay trip event, as recorded by the electricity generating authority of Thailand (EGAT).

Existing studies [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26] that focus on fault scenarios determined that faults occur in several parts of the power system. Several techniques have been proposed to detect the part of the power system where the fault occurs. Certain studies [3], [4] used leakage fluxes based on fundamental factors, namely

research [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26].

The remainder of this paper is organised as follows. Section II explains the PSCAD system developed based on EGAT. The simulation results are presented in Section III, and the influence of various factors on the system parameters is described in Section IV. Sections V and VI present the DWT analysis and discussion of the results, respectively. Finally, the conclusions of the study are summarised in Section VII.

II. POWER SYSTEM SIMULATION

The developed system is based on the high voltage capacitor bank of EGAT, which is a 48 Mvar capacitor bank installed in a back-to-back topology on a 115-kV main and transfer buses (Fig. 2(a)). Typically, a capacitor bank installed in a substation comprises capacitor units connected in a double-wye unground manner, whereas the inside of a capacitor unit comprises capacitor elements with fuses. The 48 Mvar capacitor bank in this study is double-wye ungrounded with capacitor elements connected in the internal fuse, as depicted in Fig. 2(b). As nine capacitor elements are connected with fuses, 0–9 internal fuses may be blown; here, 0 indicates that no fuses were blown, facilitating the normal operation of the system. The behaviours of these system parameters follow the IEEE Standard C37.99-2012 [26]; Table 1 lists the values of the parameters.

The parameters listed in Table 1 indicate that the number of fuses blown significantly impacts the current phase (I_{ph}) and capacitance of the capacitor unit (C_u). The capacitance continues to decrease as the number of blown fuses increases. This reduction in capacitance directly reduces the current phase. Typically, the capacitor bank is protected by an unbalance relay, which trips when the unbalance current exceeds 150 mA or the voltage element (V_e) is greater than 150% of the rated voltage according to the conventional EGAT protection standard. Considering the EGAT standard along with the system parameters (Table 1), the voltage of the affected element (V_e) was greater than 150% of the rated voltage when four internal fuses were blown. Therefore, the fault condition used in this study is based on the presence of four blown internal fuses and a reduction in the capacitance of a faulty unit from 26.743 μF (healthy unit) to 22.286 μF (faulty unit).

Fig. 2(c) depicts the system that was simulated in PSCAD, based on the system illustrated in Fig. 2(a). As the unbalance detection point was replaced by a current meter, the difference unbalance current (I_{ub}) used in the operation of a conventional relay was recorded by this detection point.

According to the PSCAD system (Fig. 2(c)), three fault scenarios were observed in this study.

- 1) Fault in capacitor bank No. 1 (CAP1);
- 2) Fault in both capacitor banks (CAP1 and CAP2); and
- 3) Fault in the transmission line.

TABLE 1. Fundamental system parameters.

Internal fuse blown	V_e (kV)	C_u (μF)	I_{ph} (A)	I_{ub} (A)
0	69.001	26.743	223.250	0.000
1	76.334	25.933	223.136	0.086
2	85.411	24.960	222.994	0.192
3	96.914	23.772	222.814	0.327
4	112.062	22.286	222.579	0.504
5	132.755	20.376	222.256	0.746
6	162.888	17.829	221.786	1.098
7	210.661	14.263	221.041	1.657
8	298.085	8.914	219.678	2.679
9	509.547	0.000	0.969	0.023

The characteristics of the current phase (I_{ph}), current phase of the capacitor bank (I_{cap}), and difference unbalance current (I_{ub}) were analysed.

III. SIMULATION

This section explains the characteristics of the system parameters considered in this study. The developed system (Fig. 2) was operated by switching capacitor bank Nos. 1 and 2 at 0.15 and 0.2 s, respectively. The characteristics of I_{ph} , I_{cap} , and I_{ub} were analysed in three scenarios of fault occurrence.

Under normal conditions, the current phase increased abruptly when capacitor bank No. 1 switched in the system. The current phase continued to increase owing to the influence of the switching of capacitor bank No. 2. However, the current phase remained constant as it converged to a stable state, as depicted in Fig. 3(a).

Fig. 3(b) and 3(c) indicate that the current phase of capacitor bank No. 1 increases abruptly when the capacitor bank is energised, which is referred to as ‘inrush current’. The inrush current can be reduced by connecting other capacitor banks in the system (back-to-back connection). Consequently, the current phase of capacitor bank No. 2 increased smoothly, without any current spike. Moreover, the inrush current of capacitor bank No. 1 caused by the switching of capacitor bank No. 2 was reduced.

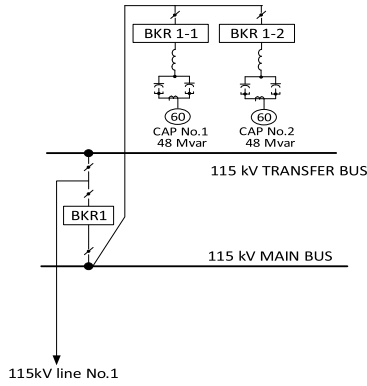
Although the current phase spiked when the capacitor bank was energised, the current phase was balanced in the stable state. Therefore, the values of difference unbalance current (I_{ub}) detected by capacitor bank Nos. 1 and 2 were approximately zero, as depicted in Figs. 4(a) and 4(b), respectively.

The analysis of these characteristics was followed by the investigation of the influence of the fault occurrence on the aforementioned system parameters.

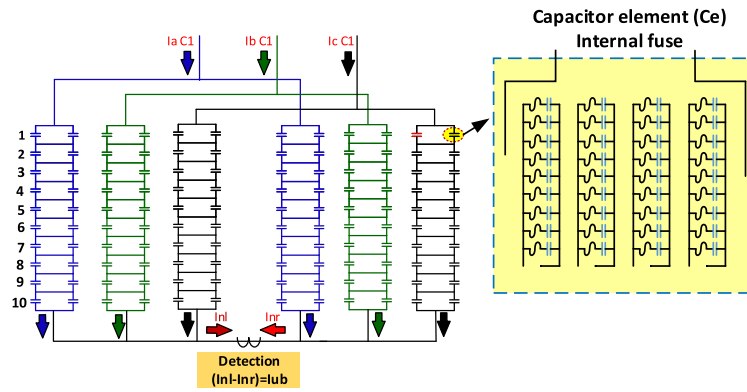
A. SCENARIO 1: FAULT OCCURRING IN CAPACITOR BANK NO. 1

Fig. 2 indicates that the fault occurred in phase A of capacitor bank No. 1 at 0.45 s; this was considered the first case study. The current phase and difference unbalance current of Scenario 1 are illustrated in Fig. 5 and 6, respectively.

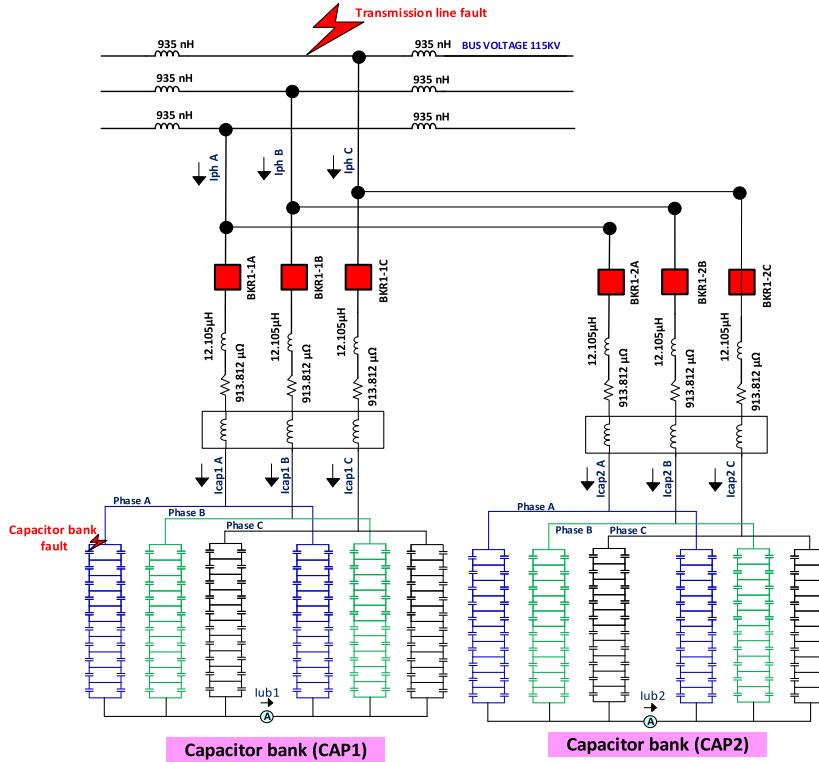
The current phase (I_{ph}) in Fig. 5(a) indicates that the current at the time of switching of capacitor banks was identical



(a) Diagram of the developed system.



(b) Components of a capacitor bank.



(c) Capacitor bank system simulated in PSCAD.

FIGURE 2. The power systems computer-aided design (PSCAD) system based on the diagram of the developed system.

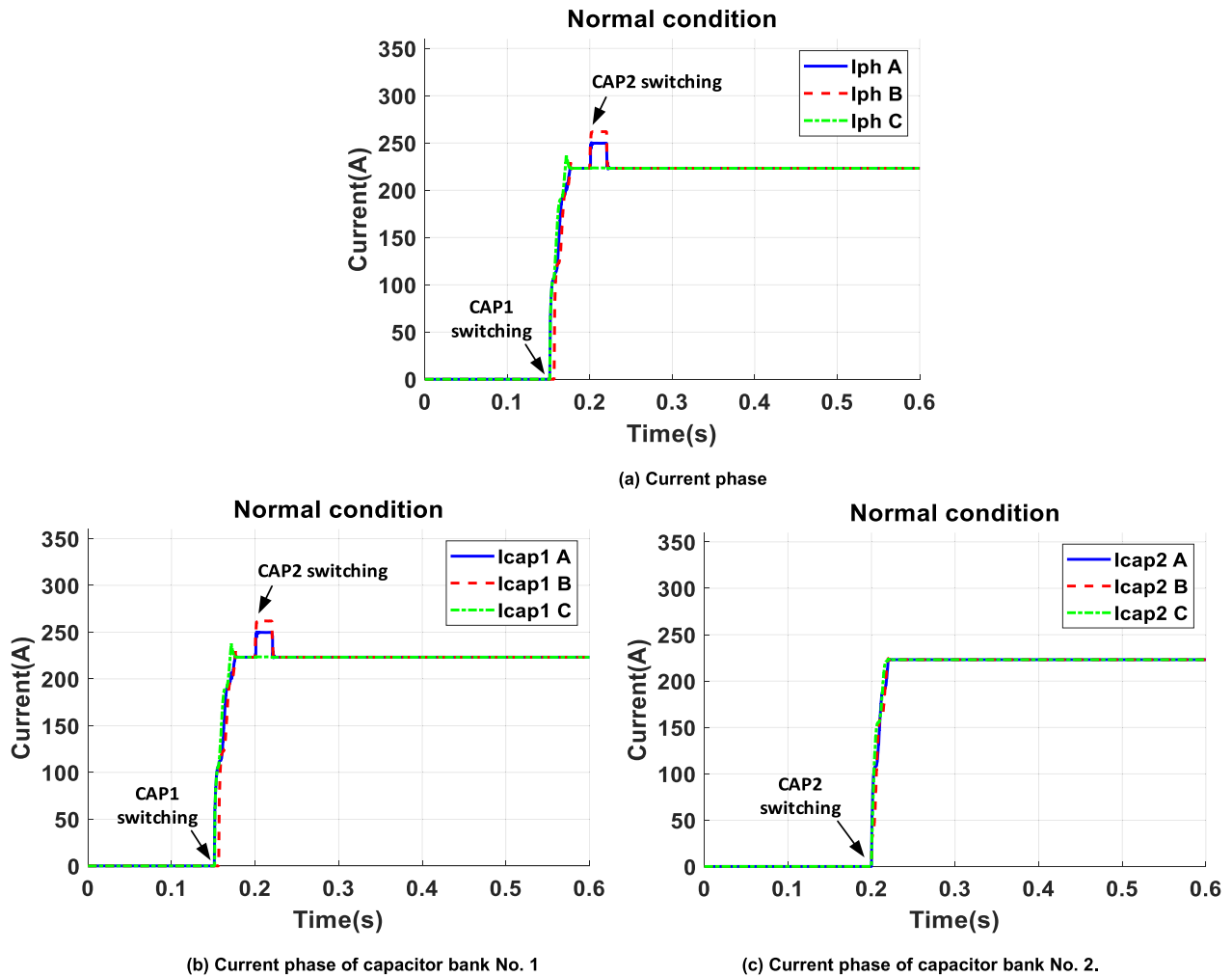


FIGURE 3. Current phase under normal conditions.

to that under normal conditions. However, when the fault occurred at 0.45 s in phase A, the phase A current ($I_{ph} A$) reduced from 223 to 222 A. In other phases where faults did not occur, the phase currents ($I_{ph} B$ and $I_{ph} C$) were maintained the same as that under normal conditions.

Fig. 5(b) indicates that the current phase of both capacitor banks (I_{cap1} and I_{cap2}) increased owing to the effect of energising the capacitor bank, similar to that observed under the normal condition. As the fault only occurred in phase A of capacitor bank No. 1, only the current phase of capacitor bank No. 1 (I_{cap1}) changed. This implies that the current of the fault phase ($I_{cap1} A$) reduced when the fault occurred, whereas other current phases maintained an approximate value of 223 A.

Fig. 6 indicates that the difference unbalance current of capacitor bank No. 1 ($I_{ub} cap1$) increased from the value that was observed under the normal condition to 0.5034 A. This can be attributed to the reduction in the capacitance of the faulty capacitor unit. Additionally, the current of the fault phase was lower than those observed in other phases. As the

current was unbalanced in all three phases, the difference unbalance current increased.

When considering the current phase of capacitor bank No. 2, no fault occurred in this capacitor bank. Therefore, the values of capacitance were identical in all capacitor units. As the current was balanced in all three phases, the difference unbalance current of capacitor bank No. 2 ($I_{ub} cap2$) was maintained at the value same as that under the normal condition.

B. SCENARIO 2: FAULT OCCURRING IN BOTH CAPACITOR BANKS

The characteristics of I_{ph} , I_{cap} , and I_{ub} were considered when the fault occurred in two capacitor banks. Fig. 7 and 8 depict the characteristics of these parameters considering the system depicted in Fig. 2. In this scenario, the fault occurred in phase A of capacitor bank No. 1 at 0.45 s. Subsequently, the fault occurred in phase A of capacitor bank No. 2 as well at 0.53 s.

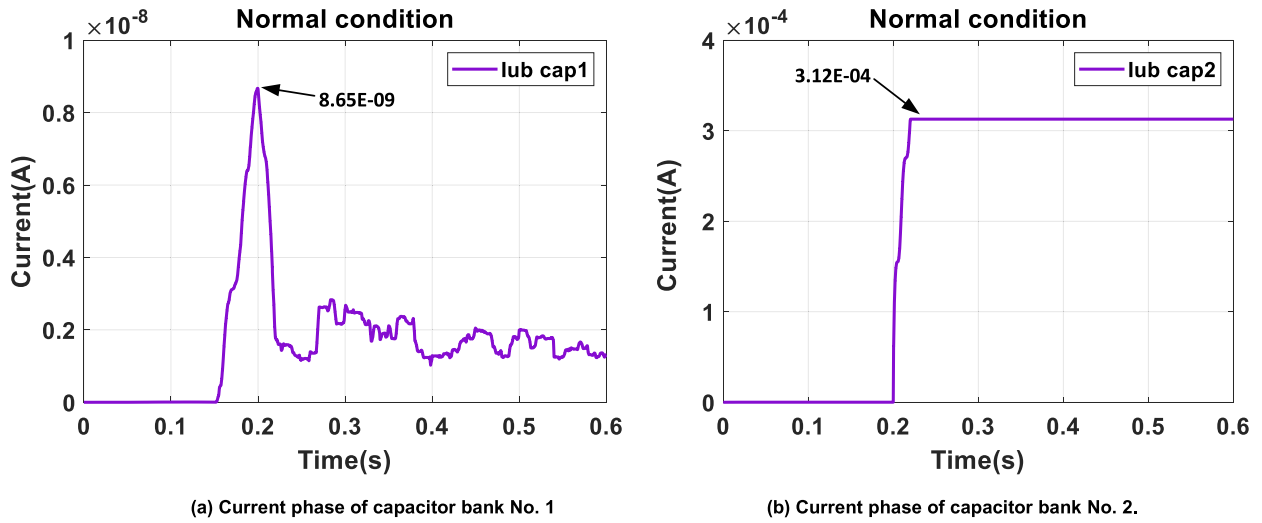


FIGURE 4. Difference unbalance current observed under normal conditions.

Two issues were identified by considering the current phase (I_{ph}) in Fig. 7(a). First, the current phase increases owing to the effect of the capacitor bank switching, and the back-to-back connection reduces the effect of the inrush current. Second, owing to the reduction in the capacitance of the faulty capacitor unit, the current in the fault phase (phase A) reduces from 223 A (normal condition) to 222 A (fault condition).

Similarly, when considering the current phase of the capacitor bank (I_{cap}) in Fig. 8(b), only the current of the fault phase was reduced owing to the capacitance of the faulty capacitor unit. In this scenario, both capacitor banks exhibited faults in phase A. Therefore, the currents in the fault phase, namely I_{cap1} A and I_{cap2} A, decreased at the time of fault occurrence, namely 0.45 and 0.53 s, respectively.

Under normal conditions, the values of each current phase were identical; therefore, the currents in all three phases were balanced. This implies that the difference unbalance current was close to zero. However, when the fault occurred, the current was unbalanced in the three phases owing to the reduction in the fault phase current. Therefore, the difference unbalance current of each capacitor bank ($I_{ub\ cap1}$ and $I_{ub\ cap2}$) depicted in Fig. 8 increases from the value observed under normal conditions to 0.5034 A.

C. SCENARIO 3: FAULT IN THE TRANSMISSION LINE

In this scenario, the fault occurred in phase A of the transmission line at 0.3 s. The capacitor bank Nos. 1 and 2 were switched at 0.15 s and 0.2 s, respectively. Figs. 9 and 10 depict the characteristics of the system parameters for Scenario 3.

Fig. 9(a) indicates that the phase A current increased significantly at the time of fault occurrence. Conversely, the currents in phases B and C exhibited almost no change, as no faults occurred. However, Fig. 9(a) indicates that when the fault occurs at the transmission line, the current of the fault phase increases abruptly from 223 A (normal condition) to

11150.52 A. Conversely, the currents in the other phases decreased slightly from the value observed under the normal condition to 217.62 A. These significant changes in the current can be attributed to the direct effect of the fault in the transmission line on its impedance.

Fig. 9(b) indicates that the current phase of the capacitor bank increases when the capacitor bank is energised. However, as the back-to-back connection reduces the inrush current generated by the switching of the capacitor bank, the inrush current of capacitor bank No. 2 was smoother than that in the capacitor bank No. 1. The fault occurring at 0.3 s in the transmission line affected the current phase of both capacitor banks (I_{cap1} and I_{cap2}). The current phase of the capacitor bank increased at the time of fault occurrence in the transmission line. Subsequently, it decreased to a value lower than that observed under the normal condition.

Fig. 10 depicts the difference unbalance current when the fault occurred in the transmission line. Although the difference unbalance current of capacitor bank No. 2 was slightly spiked at the time of fault occurrence, it reduced when the difference unbalance current converged to a stable state. The difference unbalance currents of both capacitor banks ($I_{ub\ cap1}$ and $I_{ub\ cap2}$) were maintained at values identical to that observed under the normal condition. This is because the fault in the transmission line affected only the line impedance, and the capacitance of the capacitor unit inside the capacitor bank remained unaffected. Therefore, the current phase of the capacitor bank was balanced.

IV. FACTORS INFLUENCING THE SYSTEM PARAMETERS

Section 3 discussed the characteristics of the current affected by faults. Considering the complexity of existing electrical systems, faults in the transmission line and both capacitor banks were analysed further based on the factors (Table 2) that are known to influence the system parameters.

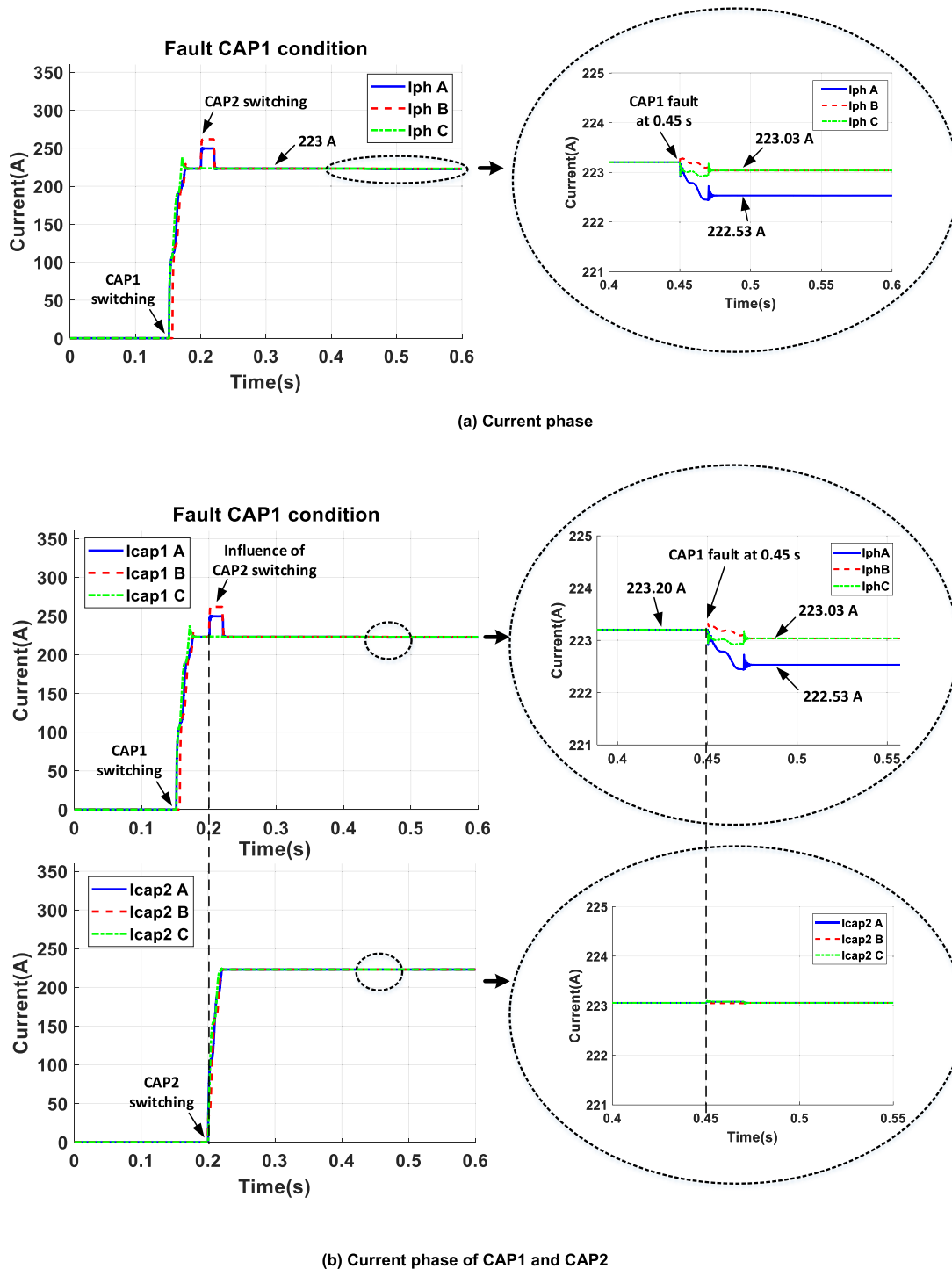


FIGURE 5. Current phase when the fault occurs in phase A of CAP1.

As indicated in Table 2, fault location was one of the factors affecting the system parameters. Table 3 summarises the data observed when the system parameters were affected by faults occurring in the transmission line, a single capacitor bank, and both capacitor banks.

The fault in the transmission line of phase A (AG case) was initially analysed (Table 3). The data indicate that the fault phase current in phase A increased significantly from the current observed under the normal condition, whereas the currents in other phases decreased slightly. This behaviour

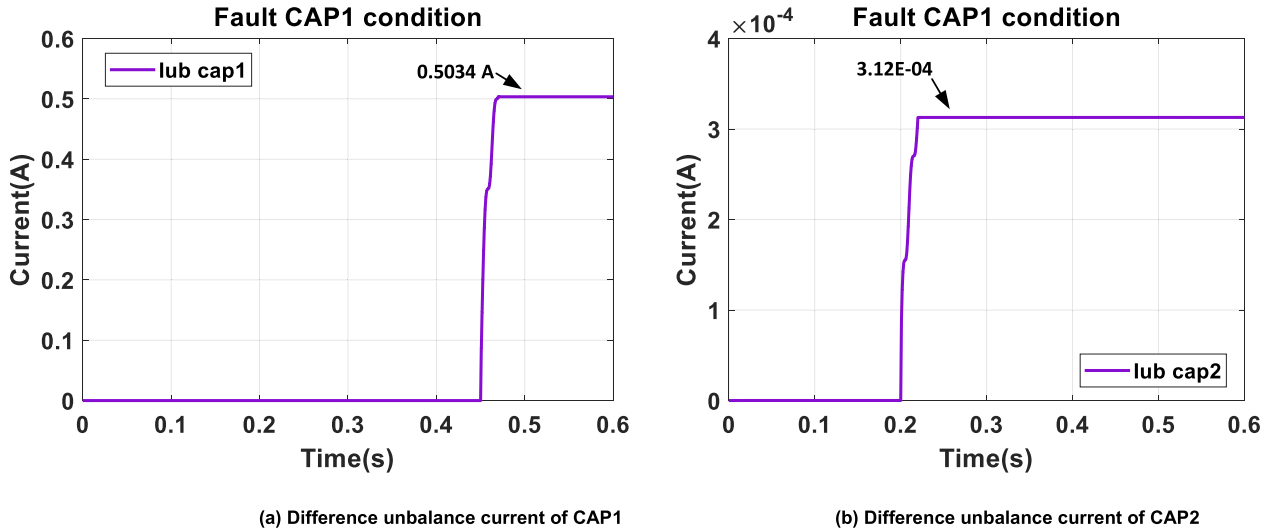


FIGURE 6. Difference unbalance current when the fault occurs in phase A of CAP1.

TABLE 2. Factors that influence the system parameters.

No.	Variable factor	Description
1.	Fault location	Transmission line, Capacitor bank No. 1, and Capacitor bank No. 2
2.	Fault phase	A, B, and C
3.	Fault of inception angle (θ)	0, 60, 120, 180, 240, and 300 °

can be attributed to the effect of the fault on the impedance line. Similarly, the changing of the current phase influenced the current phases of both capacitor banks (I_{cap1} and I_{cap2}), wherein both the current phases decreased from the value observed under normal conditions. Additionally, the difference unbalance currents of both capacitor banks ($I_{ub\ cap1}$ and $I_{ub\ cap2}$) were identical to the value obtained under the normal condition. This is because the fault in the transmission line did not affect the capacitance. Therefore, the current phase of the capacitor bank was balanced.

In the case of the fault occurring in capacitor bank No. 1 (Cap1 PhA case), the current phase A of the capacitor bank decreased slightly from 223 A (normal condition) to 222 A. This decrease can be attributed to the effect of the capacitance of the faulty capacitor unit. Owing to this decrease in the current, the difference unbalance current of capacitor bank No. 1 decreases. Furthermore, the system parameters in this scenario were compared with those observed when the fault occurred in both capacitor banks. The results indicate that the system parameters in both cases exhibit similar characteristics, wherein the current in phase A decreases when the fault occurs in the capacitor bank and other phases maintain the same value as observed under the normal condition. Additionally, the difference unbalance current detected at each capacitor bank increases owing to the fault occurrence.

The second factor influencing the system parameters was the fault phase. Table 4 summarises the data obtained by varying the fault phase. In the case of the fault in the transmission line, four types of faults, namely the single line to ground, line-to-line, double line to ground, and three-phase faults, were observed; however, the type of fault was not significant in analysing its effect on the system parameters. The current phase relied only on the impedance line. The difference unbalance current was close to zero, which was identical to the value observed under normal conditions owing to the stable capacitance.

When the fault phase of the capacitor bank changed from phase A to B, only the current of the fault phase was reduced, which in turn reduced the capacitance. Moreover, the variations in this current of the fault phase influenced the difference unbalance current.

Similarly, faults occurring in both capacitor banks and the fault phase variable were analysed. The fault phase did not significantly affect the current phase of the capacitor bank (I_{cap}) and difference unbalance current (I_{ub}). The current phase of the capacitor bank relied only on the capacitance, which increased the difference unbalance current.

The final factor influencing the system parameters was the fault inception angle. Table 5 summarises the data obtained when the inception angle was varied (0, 60, and 120°).

When the fault occurred in the transmission line and the inception angle was 0°, the current in the fault phase increased, whereas those in the other phases decreased. Additionally, the values of the current phase when faults occur at all three inception angles, namely 0, 60, and 120°, were similar.

Furthermore, the variation in the inception angle influenced the difference unbalance current slightly. However, as the value was approximately 10⁻⁹, the variation of this difference unbalance current was not considered.

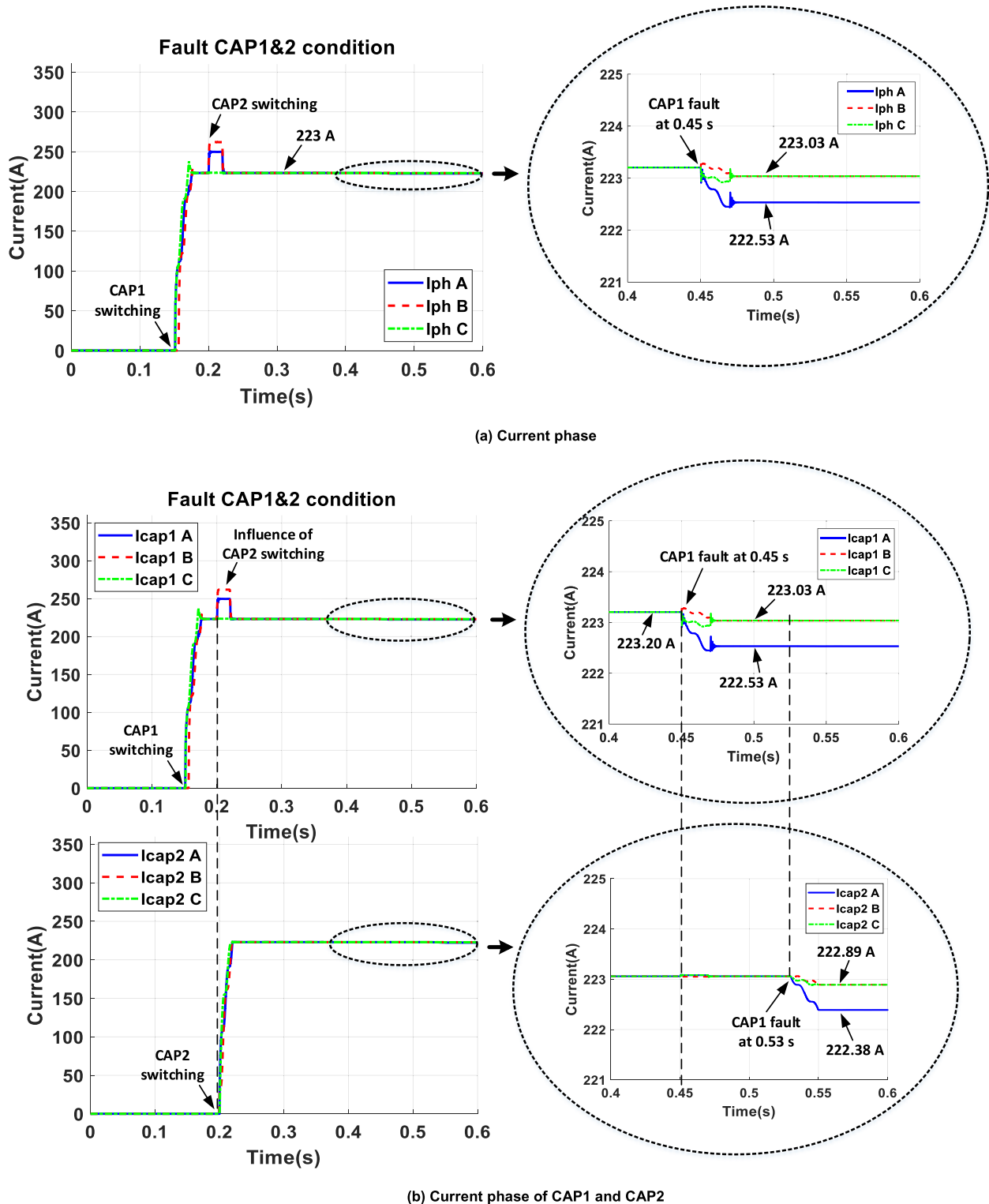


FIGURE 7. Current phase when the fault occurs in phase A of CAP1 and CAP2.

Table 5 also indicates that the system parameters in the case of faults occurring in a single capacitor bank and both capacitor banks were identical, and the variations in the inception angle did not affect the system parameters.

Therefore, the fault occurring in the capacitor banks directly influenced only two parameters, namely I_{cap} and I_{ub} .

In summary, the phase and inception angle did not affect the system parameters, and only the fault location influenced

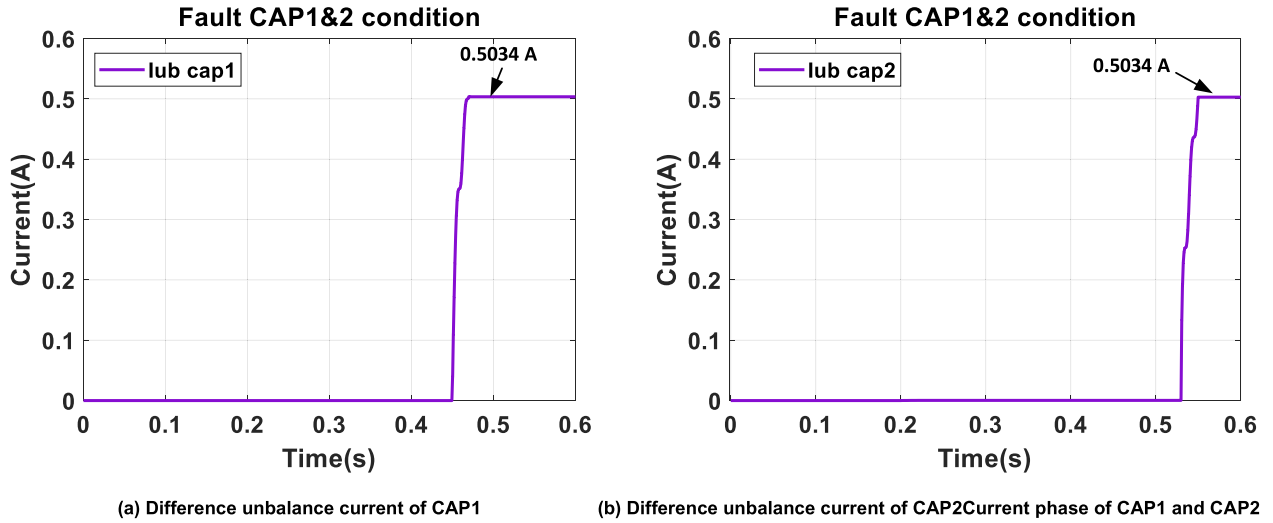


FIGURE 8. Difference unbalance current when the fault occurs in phase A of CAP1 and CAP2.

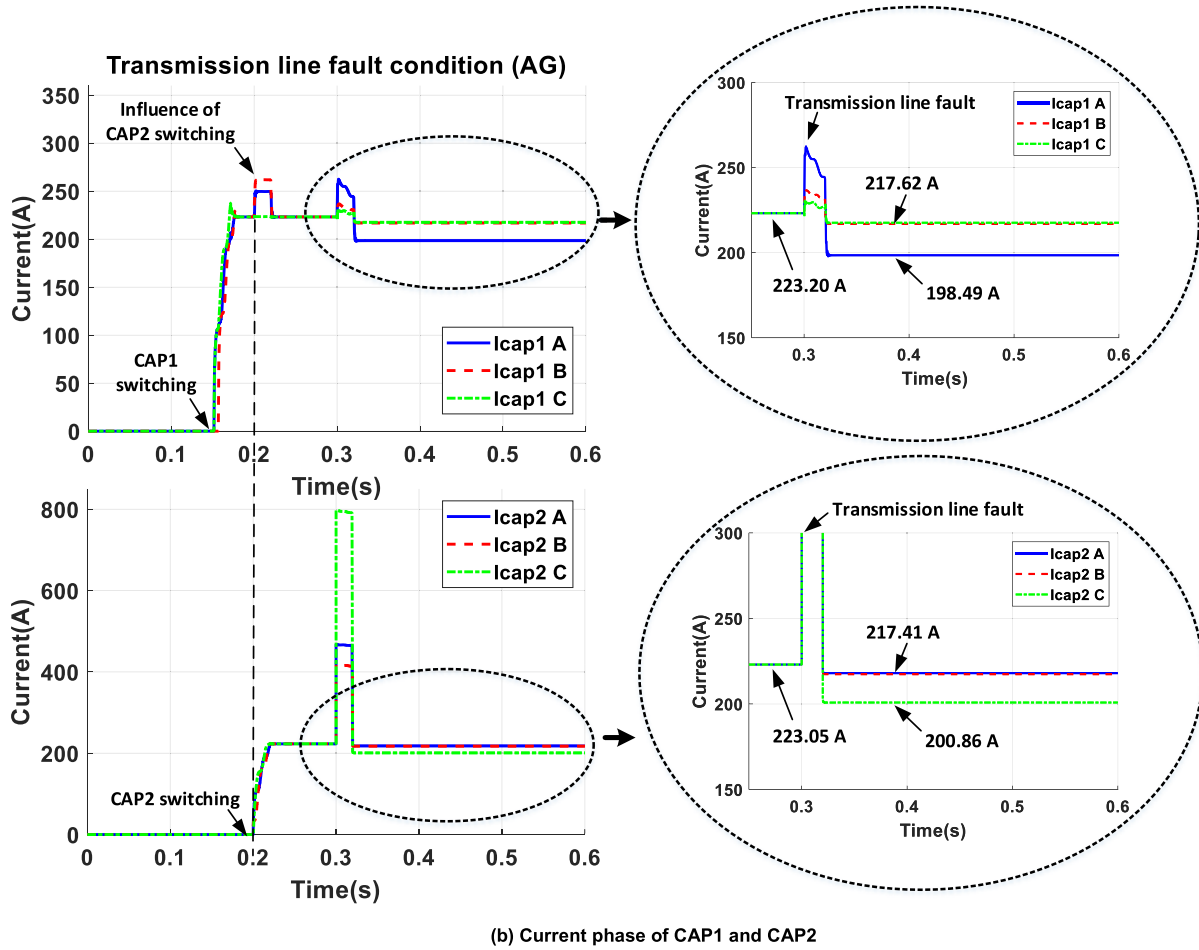


FIGURE 9. Current phase when the fault occurs in phase A of the transmission line.

the magnitude of system parameters. This is because the fault occurring in the transmission line affected the impedance of the line, changing the current phase (I_{ph}). The other

parameters, namely I_{cap} and I_{ub} remained stable. Similarly, the fault occurring in the capacitor banks affected only the capacitance of the fault phase. Therefore, the current phase

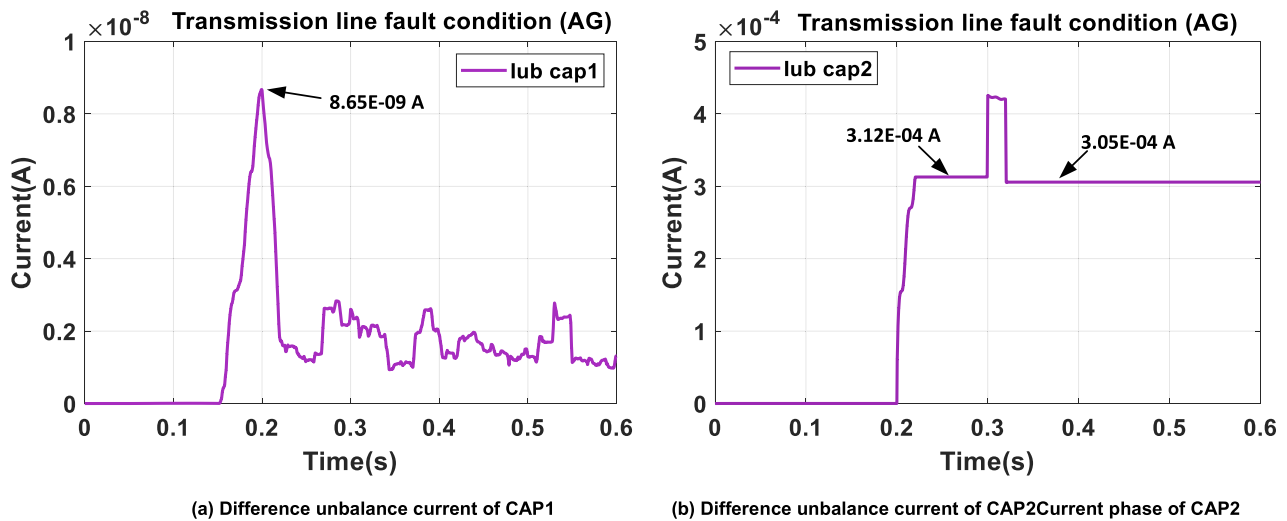


FIGURE 10. Difference unbalance current when the fault occurs in phase A of the transmission line.

of the capacitor bank and the difference unbalance current were varied.

Furthermore, the variations in the system parameters in the case of faults occurring in a single capacitor bank and both capacitor banks were similar. This similarity may result in trips caused by the error in the unbalance relay during the fault detection process. Therefore, the difference between the system parameters when faults occur in a single capacitor bank and both capacitor banks were determined by applying a mathematical method

V. APPLICATION OF DWT

The current phase of the capacitor bank (*Icap*) and difference unbalance current (*Iub*) change when faults occur because of the capacitance of a faulty capacitor unit. However, when these two parameters are compared in the case of faults occurring in a single capacitor bank (CAP1) and both capacitor banks (CAP1&2), the number of fault capacitor banks did not significantly affect them.

Additionally, in terms of capacitor bank protection, the unbalance relay detected the fault by using the difference unbalance current. If the difference unbalance currents are similar in the cases of faults occurring in a single capacitor bank and both capacitor banks, it hinders the fault detection process. The error in the unbalance relay may result in trips, which directly affects the efficiency of the fault detection and reliability of the power system. Therefore, DWT was applied to analyse the ambiguousness of the two parameters, namely *Icap* and *Iub*, in both cases.

Wavelet transform can be considered as mathematically projecting a signal into a set of basis functions, referred to as wavelets. Wavelets are based on the dilation and translation of the mother function, defined as an orthogonal basis, as follows:

$$\varnothing(s, l)(x) = 2^{-\frac{s}{2}} \varnothing(2^{-s}x - l), \tag{1}$$

where variables *s* and *l* denote the integers that scale and dilate the mother function \varnothing , respectively, to generate wavelets, such as a Daubechies wavelet (DB). The scale and location indices, namely *s* and *l* indicate the width and position of the wavelet, respectively.

DWT provides high-frequency resolution at low frequencies and high time resolution at high frequencies to span the data domain at different resolutions. The wavelet analysed was used in a scale equation, as follows:

$$w(x) = \sum_{K=-1}^{N-2} (-1)^k B_k + 1\varnothing(2X + k) \tag{2}$$

Similar to the three scenarios described in Section III, the parameters current phase of capacitor bank No. 1 (*Icap1*), current phase of capacitor bank No. 2 (*Icap2*), difference unbalance of capacitor bank No. 1 (*Iub cap1*), and difference unbalance of capacitor bank No. 2 (*Iub cap2*) were analysed. These parameters were extracted using DB, as presented in Fig. 11 to 13 and Table 6 to 8.

Fig. 11 depicts the wavelet coefficient of the current in capacitor bank No. 1 (*WT Icap1*). The wavelet characteristics indicate that the magnitude of current (*Icap1*) increases abruptly when capacitor bank No. 1 switches into the power system. Simultaneously, the wavelet coefficient increases slightly at 0.2 s owing to the influence of the switching of capacitor bank No. 2.

When considering the fault in capacitor bank No. 1, the data in Table 7 indicate that the wavelet coefficient (*WT Icap1*) during the switching of the capacitor bank was identical to that observed under the normal condition. During the fault occurrence, the wavelet coefficient of the fault increases from the coefficient of normal condition at 0.45 s, and the second peak increases at 0.47 s owing to the fault energy.

Furthermore, Fig. 11 compares these wavelet coefficients in the case of faults occurring in a single capacitor bank and

TABLE 3. Influence of fault location on the system parameters.

Fault case	I phase			I Capacitor bank No.1				I Capacitor bank No.2			
	A	B	C	A	B	C	Iub	A	B	C	Iub
Normal	223.20	223.20	223.20	223.20	223.20	223.20	2.01E-09	223.05	223.05	223.05	3.13E-04
AG	11150.84	216.96	217.63	198.50	216.95	217.63	1.10E-09	218.03	217.42	200.86	2.82E-04
Cap1 PhA	222.53	223.04	223.04	222.53	223.04	223.04	0.5034	223.06	223.06	223.06	3.13E-04
Cap1 PhA& Cap2 PhA	222.53	223.03	223.03	222.53	223.03	223.03	0.5034	222.65	222.96	222.95	0.5028

TABLE 4. Influence of variations in the fault phase on the system parameters.

Fault case	I phase			I capacitor bank No.1				I capacitor bank No.2			
	A	B	C	A	B	C	Iub	A	B	C	Iub
Normal	223.20	223.20	223.20	223.20	223.20	223.20	2.01E-09	223.05	223.05	223.05	3.13E-04
AG	11150.84	216.96	217.63	198.50	216.95	217.63	1.10E-09	218.03	217.42	200.86	2.82E-04
ABG	11406.62	10818.21	210.80	192.43	193.09	210.80	9.10E-10	211.92	195.98	195.39	2.74E-04
AB	16367.96	16591.15	223.20	177.88	177.90	223.20	1.15E-09	223.06	182.12	182.11	2.55E-04
ABCG	11086.57	11086.57	11086.75	186.36	186.36	186.36	1.09E-09	189.96	189.96	189.96	2.66E-04
Cap1 PhA	222.53	223.04	223.04	222.53	223.04	223.04	0.5034	223.06	223.06	223.06	3.13E-04
Cap1 PhB	223.04	222.53	223.04	223.04	222.53	223.04	0.5034	223.06	223.06	223.06	3.13E-04
Cap1PhA& Cap2 PhA	222.53	223.03	223.03	222.53	223.03	223.03	0.5034	222.65	222.96	222.95	0.5028
Cap1PhB& Cap2 PhA	223.03	222.53	223.03	223.03	222.53	223.03	0.5034	222.65	222.96	222.95	0.5028
Cap1PhA& Cap2 PhB	222.54	223.05	223.05	222.53	223.03	223.03	0.5034	222.63	222.49	223.20	0.5028

TABLE 5. Influence of the variations in the fault inception angle on the system parameters.

Fault case	θ	I phase			I capacitor bank No. 1				I capacitor bank No. 2			
		A	B	C	A	B	C	Iub	A	B	C	Iub
Normal	0	223.20	223.20	223.20	223.20	223.20	223.20	2.01E-09	223.05	223.05	223.05	3.13E-04
AG	0	11150.84	216.96	217.63	198.50	216.95	217.63	1.10E-09	218.03	217.42	200.86	2.82E-04
AG	60	11151.04	216.95	217.63	198.50	216.95	217.63	2.12E-09	218.03	217.42	200.86	3.06E-04
AG	120	11150.82	216.95	217.63	198.50	216.95	217.63	1.97E-09	218.03	217.42	200.86	3.06E-04
Cap1 PhA	0	222.53	223.04	223.04	222.53	223.04	223.04	0.5034	223.06	223.06	223.06	3.13E-04
Cap1 PhA	60	222.53	223.03	223.03	222.53	223.03	223.03	0.5034	223.06	223.06	223.06	3.13E-04
Cap1 PhA	120	222.53	223.04	223.04	222.53	223.04	223.04	0.5034	223.06	223.06	223.06	3.13E-04
Cap1PhA& Cap2PhA	0	222.5329	223.0371	223.0383	222.53	223.03	223.03	0.5034	222.65	222.96	222.95	0.5028
Cap1PhA& Cap2PhA	60	222.5522	223.0479	223.0568	222.53	223.03	223.03	0.5034	222.49	223.20	222.62	0.5028
Cap1PhA& Cap2PhA	120	222.5423	223.0562	223.0596	222.53	223.03	223.03	0.5034	223.24	223.39	222.81	0.5045

TABLE 6. Wavelet coefficient of the current in capacitor bank No. 1.

Fault case	Time of capacitor bank switching (0.15 to 0.2 s)			Time of fault occurrence in capacitor bank No. 1 (0.45 s)			Time of fault occurrence in capacitor bank No. 2 (0.53 s)		
	WT Icap1 A	WT Icap1 B	WT Icap1 C	WT Icap1 A	WT Icap1 B	WT Icap1 C	WT Icap1 A	WT Icap1 B	WT Icap1 C
Normal condition	676.83	876.02	676.83	2.43E-10	2.43E-10	2.43E-10	2.56E-10	2.56E-10	2.56E-10
Cap1	676.83	876.02	676.83	0.0152	0.0023	0.0122	3.10E-10	3.10E-10	3.10E-10
Cap1&2	676.83	876.02	676.83	0.0152	0.0023	0.0122	4.80E-07	5.10E-07	5.40E-07

both capacitor banks. As indicated in the figure, the wavelet coefficients of these two cases exhibit identical characteristics. Moreover, Table 6 indicates that the wavelet coefficient can aid in determining the distinctness of the parameters between the two cases. The wavelet coefficient in the case of the fault occurring in a single capacitor bank increases at

the time of fault occurrence (0.45 s). Conversely, in the case of the fault occurring in both capacitor banks, the wavelet coefficient occurs twice; the first wavelet coefficient occurred owing to the fault occurrence in capacitor bank No. 1, and the second wavelet coefficient increased slightly owing to the effect of the fault occurring in the other capacitor bank.

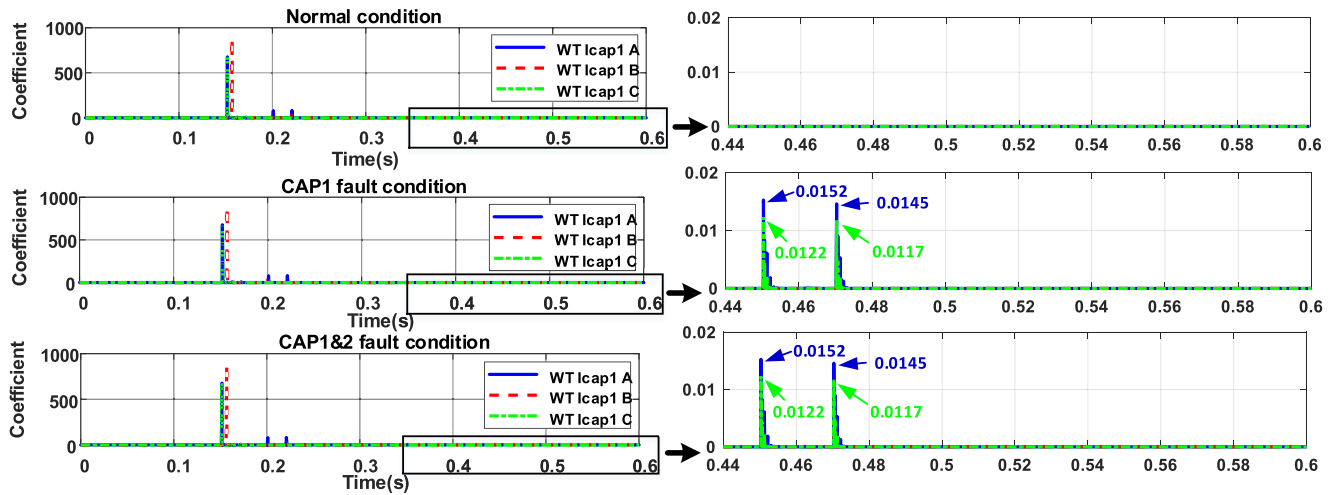


FIGURE 11. Wavelet coefficient of the current in capacitor bank No. 1.

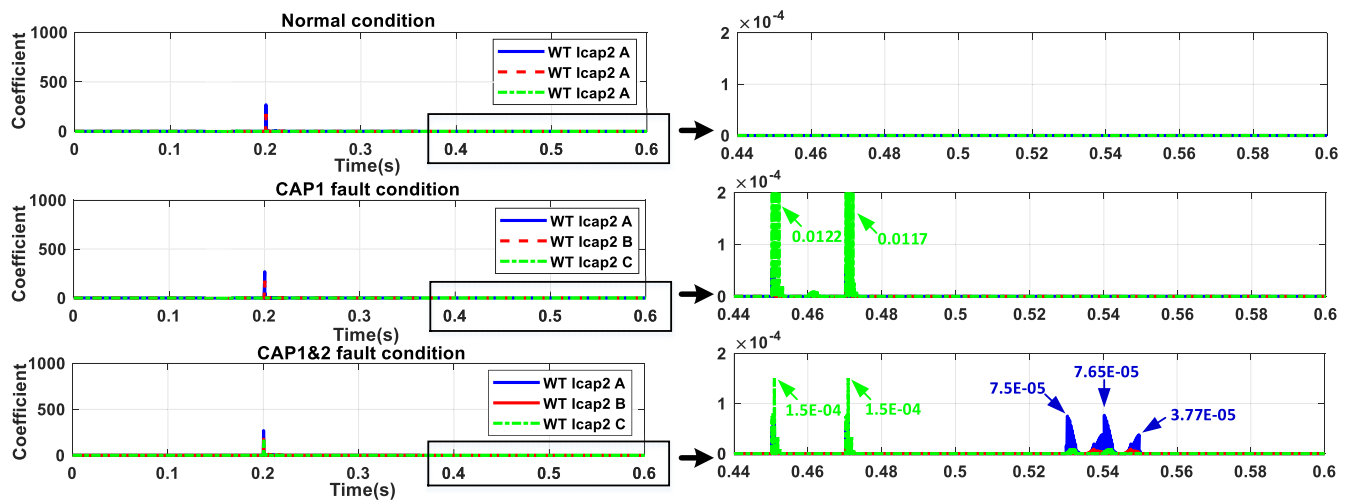


FIGURE 12. Wavelet coefficient of the current in capacitor bank No. 2.

TABLE 7. Wavelet coefficient of the current in capacitor bank No. 2.

Fault case	Time of capacitor bank switching (0.15 to 0.2 s)			Time of fault occurrence in capacitor bank No. 1 (0.45 s)			Time of fault occurrence in capacitor bank No. 2 (0.53 s)		
	WT Icap2 A	WT Icap2 B	WT Icap2 C	WT Icap2 A	WT Icap2 B	WT Icap2 C	WT Icap2 A	WT Icap2 B	WT Icap2 C
Normal condition	267.41	175.70	256.83	2.43E-10	2.43E-10	2.43E-10	2.56E-10	2.56E-10	2.56E-10
Cap1	267.41	175.70	256.83	5.40E-05	9.18E-06	0.0122	3.24E-10	3.24E-10	3.24E-10
Cap1&2	178.69	205.82	188.41	6.49E-05	8.12E-06	1.50E-04	7.65E-05	7.60E-06	1.04E-05

Fig. 12 and Table 7 present the wavelet coefficient of capacitor bank No. 2 (*WT Icap2*). The first peak of the wavelet coefficient detected from capacitor bank No. 2 occurred at 0.2 s because of the switching.

The wavelet coefficient of capacitor bank No. 2 was analysed in the case of a fault occurring in capacitor bank No. 1. The data in Table 7 indicate that the wavelet coefficient that occurred during the switching of the capacitor bank

was identical to that observed under the normal condition. Furthermore, Fig. 12 indicates that the wavelet coefficient occurred at 0.45 and 0.47 s, similar to that of capacitor bank No. 1 depicted in Fig. 11.

Similarly, the characteristics of the wavelet coefficient of capacitor bank No. 2 observed when the fault occurred in both capacitor banks were identical to the previously observed characteristics, wherein the value increased only at the time

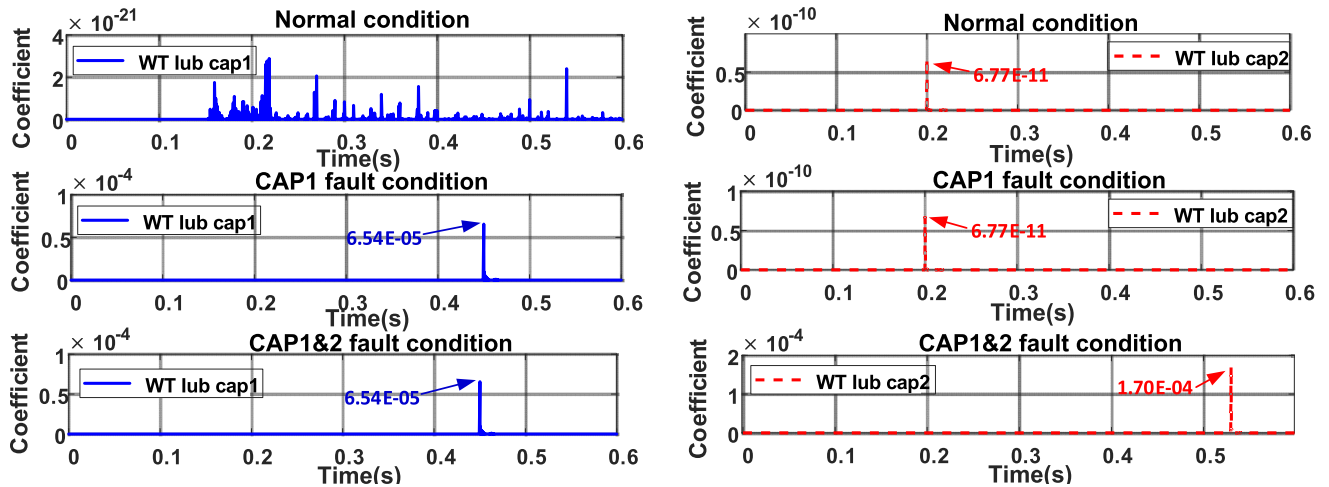


FIGURE 13. Wavelet coefficient of the difference unbalance current of the capacitor bank.

TABLE 8. Wavelet coefficient of the difference unbalance current of the capacitor bank.

Fault case	Time of capacitor bank switching (0.15 to 0.2 s)		Time of fault occurrence in capacitor bank No. 1 (0.45 s)		Time of fault occurrence in capacitor bank No. 2 (0.53 s)	
	WT Iub cap1	WT Iub cap2	WT Iub cap1	WT Iub cap2	WT Iub cap1	WT Iub cap2
Normal condition	1.74E-21	6.77E-11	2.49E-22	1.79E-26	2.39E-21	2.86E-26
Cap1	1.74E-21	6.77E-11	6.54E-05	1.25E-26	2.10E-21	5.92E-26
Cap1&2	1.74E-21	6.77E-11	6.54E-05	3.78E-21	2.54E-21	1.70E-04

of fault occurrence (0.45 and 0.53 s). However, certain discrepancies were identified when *WT Icap1* was compared to *WT Icap2* (Table 6 and 7)

When considering *WT Icap1*, the fault occurring in capacitor bank No. 1 was caused by a fault in the internal zone. As *WT Icap1* was directly affected by the fault occurrence, it increased significantly and was detected easily. By contrast, when considering *WT Icap2*, the fault occurring in capacitor bank No. 1 was caused by the fault in the external zone. Therefore, *WT Icap2* increased slightly as it was indirectly affected by the fault occurrence.

Fig. 13 and Table 8 present the wavelet coefficient of the difference unbalance current (*WT Iub cap*). Under normal conditions, the wavelet coefficient of the difference unbalance current detected from capacitor bank Nos. 1 and 2 was approximately 10^{-26} .

The analysis of *WT Iub cap* in the case of a fault occurring in capacitor bank No. 1 (Figure 13) indicates that only *WT Iub cap1* increases to 10^{-5} from the value observed under normal conditions; *WT Iub cap2* maintained the same value as observed under normal conditions. The increase in *WT Iub cap1* can be attributed to the change in the magnitude of *Iub cap1*. Additionally, the coefficient of *WT Iub cap2* was maintained identical to that observed under the normal condition because the value of *Iub cap2* remained unchanged, as explained in Section IV.

The increase in the difference unbalance current (*Iub*) when the fault occurs in the capacitor bank increases the *Iub* detected in the case of the fault occurring in both capacitor banks. Therefore, *WT Iub cap1* and *WT Iub cap2* increase at the time of fault occurrence, as depicted in Fig. 13.

Subsequently, the wavelet coefficient of current based on the Daubechies mother wavelet (DB) was analysed. This aided in addressing the ambiguity of difference unbalance currents in the cases of faults occurring in a single capacitor bank and both capacitor banks. Furthermore, other types of mother wavelets were analysed for a comprehensive investigation; Symlet (sym) and Coiflet (coif) were considered, and the results can be summarised as follows.

Fig. 14 indicates that the wavelet coefficient of difference unbalance current detected by both capacitor banks exhibits similar characteristics. The coefficient based on the Symlet wavelet was identical to that based on the Daubechies wavelet; however, the coefficient based on the Coiflet wavelet was lower than that based on the Daubechies wavelet. This implies that the wavelet coefficient changes when the type of mother wavelet is varied.

Apart from the type, the scale of the mother wavelet should also be considered as it can affect the wavelet coefficient. Fig. 15 illustrates the wavelet coefficient of difference unbalance current based on Daubechies wavelet,

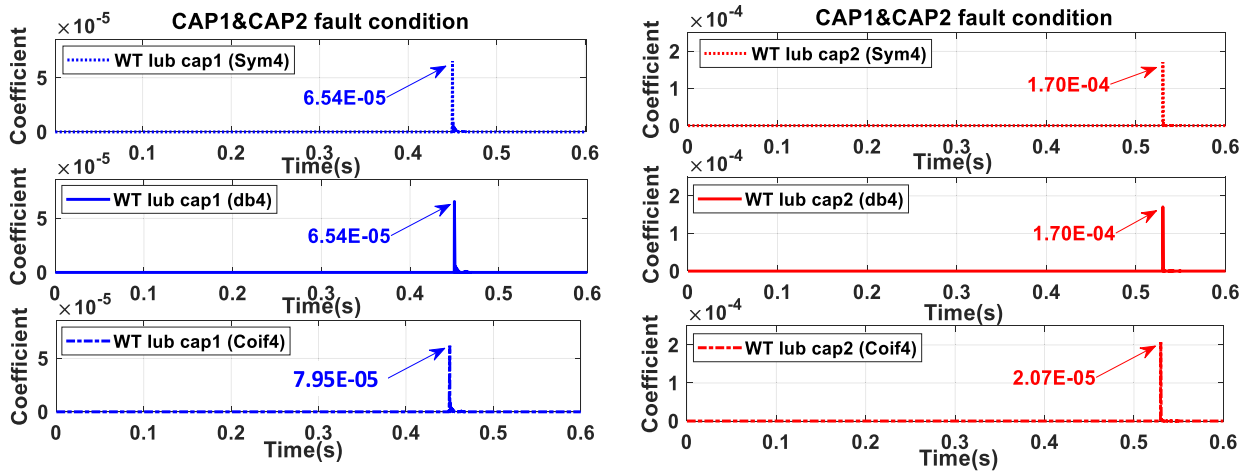


FIGURE 14. Wavelet coefficient of the difference unbalance current when the mother wavelet is varied.

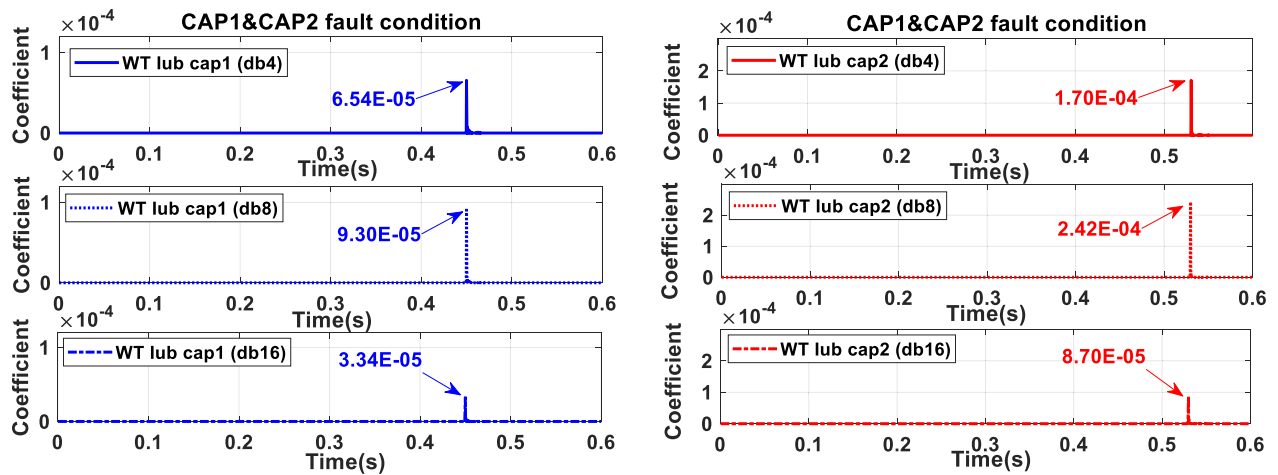


FIGURE 15. Wavelet coefficient of the difference unbalance current when the scale of the mother wavelet variable.

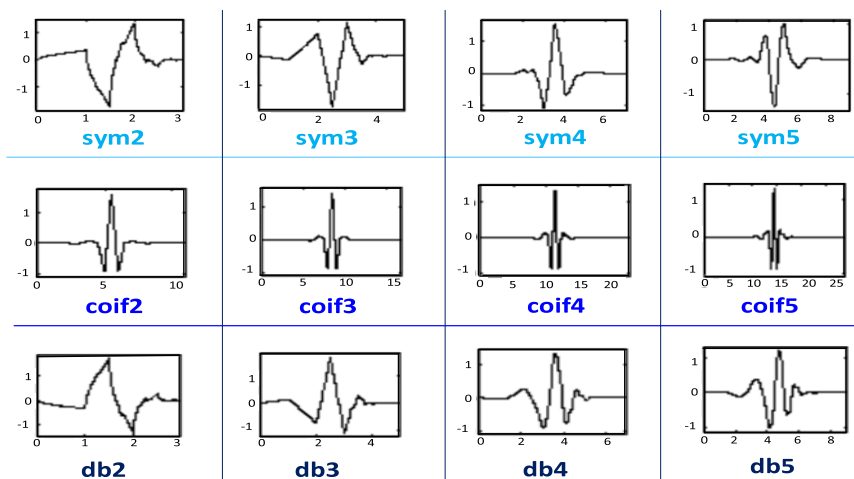


FIGURE 16. Signal shape of the mother wavelet.

wherein the scale was varied from 4 to 16. As indicated in the figure, the wavelet coefficients detected in both capacitor banks exhibit the same behaviour, wherein the wavelet

coefficient decreases when the scale of the mother wavelet is increased and the type of the mother wavelet is maintained constant.

The type and scale of the mother wavelet affecting the wavelet coefficient can be attributed to the signal shape. As depicted in Fig. 16, three types of mother wavelets exhibit different signal shapes. As the shape of the Symlet wavelet was similar to that of the Daubechies wavelet, the determined wavelet coefficients were identical. By contrast, the shape of the Coiflet wavelet differed from that of the Daubechies wavelet; consequently, the determined coefficients were different. Additionally, as the scale affected the signal shape, the wavelet coefficient changed when the scale of the mother wavelet was varied. As both type and scale of the mother wavelet influence the wavelet coefficient, appropriate wavelets should be selected based on the applications.

VI. RESULTS AND DISCUSSION

This study analysed the characteristics of system parameters considering the faults occurring in the transmission line and capacitor banks using the simulation software PSCAD. DWT was applied for a detailed analysis, and the results can be summarised as follows.

1. The current phase (I_{ph}) and current phase of the capacitor bank (I_{cap}) rely on impedance and capacitance. When the fault occurs in the transmission line, the impedance of the line changes, which in turn changes the current phase. Similarly, when the fault occurs in the capacitor bank, the reduction in the capacitance of the capacitor unit decreases the current phase of the capacitor bank.
2. Despite the occurrence of a fault in the transmission line, the value of the difference unbalance current of the capacitor bank is maintained the same as that observed under the normal condition. It changes only when the fault occurs in the capacitor bank. Therefore, the variation in the difference unbalance current of the capacitor bank is the dominant feature, which impacts the fault in the capacitor bank.
3. The ambiguity of the system parameters (I_{ph} and I_{cap}) when faults occur in a single capacitor bank and both capacitor banks can be addressed using DWT, as the wavelet coefficient was generated at the time of fault occurrence. The wavelet coefficient detected in the fault of the internal zone was higher than that detected in the fault of the external zone.

Although the wavelet coefficient of the difference unbalance current changes according to the difference unbalance current, the coefficient is more suitable for the fault analysis as it increases only at the time of fault occurrence.

VII. CONCLUSION

This study focused on the characteristics of the system parameters, including the current phase (I_{ph}), current phase of the capacitor bank (I_{cap}), and difference unbalance current (I_{ub}), which were analysed based on the fault location. The results indicate that the current of the fault phase increases significantly when the fault occurs in the transmission line owing to the effect of the line impedance. Additionally, when the fault occurs in the capacitor bank, the change in the capacitance

phase changes the current phase of the capacitor bank. Owing to the unbalanced current phase of the capacitor bank, the difference unbalance current increases compared to its value observed under the normal condition.

Furthermore, owing to the effect of the capacitance phase, the characteristics of the current phase in a single capacitor bank and two capacitor banks were identical. This similarity may result in an error during the fault detection process of the unbalance relay. Therefore, DWT was applied to analyse the current phase of the capacitor bank. The obtained results indicate that when the current phase of the capacitor bank is considered in terms of a wavelet coefficient, the faults occurring in a single capacitor bank and two capacitor banks can be distinguished easily. As the wavelet coefficient occurs only at the time of fault occurrence, the fault detection can be verified from the time of the wavelet coefficient occurrence. Moreover, the magnitude of the wavelet coefficient can be used to locate the fault area as the magnitude of the coefficient is higher when the fault occurs in the internal zone than that when the fault occurs in the external zone.

Although the proposed system successfully distinguishes the faults occurring in the transmission line, single capacitor bank, and two capacitor banks, the simulated system is equivalent to a simple electrical network. In the future, a system that can be applied to complex networks should be developed to be more consistent with the actual system, which can be achieved using AI.

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