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RESEARCH ARTICLE

CAD Modeling of mm-Wave Circuits Incorporating Avalanche Noise Diodes

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ABSTRACT This paper proposes, for the first time, a completely stand alone avalanche diode model based on a C++ code. The code, implemented within the Advanced Design Systems (ADS) environment, describes the diode behavior in terms of impedance and noise, by means of equations for which no more look-up tables are required. This also contains a modification with respect to the original Gilden and Hines model. Although completely general, the model is presented and discussed using a 20 square microns p-i-n diode, previously published by the authors. In order to validate the model in complex systems, the aforementioned diode is placed within two circuits of practical interest that have been designed using a commercial 130-nm SiGe BiCMOS technology. In particular: (a) the diode is connected with a wide-band bias tee and an 6-dB attenuator, in order to create a Noise Source (NS) system block, and (b) the same NS structure is connected with an Low-Noise Amplifier (LNA). The two prototypes have been fabricated and experimentally characterized in terms of impedance and Excess Noise Ratio (ENR). Finally the experimental results have been compared with model simulations. In the frequency range from DC to 26.5 GHz the agreement between simulated ENR and experiments is within 1.4 dB for the prototype (a) and 1.9 dB for the prototype (b). The obtained results enable the adoption of avalanche noise diodes in Computer Aided Design (CAD) tools, for the prediction of integrated circuits performances, and confirms the reliability of the developed model.

INDEX TERMS Microwave noise sources, avalanche noise, noise diodes, built-in test equipments (BITE), user compiled model.

I. INTRODUCTION

The introduction of 5G and 6G technologies pushed forward the requirement of miniaturized, low cost and high reliability electronics. At the same time new technologies such as Silicon-Carbide (SiC), Silicon-Germanium (SiGe), Bipolar-CMOS (BiCMOS) and Gallium-Nitrite (GaN) enable the development of more and more complex systems.

With the increase of circuit complexity and miniaturization levels, a considerable fraction of the production costs rely on burdensome testing phases. According to recent estimates, chip testing is responsible for 40% of the total manufacturing costs [1], due to time consuming sessions as well as to the need of expensive millimeter-wave instruments (vector network analyzers, spectrum analyzers, noise figure meters, etc.). This is the reason why companies carry out random testing as approach to restrain costs. Testing is although an essential step in order to ensure high-quality and reliability. Those are aspects become essential whenever life-critical or mission-critical applications are expected, such as self-driving cars and aerospace. More and more chips will so need to be tested, making novel and cost-effective approaches essential.

An important step towards this direction is the Built-In Test Equipment (BITE) approach, i.e., the incorporation of diagnostic functionalities at the design stage by miniaturizing measurement instruments, which are so directly placed in the Silicon (Si) chip together with the mm-wave components, [2]. This methodology, which can be applied to single devices [3] as well as to systems such as receivers [4], can dramatically

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reduce the measurement cost and time. Moreover, the integration at chip level makes possible to carry out tests during the device operational life, i.e., once it is mounted on its target application, allowing continuous monitoring.

Within this context, the adoption of noise sources for radio frequency on-chip BITEs is starting to attract growing attention. In recent years several kind of noise sources have been studied ad also presented as for BITE applications: in [5] a 90-nm source-drain to bulk pn junction in CMOS technology was demonstrate and modeled; in [6], [7] an avalanche Schottky diode built in 55-nm SiGe BiCMOS was reported up to 325 GHz, in conjunction with a modeling description; in [8] the collector-base junction of a SiGe Heterojunction Bipolar Transistor (HBT) in a 130-nm SiGe BiCMOS process was demonstrated; in [9] two p-i-n diodes in 130 nm SiGe BiCMOS technology were demonstrated and modeled too; and finally in [10] several possible noise sources have been investigated, such as nFET and pFET source/drain-to-bulk junctions, diode-configured SiGe HBT emitter-base and collector-base junctions, and a p-i-n diode. All these noise sources can be used to inject, in a simple and reliable way, a known amount of noise power at the input of a system, e.g., a receiver input. In this perspective, noise is used as a test signal and, exploiting the well-known Y-factor method, receiver gain and noise figure (parameters that are very important for the future 5G and 6G applications) can be determined. Such an approach is quite similar to that adopted for the calibration of radio astronomy receivers and microwave radiometers [11], [12], [13], [14]; a technique which has also been recently applied to a fully integrated 60 GHz radiometer, fabricated in SiGe BiCMOS technology [8].

As already said, avalanche diodes can be used to generate a noisy electrical signal. They are controlled sources which can generate different noise power levels: being biased at 0 V, the so called off or cold state, they behave like a resistor at ambient temperature; on the contrary when biased in avalanche breakdown, also referred as on or hot state, they generate a large amount of noise power. They have been introduced in the 60s when they also received an extensive theoretical treatment [15], [16], [17], [18], [19], [20]. Even if they have been widely studied, compact avalanche diode models are not yet available in modern Computer Aided Design (CAD) tools, such as Advanced Design Systems (ADS) of Keysight Technologies and Cadence.

In [21] a circuit model suitable for CAD implementation was initially proposed. This model, however, did not completely account for the electronic tuning effects that happen in the device, such as the dependence of the diode avalanche frequency f_a with the square root of the diode bias current I_d. The modeling issue have been again debated in [22], where an approach to evaluate the diode noise behavior in terms of Noise Excess Ratio (ENR) was presented. Nevertheless the proposed approach did not allow to concurrently simulate the diode impedance and noise behavior. In [23] an important step towards this direction was made. Here a compact model that enables a comprehensive diode simulation, in terms of both impedance and noise, was reported. Every component was described by its equation, yet a look-up table was required for bias dependent parameters.

In this paper, for the first time, a completely stand alone diode model is presented. The device equations are implemented within the Keysight ADS environment as a *User Compiled Model* (UCM), a powerful approach which allows to define circuital blocks by C/C++ language. The developed code describes the diode behavior in terms of impedance and noise by means of equations for which look-up tables are no more needed. Without restrictions to the generality of the methodology, the code is adapted to the 20 μm^2 p-i-n diode described in [9] for what regards the bias dependent parameters. The most valuable aspects of the proposed code are the following:

- the diode avalanche noise current I_d is evaluated in the simulation phase as a function of the voltage applied to the diode directly on the schematic;
- all the bias dependent parameters are modeled by means of equations which are function of I_d;
- the diode can be simulated also in its off state;
- both impedance and noise behavior are computed.

To validate the proposed approach, complex simulation test benches are considered. In particular, the 20 μm^2 p-i-n diode is embedded in the following circuits:

(a) the diode is connected to a wide-band bias tee and an 6-dB attenuator, in order to create a Noise Source (NS) system block;
(b) the aforementioned NS is connected to a Low-Noise Amplifier (LNA) for 5G applications.

Both devices are then implemented in a 130-nm commercial SiGe BiCMOS technology and the comparison between measurements and simulation results are reported in the following. All the circuital blocks, except for the noise diode, are modeled within the Cadence environment according to the Infineon 130-nm SiGe BiCMOS technology. To this purpose the ''dynamic link'' between Cadence and ADS environments is used.

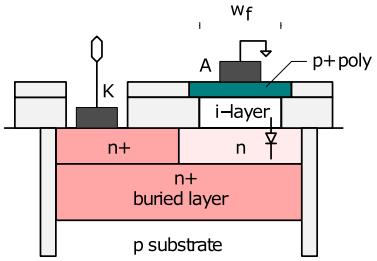
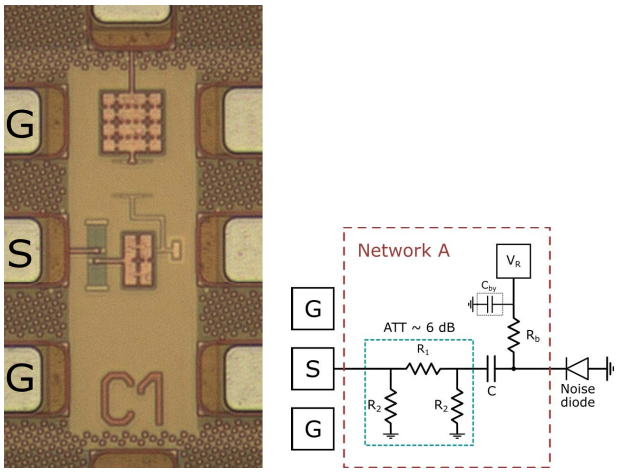


FIGURE 1. Structure of the integrated mm-wave p-i-n noise diode in 130-nm SiGe BiCMOS technology. The diode is derived from the collector region of a high-voltage bipolar and is constituted by N_f fingers in parallel. The width of each finger is $w_f = 1$ μm, whereas its length is $l_f = 5$ μm.

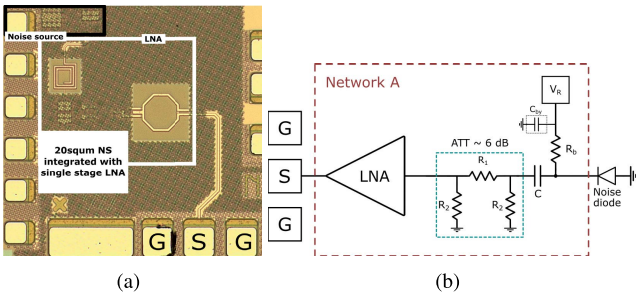
II. P-I-N DIODE

The device used in the experiments is the 20 μm^2 p-i-n diode whose structure is reported in Fig. 1. It is made using the



(a) (b)

FIGURE 2. Integrated mm-wave noise device in 130 nm SiGe BiCMOS technology. Fabricated prototype (a) and schematic (b). The device is made of a 20 μm^2 p-i-n noise diode connected to an integrated bias-tee and to a resistive attenuator (network A). The bias-tee is made up of $R_b = 300\,\Omega$, $C = 1$ pF and the bypass capacitance of $C_{by} = 2$ pF. The attenuator is composed of $R_1 = 37\,\Omega$ and $R_2 = 150\,\Omega$, which results in an attenuation factor of about 6 dB. A 24.2 μm long metal track connects the attenuator to the pad and behaves as short transmission line section.



(a) (b)

FIGURE 3. LNA with integrated noise source. Fabricated prototype (a) and schematic (b). The circuit is composed by a 20 μm^2 p-i-n noise diode, a bias-tee, a 6 dB attenuator and the LNA itself. The bias-tee is made up of $R_b = 300\,\Omega$, $C = 1$ pF and the bypass capacitance of $C_{by} = 2$ pF. The attenuator uses $R_1 = 37\,\Omega$ and $R_2 = 150\,\Omega$. A 45 μm long metal track connects the attenuator to the LNA input. The LNA output is routed to the GSG pad by means of a 286 μm long transmission line.

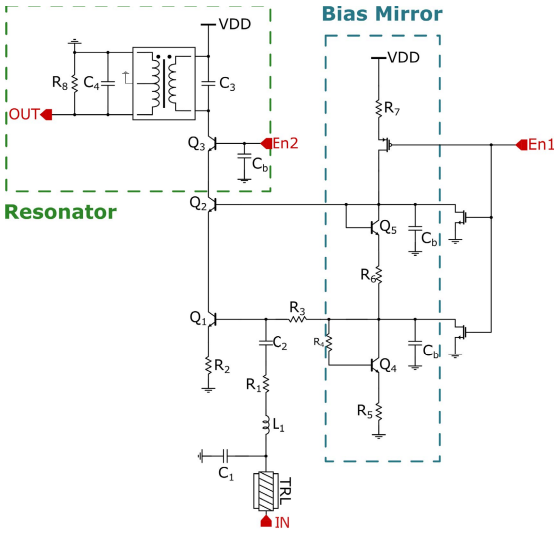


FIGURE 4. Detailed schematic of the LNA. Circuit parameters: (resonator section) $R_8 = 100\,\Omega$, $C_3 = 100$ fF, $C_4 = 40$ fF and $C_b = 601$ fF; (mirror section) $R_4 = 30$ kΩ, $R_5 = 50\,\Omega$, $R_6 = 301$ kΩ, $R_7 = 1$ kΩ; and $R_1 = 10\,\Omega$, $R_2 = 5\,\Omega$, $R_3 = 3$ kΩ, $C_1 = 30$ fF, $C_2 = 800$ fF and $L_1 = 425$ pH.

double epi concept detailed in [24] and [25]. The cathode region, K in the Fig. 1, is formed with implantation of the buried subcollector layer of a High-Voltage (HV) bipolar transistor, which results in the n+ layer of Fig. 1. The n (n epi-layer) and i-layer (intrinsic epi-layer) are then gown in consecutive steps. Finally the p+ poly (polysilicon) electrode is deposited and patterned to realize the diode anode A. The diode is isolated with shallow/deep trenches. A p/p+ guard ring, not shown is figure, is employed to keep the substrate to ground potential. According to this realization process, the 20 μm^2 diode area is implemented by $N_f = 4$ fingers, which are $w_f = 1\,\mu$m wide and $l_f = 5\,\mu$m long each.

III. COMPLEX CIRCUITS

The p-i-n diode is driven into avalanche breakdown to generate noise. As previously said, it is embedded within two complex circuits for the validation of the proposed comprehensive modeling methodology. In particular we considered: the wide-band noise source of Fig. 2 and the LNA with integrated noise source of Fig. 3.

A. NOISE SOURCE

Fig. 2 shows the fabricated prototype and schematic view of the considered integrated Noise Source (NS). The device is made of an 20 μm^2 p-i-n diode (see previous description), a wide band bias-tee for the diode biasing, and an 6-dB resistive attenuator. The bias-tee is made of a capacitance $C = 1$ pF, a resistance $R_b = 300\,\Omega$ and a bypass capacitor $C_{by} = 2$ pF. A Signal (S) pad, on the top of Fig. 2(a), is provided so to directly bias the diode on silicon by means of needle probe. The RF output of the bias-tee is then connected to a 6 dB attenuator. Such a network is in π-configuration, and uses 3 resistors, namely: $R_1 = 37\,\Omega$ and $R_2 = 150\,\Omega$. A 24.2 μm long metal track finally connects the attenuator to the Ground-Signal-Ground (GSG) pads.

B. LNA WITH INTEGRATED NOISE SOURCE

Fig. 3 shows the second complex circuit considered in the present study. The device is made of the previously described 20 μm^2 NS integrated with a LNA for 5G applications. The connection between noise source and the LNA is made by means of a 45 μm long metal track. The LNA output is then connected to the GSG pads though a 286 μm long metal track. Both metal tracks are assimilated to transmission line sections. The LNA schematic is illustrated in Fig. 4. Such a device is based on an already available Infineon LNA design, the layout of which is adapted to the presented experiment. The circuit is developed in a 130-nm proprietary

TABLE 1. Pad and metal track parameters.

R_{sub_p} (Ω)	C_{pad} (fF)	L_p (pH)	R_p (Ω)	L_k (pH)	R_k (Ω)
2.4	36.0	24.0	2.0	50.0	2.0

SiGe BiCMOS technology, and is realized in a triple-cascode configuration [26]. The output signal is coupled via an integrated transformer. Its primary winding constitutes, with the capacitor C_3, the tuned load of the last common-base stage. The secondary winding is also tuned with C_4 and loaded with R_6 to achieve a proper bandwidth. The amplifier is biased at 9 mA bias by means of a current mirror. Two enabling signals, namely *En1* and *En2*, are used to turn off the mirror section and to disconnect the resonator load. The latter option is needed to achieve a high isolation when the LNA is integrated into a transceiver front-end and the transmitter is active. This is why the triple cascode architecture, with 3 BJT in series, is preferred with respect to a simple cascode configuration adopting 2 BJT. Circuit simulations confirm the above considerations: turning Q3 off, an input-to-output isolation better than 70 dB is achieved.

The sample LNA covers the frequency range between 24.2 to 29.5 GHz that is allocated for terrestrial 5G services. In particular, its design specifications are: center frequency 24.5 GHz, −3 dB bandwidth 12 GHz, gain better than 13 dB, noise figure less than 4 dB, input and output reflection coefficients less than −10 dB.

IV. MODELING

In order to compare measurements with simulations, all the elements of the considered prototypes need to be accurately modeled. To this purpose, the passive and active components of the considered circuits have been described using the Process Design Kit (PDK) of the 130-nm Infineon SiGe BiCMOS technology, that is available for Cadence.

Regarding the GSG pads, they were modeled along with the 24 μm metal track (used for connection purpose) with the equivalent circuit of Fig. 5. In particular, the pad is represented by the series of C_{pad} and R_{sub_p}, the latter one related to the substrate losses. The metal track behaves as a short transmission line and is represented by R_p, L_p, and R_k and L_k, for the skin effect. Those parameters, the values of which are reported in Table 1, are capable to accurate describe the pad behavior up to 40 GHz and have been determined by careful measurements of sample structures.

A. DIODE MODELING

The small-signal equivalent circuit of a diode in avalanche region is shown in Fig. 6(a). As described in [7], [9], [16], and [21], it consists of 9 elements: R_s, Z_d, R_j, L_a, C_a, C_{sub}, C_p, R_{sub} and $\bar{i}^2_{na}$. In particular, the parallel of C_a and L_a describes the diode avalanche region, where carriers are formed by impact ionization. The component Z_d models the

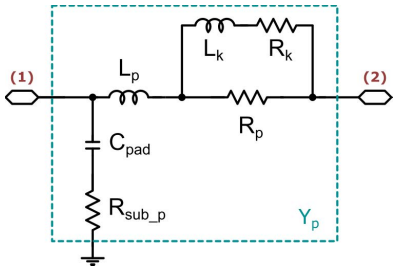


FIGURE 5. Equivalent circuit employed to model the pad and metal track. C_{pad} and R_{sub_p} take into accounts the pad capacitance and resistance parasitics. L_p is the parasitic inductance of the metal track, while R_p, R_k and L_k consider the power losses and skin effects of the track. Port 2 is the one connected to the silicon integrated components.

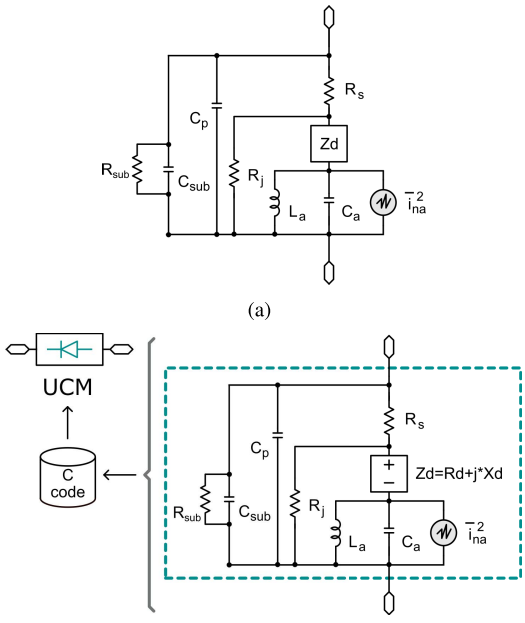


FIGURE 6. Small-signal equivalent circuit of the p-i-n diode in avalanche region (a). The circuit is implemented in C code, as a *User Compiled Model* within ADS of Keysight Technologies (b). The current source $\bar{i}^2_{na}$ accounts for the avalanche noise generation within the device.

drift zone where no carriers are formed but space-charge and transit-time effects are significant. The capacitance C_p is a parasitic capacitance, and C_{sub} and R_{sub} accounts the substrate effects. Resistances R_j and R_s represent, respectively, the depletion zone resistance and the contact resistance. R_s also accounts for microplasma and electro-thermal coupling effects [17], [20]; contributions which are responsible for the low-frequency behavior. It is given by:

$$R_s = R_0 + \frac{R_i}{1 + (\omega\,\tau_i)^{\gamma}} \tag{1}$$

where ω is the angular frequency, R_0 is the contact resistance value at high frequency, while $R_0 + R_i$ is the same resistance at DC, and τ_i represents a suitable time constant. The exponent γ, which determines the transition between low to high frequency, is assumed equals to 2. Moreover, R_0 and R_i are

TABLE 2. Bias independent parameters.

m_0 ($1/V^2$)	ϵ_r	v_d (m/s)	l_a (nm)		l_d (nm)		τ_x (ps)	τ_i (ps)
			ON	OFF	ON	OFF		
0.0157	11.9	1×10^5	60	36.3	69	36.3	0.52	425

bias-dependent parameters. The avalanche noise generation is described by the current generator $\bar{i}^2_{na}$.

The ionization coefficient derivative with respect to the E-field, α', is modeled as:

$$\alpha' = m_0 V_R^{\beta} \tag{2}$$

where V_R is the reverse diode voltage, the exponent β is assumed equal to one (see Appendix A) and m_0 is a bias-independent parameter, measured in $1/V^2$. The complete description of the model, as well as all the equations, can be found in [9].

Avalanche diode models are not yet available in modern CAD tools, thus circuit simulations involving this kind of devices are not possible. A compact solution to this limit comes from the approach described in Fig. 6(b). Within the ADS environment of Keysight Technologies, the avalanche diode equivalent circuit can be embodied in a *User Compiled Model (UCM)* component. This kind of components allows the user to define an element by means of a C/C++ code, creating a new "drag&drop" instance. Starting from the generation of the device symbol, a default code structure can be generated. From this code, the user can describe the desired device behavior by means of equations or matrix definitions, having complete access to parameters, stimulus controls, analysis type, and pin voltages. Moreover the user can define which and how many parameters can be entered from the device schematic view. The UCM Application Program Interface (API) provides a selection of functions specifically designed for the C/C++ code description. In particular, the C++ code written for the diode equivalent circuit is made up of the following blocks:

- constant definition section, where physical constants and all the non bias dependent parameters listed in Table 2 are defined;
- *pre_analysis()* is a routine recalled one time for each analysis and employed to acquire the parameters N_f, w_f, and l_f used for the diode area evaluation. Those parameters are kept fixed at this point;
- *analyze_lin()* loads the linear or constant components of the equivalent circuit, that for the present discussion are the components C_{sub}, C_p and R_{sub}. These components do not add value to the considered diode, indeed they are set to C = 0 F for the capacitances and R_{sub} = 1 TΩ for the resistance. Moreover, the equivalent circuit needs to be ideally formed: every components must be declared between two pins by means of the *add_y_branch()* function;

TABLE 3. Polynomial fitting dataset.

V_R (V)	I_0 (mA)	R_j (Ω)	R_0 (Ω)	R_i (Ω)
10.78	1.0	4990	24	70
10.84	1.5	4930	15	26
10.90	2.0	3870	10	4
11.02	3.0	3881	10	2
11.14	4.0	4000	10	2

TABLE 4. Polynomial fitting coefficients.

	a_3 (Ω/A^3)	a_2 (Ω/A^2)	a_1 (Ω/A)	a_0 (Ω)
R_j	$2.75e^{10}$	$8.24e^7$	$-1.35e^6$	$6.33e^3$
R_i	-17.6	32.7	-9.4	-0.25
R_0	$-2.16e^9$	$1.97e^7$	$-5.77e^4$	64.3

- *analyze_nl()* is used to load the nonlinear part of the model, hence all the other diode components. Every instance is described by its equation, so that its value can be autonomously evaluated. The components are here declared between two pins by means of the *add_gc()* function;
- *analyze_ac()* is required for linear simulations in which nonlinear elements contribute with their small-signal responses. The non linear contributions of the diode equivalent circuit are here again described by their equations whose value is then assigned to a conductance or susceptance component, as the ADS function requires, with *add_y_branch()*. Information about the pins are required again in this case;
- *analyze_ac_n()* is the core function for the noise diode behavior, since the noise contribution of a non linear element is here described. The avalanche noise generation is reported in this section of the code.

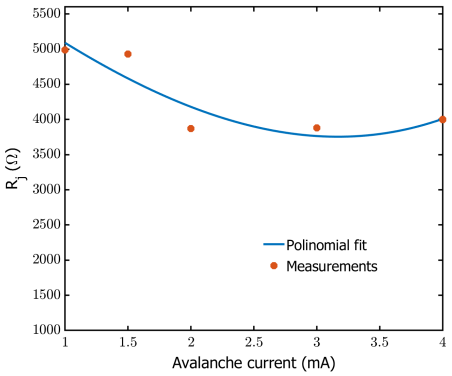
Another aspect that makes the presented implementation particularly attracting is the evaluation of the avalanche current. The current I_d employed in the simulation phase and needed for the parameters calculation is implemented inside the code according to:

$$I_d = \begin{cases} g_a(V_R - V_b), & V_R > V_b \\ 0 & elsewhere \end{cases} \tag{3}$$

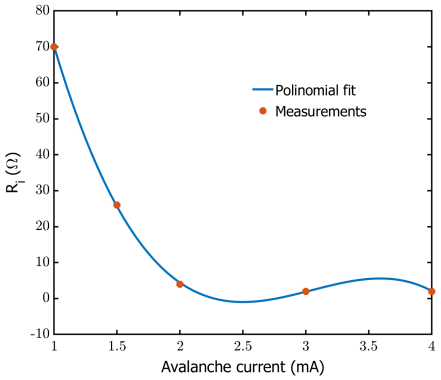
being $g_a = 8.4\,\text{mA/V}$ the slope factor and $V_b = 10.68\,\text{V}$ the breakdown voltage, [9]. The voltage V_R is calculated in the simulation phase acquiring the voltage value at the diode pin. This allows the circuit simulator to compute the avalanche (biasing) current of the device.

Just as the avalanche current I_d, the diode parameters R_j, R_i and R_0 are described through equations, function of I_d. Starting from the measured dataset of Table 3 a polynomial curve fitting routine was executed for a 3^{rd} degree polynomial $y = a_3x^3 + a_2x^2 + a_1x + a_0$, with $x = I_d$. The coefficients

resulting from the fitting algorithm are listed in Table 4. A centering and scaling transformation which improves the numerical properties of both the polynomial and the fitting algorithm is considered for the R_i polynomial, for which $x = (I_d - mean(Id))/std(Id)$. Comparison between the measured data points and the polynomial fitting curves is reported in Fig.7. The R_i and R_0 fittings feature a maximum error of less 1 Ω, whereas the R_j fitting is within 10%.



(a)



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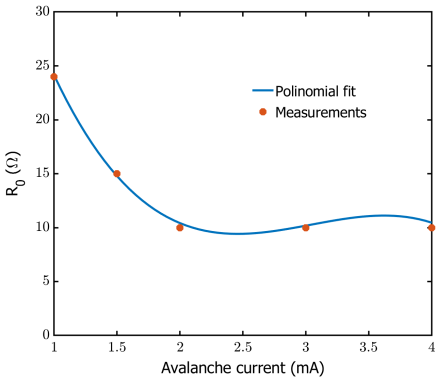


(c)

FIGURE 7. Comparison between the polynomial curve fitting implemented in the UCM and the measured data point for the parameters: R_j (a), R_i (b), and R_0 (c).

Within the described UCM code, the diode off state is also taken into account. When a diode is off it is modeled with its contact resistance R_s in series with the junction capacitance C_j. Considering the equivalent circuit of Fig. 6, in a zero bias condition the diode equivalent circuit reduces to R_s in series with C_a and the imaginary part of Z_d, i.e., C_d. The series of the two capacitances can so be adjusted to equate the capacitance C_j. In the UCM code this is accomplished by changing the l_a and l_d values to those reported for the off state in Table 2. In such a way the diode off state can be considered a limit case of the avalanche condition.

The noise behavior is described as the Excess Noise Ratio (ENR) parameter. It is defined as:

$$ENR = \frac{T_e^h - T_e^c}{T_0} \tag{4}$$

where T_e^h is the hot temperature (diode in on state), T_e^c is the cold temperature (diode in off state), and $T_0 = 290\,\mathrm{K}$ is the IEEE standard temperature. According to [27], the noise temperatures T_e^h and T_e^c are "effective" noise temperature. Therefore the ENR is evaluated on a nonreflecting load $R_l = 50\,\Omega$, whose thermal noise is not considered in the simulation phase (equivalent to consider the load resistor at 0 K). Simulations are so required for the diode on/off states.

V. METHODS

To verify the proposed modeling approach the two described complex circuits have been fabricated with the Infineon 130-nm foundry (see Fig. 2 and Fig. 3) and experimentally characterized. Such a characterization requires the measurement of both impedance and generated noise at different frequencies and bias conditions. All the measurements were carried out by means of a probe station equipped with micro-manipulators and 100 μm pitch GSG coplanar probe tips, that can operate up to 40 GHz.

The impedance measurements were executed with the Keysight PNA N5230A Vector Network Analyzer (VNA). The instrument was calibrated by means of an on-wafer Short-Open-Load-Through (SOLT) procedure, employing the CS-5 calibration substrate from GGB Industries. In such a way, the reference plane can be located at the silicon level, i.e., at the probe tip contacts.

Two additional test structures have been fabricated on the test chip as to derive the pad and metal track equivalent circuit network Y_p of Fig. 5. The first structure has Port 2, in Fig. 5, connected to an open circuit, while for the second structure Port 2 is connected to a short circuit. The parameters values reported in Table 1 are obtained by these two measurements with a best fitting procedure.

The setup adopted for the noise characterization is the one illustrated in Fig. 8 and used for both the complex circuits. It is based on the Noise Figure Meter (NFM) Measurement System, composed by the HP 8970B Noise Figure Meter, the HP 8971C Noise Figure Test Set, and the HP 8673B Signal Generator. With this NFM system, spectral noise power density measurements up to 26.5 GHz can be carried out. Referring to Fig. 8, the experimental setup has two measurement mode: the calibration mode with the C pins connected to A, and the measurement mode when the B pins are connected to

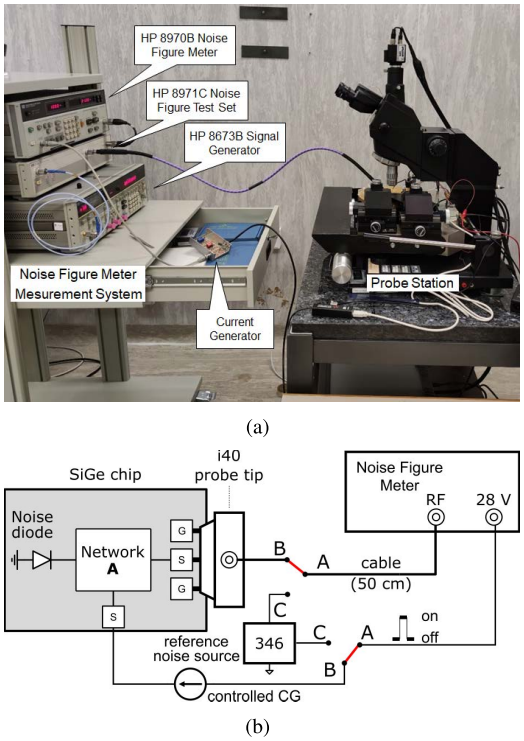


FIGURE 8. Experimental setup employed for the on-chip ENR characterization of the considered integrated device: photograph (a) and schematic (b). Measurements are carried out with a Noise Figure Meter Measurement System: an HP 8970B Noise Figure Meter, an HP 8971C Noise Figure Test Set and an HP 8673B Signal Generator. A reference noise source (Agilent 346C-K01) is used to calibrate the system. The considered test chip is contacted with a 100 μm pitch GSG probe tip (Picoprobe model 40a, up to 40 GHz). The diode is biased by means of a constant current generator (CG); the biasing pad is touched with a needle. Two SiGe test chips are considered: they are made of a p-i-n noise diode connected to the two different complex circuits described in Section III (Network A in the figure). There are two configurations of the system: measurement (B-A) and calibration (C-A).

A. In both modes, the noise sources are biased with the 28 V DC port of the NFM. For the on-wafer noise source, the NFM DC port is connected to a current source, displayed in Fig. 8, which ensures a controlled diode avalanche current.

The complex circuit ENR evaluation is reduced to the measurement of the equivalent noise temperature at the Device Under Test (DUT) output. This problem is identical to that discussed by Daywitt [28], Randa [29] at NIST, and successively applied in several other works [30], [31], [32]. To this purpose two experiments are needed: the calibration, carried out with a laboratory (or standard) noise source, and the measurement of DUT with its integrated noise diode.

In the calibration phase the equivalent noise temperature T_R and the power gain G_R of the measurement receiver are determined. To this purpose the Agilent 346C-K01 laboratory noise source was adopted. Its ENR is factory provided up to 50 GHz. As illustrated in Fig.9, noise source and NFM were connected by means of a 50-cm cable. Phase and temperature stable coaxial cables from MegaPhase were used in all the experiments. As a result, T_R and G_R of the cable-NFM system are found with the calibration.

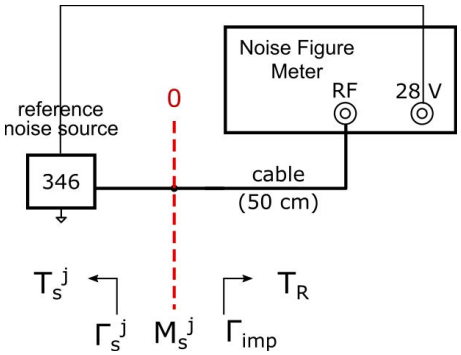


FIGURE 9. Schematic representation of calibration phase and all the parameters required for the data evaluation. The Agilent 346C-K01 reference noise source is directly connected to the NFM.

According to the Randa notation we will indicate with the capital P the available noise powers and with the lowercase p the delivered noise powers. The available noise power at the input of the cable-NFM system $P_{inp}^{s,j}$, with the reference noise source (superscript s) connected is given by:

$$P_{inp}^{s,j} = k_B \left(T_s^j + T_R\right) B \tag{5}$$

where $j = h, c$ indicates the state (h for hot and c for cold) of the reference noise source, $k_B = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant, and B is equivalent noise bandwidth of the measurement system. Due to impedance mismatches in the input section (reference plane "0" in Fig.9), however, only a fraction of such a power is delivered to the instrument and so measured. The ratio between delivered power and available power is known as the mismatch factor M, so that we can write:

$$p_{inp}^{s,j} = M_s^j P_{inp}^{s,j} \tag{6}$$

Note that M_s^j is a real number (ratio between real powers) less or equal to one, which depends on the noise source state (superscript j), since the noise source impedance changes in on/off conditions (although not too much). From microwave circuit theory we know that the mismatch factor is expressed by:

$$M_s^j = \frac{\left(1 - \left|\Gamma_s^j\right|^2\right)\left(1 - \left|\Gamma_{inp}\right|^2\right)}{\left|1 - \Gamma_s^j \Gamma_{inp}\right|^2} \tag{7}$$

Γ_s^j being the state-dependent noise source reflection coefficient and Γ_{inp} the cable-NFM reflection coefficient. In our study these reflection coefficients have been measured with a VNA before the noise experiments (characterization of the experimental setup).

The NFM is a very stable receiver that measures the noise power delivered to its internal detector. During the calibration phase such a power can be written as follows:

$$p_{out}^{s,j} = k_B M_s^j \left(T_s^j + T_R\right) G_R B \tag{8}$$

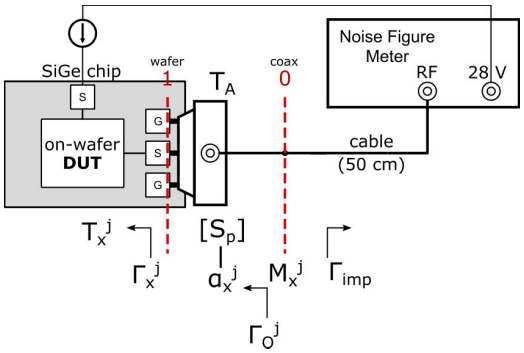


FIGURE 10. Schematic representation of measurement phase and all the parameters required for the data evaluation. A probe tip, characterized in terms of S-parameters, is necessary to carry out on-wafer measurements.

where, technically speaking, G_R is the operating power gain of the NFM receiver. As in Randa we assumed T_R approximately independent of the source impedance, although no isolator is present in our system.[1]

The HP8970B NFM normalizes the hot and cold powers to $k_B\,T_0\,B$, and directly measure them by means of the instrument "special functions":

$$S_s^h = \frac{p_{out}^{s,h}}{k_B\,T_0\,B} = M_s^h\,\frac{T_s^h + T_R}{T_0}\,G_R \tag{9a}$$

$$S_s^c = \frac{p_{out}^{s,c}}{k_B\,T_0\,B} = M_s^c\,\frac{T_a + T_R}{T_0}\,G_R \tag{9b}$$

where T_a is the ambient temperature and $T_s^c = T_a$. Solving the above system of equations with respect to the unknowns T_R and G_R gives:

$$T_R = \frac{M_s^h\,T_s^h - Y_s\,M_s^c\,T_a}{Y_s\,M_s^c - M_s^h} \tag{10}$$

$$G_R = \frac{\left(S_s^h - S_s^c\right)\,T_0}{M_s^h\,T_s^h - M_s^c\,T_a + \left(M_s^h - M_s^c\right)\,T_R} \tag{11}$$

having defined $Y_s = S_s^h/S_s^c$ as the Y-factor. Note that the equivalent noise temperature is determined by Y_s, which is a ratio of normalized power measurements. Whereas the operating power gain requires the absolute measurements of S_s^h and S_s^c, which is more challenging since it implies a high stability of the instrumentation.

In the measurement phase the developed on-wafer DUTs were considered and, for each of the two complex circuits, the output ENR was determined by switching on/off the integrated noise diode. Fig. 10 illustrates the experimental setup. A GSG probe tip was used as an interface between DUT and NFM. The evaluation of the probe tip available power gain was mandatory in order to move the measurements from the coaxial reference plane ("0" in the figure) to the on-wafer DUT output port (reference plane "1" in the figure). According to [30] such a gain can be expressed as:

$$\alpha_x^j = \frac{\left(1 - |\Gamma_x^j|^2\right)\,|S_{21}|^2}{|1 - S_{11}\,\Gamma_x^j|^2 - |S_{22} - \Delta\,\Gamma_x^j|^2} \tag{12}$$

where S_{kl}, $k, l = 1, 2$ are the probe tip scattering parameters, $\Delta = S_{11}\,S_{22} - S_{21}\,S_{12}$ is the scattering matrix determinant, and $j = h, c$ stands again for the integrated noise diode state. In our study the probe tip scattering parameters have been found experimentally by measuring the short-open-load standards of a calibration substrate with a VNA. In particular, we used the CS-5 calibration substrate of GGB Industries.

Similarly to (8), the noise power delivered to the internal NFM detector for the DUT (superscript x) measurement phase can be written as:

$$p_{out}^{x,j} = k_B M_x^j \left[\alpha_x^j T_x^j + \left(1 - \alpha_x^j\right)\,T_a + T_R\right] G_R B \tag{13}$$

These powers are due to three contributions, namely: the DUT contribution T_x^j multiplied for the probe tip available power gain α_x^j, the noise contribution due to the probe tip at ambient temperature T_a, and the receiver noise contribution T_R. The mismatch factor M_x^j is evaluated at the reference plane "0" (input section of the cable-NFM system), as shown in Fig. 10.

Normalizing the noise powers (13) to $k_B\,T_0\,B$ one obtains:

$$S_x^h = M_x^h\,\frac{\alpha_x^h T_x^h + \left(1 - \alpha_x^h\right)\,T_a + T_R}{T_0}\,G_R \tag{14a}$$

$$S_x^c = M_x^c\,\frac{\alpha_x^c T_x^c + \left(1 - \alpha_x^c\right)\,T_a + T_R}{T_0}\,G_R \tag{14b}$$

Note that, in this case, is not possible to assume $T_x^c = T_a$ since one of the studied complex circuits includes a LNA. Solving the system of equations (14) with respect to the unknowns T_x^h and T_x^c gives:

$$T_x^h = \frac{1}{\alpha_x^h}\left[\frac{S_x^h}{M_x^h G_R}T_0 - \left(1 - \alpha_x^h\right)\,T_a - T_R\right] \tag{15a}$$

$$T_x^c = \frac{1}{\alpha_x^c}\left[\frac{S_x^c}{M_x^c G_R}T_0 - \left(1 - \alpha_x^c\right)\,T_a - T_R\right] \tag{15b}$$

that are the equations adopted to process the DUT measurements. These above temperatures, however, are "available" noise temperatures. Since the ENR is defined using "effective" noise temperatures a final step is needed. According to [27] the effective temperatures are:

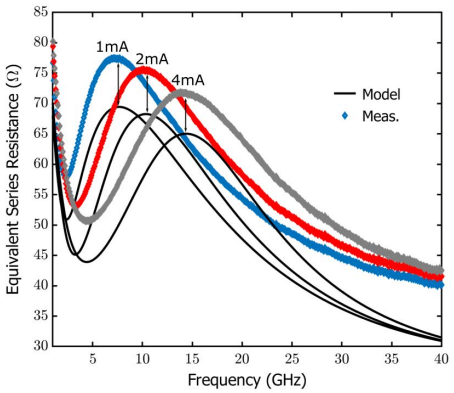
$$T_{x,e}^h = \left(1 - |\Gamma_x^h|^2\right)\,T_x^h \tag{16a}$$

$$T_{x,e}^c = \left(1 - |\Gamma_x^c|^2\right)\,T_x^c \tag{16b}$$

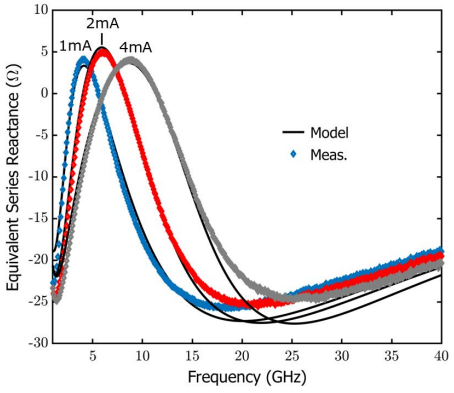
$\Gamma_x^j, j = h, c$ being the output reflection coefficient of the DUT seen at the reference plane "1" of Fig. 10. From (16) the ENR is found as a direct application of its definition (4).

All the noise measurements were systematically acquired by means of a Python code. The code controls the NFM acquisition system with the HP-IB (IEEE 488) interface. For each frequency point, it gathers the Y-factor and the so-called

[1]The dependence of the NFM noise figure (and thus that of T_R) from the source impedance is, in general, quite complex and is related to the concept of constant noise figure circles. A rigorous approach based on the determination of the full NFM noise parameters, although known in the literature, is outside the scope of this work.



(a)



(b)

FIGURE 11. Small-signal impedance versus frequency of the developed single-chip noise source composed by the 20 μm^2 p-i-n diode, the bias-tee and the 6 dB attenuator: real (a) and imaginary (b) parts. Measurements and simulations are compared for several diode avalanche currents. In both cases the pad parasitics are de-embedded from the measurements. Discrepancies between measurements and model show a maximum value of 11 Ω and 4 Ω for the real and imaginary parts, respectively, over the whole frequency range and for all the considered avalanche currents.

"Phot" and "Pcold" that, in the HP8970B terminology, correspond to S^h and S^c. The averaging factor is set to 16 and each acquisition is repeated 25 times, lasting about 12.5 s. The data is then saved to a file for the post processing operations.

VI. RESULTS

In the following section the quantitative data are presented and discussed. Experimental results and comparisons with the developed model are shown for both the considered prototypes. Every subsection starts with the impedance results followed by the ENR ones.

A. NOISE SOURCE

The fabricated prototype of Fig.2 has been characterized in terms of impedance and ENR up to mm-wave frequencies.

1) IMPEDANCE RESULTS

First, the device impedance was measured for different diode bias conditions in the avalanche state. As previously illustrated, this operation was carried out by means of a probe station and VNA, required to obtain reliable and high accuracy data. The resulting impedance is shown Fig.11. The figures show the real and imaginary parts of the impedance of the 20 μm^2 NS prototype seen at the wafer level, i.e., at the input of the GSG pads. Measurements for three different diode avalanche current are show, in particular: 1, 2, and 4 mA.

Following the measurement session, impedance simulations were carried out. The diode, as described in Sec. IV, is accounted as an UCM within the ADS Keysight environment. This UCM component is then connected to the rest of the Prototype 1 circuitry, implemented within the Cadence environment (a "dynamic link" exists between the two software tools). The simulation results are shown in Fig. 11 with solid black lines. Comparing the curves, it is clear how the model correctly predicts the impedance over the whole frequency range and for different avalanche currents. Discrepancies that arise comparing the graphs for all the considered avalanche currents have a maximum value of 11 Ω and 4 Ω for the real and imaginary parts, respectively. Those variations are partially due to the accuracy of the diode model itself, which is within ±20% with respect to the measurements for all the considered bias conditions, [9].

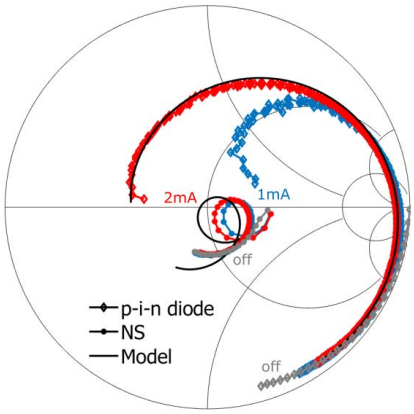


FIGURE 12. Measured reflection coefficients of the 20 μm^2 p-i-n diode and the 20 μm^2 noise source. In both cases the pad contribution are included. In the off condition the diodes are biased at 0 V. The NS implementation shows a much higher matching respect to the pure diode. As reference, a model simulation for both devices is reported for the 2 mA biasing current.

As reported in [33], the use of suitable on-chip attenuators allow to acquire a remarkable improvement in terms of matching, compared to a diode alone. As further proof of that, Fig. 12 shows the comparison between the p-i-n diode reflection coefficient and that of the proposed noise source. Both devices are reported for 1 and 2 mA avalanche current biasing, and for the off state. These data include both the pad and metal track parasitics.

2) ENR RESULTS

The ENR was measured following the approach described in Sec. V, employing the setup of Fig. 8, and the processing

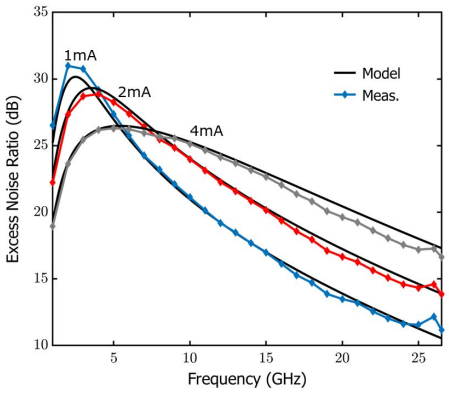


FIGURE 13. ENR as a function of frequency for the developed noise source. Measurements and UCM simulations are displayed for several diode avalanche currents. The pad contributions are considered. In the whole frequency range the deviation between model and experiments is within 1.4 dB.

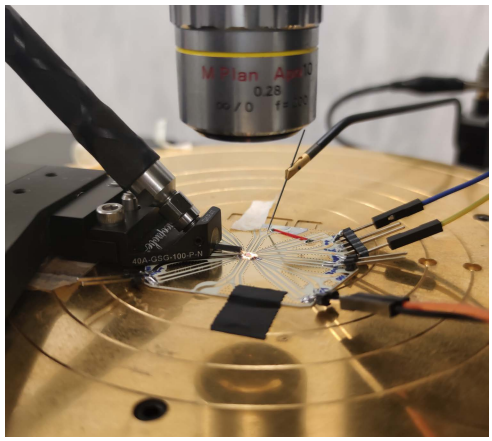


FIGURE 14. LNA with integrated noise source, during the on-wafer noise measurements. The picture is taken under the Alessi REL-4500 probe station: it is possible to see the Picoprobe 40a 100 μm pitch GSG probe tip touching the die, the SPI cables coming from an Arduino Uno board and the needle probe used to bias the integrated noise diode.

routine detailed from (8) to (16). The measurement system was carefully characterized in terms of instrument gain G_R and equivalent noise source T_R as a result of the calibration phase. Furthermore, mismatch factors have been determined for both the calibration M_s^j and measurement phase M_x^j.

The measured ENR is reported in Fig. 13 as a function of frequency and for three biasing currents, namely: 1, 2 and 4 mA. The whole Noise Figure Meter (NFM) frequency range up to 26.5 GHz is acquired. Again, circuit simulations based on the developed model (black lines) are compared to the experiments (color lines). The maximum deviation between model and experiments is of 1.4 dB, for all the considered frequencies and bias conditions. As a matter of comparison, the agreement between model and experiments for the $20\,\mu\text{m}^2$ p-i-n diode alone is ± 1.5 dB at all frequencies, [9], so the discrepancies can be attributed to the noise diode model parameters themselves.

B. LNA WITH INTEGRATED NOISE SOURCE

The second complex circuit that has been considered is constituted by a LNA with integrated noise source, see Fig. 3. As for the previous case, it has been characterized in terms of both impedance and ENR up to mm-wave frequencies.

1) IMPEDANCE RESULTS

Impedance measurements were carried out at the same avalanche currents adopted for the previously described noise source. The probe station and the VNA were again required to ensure reliable and accurate data. A close up of the device during the test operations is shown in Fig. 14. An Arduino board provided the 3.3 V LNA biasing and enabled, via a SPI connection, the control pins of the LNA (En1 and En2 in the circuit schematic of Fig. 3).

The impedance measurement results are reported in Fig. 15. Such a figure shows the real and imaginary parts of the impedance seen at the circuit output (noise source and LNA). In these experiments the integrated noise source is on, and data are captured for 1, 2, and 4 mA avalanche currents. As expected, the output LNA impedance is not influenced by the diode bias currents (which induces diode impedance variations), and all the curves collapse one over another. This behavior is confirmed by simulations, and is due to the high reverse isolation of the designed gain stage. This comparison highlight the capability of the model to correctly predict the device impedance behavior of a complex circuit over a wide frequency range. Note that at low-frequencies there is a significant mismatch between the integrated noise source and the LNA, but this is correctly modeled.

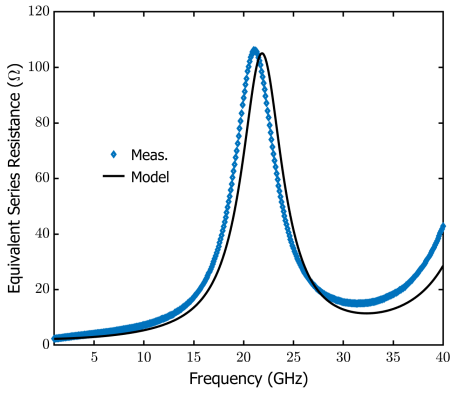
2) ENR RESULTS

The ENR is measured as in the previous case and the measurement system is carefully characterized both in terms of instrument parameters and mismatch factors, so to acquire a more accurate on-wafer noise temperature estimation.

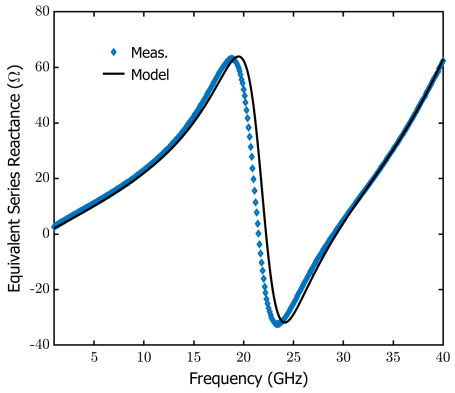
The measured ENR is finally shown in Fig. 16. It is reported for the same avalanche currents (1, 2, and 4 mA) up to 26.5 GHz. Again the experiments are compared to the simulations. The maximum deviation between model and experiments for all the considered frequency and bias conditions is better than that 1.9 dB. Such an agreement, which is quite impressive, is, at the best author knowledge, the first result of this kind ever reported in the scientific literature. Furthermore, from the analysis of Fig. 13 and Fig. 16, it is apparent that the generated noise power can be controlled by acting on the avalanche current, and this effect is accurately predicted. Multi-level noise source can thus be devised allowing, for example, the correction of detector linearity errors in radiometers.

3) STAND ALONE LNA

As a final check, a standalone LNA prototype (i.e. the LNA without the noise source) is fabricated and measured. Table 5, reports the results obtained in this case, showing that the



(a)



(b)

FIGURE 15. Small-signal impedance versus frequency of the developed noise source connected to the LNA: real (a) and imaginary (b) parts. Measurements and simulations are compared for several diode avalanche currents. Even if the current is varied, both model and measurements curves are collapsed one over another, resulting in the diode impedance to be completely transparent at the output of the LNA. In both cases the pad contributions are considered.

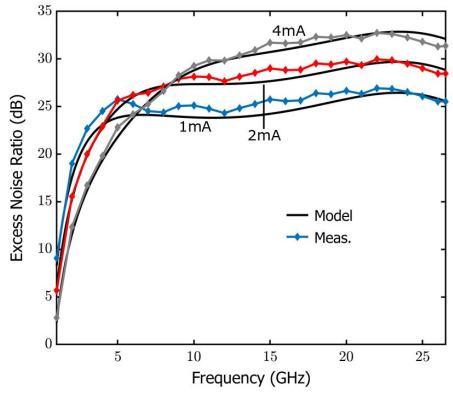


FIGURE 16. ENR as a function of frequency for the developed device made up of the noise source connected to the LNA. Measurements and simulations are considered for several diode avalanche currents. The pad contributions are taken into account. In the whole frequency range the deviation between model and experiments is within 1.9 dB.

LNA simulations are in good agreement with the experiments. The comparison is carried out at center frequency, i.e. at 24.5 GHz. The LNA has an overall current consumption of 12 mA at 3.3 V supply (cascode, current mirror and control stages). The simulated output 1-dB compression point (P1dB) and third-order intercept point (OIP3) are equal to 2.3 and 14.1 dBm respectively.

TABLE 5. LNA performance at center frequency.

	$\|S_{11}\|$ (dB)	$\|S_{21}\|$ (dB)	$\|S_{12}\|$ (dB)	$\|S_{22}\|$ (dB)	NF (dB)	-3 dB BW (GHz)
sim.	-9.3	13.8	-64.5	-8.4	3.2	12.9
meas.	-9.0	13.5	-57.0	-8.7	3.6	12

VII. CONCLUSION

In this paper, for the first time, an avalanche noise diode model based on a C++ code is presented, enabling a stand alone CAD component of this kind. The device is described in its equivalent circuit and noise behavior with equations implemented inside the C++ block. This implementation is particularly attracting since it allows to calculate the diode avalanche noise current as a function of the reverse voltage applied to the diode, taken directly from the schematic, and all the parameters which were previously bias dependent can now be evaluated by means of polynomial approximations. These make the previously required look-up table useless. Moreover the diode still accounts for the off state. With this improved model, complex circuit-level and system-level simulations can be easily performed. In demonstration of that, two circuital blocks embedding a $20\,\mu m^2$ p-i-n diode were considered: in the first case the diode is connected to a bias-tee and to a 6-dB attenuator as to form a single-chip noise source. In the second case such a noise source is connected to a LNA for 5G applications. Comparison between measurements and simulations, in terms of impedance and noise, are reported in this work. In particular, the modeled ENR is within 1.4 dB and 1.9 dB in the whole frequency band from DC to 26.5 GHz, for the noise source and the noise source with LNA respectively. The presented results confirms the reliability of the simulated systems outcomes. Furthermore, the generated noise power can be controlled acting on the avalanche current, and this effect is accurately predicted by the model. Multi-level noise source can thus be devised allowing, for example, the correction of detector linearity errors in top-class receivers and radiometers.

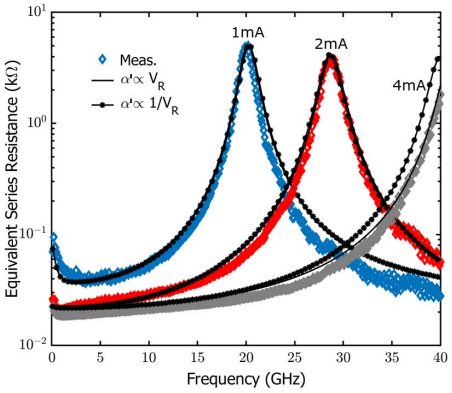
Extending the presented results to other avalanche noise diode previously published opens the way to the creation of a noise diodes CAD library, useful for the prediction of integrated circuits performance.

APPENDIX A
IONIZATION COEFFICIENT

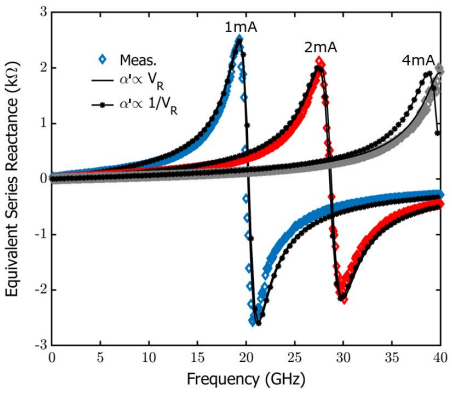
This appendix discusses the ionization coefficient derivative with respect to the E-field α', that depens on the reverse diode voltage V_R as illustrated in (2). The main modification with respect to the approach presented in [9], relies on the value

TABLE 6. Bias independent parameters.

	β	m_0 $1/V^2$	τ_x (ps)
This work - ($\alpha' \propto V_R$)	1	0.0157	0.52
[9] - ($\alpha' \propto 1/V_R$)	-1	1.86	0.48



(a)



(b)

FIGURE 17. Small signal impedance of the 20 μm^2 p-i-n diode in avalanche as a function of frequency: real (a) and imaginary (b) part. Measurements are compared with the presented approach depicted with solid black lines and the approach described in [9] reported with black circle markers. The real part is drawn with the y-axis in log scale.

attributed to β which determines the relationship between α' and V_R. Indeed, while in [9] α' was taken inversely proportional to V_R, from which $\beta = -1$; in the above discussion it is considered proportional to V_R, hence $\beta = 1$. As obvious, this different approach influences also the value taken for m_0. At the same time the value of the τ_x parameter needs to be slightly adjusted. Values for those parameters in the two different approaches are reported in Table 6.

The most valuable impact of such a different relationship can be observed considering the p-i-n diode alone. Fig. 17 shows the small signal impedance of the diode, in which measurements are reported with markers, the approach presented in this work is depicted with black solid lines, while the approach reported in [9] is shown in black markers. The figure

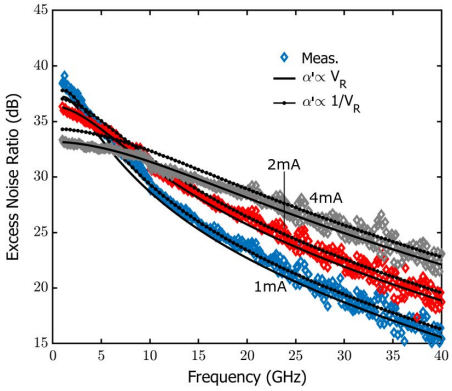


FIGURE 18. ENR of the 20 μm^2 p-i-n as a function of frequency. Measurements are compared with the presented approach depicted with solid black lines and the approach described in [9] reported with black circle markers.

represents the real (a) and imaginary part (b) of the diode intrinsic impedance. As apparent from the image, the major improvement on the diode modeled impedance can be seen at high frequency in the 4 mA case. Indeed, with the presented approach the modeling error lowers from a maximum of 2500 Ω to 500 Ω for the real part and from 2000 Ω to 200 Ω for the imaginary part. Considering the diode ENR, reported in Fig. 18, again the major improvement is at 4 mA. In this case the ENR maximum error lowers from 1.4 dB to 0.4 dB, in the range 0-20 GHz. This improvement is then reflected on the system level simulations.

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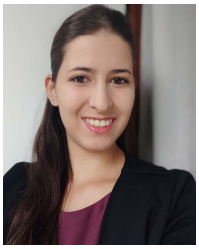

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