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RESEARCH ARTICLE

Design-Oriented All-Regime All-Region 7-Parameter Short-Channel MOSFET Model Based on Inversion Charge

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ABSTRACT This paper presents a 7-parameter analytical model of the MOS transistor based on the inversion charge targeted at the development of simplified analytical circuit design methodologies that take into account the physics of the MOS transistor. The proposed design-oriented model allows for the first time to describe both the main short-channel effects of advanced nanometric technologies and the dependence of the transistor drain current on the drain voltage, while the model remains valid for all bias regimes (from weak to strong inversion) and for all operating regions (linear and saturated). A simple procedure based on the device physics is proposed to estimate the transistor model parameters for a given technology. Furthermore, analytical expressions of the current derivatives are developed targeting different design scenarios. The accuracy of the proposed model is validated by direct comparison to silicon measurements of N-MOS transistors in 28 nm FD-SOI technology for channel width of 1 μm and channel lengths of 30 nm, 60 nm and 150 nm, and also to simulations performed with an industry-standard compact model.

INDEX TERMS Analytical MOSFET modeling, charge-based MOSFET model, design-oriented MOSFET model, inversion coefficient, nonlinear distortion, short-channel effects, 28 nm FD-SOI.

I. INTRODUCTION

Current market and technology scaling trends in the IC industry towards low-power applications are pushing transistor operation to the moderate and weak inversion regimes. From a designer's point of view, operation in such regimes can be accurately simulated by commercially available simulators using complex transistor models provided by the foundries, such as BSIM-IMG [1], [2] or UTSOI2 compact models [3], [4] for FD-SOI technologies. However, as technology scaling goes deeper into nanometric sizes, the complexity of these simulation models grows, requiring hundreds of parameters per transistor to properly model short-channel effects. Transistor models become then too complex to be used in analytical design methodologies. As a consequence, designers are left with the choice of relying on simplified long channel piecewise models, which will not be accurate enough in advanced nanometric technologies, or depending on extensive simulation campaigns in order to properly size transistors to comply with a set of given design specifications.

In this scenario, design time increases and the designer's intuitive understanding of the link between electrical behavior and circuit performance may be dramatically reduced. In this context, there is a need for simple design-oriented

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models that differ from complex compact models in the sense that they employ a very reduced set of parameters while remaining sufficiently accurate to allow the analytical sizing of an electrical circuit to achieve a given set of design targets. For the last few years, such design-oriented models, mainly based on the transistor inversion level [5], [6], [7], [8], [9], [10], [11], [12], [13], have been gaining strength, enabling the development of new design methods using the inversion coefficient (IC) or the g_m/I_D ratio. Compared to the conventional piecewise model, these design-oriented models allow a better approximation of the transistor behavior in advanced technologies with a small set of parameters especially in moderate inversion regime which is gaining interest as the voltage supply reduces in advanced technologies.

As presented by Schneider *et al.* in [14] based on the ACM model or by Jespers *et al.* in [15] based on the basic EKV model, the most simple inversion coefficient-based model uses three main parameters: the threshold voltage (V_{T0}), the specific current (I_{S0}) and the subthreshold slope factor (n). In this model the current in saturation region is independent on V_D. This limitation is considered by Jespers in [15], where the dependence on V_D is introduced through calibration curves that gives the threshold voltage and the specific current, as a function of V_D. Obviously, this solution is unpractical for hand calculations with arbitrary transistor biasing.

Recent versions of ACM and EKV models include an additional parameter (denoted as ζ or λ_C, in the ACM or EKV formalism, respectively) that models short-channel effects (mainly carrier velocity saturation) in saturated transistors in strong inversion regime [12], [16]. The resulting 4-parameter model may be useful in many analog and RF design scenarios, representing a good trade-off between complexity and accuracy. However, the simplicity of the model comes at the cost of not describing the linear region and being limited to a fixed value of V_D.

The work presented in this paper intends to provide an updated analytical design-oriented physics-based model for advanced nanometric technologies, where many short-channel effects occur. The proposed model is valid in all bias regimes (from weak to strong inversion regime) and in all operating regions (from linear to saturated region), while it introduces for the first time an analytical description of the specific V_D dependency due to Short Channel Effects (SCEs). It has to be noted that this model does not intend to replace a full compact model as the ones included in the Design Kits of advanced technologies, but aims to bring the designer closer to the physics of the transistor through a small set of parameters. Hence, this design-oriented model aims to simplify the first sizing step of a circuit design using simple physics-based analytical equations instead of inaccurate piecewise models or precomputed look-up tables [15], [27], [28]. To this end, based on the developed model, novel analytical expressions for AC analysis and design, such as the transconductance, its derivatives and the output conductance, are explicitly derived in this work.

The proposed model is based on the core equations of the ACM model [11] (equivalent to the basic EKV model presented in [8]). The model has been expanded to include four key short-channel physical effects by the addition of four parameters to the core 3-parameter model. Namely, the proposed model includes the effects of Drain-Induced Barrier Lowering (DIBL), carrier velocity saturation as in [12], [16], and [17], carrier mobility reduction and Channel Length Modulation (CLM), modeled by four scalar parameters, σ, ζ, θ and V_E, respectively.

The rest of the paper is organized as follows. Section II is devoted to the construction of the new analytical model following a didactical approach by gradually introducing in the current equation each of the four short-channel effects previously mentioned. For each step, the resulting transistor characteristic is compared to silicon measurements over N-MOS transistors in the 28 nm FD-SOI technology node [18]. Then, section III describes the parameter extraction procedure for model construction. Section IV validates the proposed 7-parameter model for three different channel lengths. Section V discusses the application of the model in the context of circuit design. In particular, a set of equations describing the transconductance, its derivatives and the output conductance are provided and compared to measurements showing that the model successfully implements the V_D dependence and successfully describes the non-linear behavior in all operating regions. Finally, section VI presents a brief discussion and section VII summarizes our main contributions.

II. 7-PARAMETER MODEL

Basic 3-parameter EKV and ACM inversion coefficient-based models [6], [8], although accurate enough for describing a long channel transistor behavior, are not appropriate for advanced technologies, where the behavior of the transistor is dominated by short-channel effects. In this section, we present an all-region all-regime 7-parameter inversion coefficient-based model that considers the main short-channel effects present in nanometric technologies, i.e., DIBL, carrier velocity saturation, carrier mobility reduction and CLM.

This section follows a didactical approach to present the proposed model. As the starting point in our derivation, we first present the basic 3-parameter ACM model. This model employs the threshold voltage (V_{T0}), the specific current (I_{S0}) and the subthreshold slope factor (n) to describe an all-region DC model of a long channel MOS transistor. Then, short-channel effects are introduced one by one and incrementally added in the model equations illustrating their effects on the I-V characteristics of the MOS. Comparisons to silicon measurements are provided to show the cumulative improvement of the model fitting as each new parameter is introduced.

A. 3-PARAMETER MODEL: n, I_{S0} AND V_{T0}

ACM and EKV models are inversion charge linearization-based models that describe, continuously, the MOS transistor

drain current characteristic as a function of its source, drain, gate, and body voltages. The main differences between ACM and EKV lies in a different definition for the normalization charge and the pinch-off voltage, V_P. However, from a designer's point of view, the equation sets are similar and the following work can be transposed from ACM to EKV. In the coming discussion, voltages are referred to the body terminal, whose voltage, V_{BB}, is set to zero. However, the discussion remains valid for any V_{BB} value knowing that a unique set of parameters must be extracted for specific values of V_{BB}.

The drain current is a function of the forward and reverse currents, I_F and I_R. In an ideal MOS, these currents are independent of each other and are a function of the gate (V_G), drain (V_D) and source voltages (V_S) as: $I_F = I(V_G, V_S)$ and $I_R = I\,(V_G, V_D)$. So, I_D can be expressed as [11]

$$I_D = I_F - I_R = I_{S0}\left(i_f - i_r\right), \tag{1}$$

where, $i_f = I_F/I_{S0}$, $i_r = I_R/I_{S0}$, and I_{S0} is the specific current, defined for the n-channel transistor as

$$I_{S0} = \mu_n C'_{ox} n \frac{U_T^2}{2} \frac{W}{L_{eff}}, \tag{2}$$

where, μ_n is the electron mobility, W and L_{eff} are the width and the effective length of the transistor, respectively, $U_T = kT/q$, is the thermal voltage, $C'_{ox} = \varepsilon_{ox}/t_{ox}$, is the oxide capacitance per unit area, and ε_{ox} and t_{ox} are the permittivity and equivalent thickness of the oxide, respectively. i_f and i_r are the inversion coefficients which are directly related to the density of the inversion charges at the source and the drain terminals of the transistor, Q'_{IS} and Q'_{ID}, respectively.

These charges, after normalization, are

$$q_S = \frac{Q'_{IS}}{Q'_{IP}}, \tag{3}$$

$$q_D = \frac{Q'_{ID}}{Q'_{IP}}, \tag{4}$$

with, $Q'_{IP} = -nC'_{ox}U_T$ for the n-channel transistor.

q_S and q_D are related to the inversion coefficients as

$$q_S = \sqrt{1 + i_f} - 1, \tag{5}$$

$$q_D = \sqrt{1 + i_r} - 1. \tag{6}$$

Therefore, the normalized drain current can be also expressed as [10]

$$i_d = \frac{I_D}{I_{S0}} = (q_S - q_D)\,(q_S + q_D + 2). \tag{7}$$

As described in the literature, inversion regimes are usually defined as a function of i_d. Thus, weak inversion corresponds to $i_d < 0.1$, moderate inversion to $0.1 < i_d < 10$ and strong inversion to $i_d > 10$.

In long channel devices, the use of normalized inversion level coefficients (i_f and i_r) is quite convenient since it can be easily related to the g_m transconductance, which is a major design parameter. However, to introduce short-channel effects, the use of normalized drain and source charges (q_D and q_S) is straightforward and simplifies the derivations.

Using q_D and q_S for the simple model above, the g_m/I_D characteristic can be deduced as follows [10],

$$\frac{g_m}{I_D} = \frac{2}{nU_T(q_S + q_D + 2)}. \tag{8}$$

The computation of the normalized charges is done as follows. The pinch-off voltage V_P, is the channel to substrate voltage for which the channel charge densities equal Q'_{IP}, or $Q'_{IS} = Q'_{ID} = Q'_{IP}$. The threshold voltage, V_T, is defined as the gate voltage for which $V_P = 0$ and is linearly approximated by [5]

$$V_P \approx \frac{V_G - V_T}{n}. \tag{9}$$

The pinch-off voltage is then related to the source and drain voltages, V_S and V_D, through their corresponding normalized charges as [10]

$$V_P - V_S = U_T\,(q_S - 1 + ln\,(q_S)), \tag{10}$$

$$V_P - V_D = U_T\,(q_D - 1 + ln\,(q_D)). \tag{11}$$

Therefore, the drain to source voltage, V_{DS}, normalized by U_T is given by

$$\frac{V_{DS}}{U_T} = q_S - q_D + ln\left(\frac{q_S}{q_D}\right). \tag{12}$$

Fig. 1 shows a comparison between the 3-parameter model, extracted in weak and moderate inversion regimes as explained in section III, and the measurements for a 30 nm length, L, and 1 μm width n-channel transistor of the 28 nm FD-SOI technology. The two main characteristic curves $I_D(V_G)$ and $I_D(V_D)$ are presented, the $I_D(V_G)$ is plotted for two values of V_D: in linear region (for $V_D = 50$ mV), and in saturated region (for $V_D = 500$ mV), using linear and semilogarithmic scales (a). $I_D(V_D)$ is plotted in weak inversion regime for $V_G = 100$ mV (b), and in strong inversion regime for $V_G = 900$ mV (c).

As it can be noticed in the $I_D(V_G)$ characteristic (Fig. 1(a)), the model has a good accuracy in the weak and moderate inversion regimes of the transistor ($V_G < 600$ mV), but presents an overestimation of the drain current in the strong inversion regime also visible in Fig. 1(c), this can be explained by two short-channel phenomena in strong inversion regime: the voltage drop in the series resistances and the carrier velocity saturation. The first one mainly impacts the triode region ($V_D = 50$ mV) and the second one, the saturated region of operation ($V_D = 500$ mV).

Besides, the semilogarithmic scale of $I_D(V_G)$ (Fig. 1(a)) brings to light two discrepancies with respect to the measured current in saturated region ($V_D = 500$ mV) for weak to moderate regime ($V_G < 500\,mV$). The first one is a difference of the slope, n, and the second one is an underestimation of the drain current. The first discrepancy can be minimized by slightly adjusting the slope factor, n, to optimize the fit with the measurements [19], noticing that the variation of n vs. V_D is small enough to be neglected.

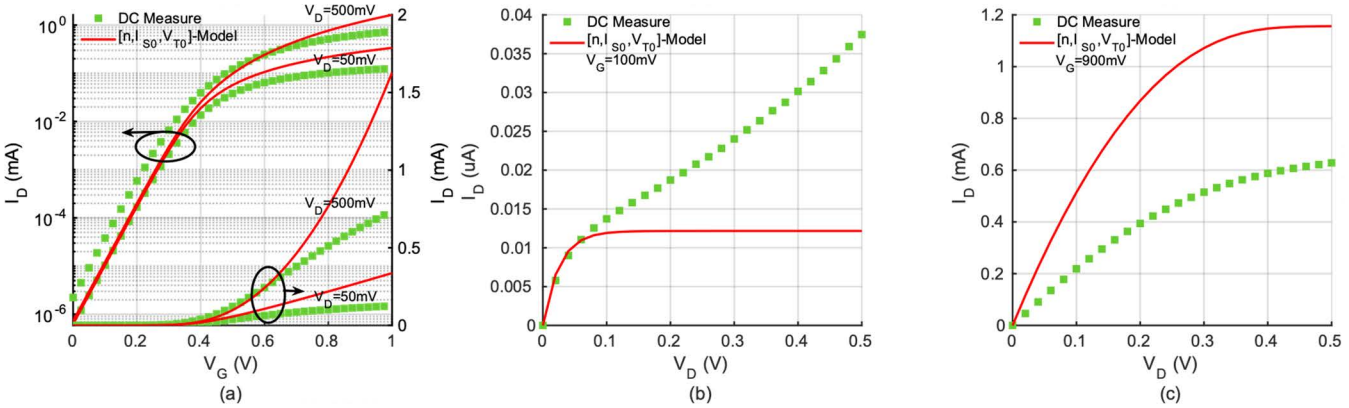

FIGURE 1. $L = 30$ nm and $W = 1$ μm N-MOS transistor characteristic curves: $I_D(V_G)$ for $V_D = 50$ mV and 500 mV in linear (right axis) and in semilogarithmic scale (left axis) (a), $I_D(V_D)$ for $V_G = 100$ mV (b) and for $V_G = 900$ mV (c): Comparison between measures (green squares) and model based on 3 parameters (solid red line): $n = 1.377$, $I_{S0} = 5.9$ μA and $V_T = 380.3$ mV.

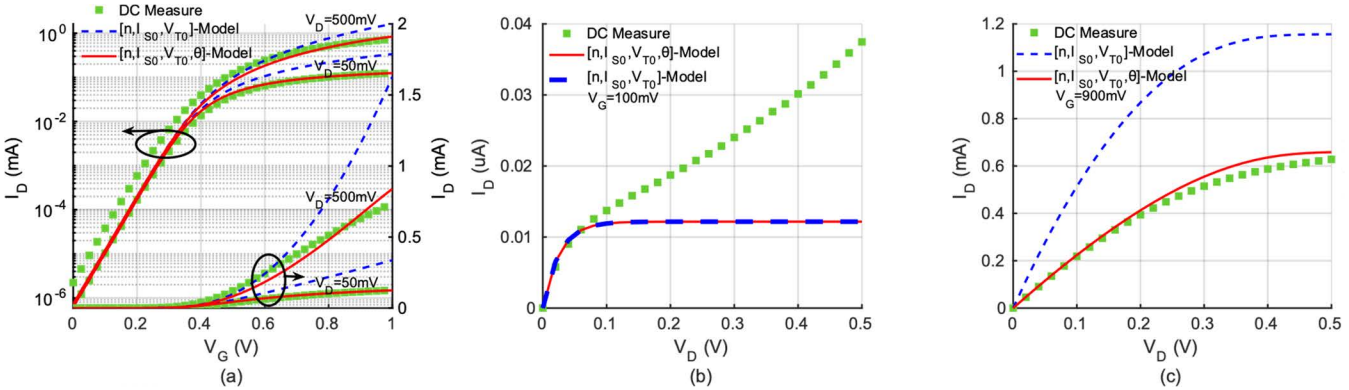

FIGURE 2. $L = 30$ nm and $W = 1$ μm N-MOS transistor characteristic curves: $I_D(V_G)$ for $V_D = 50$ mV and 500 mV in linear (right axis) and in semilogarithmic scale (left axis) (a), $I_D(V_D)$ for $V_G = 100$ mV (b) and for $V_G = 900$ mV (c): Comparison between measures (green squares) model based on 3 parameters (dashed blue line) and on 4 parameters (red solid line): $n = 1.377$, $I_{S0} = 5.9$ μA, $V_T = 380.3$ mV and $\theta = 0.115$. Note that for (b) there is no change between both models based on 3 and 4 parameters, as the effect of mobility reduction (θ) appears only in strong inversion.

On the contrary, the current increase with V_D has to be modeled by taking into account two major short-channel effects: the DIBL and the CLM.

In the absence of these two effects, the 3-parameter model cannot correctly reproduce the I_D (V_D) behavior. As shown in Fig. 1, the current is underestimated in weak inversion while in saturated region it remains constant with V_D.

In the following subsections, we address the introduction of each of the four above-mentioned physical effects into the transistor model. The discussion starts with the mobility reduction, which has a major impact in linear region in strong inversion regime and continues with the V_D dependence in saturated region operation.

B. MODELING THE CARRIER MOBILITY REDUCTION EFFECT: θ

The drain current reduction in strong inversion shown in the DC measurements presented in Fig. 1(a) for $V_D = 50$ mV, is first due to the reduction of the carrier mobility. When a high vertical electric field is applied, the mobility in the inversion layer near to the semiconductor-oxide interface is reduced, due to several scattering mechanisms that produce a reduction of the mobility in the channel [9]. In short-channel transistors, the apparent carrier mobility is further reduced due to the presence of source and drain series resistances.

Both effects can be introduced in the drain current expression through a parameter related to the mobility reduction,θ, and the average inversion charge, $(q_S + q_D)/2$, which traduces the vertical field dependence. Hence (7) is modified as

$$I_D = I_{S0} \frac{(q_S - q_D)\,(q_S + q_D + 2)}{1 + \theta\left(\frac{q_S + q_D}{2}\right)}. \tag{13}$$

In Fig. 2(a), the impact of carrier mobility reduction is visible. Compared with the 3-parameter (n, I_{S0} and V_{T0}) model presented in the previous section, the fitting with the measurements is better in strong inversion without degrading the behavior at weak and moderate inversion levels in triode region ($V_D = 50$ mV), proving that a 4-parameter (n, I_{S0}, V_{T0} and θ) model could be enough to describe the $I_D(V_G)$ behavior for a single V_D. For a $V_D = 500$ mV, the model also

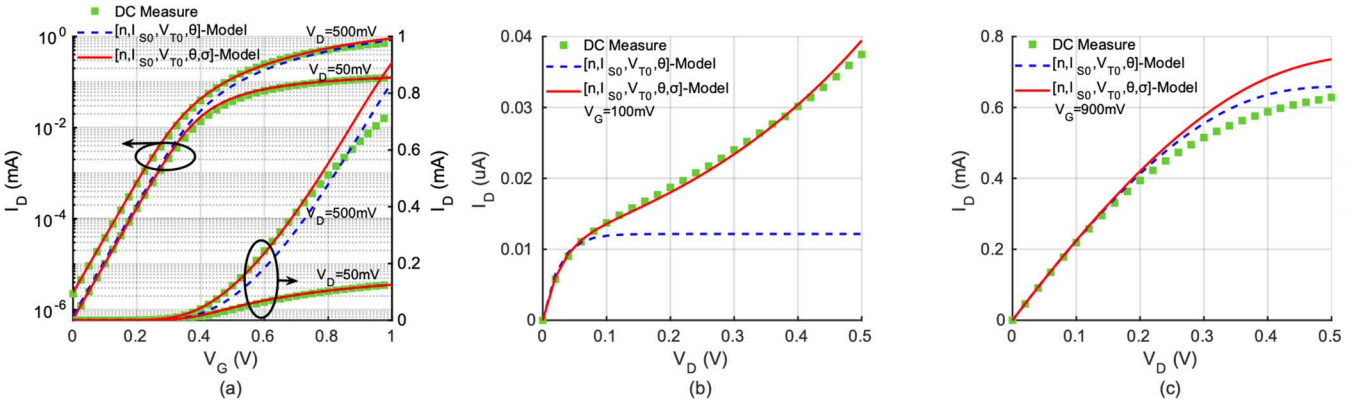

FIGURE 3. $L = 30$ nm and $W = 1$ μm N-MOS transistor characteristic curves: $I_D(V_G)$ for $V_D = 50$ mV and 500 mV in linear (right axis) and in semilogarithmic scale (left axis) (a), $I_D(V_D)$ for $V_G = 100$ mV (b) and for $V_G = 900$ mV (c): Comparison between measures (green squares) model based on 4 parameters (dashed blue line) and on 5 parameters (red solid line): $n = 1.377$, $I_{S0} = 5.9$ μA, $V_{T0} = 384.9$ mV, $\theta = 0.115$ and $\sigma = 0.093$.

improves the estimation of the current in strong inversion, even if the latter is still overestimated.

On the other hand, the underestimation of the drain current in weak inversion as the drain voltage increases (Fig. 2(a) for $V_G < 500$ mV and Fig. 2 (b)) is still there and due to the DIBL effect, as explained in the next section.

Fig. 2(b) clearly shows that the carrier mobility reduction (θ) does not have any effect on the modeling of the weak inversion regime. Contrary to this, Fig. 2(c) depicts the importance of including this effect on the modeling of the strong inversion regime. Unlike other design-oriented analytical models previously proposed, the inclusion of this parameter directly linked to the carrier mobility reduction, θ, allows to fully model the linear region of operation of the MOS transistor for a given V_D. As it will be shown, the V_D dependence will be further improved in this paper thanks to the introduction of additional parameters.

C. MODELING THE DRAIN-INDUCED BARRIER LOWERING EFFECT: σ

The DIBL effect consists in a reduction of the barrier potential for the carriers at the source side when the drain voltage increases. This creates a conduction channel at a lower gate voltage, which can thus be interpreted as a reduction of the threshold voltage, V_T. The DIBL is modeled by $\sigma(V_D + V_S)$ term in the V_T expression as [11]

$$V_T = V_{T0} - \sigma(V_D + V_S). \tag{14}$$

As a consequence, the pinch-off voltage increases and can be expressed from (9) as

$$V_P \approx \frac{V_G - V_{T0} + \sigma(V_D + V_S)}{n}. \tag{15}$$

Fig. 3(a), and (b) show how important is the DIBL effect to correctly model the current in weak and moderate inversion regimes, introducing a dependence on V_D which was not accounted for in previous analytical models. The drain current overestimation by the model, mainly in strong inversion regime as shown in Fig. 3(c) is related to carrier velocity saturation effect which will be treated in the next section.

In the perspective of efficiently linking the circuit performance to the technology features, it is possible to express the DIBL parameter σ as a function of insulators and silicon film thicknesses. However, to keep the presented design-oriented model as simple as possible, this link is not done explicitly here.

D. MODELING THE CARRIER VELOCITY SATURATION EFFECT: ζ

The carrier velocity saturation effect models the limited increase of the velocity of the carriers when the longitudinal electric field (V_{DS}/L) increases [9]. This effect has already been widely considered in the literature [12], [16], [17], [19]. In those published models, the carrier velocity saturation parameter is represented by ζ, which is defined as

$$\zeta = \frac{\mu_n U_T}{L v_{sat}}, \tag{16}$$

where, v_{sat} is the saturation velocity of the carriers. To be more accurate, μ_n in (16) should be replaced by the effective mobility that includes the effects of the vertical electric field and series resistances presented in section II.B. Keeping here μ_n for simplicity purpose will lead to an effective value of ζ.

When the carrier velocity saturation is reached, the drain current is given by [9]

$$I_{Dsat} = -W v_{sat} Q'_{IDsat}. \tag{17}$$

Or, using the normalized quantities,

$$i_{dsat} = \frac{I_{Dsat}}{I_{S0}} = \frac{2}{\zeta} q_{Dsat}. \tag{18}$$

Then, the approximation introduced in [20], considering that the saturation of carrier velocity only occurs at the drain side is made. This assumption simplifies the model equations at the cost of a lower accuracy in the transition from linear to saturated region. With these considerations, the general

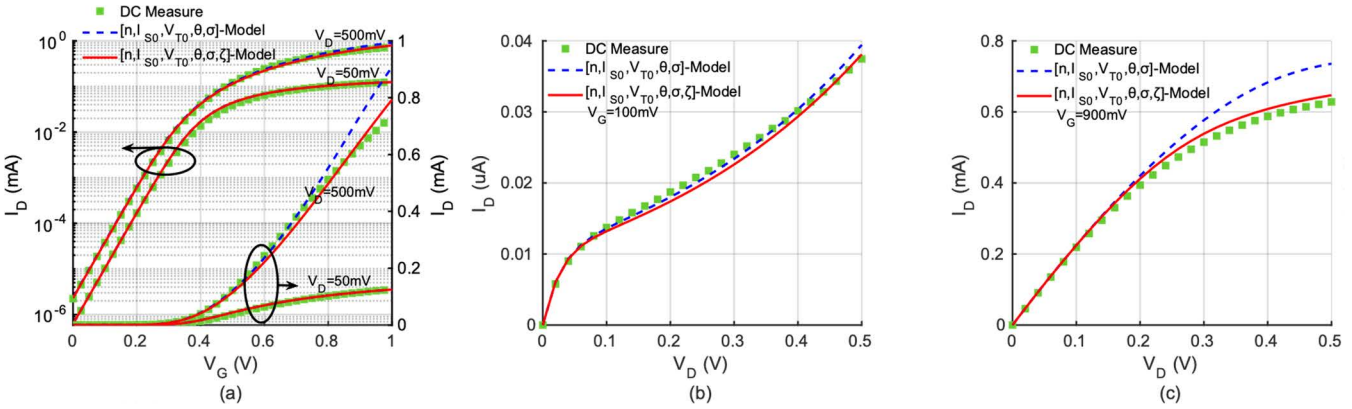

FIGURE 4. $L = 30$ nm and $W = 1$ μm N-MOS transistor characteristic curves: $I_D(V_G)$ for $V_D = 50$ mV and 500 mV in linear (right axis) and in semilogarithmic scale (left axis) (a), $I_D(V_D)$ for $V_G = 100$ mV (b) and for $V_G = 900$ mV (c): Comparison between measures (green squares) model based on 5 parameters (dashed blue line) and on 6 parameters (red solid line): $n = 1.377$, $I_{S0} = 5.9$ μA, $V_{T0} = 384.9$ mV, $\theta = 0.115$, $\sigma = 0.093$ and $\zeta = 0.035$.

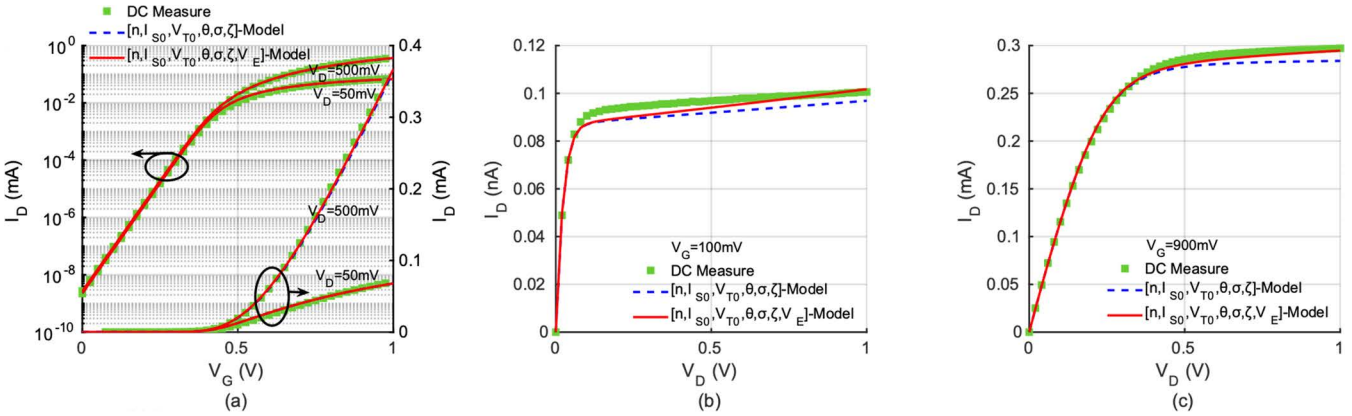

FIGURE 5. $L = 150$ nm and $W = 1$ μm N-MOS transistor characteristic curves: $I_D(V_G)$ for $V_D = 50$ mV and 500 mV in linear (right axis) and in semilogarithmic scale (left axis) (a), $I_D(V_D)$ for $V_G = 100$ mV (b) and for $V_G = 900$ mV (c): Comparison between measures (green squares) model based on 6 parameters (dashed blue line) and on 7 parameters (red solid line): $n = 1.092$, $I_{S0} = 1.83$ μA, $V_{T0} = 427$ mV, $\theta = 0.047$, $\sigma = 0.003$, $\zeta = 0.06$ and $V_E = 18.5$ V.

expression of the drain current (13) can be used to extract q_{Dsat} value, replacing q_D by q_{Dsat},

$$i_{dsat} = \frac{2}{\zeta} q_{Dsat} = \frac{(q_S + q_{Dsat} + 2)(q_S - q_{Dsat})}{1 + \theta\left(\frac{q_S + q_{Dsat}}{2}\right)}. \quad (19)$$

Doing so, we obtain the following relation between q_S and q_{Dsat}:

$$q_S = \frac{\theta}{2\zeta} q_{Dsat} - 1 + \sqrt{1 + q_{Dsat}\left(2 + \frac{2}{\zeta} - \frac{\theta}{\zeta}\right) + q_{Dsat}^2\left(1 + \frac{\theta}{\zeta} + \frac{\theta^2}{4\zeta^2}\right)} \quad (20)$$

Defining V_{DSsat} as the drain-to-source voltage for which $q_D = q_{Dsat}$, and using (12), one obtains [9]

$$\frac{V_{DSsat}}{U_T} = q_S - q_{Dsat} + ln\left(\frac{q_S}{q_{Dsat}}\right). \quad (21)$$

In order to preserve the continuity of the model from linear to saturated region, we can define an effective drain-to-source voltage accounting for the carrier velocity saturation effect,

$$V'_{DS} = \frac{V_{DS}}{\sqrt[4]{1 + \left(\frac{V_{DS}}{V_{DSsat}}\right)^4}}. \quad (22)$$

This formulation, inspired from industry-standard compact models, allows to preserve a smooth behavior of the model around $V_{DS} = V_{DSsat}$.

Similarly, one can define an effective drain voltage,

$$V'_D = V'_{DS} + V_S, \quad (23)$$

and its associated drain charge q'_D, using (11),

$$V_P - V'_D = U_T\left(q'_D - 1 + ln\left(q'_D\right)\right). \quad (24)$$

Finally, the drain current expression of (13), becomes

$$I_D = I_{S0}\frac{\left(q_S + q'_D + 2\right)\left(q_S - q'_D\right)}{1 + \theta\left(\frac{q_S + q'_D}{2}\right)}. \quad (25)$$

Fig. 4 illustrates the benefits of introducing the carrier velocity saturation effect in the model through the sixth

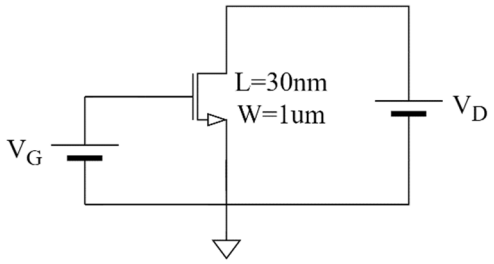

FIGURE 6. Common source configuration circuit for parameter extraction.

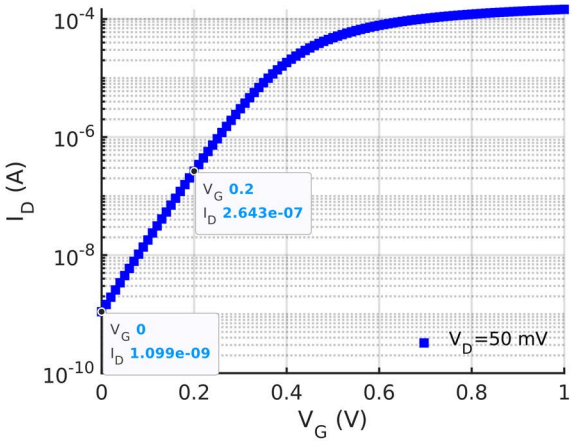

FIGURE 7. Extraction of slope factor, $n = 1.41$, based on log $I_D(V_G)$ characteristic for $V_D = 50$ mV.

parameter, ζ, especially in strong inversion regime for a transistor in saturated region (Fig. 4(a) for $V_D = 500$ mV).

As expected, ζ parameter has no impact in linear regime ($V_D = 50$ mV).

E. MODELING THE CHANNEL LENGTH MODULATION EFFECT: V_E

The CLM effect leads to an increase of the drain current when the drain voltage keeps increasing after the pinch-off occurs [9]. Considering this effect on the presented analytical model allows a second parameter linked to the drain current dependency on V_D, which will be essential for the modeling of long channel transistors.

This effect can be accounted for by introducing a seventh parameter, V_E, leading to the following drain current expression

$$I_D = \left(1 + \frac{V_{DS} - V'_{DS}}{V_E}\right) \frac{I_{S0}\left(q_S + q'_D + 2\right)\left(q_S - q'_D\right)}{1 + \frac{\theta}{2}\left(q_S + q'_D\right)}. \tag{26}$$

The effect of V_E is illustrated in Fig. 5 for a N-MOS transistor with $L = 150$ nm and $W = 1$ μm. The CLM effect is overshadowed by the DIBL effect in the case of the 30 nm transistor whereas it is clearly visible on the output characteristic of a larger transistor as for 150 nm (Fig. 5(b), and (c)).

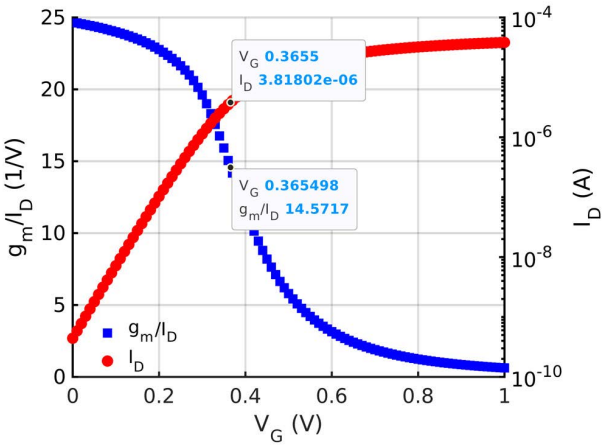

FIGURE 8. g_m/I_D and I_D characteristics vs V_G for extraction of threshold voltage, $V_{T0} = 365.6$ mV, and specific current, $I_{S0} = 4.4$ μA.

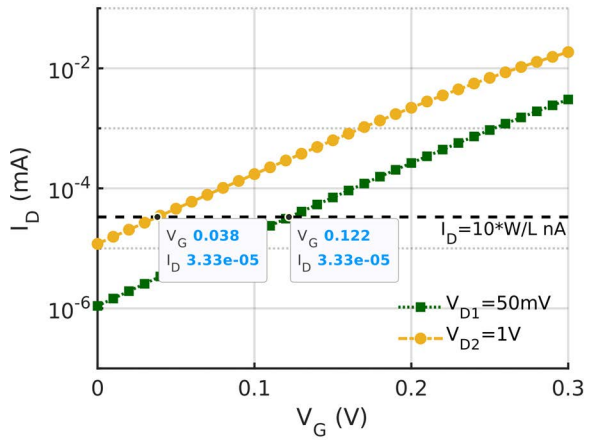

FIGURE 9. Extraction of DIBL parameter, $\sigma = 0.088$, based on $I_D(V_G)$ characteristic for $V_{D1} = 50$ mV and $V_{D2} = 1$ V.

III. PARAMETER EXTRACTION

A brief description of the extraction of each model parameter is given below. The procedure can be applied using simulation or measurements results. It will be illustrated here with electrical simulations of an n-channel low threshold voltage transistor of $L = 30$ nm and $W = 1$ μm using the transistor models from a 28 nm FD-SOI technology PDK.

Most of the parameters can be directly extracted from a common source configuration as illustrated in Fig. 6, sweeping V_G with a fixed V_D value.

The procedure presented in [21] is followed to extract the 3 main physical parameters, n, I_{S0} and V_{T0}.

A. SLOPE FACTOR

The slope factor is determined by calculating the subthreshold slope of the semilogarithmic $I_D(V_G)$ curve, for small values of V_G in linear region ($V_D = V_{D1} = 50$ mV) as

$$n = \frac{1}{U_T} \frac{\Delta V_G}{\Delta \ln(I_D)}. \tag{27}$$

For the 30 nm transistor simulated, the value of the slope factor corresponds to $n = 1.41$ as illustrated in Fig. 7.

B. THRESHOLD VOLTAGE AND SPECIFIC CURRENT

Based on the procedure describe in [22], V_{T0} and I_{S0} are extracted from the $I_D\,(V_G)$ and $g_m/I_D\,(V_G)$ characteristics in a common source configuration (Fig. 6) with V_{DS} fixed to $U_T/2$.

When $V_G = V_{T0}$, the diffusion and drift currents are equal, leading to $q_S = 1$, which is equivalent to $i_f = 3$, (5). Then, (12) leads to $q_D = 0.77$, (6) gives $i_r = 2.12$ and (8) leads to $g_m/I_D = 0.531/nU_T$. The threshold voltage is therefore equal to the gate voltage for which $g_m/I_D = 0.531/nU_T$.

From the same operating point ($V_G = V_{T0}$), I_{S0} is computed from (7). Fig. 8 illustrates this procedure for $L = 30$ nm resulting in $V_{T0} = 365.6$ mV and$I_{S0} = 4.4\ \mu$A.

C. DIBL

The DIBL parameter, σ, can be extracted from the semilogarithmic $I_D(V_G)$ characteristic. Adding a second curve of $I_D\,(V_G)$ to Fig. 7 for a higher value of V_D ($V_{D2} = 1$ V) as illustrated in Fig. 9 and extracting the gate voltages corresponding to a given current level allows the evaluation of DIBL parameter as the ratio between the difference of the gate voltages and difference of the drain voltages, as stated below:

$$\sigma = -\frac{\Delta V_G}{\Delta V_D} = \frac{V_{G1} - V_{G2}}{V_{D2} - V_{D1}}. \tag{28}$$

D. MOBILITY REDUCTION FACTOR, CARRIER VELOCITY SATURATION AND CLM

As explained in section II.B, the mobility reduction effect mainly impacts the strong inversion regime for the linear region of the transistor. As the other 4 parameters (n, I_{S0}, V_{T0} and σ) are already extracted, the value of this parameter can be found by fitting the model with the simulation results (or measurements) for a small V_D and high gate voltages values as shown in Fig. 2. The optimized parameter value is $\theta = 0.09$.

On the other hand, the carrier velocity saturation effect is more relevant for large values of V_D and in strong inversion regime. Therefore, the corresponding parameter value is determined by fitting the $I_D(V_G)$ characteristic of the MOS in saturation region, as depicted in Fig. 4, leading to an optimized value of $\zeta = 0.04$.

Finally, the CLM parameter, or V_E, is a challenging parameter to determine as it varies with V_G and the length of the transistor. In short-channel devices this effect can be hidden by the DIBL, while for longer channel devices its effect becomes more visible. In our derivation, the estimation of the V_E is done by fitting, comparing the model built with the 6 previous presented parameters and the simulation of the output characteristic of the MOS transistor, for the evaluated device we obtain $V_E = 5$ V.

TABLE 1. Model parameters for three N-MOS transistor lengths (30 nm, 60 nm and 150 nm) in 28 nm FD-SOI technology.

Parameter/Length	30 nm	60 nm	150 nm
Slope factor: n	1.377	1.138	1.092
Specific current: I_{S0} (uA)	5.9	3.25	1.83
Threshold voltage: V_{T0} (mV)	384.9	390.5	427
Mobility reduction: θ	0.115	0.079	0.047
DIBL: σ	0.093	0.018	0.003
Velocity saturation: ζ	0.035	0.056	0.06
CLM: V_E (V)	5	15	18.5

IV. CONSISTENCY OF THE PROPOSED MODEL

The 7-parameter model related to physical effects, as presented in the previous section, accurately describes the DC characteristics of the MOS transistors for long and short channel lengths. Indeed, as it has been already published in the literature, the main parameters of the model can be made scalable with L [12], [19], [21]. However, in a practical design application, designers often prefer to extract the model parameters for a fixed L in order to keep the model as simple as possible and reduce the set of parameters to be extracted. In that case, L cannot be used as a design variable. This drawback is mitigated by the fact that L is often determined at the beginning of the sizing stage as a function of the design application requirements [12], [26].

In order to analyze the variation of the parameters according to different transistor channel lengths, a set of parameters has been extracted from measurements for three electrical n-channel transistor lengths in 28 nm FD-SOI technology: 30 nm, 60 nm and 150 nm all of them with a width of 1 μm. These parameters are presented in Table 1. The evolution of parameter values for different transistor lengths illustrates the physical mechanisms behind the parameters.

The slope factor, n, and the DIBL factor, σ, increase for shorter channel devices, which is consistent with the larger impact of source-drain region on transistor electrostatics when the channel length reduces.

When the channel length gets smaller, a consistent evolution in the value of the specific current is perceived, following (2), and the mobility reduction factor increases due to the series resistances contribution embedded in this factor.

According to (16), the carrier velocity saturation parameter, ζ, should monotonously increase when L reduces, which is not observed in the reported values of Table 1. As explained in section II.D, this is due to the impact of mobility reduction factor which lowers the carrier velocity saturation parameter value for small gate lengths.

Finally, the V_E value increases with the channel length, which is expected since CLM effect is proportional to $1/V_E$ and more pronounced on short-channel transistors.

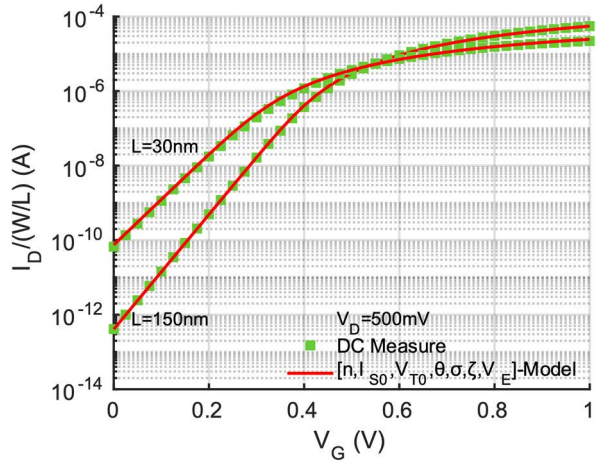

FIGURE 10. $I_D/(W/L)$ (V_G) curve: Comparison of a long ($L = 150$ nm) and a short ($L = 30$ nm) channel NMOS transistor, DC measures (green squares) and 7-parameters model (red solid line). The short channel effects: slope factor, threshold voltage, velocity saturation and series resistance are clearly visible in this curve.

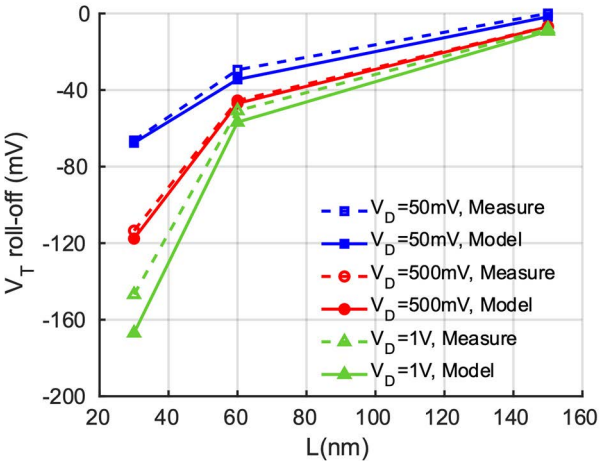

FIGURE 11. V_T roll-off for three values of drain voltage, $V_D = 50$ mV (square blue line), $V_D = 500$ mV (circle red line) and $V_D = 1$ V (triangle green line) for DC measures (dashed curves) and 7-parameter model (solid curves).

To further appreciate the integration of SCEs in the proposed model, a comparison of the drain current normalized with respect to the ratio W/L is done between a short ($L =$ 30 nm) and a long ($L = 150$ nm) channel NMOS transistor in Fig. 10. Several SCEs are visible when comparing both curves. First of all, the slope in subthreshold region, which reflects the slope factor n, increases for the shorter transistor. The reduction of the threshold voltage when the channel length is reduced is also visible in this figure. Finally, the current reduction in strong inversion can be observed in Fig. 10 for short channel showing the effect of the velocity saturation and the voltage drop in the series resistances. The threshold voltage roll-off ($V_{T\_Roll-off}$) is also an accurate measure of the SCEs as presented in [23]. Fig. 11 presents the $V_{T\_Roll-off}$ for three different values of V_D evaluated on the three channel lengths studied in this chapter. Our proposed model, in solid lines, shows a good agreement against the DC measurements, in dashed lines, with a maximum error of around 20 mV in the worst-case scenario.

To further evaluate the accuracy of the 7-parameter model, we estimated, for each channel length, the Relative Error (RE) between the simulated and measured $I_D(V_G)$ and $I_D(V_D)$ characteristics as follows:

$$\mathrm{RE}\,(\%) = \frac{Model - Measure}{Measure} * 100\%, \tag{29}$$

As presented in Fig. 12, the relative error is well contained in the weak and strong inversion regimes for the $I_D(V_G)$ and $I_D(V_D)$ curves, while the maximum relative error reaches 30% close to the threshold voltage (near to 0.4 V) for small values of V_D ($V_D = 50$ mV) in triode region. Regarding the $I_D(V_D)$ curves, for V_D values above 150 mV the relative error does not exceed 15%.

Finally, we compare our design-oriented model to the industry-standard UTSOI2 model used for this 28 nm FD-SOI technology. As shown in Fig. 13 (a), (b) and (c) for a 30 nm length transistor, the proposed design-oriented model slightly differs from UTSOI2 (that perfectly matches the experimental characterization measurements). In weak inversion, the current is overestimated for small V_D and underestimated for large V_D, whereas in strong inversion the current is underestimated for mid V_D. However, the main characteristics of the curve shapes are well captured, which is found to be enough for a design-oriented model whose main purpose is the sizing of the circuit. In order to get further insight, Fig. 13 (d), (e), and (f) show a direct comparison between the UTSOI2 model and a state-of-the-art design-oriented 4-parameter model recently published [29], that we have fine-tuned for this technology and transistor geometry. It is clear to see that our proposed 7-parameter model offers a better representation of the V_D dependency, while the 4-parameter model struggles to follow the actual MOST behavior when V_D increases. It is worth noticing that authors in [29] propose the 4-parameter model for low-voltage applications, restricting the validity of the model, as can be observed in Fig. 13, to a low-V_D scenario. Our 7-parameter model does not show this limitation and remains valid for all regimes and all regions of operation.

V. MODEL APPLICATION IN A DESIGN CONTEXT

On top of an accurate description of the MOS DC behavior, the presented model, provides analytical formulas for the transconductance, the conductances and their derivatives. This is the first step to allow analog/RF designers to develop analytical design methodologies for transistors sizing. Furthermore, our model, which includes the dependence on V_D, allows to study nonlinear effects that impact the performance of many analog/RF designs exhibiting large V_D swings.

In this section, we compare the modeled transconductances with actual measurements for a FD-SOI transistor of $L = 30$ nm to demonstrate the wide validity domain of the

proposed model. Furthermore, analytical expressions of the transconductance and its derivatives are proposed. Since the region of operation of the MOS transistors is often defined at the beginning of the design process, this information can be used to provide simple analytical expressions of the current derivatives by considering the linear and saturated regions separately. These expressions are developed in the following subsections.

A. GATE TRANSCONDUCTANCE AND ITS DERIVATIVES: NUMERICAL DERIVATION APPROACH

Gate transconductance, g_m, and transconductance efficiency, g_m/I_D, are key parameters for small-signal design [24], [25], [26]. At the same time, the second and third derivative of I_D, g_{m2} and g_{m3}, determine circuit linearity performances, such as harmonic distortion, intermodulation products and compression point and thus must be accurately modeled.

Fig. 14, Fig. 15, Fig. 16 and, Fig. 17 show the numerical derivatives of the 7 parameters model, i.e., g_m, g_{m2} and g_{m3}, and transconductance efficiency g_m/I_D, respectively. Numerical derivations are compared with measurement results of a 30 nm length FD-SOI N-MOS transistor for several values of the drain voltage. The transconductance is depicted against the normalized current, $i_d = I_D/I_{S0}$. It can be observed that, the model estimates very well the behavior of the transconductance with a good accuracy in all operation regions, especially for values of i_d below 10. A good agreement is also observed in Fig. 15 and Fig. 16 for g_{m2} and g_{m3}. It is worth noticing that these curves allow an accurate estimation of the sweet spot (the value of i_d that makes $g_{m3} = 0$). This estimation is not possible with simpler models that do not count for short-channel effects. The maximum and minimum of these derivatives are also in good agreement with the measurements. In Fig. 17, we observe consistent modeled and measured transconductance efficiency, with a slight over estimation (lower than 10%) in moderate inversion in linear region.

B. ANALYTICAL EXPRESSION OF THE CURRENT DERIVATIVES IN ABSENCE OF CARRIER VELOCITY SATURATION

In advanced technologies, where frequency limitations are relaxed due to large f_T, weak and moderate inversion are often selected for design in order to increase the energy efficiency of the MOS. In this particular biasing conditions where carrier velocity saturation can be neglected, expression (13) can be employed to obtain analytical expressions of the current derivatives valid for any transistor geometry as,

$$\frac{\partial i_d}{\partial v_x} = \frac{1}{B}\left[\left(2+2q_S-\frac{\theta}{2}i_d\right)\frac{\partial q_S}{\partial v_x}-\left(2+2q_D+\frac{\theta}{2}i_d\right)\frac{\partial q_D}{\partial v_x}\right], \tag{30}$$

with v_x standing for the considered normalized voltage, $v_g = V_G/U_T$, $v_d = V_D/U_T$, or $v_s = V_S/U_T$ and

$$B = 1 + \frac{\theta}{2}(q_S + q_D), \tag{31}$$

and from equations (10), (11) and (15),

$$\frac{\partial q_{S(D)}}{\partial v_g} = \frac{1}{n}\frac{q_{S(D)}}{q_{S(D)}+1}, \tag{32}$$

$$\frac{\partial q_D}{\partial v_d} = \left(1-\frac{\sigma}{n}\right)\frac{q_D}{q_D+1}, \tag{33}$$

$$\frac{\partial q_S}{\partial v_d} = \frac{\sigma}{n}\frac{q_S}{q_S+1}, \tag{34}$$

$$\frac{\partial q_D}{\partial v_s} = \frac{\sigma}{n}\frac{q_D}{q_D+1}, \tag{35}$$

$$\frac{\partial q_S}{\partial v_s} = \left(1-\frac{\sigma}{n}\right)\frac{q_S}{q_S+1}. \tag{36}$$

Equations (30), (31), (32) give an explicit analytical expression of the gate transconductance,

$$g_m = \frac{\partial i_d}{\partial v_g} = \frac{2}{B}\left[q_S - q_D - i_d\frac{\theta}{4}\left(\frac{q_S}{1+q_S}+\frac{q_D}{1+q_D}\right)\right]. \tag{37}$$

This relatively simple expression, represented in Fig. 14 allows to predict the existence of a maximum of g_m for a given value of i_d. Fig. 14 compares the analytical approximation against the numerical derivatives from the DC measurements and the 7-parameter model. It shows that (37) is accurate and valid in all inversion regimes in the linear region (Fig. 14(a)). However, neglecting the carrier velocity saturation limits the accuracy of the model in the saturated region (Fig. 14(b) and (c)) in strong inversion, but continues to provide a good estimation in weak and moderate inversion regimes.

C. ANALYTICAL EXPRESSION OF THE CURRENT DERIVATIVES IN SATURATED REGION

Similarly, simple generic analytical expressions can be drawn for the derivatives of the current in the saturated region, using the saturation expression of the drain current I_{Dsat} in (18). This expression includes the effects of carrier velocity saturation, mobility reduction and DIBL. Using (18), the transconductance (or conductances) can be expressed as,

$$\frac{\partial i_{dsat}}{\partial v_x} = \frac{\partial i_{dsat}}{\partial q_S}\frac{\partial q_S}{\partial v_x} = 2\frac{E}{D+\frac{\theta}{2}E}\frac{\partial q_S}{\partial V_x}. \tag{38}$$

Using the same naming convention for the transistor terminals as before and with

$$D = 1 + \zeta - \frac{\theta}{2} + q_{Dsat}\left(\zeta+\theta+\frac{\theta^2}{2\zeta}\right), \tag{39}$$

$$E = \sqrt{1+q_{Dsat}\left(2+\frac{2}{\zeta}-\frac{\theta}{\zeta}\right)+q_{Dsat}^2\left(1+\frac{\theta}{\zeta}+\frac{\theta^2}{4\zeta^2}\right)}, \tag{40}$$

$\partial q_S/\partial v_x$ is given by (32), (34) or (36) depending on the considered terminal.

Fig. 14(b) and (c) show the gate transconductance, g_m, under saturation approximation, compared to actual measurements and numerical derivatives of the 7-parameter model.

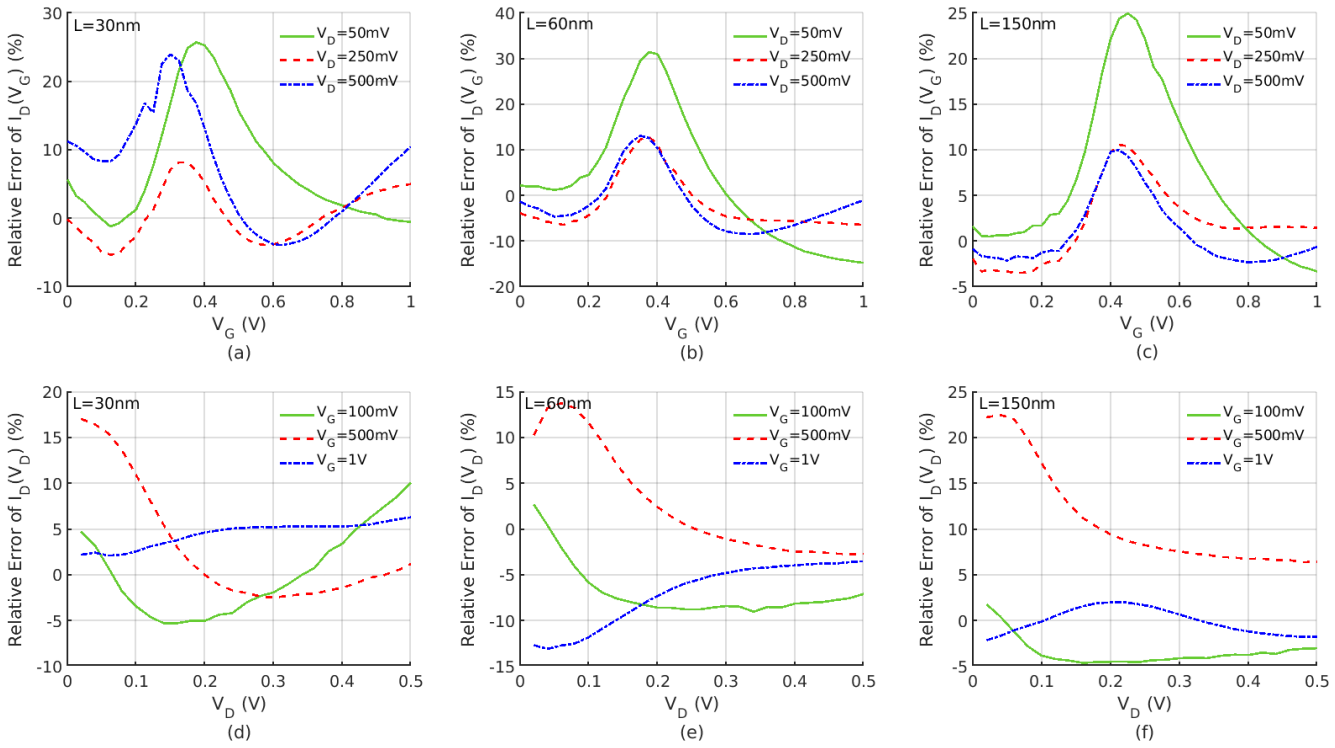

FIGURE 12. Top: Relative error for three $I_D(V_G)$ curves for $L = 30$ nm (a), $L = 60$ nm (b) and $L = 150$ nm (c) N-MOS transistors for different values of V_D : 50 mV (solid green line), 250 mV (dashed red line) and 500 mV (dot-dashed blue line). Bottom: Relative error for three $I_D(V_D)$ curves for $L = 30$ nm (d), $L = 60$ nm (e) and $L = 150$ nm (f) N-MOS transistors for different values of V_G : 100 mV (solid green line), 500 mV (dashed red line) and 900 mV (dot-dashed blue line).

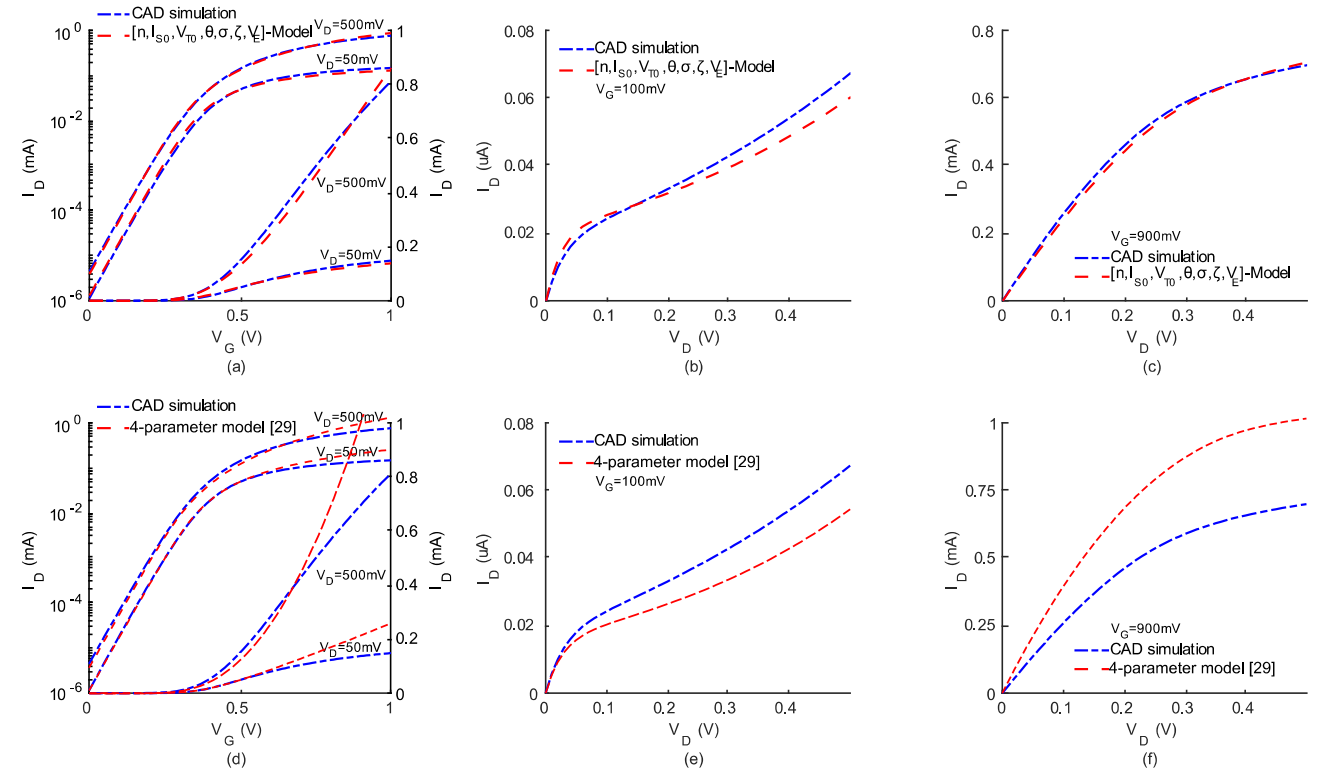

FIGURE 13. Comparison between CAD-oriented model UTSOI2 and: (a)-(b)-(c) the proposed design-oriented model for $L = 30$ nm, $I_D(V_G)$ curves for $V_D = 50$ mV and $V_D = 500$ mV, $I_D(V_D)$ curves for $V_G = 100$ mV, and $I_D(V_D)$ curves for $V_G = 900$ mV, respectively; (d)-(e)-(f) the 4-parameter design-oriented model in [29] for $L = 30$ nm, $I_D(V_G)$ curves for $V_D = 50$ mV and $V_D = 500$ mV, $I_D(V_D)$ curves for $V_G = 100$ mV, and $I_D(V_D)$ curves for $V_G = 900$ mV, respectively.

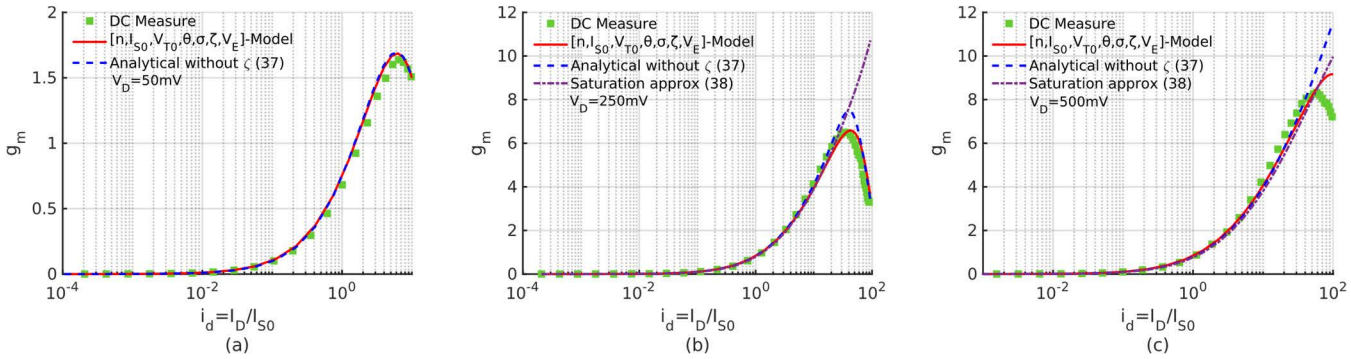

FIGURE 14. $L = 30$ nm and $W = 1$ μm N-MOS transistor $g_m(i_d)$ curve for V_D =50mV (a), 250 mV (b) and 500 mV (c): Comparison between measures (green squares), numerical derivative based on 7 parameters model (red solid line) and analytical expression based on linear (dashed blue line) and saturation approximation (dot-dashed violet line).

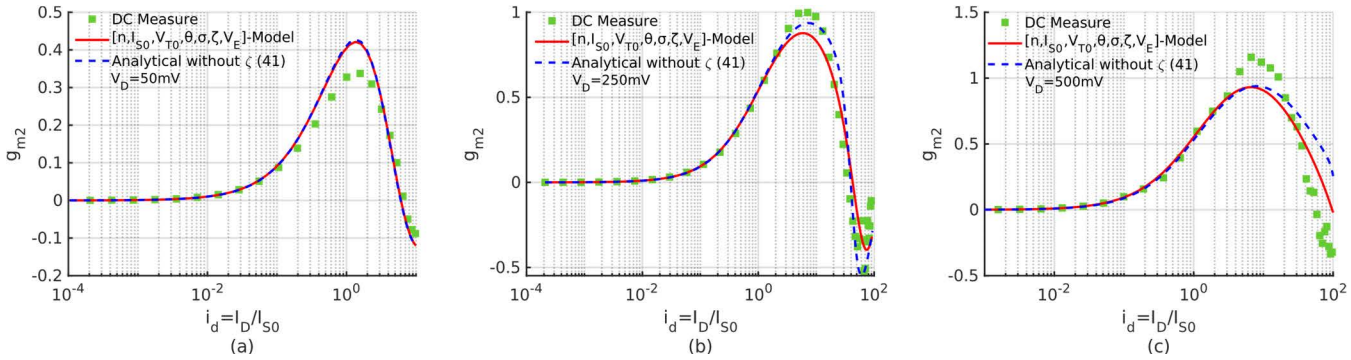

FIGURE 15. $L = 30$nm and $W = 1$ μm N-MOS transistor g_{m2} (i_d) curve for $V_D = 50$ mV (a), 250 mV (b) and 500 mV (c): Comparison between measures (green squares), numerical derivative based on 7 parameters model (red solid line) and analytical expression based on linear approximation (dashed blue line).

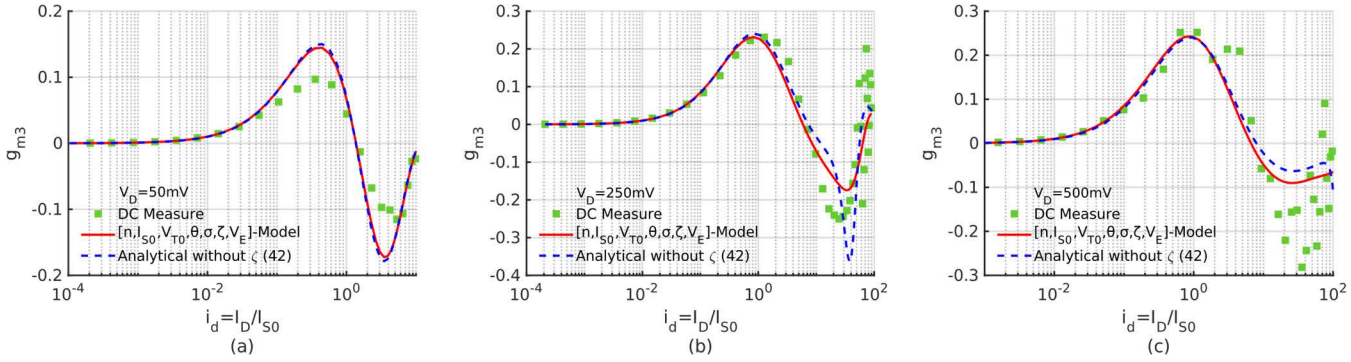

FIGURE 16. $L = 30$nm and $W = 1$ μm N-MOS transistor g_{m3} (i_d) curve for $V_D = 50$ mV (a), 250 mV (b) and 500 mV (c): Comparison between measures (green squares) and numerical derivative based on 7 parameters model (red solid line) and analytical expression based on linear approximation (dashed blue line).

As it can be seen, the proposed expression is in good agreement with the measurements and the numerical derivative in the saturated region ($V_D = 500$ mV) up to a large inversion level ($i_d = 50$). However, since the computation is only valid when the transistor is in deep saturated region, the results are less accurate for all the other biasing conditions. Hence, and as shown on Fig. 14(b) and (c), the analytical expression of the gate transconductance neglecting the carrier velocity saturation is still relevant in saturated region, especially for weak and moderate inversion regimes.

D. ANALYTICAL APPROXIMATION OF THE SECOND- AND THIRD-ORDER DERIVATIVES OF ID WITH RESPECT TO VG

According to the results above, the second and third order current derivatives (g_{m2}, g_{m3}) can be expressed under the same assumption used for estimating the transconductance

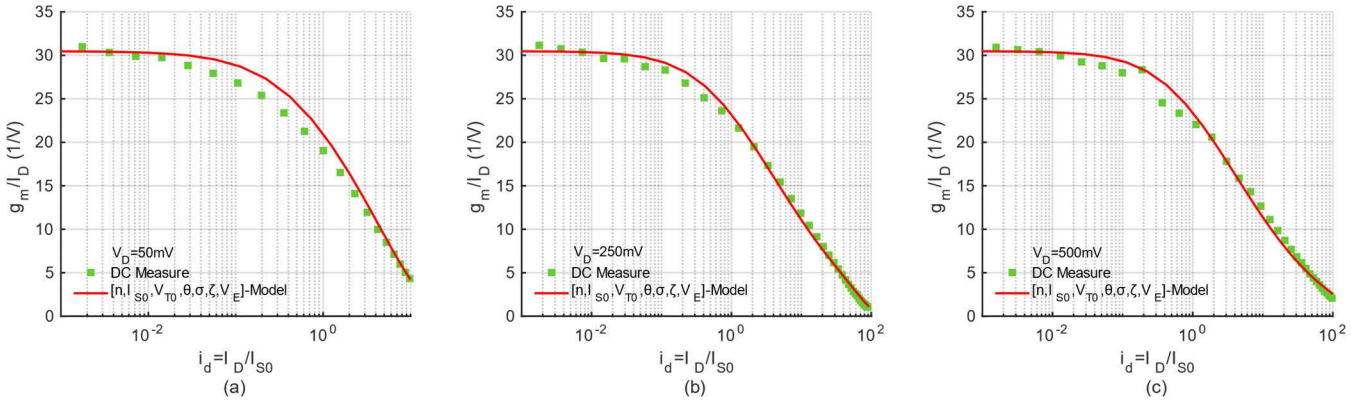

FIGURE 17. $L = 30$nm and $W = 1$ μm N-MOS transistor $g_m/I_D(i_d)$ curve for $V_D = 50$ mV (a), 250 mV (b) and 500 mV (c): Comparison between measures (green squares) and numerical derivative based on 7 parameters model (red solid line).

(i.e., considering the effect of the DIBL and carrier mobility reduction but neglecting the carrier velocity saturation). Thus, g_{m2} and g_{m3} can be expressed as follows,

$$g_{m2} = \frac{\partial^2 i_d}{\partial v_g^2} = \frac{2}{B}\left[\frac{q_S}{1+q_S} - \frac{q_D}{1+q_D} - \frac{\theta}{4}\left[2g_m\left(\frac{q_S}{1+q_S} + \frac{q_D}{1+q_D}\right) + i_d\left(\frac{q_S}{(1+q_S)^3} + \frac{q_D}{(1+q_D)^3}\right)\right]\right], \tag{41}$$

$$g_{m3} = \frac{\partial^3 i_d}{\partial v_g^3} = \frac{2}{B}\left[\frac{q_S}{(1+q_S)^3} - \frac{q_D}{(1+q_D)^3} - \frac{\theta}{4}\left[3g_{m2}\left(\frac{q_S}{1+q_S} + \frac{q_D}{1+q_D}\right) + 3g_m\left(\frac{q_S}{(1+q_S)^3} + \frac{q_D}{(1+q_D)^3}\right) + i_d\left(\frac{q_S\,(1-2q_S)}{(1+q_S)^5} + \frac{q_D\,(1-2q_D)}{(1+q_D)^5}\right)\right]\right]. \tag{42}$$

Fig. 15 and Fig. 16 represent the analytical expressions of g_{m2} and g_{m3} in (41) and (42), respectively, as a function of i_d. It can be seen that there is a good agreement with both measurements and numerical derivations of the complete model. As g_{m2} and g_{m3} are used to estimate non-linearities of analog/RF circuits, the proposed model provides accurate results (using numerical derivatives) in all regions and inversion domains. Also, the simplified g_{m2} and g_{m3} expressions can be used in analytical design methodologies to get an estimate of the circuit behavior.

VI. DISCUSSION

The results presented so far demonstrate that the analytical design-oriented model proposed is robust and able to describe the behavior of the transistor drain current in all inversion regimes and all operation regions of the transistor. Although a certain degree of complexity has been added through these 7 parameters, they are required for a meaningful description of the main physical short-channel effects present in the MOS transistor in advanced nanometric nodes. One additional benefit of keeping an explicit link between the model parameters and the physical effects is that it may allow to optimize the circuit performance via technology optimization.

Proposing a multi-parameter model allows for a clear separation of the different effects so that technologists can clearly understand limitations and work for technology optimization. For instance, considering both the mobility reduction factor, θ, and the carrier velocity saturation, ζ, allows to discriminate the effect of the high transverse and longitudinal electric fields, respectively. So, if the θ parameter was not present in the model, the current reduction would be accounted for by overestimating the carrier saturation velocity, and thus linearity issue root cause would not be identified in the simulations/calculation results. In this sense, our 7 parameters model paves the way for a design/technology co-optimization approach.

Another key point of the proposed 7-parameter model is its validity for all V_D values which is not generally considered in similar analytical design-oriented models. The increased complexity of the model has to be compared to previously presented approaches based on look-up tables or artificial V_D-dependent parameters. The proposed model extends the field of analytical based design, especially in the domain of non-linearities estimation, and increases the variety of possible circuits addressed by this design approach (especially the ones with low gate voltage swing and high drain voltage swing – Transimpedance Amplifier as an example).

To summarize the pros and cons of the proposed approach using a design-oriented model, Table 2 below presents a comparison of its main features with the ones of design methodologies based on compact models, 4-parameter EKV/ACM models, and Look-Up Table (LUT) models. The comparison is illustrated using "+" and "-" signs for advantages and disadvantages respectively. Besides, the degree of improvement of a model according to a feature is highlighted by the number of these signs, where "+++" refers to the best-in-class.

In addition, as a future line of work, the presented model could be extended to describe the noise and AC behavior of

TABLE 2. Comparison of the main design methodology features.

Features	Compact models	4-param. EKV/ACM models	LUT models	This work
Simulation accuracy	+++	+	+(+)	++
Model simplicity	--	++	++	+
VD dependency	+++	-	+	++
Ease of use	++	++	+	++
Explicit link with technology	++	+	-	++

+++ Very good, ++ Good, + Fair, - Poor

the transistor. An interesting starting point for this extension is sketched in [11], where a dynamic model is described.

VII. CONCLUSION

In this paper we have presented a 7-parameter inversion charge-based model for MOS transistors. The aim of this design-oriented model is to provide a set of analytical equations for the DC and small signal MOSFET behavior to help designers in developing analytical design methods for the first sizing of a circuit. The model includes the main short-channel effects in advanced nanometric technologies and models the dependency of the current on the drain voltage using meaningful physical parameters. A simple extraction procedure was proposed to estimate the model parameters for a given technology based on simple simulations and/or measurements. The validity of the model and especially its dependency with the drain voltage has been demonstrated by comparison with measurements of fabricated transistors in 28nm FD-SOI technology. From this model, analytical expressions of g_m, g_{m2}, g_{m3} and g_{ds} valid for the different regions under consideration have been derived for inclusion in analytical design methodologies. This motivates the authors to extend their work to a design circuit application with non-linear studies in advanced technologies.

Finally, the physical nature of the proposed parameters model offers an insight into the device behavior and the technology fabrication process, which may open the door to technology improvements for optimized performance.

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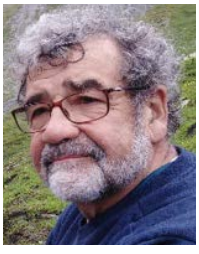

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