

RESEARCH ARTICLE

Analytical Modeling of 3D NAND Flash Cell With a Gaussian Doping Profile

AMIT KUMAR, (Student Member, IEEE), RAUSHAN KUMAR^{ID},
AND SHUBHAM SAHAY^{ID}, (Member, IEEE)

Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur 208016, India

Corresponding author: Shubham Sahay (ssahay@iitk.ac.in)

This work was supported in part by the Startup Research Grant (SRG) from Science and Engineering Research Board (SERB) under Grant SERB/EE/2021358.

ABSTRACT The incessantly increasing demand for highly dense storage medium in this era of big-data has led to the development of 3D NAND Flash memories. 3D NAND Flash based SSDs have revolutionized edge storage and become an integral part of the data warehouses and the cloud storage systems. The conventional 3D NAND flash memory with greater than hundred stacked word-line (WL) layers suffer from channel tapering and non-uniformity in the threshold voltage of cells in different WL layers which necessitates the use of different programming voltages for different WL layers and a complex error-correction circuitry. A non-uniform vertical (Gaussian) channel doping profile alleviates the threshold voltage non-uniformity and leads to a significant reduction in the complexity of the error-correction circuitry and a simple (uniform) programming scheme for all WLs. Although behavioral models have been proposed to utilize 3D NAND flash memory for circuit and system-level applications, an analytical model is important to understand the intricate details of the device physics and propose design guidelines for efficient cell design. To this end, in this paper, for the first time, we have proposed an analytical model for the characteristic length, surface potential and inner potential of the Macaroni-body 3D NAND flash cell with vertical Gaussian doping profile. A strong agreement between the analytical model and the TCAD simulations for different gate lengths (down to 25 nm), inner and outer radius, channel and oxide thickness of the 3D NAND flash cell validates the efficacy of the developed model.

INDEX TERMS 3D NAND flash memory, Macaroni body, vertical Gaussian doping, analytical model.

I. INTRODUCTION

The dramatic shift from the compute-centric paradigm to the data-centric paradigm in this era of big data has led to a surge in the flow of asynchronous data [1], [2]. Ultra-dense storage technologies are urgently required to cope up with this data explosion [3]. Therefore, to achieve the bit density levels required for efficient storage of big data, conventional planar 2D NAND flash cells were incessantly scaled [3], [4], [5]. However, the performance of planar flash cells deteriorates significantly with shrinking of the feature size owing to the considerably large neighboring cell coupling disturbances and crosstalk [6], [7], [8], [9]. To overcome these challenges, several architectures exploiting vertical (3D) stacking

of NAND flash cells such as BiCS, TCAT, VRAT, VNAND, ZNAND etc. were proposed [10], [11]. 3D NAND flash memory has emerged as the most promising candidate for handling big data [2].

The vertical gate-all-around (GAA) Macaroni body structure has gained significant popularity and emerged as a promising candidate for 3D NAND flash memory cell due to its smaller footprint, efficient gate control, enhanced sub-threshold characteristics and higher short-channel immunity as compared to the planar structures [6], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19]. In the Macaroni body FETs, a hollow cylindrical channel with a thickness smaller than the depletion region width is used to enhance the electrostatic integrity and the core of the channel is filled with a dielectric [10], [11], [12], [13], [14], [15], [16], [17], [18], [19]. Furthermore, the narrow channel in the Macaroni

The associate editor coordinating the review of this manuscript and approving it for publication was Cristian Zambelli^{ID}.

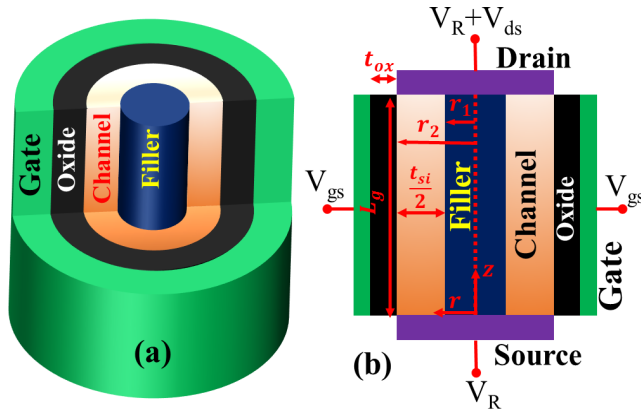


FIGURE 1. (a) 3D schematic view and (b) 2D cross-sectional view of the Macaroni body 3D NAND flash cell with a vertical Gaussian doping profile.

body 3D NAND flash cell reduces the volume of polysilicon and the associated trap charges at the grain boundaries [6]. Therefore, the threshold voltage of the Macaroni body 3D NAND flash cell is less sensitive to the traps as compared to the gate-all-around (GAA) architecture [15], [16].

Moreover, to achieve an ultra-high bit density, several (≥ 176) word line (WL) layers are stacked in commercial 3D NAND flash arrays [20]. This leads to a significant increase in the string height (mold height). Etching a narrow hole in such stacks with a high aspect ratio (typically greater than 40:1) without substantial tapering of the channel region from the source select line (SSL) to the bit select line (BSL) is a technological challenge [17], [21]. This undesirable tapering of the channel region results in cells with different channel thickness at different location along the string [18]. Therefore, the fabrication process for 3D NAND flash induces an inherent non-uniformity in the intrinsic threshold voltage of the cells at different WL layers and necessitates a complex error correction circuitry [17]. To mitigate this non-uniformity in the threshold voltage across the charge-trap flash cells in a string, several techniques such as a non-uniform vertical (Gaussian) channel doping profile, compensated blocking oxide thickness, position-dependent programming/erase voltage or duration, etc. were proposed [17].

Furthermore, to facilitate the utilization of Macaroni body 3D NAND flash array for circuit and system-level applications, behavioral compact models of 3D NAND flash memory cells with uniform channel doping were proposed [19], [22], [23], [24]. Although the behavioral compact model [19] accurately captures the static string current characteristics and the parasitic capacitance components applicable to the Macaroni body 3D NAND flash memory cells with uniform channel doping, it fails to describe the intricate device physics. Therefore, an analytical model is required to understand the electrostatic characteristics and propose design guidelines for optimum performance of Macaroni body 3D NAND flash cells.

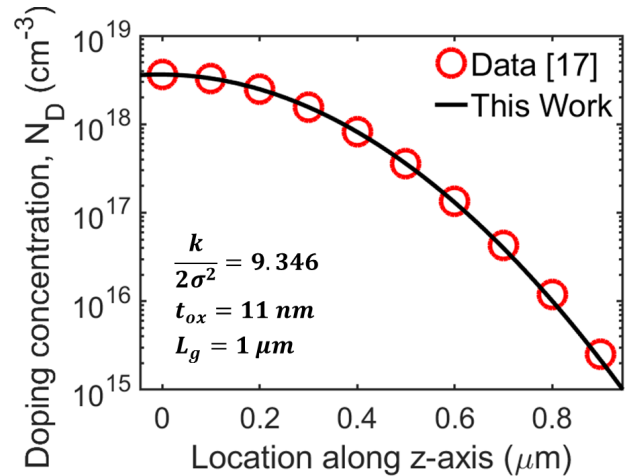


FIGURE 2. Vertical Gaussian doping profile in the channel region proposed in [17] and used in this work.

Analytical models are more accurate since they are derived from the first principles utilizing the fundamental laws of physics such as Maxwell equations and Poisson's equation along with appropriate boundary conditions emanating from Gauss law. These models provide additional information regarding the electrostatics and microscopic properties which are not evident from the experimental results. The behavioral compact models treat the device under test (DUT) as a black box and utilize curve fitting techniques to mimic the macroscopic experimental characteristics by tweaking the empirical parameters. Although even a behavioral compact model may also provide some physical insight, its accuracy while performing any parametric analysis such as investigating impact of change in the structural parameters on the output/transfer characteristics is dubious since the empirical parameters are fitted only to a limited experimental data. Therefore, analytical models are more important for device physicists and technologists to understand the microscopic properties, whereas behavioral compact models are more useful for circuit designers [25].

To this end, an analytical model for the surface potential, inner potential, and the characteristic length (which provides a measure of the electrostatic integrity) of a GAA Macaroni body MOSFET with a uniform doping profile in the channel region were also formulated [12], [13], [26]. However, to mitigate the impact of process-induced substantial tapering of the channel region and the non-uniform threshold voltage in 3D NAND flash cells without introducing significant fabrication overheads or complexity, a vertical Gaussian doping profile in the channel region appears promising [17]. In this technique, to realize a uniform threshold voltage distribution across the string, a high dopant dose is applied at the source end of the channel region to increase the threshold voltage of the cells and a low dopant dose is applied at the drain end of the channel region to reduce the threshold voltage of the cells [17], [27], [28], [29]. Although the analytical model developed in [12] predicts the electrostatic behavior

of the conventional uniformly doped 3D NAND flash, the model cannot be extended to provide the design guidelines for the 3D NAND flash cell with non-uniform doping profile presented in [17]. Moreover, to the best of our knowledge, an analytical model for Macaroni body 3D NAND flash cell with a vertical Gaussian doping profile in the channel region is still elusive.

Therefore, in this work, for the first time, we develop an analytical model for the 3D NAND flash cell with uniform threshold voltage distribution and non-uniform (vertical Gaussian) doping profile which may help in providing the necessary design guidelines for further optimizing its performance. We solve the 3D Poisson's equation in cylindrical coordinates with appropriate boundary conditions to derive an analytical model for the characteristic length, surface potential, and inner potential of a Macaroni body 3D NAND flash cell with a vertical Gaussian doping profile in the channel region. Furthermore, we analyze the accuracy of the developed model by comparing results obtained from the analytical model against the data obtained from 3D TCAD simulations. A strong agreement between our model and the TCAD simulations for different structural parameters such as doping concentration of the channel region, gate length, oxide thickness, inner and outer radius validates the efficacy of the developed model. Although the insights provided by the developed analytical model can be also be obtained with the help of TCAD simulations, considering the computational complexity and the resource (processing power and memory)-intensive requirement of the TCAD simulations, it is better to perform the design exploration across the structural and design parameters utilizing the proposed analytical model which provides accurate results while consuming only a fraction of time and resources of the TCAD simulations. Moreover, as the BSIM-CMG model does not allow the user to define a non-uniform doping profile, the compact model developed for conventional 3D NAND flash cell with uniform doping profile utilizing BSIM-CMG model [19] may not be used for design exploration of 3D NAND flash cell with the non-uniform (vertical Gaussian) doping profile.

TABLE 1. Parameters used for the macaroni body 3D NAND flash cell with a vertical gaussian doping profile.

Parameters	Values
Channel doping (N_D)	$10^{18} - 10^{15} \text{ cm}^{-3}$
Gate Length (L_g)	25 nm, 50 nm, 100nm
Effective oxide thickness (t_{ox})	3 nm, 6 nm, 12 nm
Gate work function (ϕ_m)	5.1 eV
Outer radius (r_2)	17.5 nm, 19.5 nm, 21.5 nm, 23.5 nm
Inner radius (r_1)	13.5 nm, 15.5 nm, 17.5 nm, 19.5 nm

II. DEVICE STRUCTURE

The 3D schematic view and the cross-sectional view of a Macaroni body 3D NAND flash cell with a vertical Gaussian doping in the channel region are shown in Fig. 1(a) and Fig. 1(b), respectively. As can be observed from Fig. 1, in a Macaroni body cell, the polysilicon channel is etched at the

center and filled with a core dielectric filler to realize an ultra-thin channel. This ensures a minimal threshold voltage variation due to the inherent grain boundaries and associated traps owing to a reduction in the volume of grain boundaries and traps present within the channel region. Since the thickness of the polysilicon layer is less than the depletion region width contributed by the gate electrode [10], the Macaroni body cell exhibits an enhanced gate control and a high electrostatic integrity.

The structural parameters used for the Macaroni body 3D NAND flash cell with a vertical Gaussian doping profile in this work are summarized in Table 1. The parameters of the Gaussian doping profile (N_D, k, σ in $N_D(z) = N_D \exp(\frac{-kz^2}{2\sigma^2})$) were tuned to reproduce the non-uniform doping profile reported in [17] for minimizing the threshold voltage non-uniformity as shown in Fig. 2. As shown in Fig. 2 and Table 1, the peak doping concentration at the source end is $N_D \sim 10^{18} \text{ cm}^{-3}$ and the channel doping concentration at the drain end is $N_D \sim 10^{15} \text{ cm}^{-3}$ [17]. Moreover, such a doping profile can be realized experimentally utilizing the multi-implant process and tuning the implant energy and ion dose according to the desired doping levels as done in [17].

III. MODEL DESCRIPTION

To understand the impact of vertical Gaussian doping profile in the channel region of a Macaroni body 3D NAND flash cell, starting from the first principles, we have modelled the key parameters dictating the device performance such as the surface potential, inner potential and the characteristic length (which is a measure of scalability and electrostatic integrity [30], [31]). Since the structure of the Macaroni body 3D NAND flash cell is cylindrical, we use the cylindrical coordinate system instead of Cartesian coordinate system to formulate the analytical model. To obtain the characteristic length and the potential profiles, we solved the three-dimensional Poisson's equation.

A. CHARACTERISTIC LENGTH

The 3D Poisson's equation in cylindrical coordinate system can be expressed as:

$$\frac{\partial^2 \psi}{\partial r^2} + \frac{1}{r} \left(\frac{\partial \psi}{\partial r} \right) + \frac{1}{r^2} \frac{\partial}{\partial \theta} \left(\frac{\partial \psi}{\partial \theta} \right) + \frac{\partial^2 \psi}{\partial z^2} = \frac{-qN_D(z)}{\epsilon_{Si}} \quad \text{for } r_1 \leq r \leq r_2 \quad (1)$$

where $r, \theta,$ and z are the cylindrical coordinate axes along the radial, angular, and axial (along the channel length) directions, ψ is the channel potential, q is the electron charge, ϵ_{Si} is the dielectric constant of silicon and $N_D(z)$ is the donor concentration in the channel region of the Macaroni body cell. As discussed in Section II, the donor concentration $N_D(z)$ varies from the drain end to the source end along the vertical channel in the proposed 3D NAND flash cell as:

$$N_D(z) = N_D \exp\left(\frac{-kz^2}{2\sigma^2}\right) \quad (2)$$

where k and σ are constants tuned to reproduce the optimal doping profile in [17]. Due to the symmetric structure along the axial direction, the channel potential does not vary with the angle in the radial plane. Therefore, ψ is independent of θ i.e. $\frac{\partial \psi(r,\theta,z)}{\partial \theta} = 0$. Equation (1) can then be simplified as a 2D Poisson's equation given by:

$$\frac{\partial^2 \psi}{\partial r^2} + \frac{1}{r} \left(\frac{\partial \psi}{\partial r} \right) + \frac{\partial^2 \psi}{\partial z^2} = \frac{-qN_D}{\epsilon_{Si}} \exp\left(\frac{-kz^2}{2\sigma^2}\right) \quad (3)$$

Now, Young's parabolic potential approximation [32] can be utilized to simplify the 2D electrostatic potential distribution along the radial direction inside the channel region as:

$$\psi(r, z) = C_1(z) + r.C_2(z) + r^2.C_3(z) \quad (4)$$

Since the silicon body is located between r_1 and r_2 ($r_1 \leq r \leq r_2$), we shift the origin to $r = r_1$ and express equation (4) as:

$$\psi(r, z) = C_1(z) + (r - r_1) C_2(z) + (r - r_1)^2 C_3(z) \quad (5)$$

where $C_1(z)$, $C_2(z)$ and $C_3(z)$ are arbitrary coefficients.

To find out the unknown coefficients in equation (5), we have assumed that the electric field lines inside the channel terminate at the silicon body-core filler dielectric interface i.e. the electric field at $r = r_1$ is zero: $\frac{\partial \psi(r_1,z)}{\partial r} = 0$ yielding $C_2(z) = 0$.

Furthermore, we have considered the boundary condition i.e. the electric flux at the interface between the silicon film and the gate oxide must be continuous at $r = r_2$: $\epsilon_{Si} \frac{\partial \psi(r_2,z)}{\partial r} = C_{ox} (V_{gs} - V_{fb} - \psi_s)$ yielding $C_3(z) = \frac{C_{ox}}{\epsilon_{Si} t_{Si}} (V_{gs} - V_{fb} - \psi_s)$ where, t_{Si} is the channel thickness, V_{fb} is the flat-band voltage, ψ_s is the surface potential ($\psi_s = \psi(r = r_2, z)$) and C_{ox} is the effective gate oxide capacitance per unit area of cylindrical Macaroni body cell given by [12]:

$$C_{ox} = \frac{\epsilon_{ox}}{r_2 \ln\left(1 + \frac{t_{ox}}{r_2}\right)} \quad (6)$$

where ϵ_{ox} is the dielectric constant of oxide and t_{ox} is the gate oxide thickness.

Now, we define the potential at the channel-core filler interface ($r = r_1$) as the inner potential, $\psi_o = \psi(r = r_1, z)$. This yields $C_1(z) = \psi_o$.

Utilizing these assumptions and boundary conditions, equation (5) can be simplified as:

$$\psi(r, z) = \psi_o + \frac{C_{ox}}{\epsilon_{Si} t_{Si}} (V_{gs} - V_{fb} - \psi_s) (r - r_1)^2 \quad (7)$$

To find an expression for the surface potential, we use $r = r_2$ in equation (7) to get:

$$\psi_s(z) = \frac{\psi_o(z) + \frac{C_{ox} t_{Si}}{\epsilon_{Si}} (V_{gs} - V_{fb})}{1 + \frac{C_{ox} t_{Si}}{4\epsilon_{Si}}} \quad (8)$$

Now, substituting the value of ψ_s obtained from equation (8) in equation (7), we get:

$$\psi(r, z) = \psi_o(z) + \frac{4C_{ox} (V_{gs} - V_{fb} - \psi_o(z))}{4\epsilon_{Si} t_{Si} + C_{ox} t_{Si}^2} (r - r_1)^2 \quad (9)$$

Substituting $\psi(r, z)$ from equation (9) in equation (3) and using $r = r_1$, we get a second-order differential equation for the inner potential $\psi_o(z)$ as:

$$\frac{d^2 \psi_o(z)}{dz^2} - \frac{\psi_o(z)}{\lambda^2} = \frac{-(V_{gs} - V_{fb})}{\lambda^2} - \frac{qN_D}{\epsilon_{Si}} \exp\left(\frac{-kz^2}{2\sigma^2}\right) \quad (10)$$

where λ is characteristic length of the Macaroni body NAND flash cell expressed as:

$$\lambda = \sqrt{\frac{4\epsilon_{Si} t_{Si} + C_{ox} t_{Si}^2}{8C_{ox}}} \quad (11)$$

B. INNER POTENTIAL, $\psi_o(z)$

To obtain an expression for the inner potential, we solved the differential equation (10) using the superposition principle where the solution consists of a complimentary function and a particular integral (PI). The inner potential ($\psi_o(z)$) can then be expressed as:

$$\psi_o(z) = C_1 \exp\left(\frac{z}{\lambda}\right) + C_2 \exp\left(-\frac{z}{\lambda}\right) + PI \quad (12)$$

where C_1 and C_2 are constants and PI represents the particular integral.

The particular integral (PI) of equation (12) can be obtained from equation (10) as:

$$PI = \left(1 - (\lambda D)^2\right)^{-1} \left\{ (V_{gs} - V_{fb}) + \frac{qN_D \lambda^2}{\epsilon_{Si}} \exp\left(\frac{-kz^2}{2\sigma^2}\right) \right\} \quad (13)$$

where D is the derivative with respect to z (along the axial direction). Although calculation of PI including the Gaussian term is mathematically challenging [29], considering the fact that the channel doping has a constant value at any particular position in the channel along the z -axis, the PI can be approximated as:

$$PI = (V_{gs} - V_{fb}) + \lambda^2 \left(\frac{qN_D}{\epsilon_{Si}}\right) \exp\left(\frac{-kz^2}{2\sigma^2}\right) \quad (14)$$

The details regarding the calculation of PI are discussed in the Appendix.

Now, to determine the constants C_1 and C_2 , we have used two boundary conditions: (a) the inner potential at the source terminal $\psi_o(z = 0) = V_R$, where V_R is the difference between the donor Fermi level and the intrinsic Fermi level, expressed as $V_R = \phi_i \ln\left(\frac{N_D}{n_i}\right)$ and (b) the inner potential at the drain end $\psi_o(z = L_g) = V_R + V_{ds}$ [12], where L_g is the gate length. Applying these boundary conditions in equation (12), C_1 and C_2 are obtained as:

$$C_1 = \frac{V_{ds} + K_1 \cdot \exp\left(-\frac{L_g}{\lambda}\right) - K_2 - V_R \left(\exp\left(-\frac{L_g}{\lambda}\right) - 1\right)}{2 \sinh\left(\frac{L_g}{\lambda}\right)} \quad (15)$$

$$C_2 = \frac{V_R \left(\exp \left(\frac{L_g}{\lambda} \right) - 1 \right) - V_{ds} - K_1 \exp \left(\frac{L_g}{\lambda} \right) + K_2}{2 \sinh \left(\frac{L_g}{\lambda} \right)} \quad (16)$$

where K_1 and K_2 are constants that can be expressed as:

$$K_1 = (V_{gs} - V_{fb}) + \lambda^2 \left(\frac{qN_D}{\epsilon_{Si}} \right) \quad (17)$$

$$K_2 = (V_{gs} - V_{fb}) + \lambda^2 \left(\frac{qN_D}{\epsilon_{Si}} \right) \exp \left(\frac{-kL_g^2}{2\sigma^2} \right) \quad (18)$$

Now, the exact expression of inner potential $\psi_0(z)$ can be obtained by substituting the value of C_1 , C_2 , and PI in equation (12) as:

$$\begin{aligned} \psi_0(z) &= \left[\frac{(V_R - K_1) \sinh \left(\frac{L_g - z}{\lambda} \right) + (V_R + V_{ds} - K_2) \sinh \left(\frac{z}{\lambda} \right)}{\sinh \left(\frac{L_g}{\lambda} \right)} \right] \\ &+ \left\{ (V_{gs} - V_{fb}) + \frac{qN_D \lambda^2}{\epsilon_{Si}} \exp \left(\frac{-kz^2}{2\sigma^2} \right) \right\} \end{aligned} \quad (19)$$

As can be observed from equation (19), the inner potential has a strong dependence on the doping density, gate voltage (V_{gs}), oxide thickness, and the difference of outer and inner radius ($r_2 - r_1$) (channel thickness).

C. SURFACE POTENTIAL, $\psi_s(z)$

Now, an analytical model for the surface potential ($\psi_s = \psi(r = r_2)$) distribution of the Macaroni body 3D NAND flash cell can be obtained from equation (9) as:

$$\psi_s(z) = \psi'_0(z) + (V_{gs} - V_{fb} - \psi'_0(z)) \left(\frac{t_{Si}^2}{8\lambda^2} \right) \quad (20)$$

where $\psi'_0(z)$ is given as:

$$\psi'_0(z) = C'_1 \exp \left(\frac{z}{\lambda} \right) + C'_2 \exp \left(-\frac{z}{\lambda} \right) + PI \quad (21)$$

and C'_1 and C'_2 are constants. To estimate these constants, we have again used two boundary conditions: (a) the surface potential at the source terminal $\psi_s(z = 0) = V_R$ and (b) the surface potential at the drain end $\psi_s(z = L_g) = V_R + V_{ds}$ [12]. PI can be obtained following the same methodology (equation (14)) as discussed in the Appendix. Applying the aforementioned boundary conditions, C'_1 and C'_2 can be obtained as:

$$C'_1 = \frac{\left[V_R \left(\exp \left(-\frac{L_g}{\lambda} \right) - 1 \right) + K_3 \left(\frac{t_{Si}^2}{8\lambda^2} \right) \exp \left(-\frac{L_g}{\lambda} \right) \right] + K_2 - K_1 \exp \left(-\frac{L_g}{\lambda} \right) - K_4 \left(\frac{t_{Si}^2}{8\lambda^2} \right) - V_{ds}}{2 \left(\left(\frac{t_{Si}^2}{8\lambda^2} \right) - 1 \right) \sinh \left(\frac{L_g}{\lambda} \right)} \quad (22)$$

$$C'_2 = \frac{\left[V_{ds} + K_1 \exp \left(\frac{L_g}{\lambda} \right) + K_4 \left(\frac{t_{Si}^2}{8\lambda^2} \right) - K_2 \right] - K_3 \left(\frac{t_{Si}^2}{8\lambda^2} \right) \exp \left(\frac{L_g}{\lambda} \right) - V_R \left(\exp \left(\frac{L_g}{\lambda} \right) - 1 \right)}{2 \left(\left(\frac{t_{Si}^2}{8\lambda^2} \right) - 1 \right) \sinh \left(\frac{L_g}{\lambda} \right)} \quad (23)$$

where K_3 and K_4 are constants expressed as:

$$K_3 = \lambda^2 \left(\frac{qN_D}{\epsilon_{Si}} \right) \quad (24)$$

$$K_4 = \lambda^2 \left(\frac{qN_D}{\epsilon_{Si}} \right) \exp \left(\frac{-kL_g^2}{2\sigma^2} \right) \quad (25)$$

Now, substituting the values of C'_1 , C'_2 and PI in equation (21) $\psi'_0(z)$ can be expressed as:

$$\begin{aligned} \psi'_0(z) &= \left[\frac{K_6 \sinh \left(\frac{z}{\lambda} \right) - K_5 \sinh \left(\frac{L_g - z}{\lambda} \right)}{\sinh \left(\frac{L_g}{\lambda} \right) \left(1 - \frac{t_{Si}^2}{8\lambda^2} \right)} \right] \\ &+ \left\{ (V_{gs} - V_{fb}) + \frac{qN_D \lambda^2}{\epsilon_{Si}} \exp \left(\frac{-kz^2}{2\sigma^2} \right) \right\} \end{aligned} \quad (26)$$

where K_5 and K_6 are constants expressed as:

$$K_5 = K_1 - V_R - K_3 \left(\frac{t_{Si}^2}{8\lambda^2} \right) \quad (27)$$

$$K_6 = V_R + V_{ds} - K_2 + K_4 \left(\frac{t_{Si}^2}{8\lambda^2} \right) \quad (28)$$

The exact expression for the surface potential $\psi_s(z)$ can then be obtained by substituting the value of $\psi'_0(z)$ from equation (26) in equation (20) as:

$$\begin{aligned} \psi_s(z) &= (V_{gs} - V_{fb}) + K_7 \exp \left(\frac{-kz^2}{2\sigma^2} \right) \\ &+ \left[\frac{K_6 \sinh \left(\frac{z}{\lambda} \right) - K_5 \sinh \left(\frac{L_g - z}{\lambda} \right)}{\sinh \left(\frac{L_g}{\lambda} \right)} \right] \end{aligned} \quad (29)$$

where K_7 is a constant given by:

$$K_7 = \frac{qN_D \lambda^2}{\epsilon_{Si}} \left(1 - \frac{t_{Si}^2}{8\lambda^2} \right) \quad (30)$$

IV. RESULTS AND DISCUSSION

To validate the developed analytical model for the inner potential and the surface potential of the Macaroni body 3D NAND flash cell, we have compared the results obtained from the analytical model against the TCAD simulations for different device parameters such as outer radius (r_2), inner radius (r_1), gate length (L_g), oxide thickness (t_{ox}) and gate bias (V_{gs}). Sentaurus TCAD [33] was utilized for performing device simulations. Carrier transport was modelled using the drift-diffusion formalism. The degradation in the carrier mobility due to dopant scattering and high electric field

was considered using the doping-dependent mobility model and the normal field-dependent mobility model. The model parameters of the TCAD simulation setup were calibrated by reproducing the experimental static characteristics of the 3D NAND flash string with 10 WLs [34] as done in [19]. As can be observed from Fig. 3, the simulation results match with the experimental data of [34] validating the accuracy of the TCAD simulation setup used in this work.

To analyze the variation in the inner potential along the channel length (axial direction) of the Macaroni body 3D NAND flash cell for different channel thickness, we varied the outer radius, r_2 (inner radius, r_1) without changing the inner radius (outer radius) and other device parameters such as oxide thickness, channel length and doping profile. First, we fixed the inner radius at 13.5 nm and varied the outer radius to 17.5 nm ($\frac{t_{si}}{2} = 4\text{ nm}$), 19.5 nm ($\frac{t_{si}}{2} = 6\text{ nm}$), 21.5 nm ($\frac{t_{si}}{2} = 8\text{ nm}$), and 23.5 nm ($\frac{t_{si}}{2} = 10\text{ nm}$) as shown in Fig. 4(a).

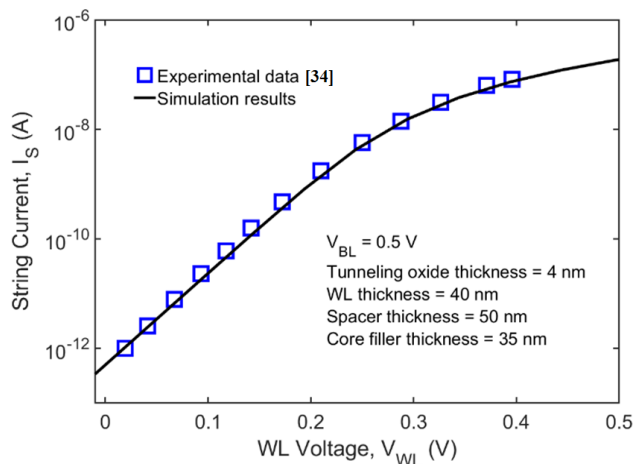


FIGURE 3. Calibration of the TCAD simulation setup by reproducing the experimental string current (static) characteristics of a 3D NAND flash string with 10 WLs of [34].

Then, we varied the inner radius to 13.5nm ($\frac{t_{si}}{2} = 10\text{ nm}$), 15.5nm ($\frac{t_{si}}{2} = 8\text{ nm}$), 17.5nm ($\frac{t_{si}}{2} = 6\text{ nm}$), 19.5nm ($\frac{t_{si}}{2} = 4\text{ nm}$) while keeping the outer radius as 23.5 nm as shown in Fig. 4(b). As can be observed from Fig. 4, a reduction in the channel thickness leads to a larger dynamic range of the inner potential and a better gate control [35]. Although the characteristic length which represents the electrostatic integrity (equation (11)) is not a direct function of r_1 or r_2 individually, it depends significantly on the channel thickness ($r_2 - r_1$). A smaller value of ($r_2 - r_1$) implies a lower characteristic length representing an efficient gate control, a higher scalability and a lower leakage current [12]. Therefore, an ultra-thin Macaroni body should be utilized while designing the 3D NAND flash cell with vertical Gaussian doping profile with significantly enhanced electrostatic integrity. Moreover, an ultra-thin Macaroni body also ensures a minimal spatial (cell-to-cell) threshold voltage fluctuation owing to the reduced number of polysilicon grains

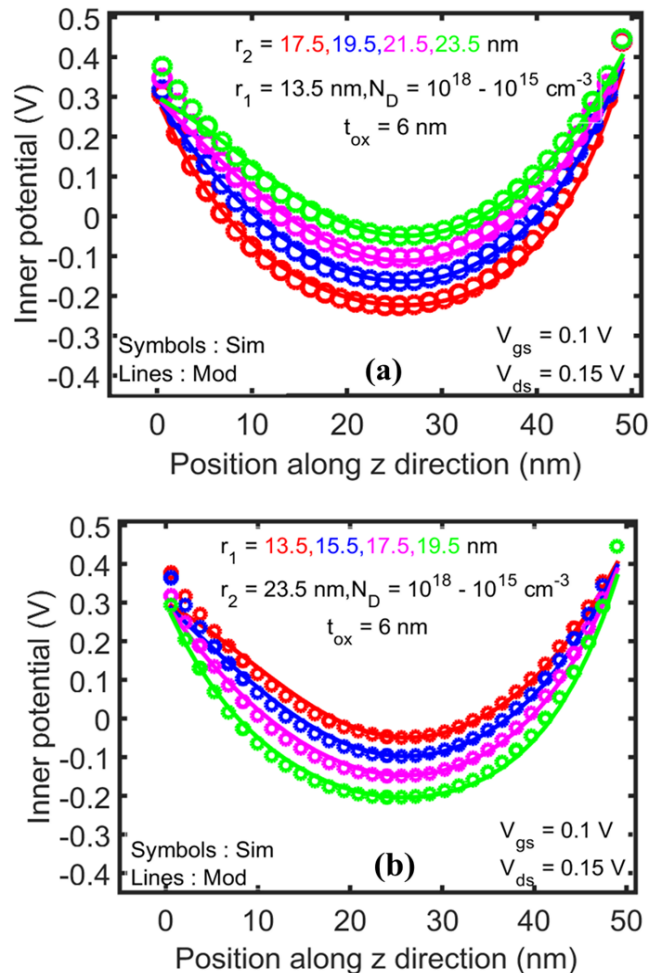


FIGURE 4. Variation of the inner potential along the channel length (axial direction) for different (a) outer radius (r_2) and (b) inner radius (r_1).

in the channel region [10]. Also, r_2 dictates the footprint of the vertical Macaroni body 3D NAND flash cell and should be kept as minimum as possible. Furthermore, the results obtained from the analytical model match exactly with the TCAD simulations validating the proposed model.

We have also analyzed the impact of oxide thickness (t_{ox}) on the distribution of inner potential along the channel length (axial direction) as shown in Fig. 5(a). As t_{ox} increases, the electrostatic integrity reduces due to an increase in the characteristic length (equation (11)). Therefore, the inner potential at the center of the channel region increases leading to a reduction in the dynamic range indicating a poor gate control. This leads to a complex design guideline for the 3D NAND flash cell with vertical Gaussian doping profile with respect to the oxide stack thickness. While an ultra-thin gate oxide stack (yielding a smaller characteristic length) should be used to increase the immunity against the short channel effects, incessant scaling of the gate oxide may degrade the retention characteristics owing to the stress-induced leakage current (SILC) [10], [36].

Furthermore, to understand the scaling prospects, we have also analyzed the impact of gate length (L_g) on the

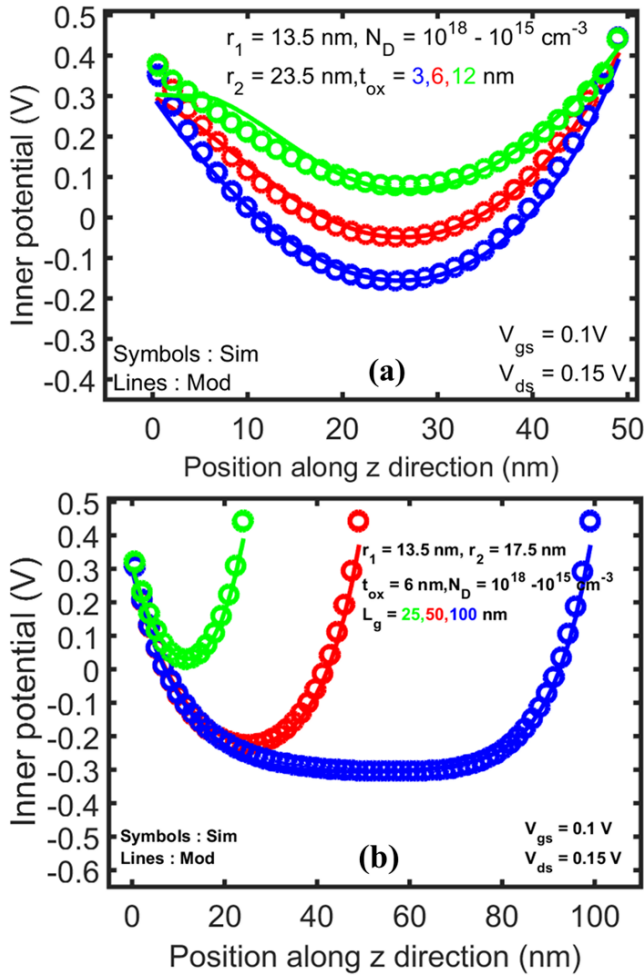


FIGURE 5. Variation of the inner potential along the channel length (axial direction) for different (a) oxide thickness (t_{ox}) and (b) gate length (L_g).

distribution of inner potential along the channel length (axial direction) as shown in Fig. 5(b). As the gate length reduces, the influence of drain electric field on the channel region increases resulting in a reduction in the electrostatic integrity [35]. Therefore, the dynamic range of inner potential distribution is larger for the Macaroni body 3D NAND flash cell with higher gate lengths indicating a better gate control of the channel region. Since 3D NAND flash cell is essentially a vertical structure, we may utilize cells with a larger gate length and improved electrostatic integrity without increasing the area overhead. However, using 3D NAND flash cell with large gate length may restrict the number of word line layers which may be stacked owing to the fabrication constraints while etching deep trenches with high aspect ratio.

To understand the influence of inner and outer radius on the channel electrostatics, we investigated the surface potential distribution by selecting different combinations of the inner radius (r_1) and the outer radius (r_2) while keeping a constant channel thickness ($r_2 - r_1 = \frac{t_{si}}{2}$) in an attempt to decouple the impact of channel thickness and the inner and outer radius. We observe from Figs. 6 (a) and (b) (also

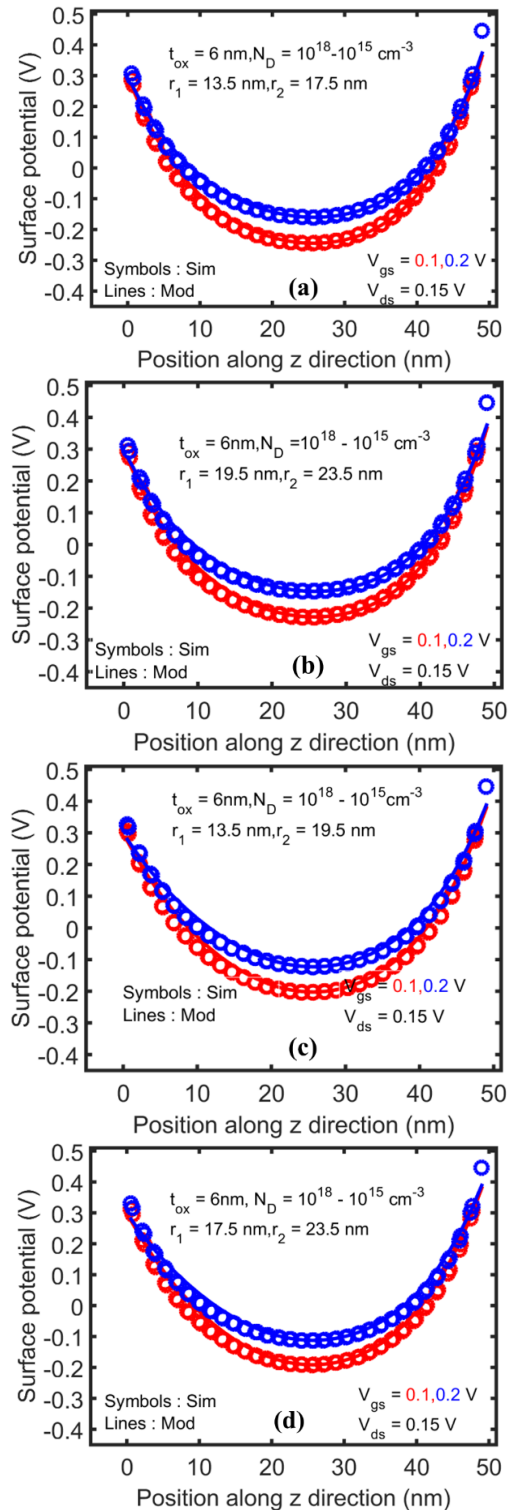


FIGURE 6. Variation in the surface potential along the channel length (axial direction) for different inner and outer radius (a) $r_1=13.5$ nm and $r_2=17.5$ nm ($\frac{t_{si}}{2} = 4$ nm), (b) $r_1=19.5$ nm and $r_2=23.5$ nm ($\frac{t_{si}}{2} = 4$ nm), (c) $r_1=13.5$ nm and $r_2=19.5$ nm ($\frac{t_{si}}{2} = 6$ nm), (d) $r_1=17.5$ nm and $r_2=23.5$ nm ($\frac{t_{si}}{2} = 6$ nm) at two different gate to source voltage for fixed oxide thickness and doping profile.

Figs. 6(c) and (d) that the surface potential profiles are same for different combinations of inner and outer radius when

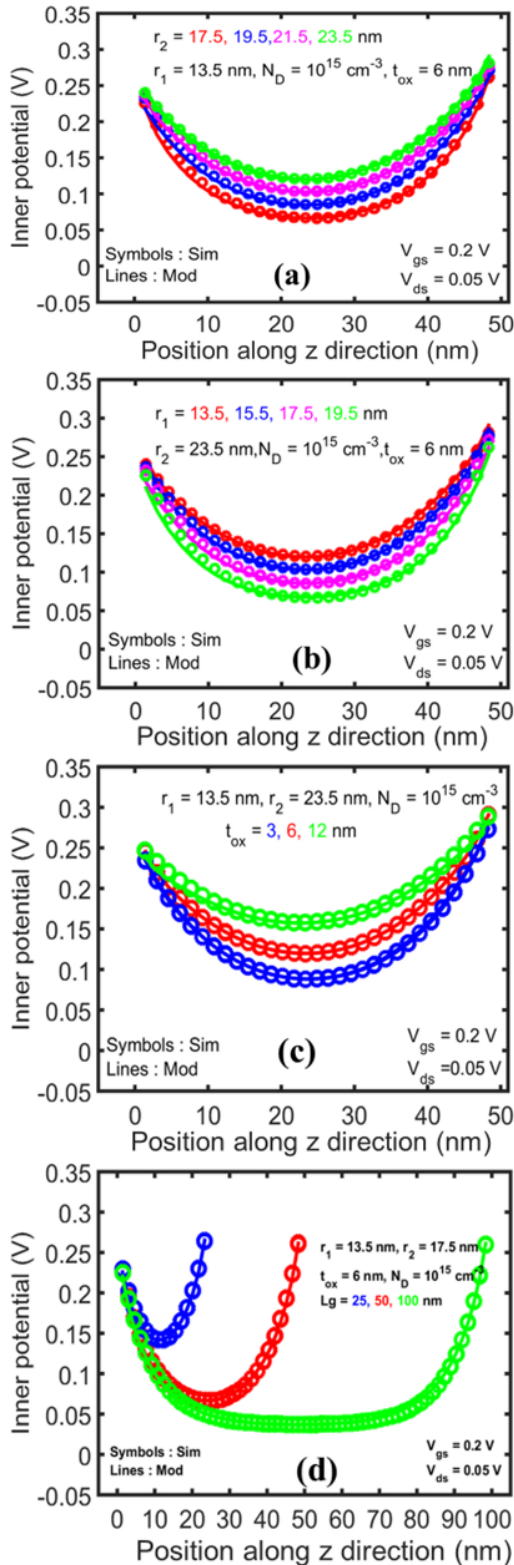


FIGURE 7. Variation of the inner potential along the channel length (axial direction) for different (a) outer radius (r_2), (b) inner radius (r_1), (c) oxide thickness (t_{ox}), and (d) gate length (L_g) for 3D NAND flash cell with uniform doping along the channel.

the channel thickness is constant. This clearly indicates that the surface potential is independent of the value of inner and

outer radius and depends only on the channel thickness as also suggested by our analytical model (equation (29)).

While the channel thickness [$2(r_2 - r_1)$] needs to be small, the outer radius (r_2) should also be kept as minimum as possible since r_2 dictates the footprint of the vertical Macaroni body 3D NAND flash cell. Moreover, as the gate voltage increases, the surface potential reduces gradually approaching its minimum value at the threshold voltage [13].

V. EXTENDING THE MODEL FOR CONSTANT DOPING PROFILE

The developed model can be extended to obtain an analytical model for 3D NAND flash cell with a uniform doping profile [12] by simply using $z = 0$ in equation (2). The final expressions obtained for the characteristic length, the inner potential and the surface potential corroborates well with the results presented in [12]. The results of the analytical model and TCAD simulations for the inner potential distribution for different parameters such as channel thickness, oxide thickness, and gate length are shown in Fig. 7. It is evident from Fig. 7 that the dynamic range of the inner potential in 3D NAND flash cell with uniform doping profile is significantly lower as compared to the dynamic range of the inner potential of 3D NAND flash cells with vertical Gaussian doping profile (Figs. 4 and 5) for same silicon thickness, oxide thickness, and gate length. This clearly indicates the enhanced electrostatic integrity in 3D NAND flash cell with a non-uniform (vertical Gaussian) doping profile. Therefore, the proposed analytical model helps in providing necessary design guidelines for realizing 3D NAND flash cell with optimal performance.

VI. CONCLUSION

In this work, for the first time, we derived an analytical model for the characteristic length, surface potential, and inner potential distribution of Macaroni body 3D NAND flash cell with vertical Gaussian doping profile. To analyze the efficacy of the developed model, we compared the results obtained from the analytical model against the TCAD simulations. A strong agreement between the analytical model and the TCAD simulations for different device parameters such as oxide thickness, channel length, inner and outer radius, channel thickness and doping profile validates the accuracy of the developed model. The design guidelines obtained from the developed model may provide incentive for efficient design of 3D NAND flash cells.

APPENDIX

The particular integral (PI) of equation (10) can be obtained as:

$$PI = \frac{1}{((\lambda D)^2 - 1)} \left\{ -(V_{gs} - V_{fb}) - \frac{qN_D\lambda^2}{\epsilon_{Si}} \exp\left(\frac{-kz^2}{2\sigma^2}\right) \right\} \quad (A1)$$

$$PI = \left(1 - (\lambda D)^2\right)^{-1} \left\{ (V_{gs} - V_{fb}) + \frac{qN_D\lambda^2}{\epsilon_{Si}} \exp\left(\frac{-kz^2}{2\sigma^2}\right) \right\} \quad (A2)$$

Expanding $(1 - (\lambda D)^2)^{-1}$, we obtain:

$$(1 - (\lambda D)^2)^{-1} = 1 + (\lambda D)^2 + (\lambda D)^4 + \dots + (\lambda D)^{2n} \quad (A3)$$

Substitute the value of $(1 - (\lambda D)^2)^{-1}$ in equation (A2), PI can be expressed as:

$$PI = \left(1 + (\lambda D)^2 + (\lambda D)^4 + \dots + (\lambda D)^{2n}\right) \left\{ (V_{gs} - V_{fb}) + \frac{qN_D\lambda^2}{\epsilon_{Si}} \exp\left(\frac{-kz^2}{2\sigma^2}\right) \right\} \quad (A4)$$

which can be further simplified as:

$$PI = (V_{gs} - V_{fb}) + \frac{qN_D\lambda^2}{\epsilon_{Si}} \sum_{i=0}^n (\lambda D)^{2i} \exp\left(\frac{-kz^2}{2\sigma^2}\right) \quad (A5)$$

Although calculation of PI including the Gaussian term $\left(\sum_{i=0}^n (\lambda D)^{2i} \exp\left(\frac{-kz^2}{2\sigma^2}\right)\right)$ is non-trivial and complex [29], considering the fact that the channel doping has a constant value at any particular position in the channel along the z -axis, the exponential term in equation (A4) yields a constant value. Therefore, the higher order terms of the differential operator reduce to zero and the final expression of particular integral (PI) can be obtained as:

$$PI = (V_{gs} - V_{fb}) + \lambda^2 \left(\frac{qN_D}{\epsilon_{Si}}\right) \exp\left(\frac{-kz^2}{2\sigma^2}\right) \quad (A6)$$

ACKNOWLEDGMENT

(Amit Kumar and Raushan Kumar contributed equally to this work.)

REFERENCES

- [1] S. Okamoto, C. Sun, S. Hachiya, T. Yamada, Y. Saito, T. O. Iwasaki, and K. Takeuchi, "Application driven SCM and NAND flash hybrid SSD design for data-centric computing system," in *Proc. IEEE Int. Memory Workshop (IMW)*, May 2015, pp. 1–4, doi: [10.1109/IMW.2015.7150277](https://doi.org/10.1109/IMW.2015.7150277).
- [2] S. Liang, Z. Qiao, S. Tang, J. Hochstetler, S. Fu, W. Shi, and H.-B. Chen, "An empirical study of quad-level cell (QLC) NAND flash SSDs for big data applications," in *Proc. IEEE Int. Conf. Big Data (Big Data)*, Dec. 2019, pp. 3676–3685, doi: [10.1109/BigData47090.2019.9006406](https://doi.org/10.1109/BigData47090.2019.9006406).
- [3] S. Tanakamaru, M. Doi, and K. Takeuchi, "Unified solid-state-storage architecture with NAND flash memory and ReRAM that tolerates 32× higher BER for big-data applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 2013, pp. 226–227, doi: [10.1109/ISSCC.2013.6487711](https://doi.org/10.1109/ISSCC.2013.6487711).
- [4] C. M. Compagnoni, A. Goda, A. S. Spinelli, P. Feeley, A. L. Lacaita, and A. Visconti, "Reviewing the evolution of the NAND flash technology," *Proc. IEEE*, vol. 105, no. 9, pp. 1609–1633, Sep. 2017, doi: [10.1109/JPROC.2017.2665781](https://doi.org/10.1109/JPROC.2017.2665781).
- [5] R. Micheloni, S. Aritome, and L. Crippa, "Array architectures for 3-D NAND flash memories," *Proc. IEEE*, vol. 105, no. 9, pp. 1634–1649, Sep. 2017, doi: [10.1109/JPROC.2017.2697000](https://doi.org/10.1109/JPROC.2017.2697000).
- [6] H. Tanaka, M. Kido, K. Yahashi, M. Oomura, R. Katsumata, M. Kito, Y. Fukuzumi, M. Sato, Y. Nagata, Y. Matsuoka, Y. Iwata, H. Aochi, and A. Nitayama, "Bit cost scalable technology with punch and plug process for ultra high density flash memory," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2007, pp. 14–15, doi: [10.1109/VLSIT.2007.4339708](https://doi.org/10.1109/VLSIT.2007.4339708).
- [7] H. Kim, S.-J. Ahn, Y. G. Shin, K. Lee, and E. Jung, "Evolution of NAND flash memory: From 2D to 3D as a storage market leader," in *Proc. IEEE Int. Memory Workshop (IMW)*, May 2017, pp. 1–4, doi: [10.1109/IMW.2017.7939081](https://doi.org/10.1109/IMW.2017.7939081).
- [8] T. Tanaka, M. Helm, T. Vali, R. Ghodsi, K. Kawai, J.-K. Park, S. Yamada, F. Pan, Y. Einaga, A. Ghalam, and T. Tanzawa, "A 768 Gb 3b/cell 3D-floating-gate NAND flash memory," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 142–144, doi: [10.1109/ISSCC.2016.7417947](https://doi.org/10.1109/ISSCC.2016.7417947).
- [9] M. Bavandpour, S. Sahay, M. R. Mahmoodi, and D. Strukov, "Mixed-signal vector-by-matrix multiplier circuits based on 3D-NAND memories for neurocomputing," in *Proc. Design, Automat. Test Eur. Conf. Exhib. (DATE)*, Mar. 2020, pp. 696–701, doi: [10.23919/DATE48585.2020.9116401](https://doi.org/10.23919/DATE48585.2020.9116401).
- [10] R. Micheloni, *3D Flash Memories*. Dordrecht, The Netherlands: Springer, 2016.
- [11] Y. Nishi and B. Magyari-Kope, *Advances in Non-Volatile Memory and Storage Technology*. Sawston, U.K.: Woodhead Publishing, 2019.
- [12] Q. Nguyen-Gia, M. Kang, J. Jeon, and H. Shin, "Characteristic length of macaroni channel MOSFET," *IEEE Electron Device Lett.*, vol. 40, no. 11, pp. 1720–1723, Nov. 2019, doi: [10.1109/LED.2019.2942619](https://doi.org/10.1109/LED.2019.2942619).
- [13] Q. Nguyen-Gia, M. Kang, J. Jeon, and H. Shin, "Models of threshold voltage and subthreshold slope for macaroni channel MOSFET," *IEEE Electron Device Lett.*, vol. 41, no. 7, pp. 973–976, Jul. 2020, doi: [10.1109/LED.2020.2995642](https://doi.org/10.1109/LED.2020.2995642).
- [14] H. Aochi, "BiCS flash as a future 3D non-volatile memory technology for ultra high density storage devices," in *Proc. IEEE Int. Memory Workshop*, May 2009, pp. 1–2, doi: [10.1109/IMW.2009.5090581](https://doi.org/10.1109/IMW.2009.5090581).
- [15] G. M. Paolucci, A. S. Spinelli, C. M. Compagnoni, and P. Tessariol, "A semi-analytical model for Macaroni MOSFETs with application to vertical flash memories," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 1871–1876, May 2016, doi: [10.1109/TED.2016.2543605](https://doi.org/10.1109/TED.2016.2543605).
- [16] A. S. Spinelli, C. M. Compagnoni, and A. L. Lacaita, "Variability effects in nanowire and macaroni MOSFETs—Part I: Random dopant fluctuations," *IEEE Trans. Electron Devices*, vol. 67, no. 4, pp. 1485–1491, Apr. 2020, doi: [10.1109/TED.2020.2971219](https://doi.org/10.1109/TED.2020.2971219).
- [17] U. M. Bhatt, S. K. Manhas, A. Kumar, M. Pakala, and E. Yieh, "Mitigating the impact of channel tapering in vertical channel 3-D NAND," *IEEE Trans. Electron Devices*, vol. 67, no. 3, pp. 929–936, Mar. 2020, doi: [10.1109/TED.2020.2967869](https://doi.org/10.1109/TED.2020.2967869).
- [18] K. T. Kim, S. W. An, H. S. Jung, K.-H. Yoo, and T. W. Kim, "The effects of taper-angle on the electrical characteristics of vertical NAND flash memories," *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1375–1378, Oct. 2017, doi: [10.1109/LED.2017.2747631](https://doi.org/10.1109/LED.2017.2747631).
- [19] S. Sahay and D. Strukov, "A behavioral compact model for static characteristics of 3D NAND flash memory," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 558–561, Apr. 2019, doi: [10.1109/LED.2019.2901211](https://doi.org/10.1109/LED.2019.2901211).
- [20] J.-W. Park, D. Kim, S. Ok, J. Park, T. Kwon, H. Lee, S. Lim, S. Y. Jung, H. Choi, T. Kang, and G. Park, "A 176-stacked 512 Gb 3b/cell 3D-NAND flash with 10.8 Gb/mm² density with a peripheral circuit under cell array architecture," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 422–423, doi: [10.1109/ISSCC42613.2021.9365809](https://doi.org/10.1109/ISSCC42613.2021.9365809).
- [21] S. Sahay, M. Klachko, and D. Strukov, "Hardware security primitive exploiting intrinsic variability in analog behavior of 3-D NAND flash memory array," *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2158–2164, May 2019, doi: [10.1109/TED.2019.2903786](https://doi.org/10.1109/TED.2019.2903786).
- [22] D. Son, J. Park, and H. Shin, "Investigation and compact modeling of hot-carrier injection for read disturbance in 3-D NAND flash memory," *IEEE Trans. Electron Devices*, vol. 67, no. 7, pp. 2778–2784, Jul. 2020, doi: [10.1109/TED.2020.2993772](https://doi.org/10.1109/TED.2020.2993772).
- [23] M. Kim and H. Shin, "Investigation and SPICE compact model of spacer region for static characteristics of 3-D NAND flash memories," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 4158–4165, Oct. 2020, doi: [10.1109/TED.2020.3014066](https://doi.org/10.1109/TED.2020.3014066).
- [24] M. Bavandpour, S. Sahay, M. R. Mahmoodi, and D. B. Strukov, "3D-aCortex: An ultra-compact energy-efficient neurocomputing platform based on commercial 3D-NAND flash memories," *Neuromorphic Comput. Eng.*, vol. 1, no. 1, Sep. 2021, Art. no. 014001, doi: [10.1088/2634-4386/ac0775](https://doi.org/10.1088/2634-4386/ac0775).
- [25] S. Sahay and M. J. Kumar, *Junctionless Field-Effect Transistors: Design, Modeling, and Simulation*. Hoboken, NJ, USA: Wiley, 2019.
- [26] Q. Nguyen-Gia and H. Shin, "A potential model of triple macaroni channel MOSFETs in subthreshold region," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4195–4200, Sep. 2021, doi: [10.1109/TED.2021.3095023](https://doi.org/10.1109/TED.2021.3095023).

- [27] S. Dubey, P. K. Tiwari, and S. Jit, "A two-dimensional model for the potential distribution and threshold voltage of short-channel double-gate metal-oxide-semiconductor field-effect transistors with a vertical Gaussian-like doping profile," *J. Appl. Phys.*, vol. 108, no. 3, pp. 034518-1–034518-7, 2010, doi: [10.1063/1.3460796](https://doi.org/10.1063/1.3460796).
- [28] B. Singh, D. Gola, K. Singh, E. Goel, S. Kumar, and S. Jit, "Analytical modeling of channel potential and threshold voltage of double-gate junctionless FETs with a vertical Gaussian-like doping profile," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2299–2305, Jun. 2016, doi: [10.1109/TEDE.2016.2556227](https://doi.org/10.1109/TEDE.2016.2556227).
- [29] A. Nandi, A. K. Saxena, and S. Dasgupta, "Analytical modeling of a double gate MOSFET considering source/drain lateral Gaussian doping profile," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3705–3709, Nov. 2013, doi: [10.1109/TEDE.2013.2282632](https://doi.org/10.1109/TEDE.2013.2282632).
- [30] B.-J. Moon, C.-K. Park, K. Lee, and M. Shur, "New short-channel n-MOSFET current-voltage model in strong inversion and unified parameter extraction method," *IEEE Trans. Electron Devices*, vol. 38, no. 3, pp. 592–602, 1991, doi: [10.1109/16.75171](https://doi.org/10.1109/16.75171).
- [31] Z.-H. Liu, C. Hu, J.-H. Huang, T.-Y. Chan, M.-C. Jeng, P. K. Ko, and Y. C. Cheng, "Threshold voltage model for deep-submicrometer MOSFETs," *IEEE Trans. Electron Devices*, vol. 40, no. 1, pp. 86–95, Jan. 1993, doi: [10.1109/16.249429](https://doi.org/10.1109/16.249429).
- [32] K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 36, no. 2, pp. 399–402, Feb. 1989, doi: [10.1109/16.19942](https://doi.org/10.1109/16.19942).
- [33] *Sentaurus Device User Guide*, Synop., Mountain View, CA, USA, 2010.
- [34] D. Resnati, A. Mannara, G. Nicosia, G. M. Paolucci, P. Tessariol, A. S. Spinelli, A. L. Lacaita, and C. M. Compagnoni, "Characterization and modeling of temperature effects in 3-D NAND flash arrays—Part I: Polysilicon-induced variability," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3199–3206, Aug. 2018, doi: [10.1109/TEDE.2018.2838524](https://doi.org/10.1109/TEDE.2018.2838524).
- [35] C. Li, Y. Zhuang, S. Di, and R. Han, "Subthreshold behavior models for nanoscale short-channel junctionless cylindrical surrounding-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3655–3662, Nov. 2013, doi: [10.1109/TEDE.2013.2281395](https://doi.org/10.1109/TEDE.2013.2281395).
- [36] D. J. Dumin and J. R. Maddux, "Correlation of stress-induced leakage current in thin oxides with trap generation inside the oxides," *IEEE Trans. Electron Devices*, vol. 40, no. 5, pp. 986–993, May 1993, doi: [10.1109/16.210209](https://doi.org/10.1109/16.210209).



AMIT KUMAR (Student Member, IEEE) received the B.Tech. degree in electronics and communication engineering from the Haldia Institute of Technology, West Bengal, India, in 2016, and the M.Tech. degree in VLSI and embedded system from the Indian Institute of Technology Patna, India, in 2020. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, Indian Institute of Technology Kanpur, Uttar Pradesh.

His research interests include modeling and simulation of 3D NAND flash and other emerging memory devices.



RAUSHAN KUMAR received the B.Tech. degree in electronics and communication engineering from the National Institute of Technology (NIT), Arunachal Pradesh, in 2018, and the M.Tech. degree in microelectronics and VLSI from the Indian Institute of Technology (IIT) Kanpur, India, in 2021.

His current research interests include design of high-speed peripheral blocks and analytical and compact modeling of memory devices.



SHUBHAM SAHAY (Member, IEEE) received the B.Tech. degree (Hons.) in electronics engineering from IIT (BHU) Varanasi, in 2014, and the Ph.D. degree in electrical engineering from IIT Delhi, in 2018.

He is currently an Assistant Professor with the Department of Electrical Engineering, Indian Institute of Technology (IIT) Kanpur, India. Prior to joining IIT Kanpur, he has worked as a Post-doctoral Research Scholar at the University of California, Santa Barbara, from 2018 to 2020. He has authored a book on *Junctionless Field-Effect Transistors: Design, Modeling, and Simulation* which was published by the Wiley-IEEE Press. He has also published several peer-reviewed articles on topics, including semiconductor device design and modeling, neuromorphic computing, and hardware security primitives utilizing emerging non-volatile memories. His current research interests include hardware neuromorphic computing platforms, hardware security primitives, novel device architectures for sub-10 nm regime, analytical and compact modeling of semiconductor devices and non-volatile memories, and spintronics. He has received four gold medals and several cash prizes from IIT (BHU) Varanasi for his B.Tech. degree. He is the Vice-Chair of IEEE EDS UP Section. He also appeared in the list of Golden Reviewers for IEEE TRANSACTIONS ON ELECTRON DEVICES and IEEE ELECTRON DEVICE LETTERS, from 2016 to 2020. He is an Editor of *IETE Technical Review* and a Review Editor of *Frontiers in Neuroscience: Neuromorphic Engineering* and *Frontiers in Electronics: Integrated Circuits and VLSI*. More details about him can be found at (<http://home.iitk.ac.in/~ssahay>).

...