

RESEARCH ARTICLE

New Driving Structure to Increase Pixel Charging Ratio for UHD TFT-LCDs With High Frame Rate

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ABSTRACT This paper proposes a new driving structure of the thin-film transistor liquid crystal display (TFT-LCD) that can yield a high image quality with a reduction in the number of source driver ICs for use in narrow-bezel notebook displays with ultra-high definition (UHD) and a high frame rate. The proposed driving structure improves the pixel charging ratio by reducing the RC loadings of TFTs of de-multiplexers on data lines and extending the available row-line time for pixel charging. A new gate driver circuit that generates two output waveforms in a single stage is presented to reduce the cost and occupied layout area of gate driver ICs, enabling the realization of high-resolution displays with a narrow bezel. To verify the feasibility of the proposed driving structure, a 12.3-inch panel with UHD (3840 × 2160) and a frame rate of 120 Hz is fabricated. Experimental results demonstrate that the proposed driving structure yields a measured pixel charging ratio of more than 97.09% for a heavy loading pattern with a gray level of 255. Following an accelerated lifetime test, the measured waveforms of the proposed gate driver circuit are stable without any malfunction, demonstrating its high reliability. Therefore, the proposed driving structure and the gate driver circuit are highly suitable for use in UHD TFT-LCD notebook applications.

INDEX TERMS Pixel charging ratio, thin-film transistor liquid crystal display (TFT-LCD), ultra-high definition (UHD).

I. INTRODUCTION

Thin-film transistor liquid crystal displays (TFT-LCDs) [1], [2], [3], [4], [5], [6] are applied in many electronic devices because of their excellent properties such as good image quality, long lifetime, low cost, and highly automated production. With advancements in display technology, the resolution and the frame rate of panels are increasing, enabling the display of high-quality images. Reducing the required number of source driver ICs of TFT-LCDs to yield a high-quality image

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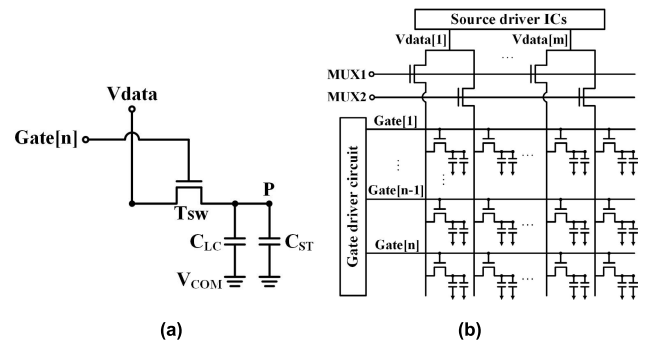
at a lower total manufacturing cost is important to modern display-related industries. Hydrogenated amorphous silicon (a-Si:H) TFTs are commonly used in the TFT-LCDs due to their mature fabrication process and uniform electrical characteristics [7], [8], [9], [10]. However, the low mobility ($<1 \text{ cm}^2/\text{V}\cdot\text{s}$) of a-Si:H TFTs makes them inappropriate for use in ultra-high-definition (UHD) displays because of their low current driving capability. In contrast, low-temperature polycrystalline-silicon (LTPS) TFTs with high mobility and less parasitic capacitance have a better current driving capability [11], [12], [13], [14], and so they are considered to be promising candidates for UHD displays.

TABLE 1. Comparison between proposed and previous works.

	Ref. [19]	Ref. [20]	Ref. [21]	Ref. [22]	Ref. [23]	Ref. [24]	Ref. [25]	This work
Structure	1T2C	1T2C	3T2C1R	2T4C	2T2C	2T2C	1T2C	1.5T2C
Process	a-Si:H TFT	-	LTPS TFT	-	-	a-Si:H TFT	a-Si:H TFT	LTPS TFT
Improving method	Overlapping driving scheme	Overdriving scheme	Pixel circuit	Pixel circuit	Pixel circuit	Pixel circuit	Double rate driving scheme	Pixel circuit
Cost reduction	No (Without reducing number of source driver ICs)	No (Require modified source driver ICs and TCONs)	Yes (Without R-DAC and output buffers in source driver ICs)	No (Double number of source driver ICs)	Yes (Half number of source driver ICs)	Yes (Half number of source and gate driver ICs)	Yes (Half number of source driver ICs)	Yes (Half number of source driver ICs)
Number of gate drivers for each row of pixels	1	1	1	1	1	$\frac{1}{2}$ (1 gate line is shared with 2 rows of pixels)	2 (Double number of gate lines)	1
Type of gate drivers	Integrated gate drivers on glass	-	-	-	Gate driver ICs	Gate driver ICs	Integrated gate drivers on glass	Integrated gate drivers on glass
Simple driving waveform	Yes	Yes	Yes	Yes	No	No	Yes	Yes
Pixel charging ratio	High	High	Low	High	High	Low	High	High
Verification level	Measurement+ Display demonstration	Measurement	Simulation	Display demonstration	None	Calculation	Measurement+ Display demonstration	Measurement+ Display demonstration
Specification	47-inch panel FHD (1920 × 1080) 240 Hz	65-inch panel QUHD (7680 × 4320) 120 Hz	6-inch panel FHD (1920 × 1080) 60 Hz	FHD (1920 × 1080) 120 Hz	-	40-inch FHD (1920 × 1080) 60 Hz	17-inch FHD (1920 × 1080) 60 Hz	12.3-inch UHD (3840 × 2160) 120 Hz
Application	Television (TV)	Television (TV)	Mobile Phone	Television (TV)	-	Television (TV)	Monitor	Narrow-bezel Notebook Computer

Fig. 1(a) shows the conventional pixel circuit for TFT-LCDs that was proposed by Lechner *et al.* [15]. This circuit is extensively used for TFT-LCDs in the display industry because of its simplicity. A pixel is physically comprised of one transistor (T), a liquid crystal capacitor (C_{LC}), and a storage capacitor (C_{ST}); herein, the structure of the conventional pixel circuit is expressed as the conventional 1T2C pixel circuit, but not the standard 1T1C pixel circuit, to compare the total transistors and capacitors in structures among different pixel circuits. To cut the cost of source driver integrated circuits (ICs) [16], [17], [18], the 1-to-2 de-multiplexer (De-MUX) is applied to halve the number of required data pins in source driver ICs, as shown in Fig. 1(b). However, as the resolution and the frame rate of TFT-LCDs increase, the row-line time for updating the data voltages of the pixels in a row shrinks, decreasing the time for charging and discharging pixels. Although the overlapping driving and overdriving methods proposed by Shin *et al.* [19] and Seo *et al.* [20], respectively, are used to reduce pixel voltage distortion and thus provide images of high quality, they do not reduce the number of required data pins of the source driver ICs. The method of [20] imposes the additional cost of modifying the source driver ICs and timing controllers to extend the input data from 8 bits to 10 bits to supply an overdrive voltage. If De-MUXs are adopted to reduce the number of source driver ICs, then the charging ratio for pixels will be reduced. The TFTs of De-MUXs that are connected between the pins of source driver ICs and the data lines significantly increase the loadings on the data lines, causing the programming of the data voltages to each pixel within a short row-line time to fail.

Many studies have developed various methods to reduce the number of source and gate driver ICs, achieve low power consumption, and improve pixel charging to satisfy the requirements of high-resolution displays; these involve enhancing the performance of pixel driving

**FIGURE 1.** (a) Conventional 1T2C pixel circuit [15] and (b) structure of pixel array with 1-to-2 de-multiplexer.

schemes [19], [20], new driving structures [21], [22], [23], [24], [25], and TFT devices [26], [27]. Tai *et al.* proposed a new pixel circuit for TFT-LCDs that was based on a digital pulse width modulation (PWM) method [21]; it has no operational amplifiers (OP AMPs) and resistor-string digital-to-analog converters (R-DACs), reducing the power consumption of the source driver ICs. However, the inserted resistor in the pixel circuit is difficult to be patterned in a sophisticated manner with TFT backplane technologies, and the RC time constant is affected by the non-uniformity of resistance, threshold voltage (V_{TH}) variations, and the dynamic capacitance of liquid crystal, making control of the pixel voltage difficult. You *et al.* proposed a pixel circuit to increase the charging ratio for TFT-LCDs [22]. The driving structure enables one column of subpixels to be charged by two data lines and thereby increases the charging ratio. However, since twice as many data lines as in the conventional pixel circuit are used, the required number of source driver ICs is doubled, increasing the manufacturing cost. In this driving structure, one subpixel is split into two small subpixels, so luminance differs between the two small subpixels.

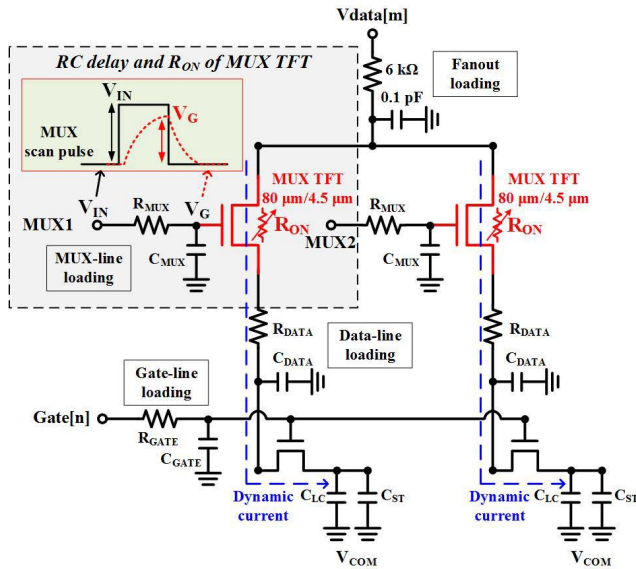


FIGURE 2. Schematic of RC loadings for conventional 1T2C pixel circuit with de-multiplexer.

In addition, the demand for the number of source driver ICs considerably increases as the resolution of displays increases. To keep the required source driver ICs in a limited area of the top bezel and cut down the cost, several pixel circuits with data line sharing methods have been proposed to reduce the required number of source driver ICs [23], [24], [25]. The pixel circuits presented by Sung *et al.* [23] and Choi and Kwon [24] both use complicated row-line signals to drive their pixels, and these signals are not generated by the gate driver circuit on arrays (GOAs) [28], [29], [30], increasing the cost of using gate driver ICs. Although the pixel circuits in [24] share a data line and a gate line to four subpixels, these circuits connect the global control signals to each pixel throughout the panel. The RC loadings on global lines increase significantly, causing the pixel circuits to suffer from a serious delay. For a full high-definition (FHD, 1920 × 1080) LCD panel, since the control signals are switched at the row frequency of 32.4 kHz rather than at a frame rate of 60 Hz, the power consumption of the gate driver ICs is increased. Kim and Kwon [25] proposed a pixel circuit that shares the data lines between adjacent subpixels by the double rate driving method and alters the charging sequence of subpixels. Nevertheless, rearranging subpixels in the driving structure increases the complexity of the timing controller that is used to provide the rearranged data sequence. Also, the numbers of gate lines and gate driver circuits for pixels in one row are doubled. The added gate driver circuits increase the occupied layout area, enlarging the bezel of the display. Oke and Nakagawa [31] proposed an adaptive pre-charge driving scheme to improve pixel charging ratios and mitigate the image-sticking phenomenon. In that study, adaptive pre-charge driving (APD) tables composed of 5 × 9 look-up tables were used to optimize images with a combination of all gray levels. Lee *et al.* [32] proposed a new

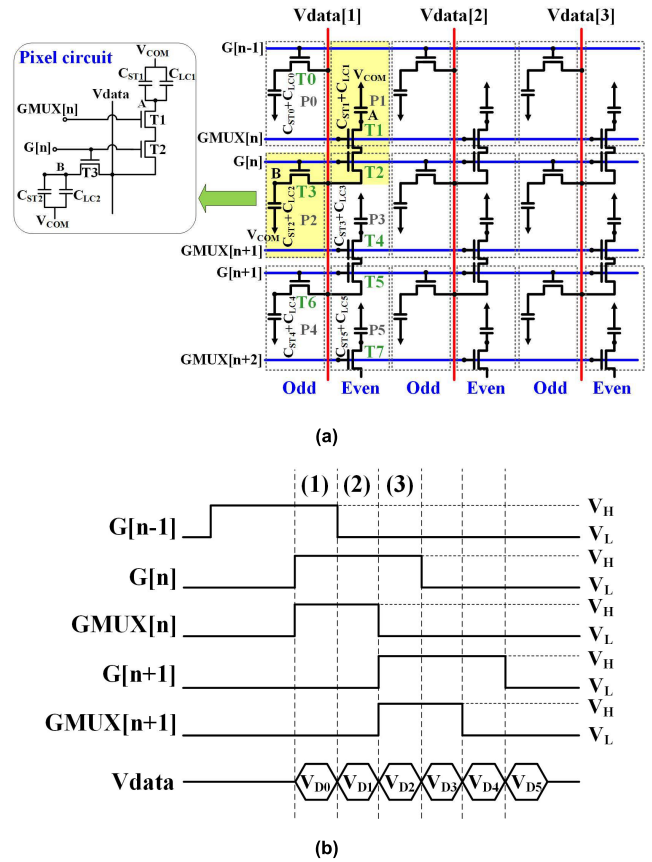


FIGURE 3. (a) Schematic of proposed driving structure of pixel array and (b) timing diagram of control signals.

line artifact-compensating pre-charging (LCP) method that is implemented using look-up tables. It enables the pixel voltage to reach the target voltage as the overdriven charging voltage eliminates the dark line artifact. However, this work focuses on the circuit design and not on the complex algorithm that uses several look-up tables with the pre-charging method.

This work proposes a new pixel circuit that consists of n-type LTPS TFTs for use in UHD TFT-LCDs with a frame rate of 120 Hz. Removing the TFTs from the De-MUXs greatly reduces the RC loadings of the MUX TFTs on the data lines, improving the pixel charging ratio. A novel gate driver circuit that generates two output waveforms in a single stage is proposed. To provide a fair comparison, Table 1 compares the pixel circuit and driving method in this work with those in previous works [19], [20], [21], [22], [23], [24], and [25], concerned only with the structure, process, driving waveforms, gate drivers, cost reduction, specification, applications, and method of improving the pixel charging ratio. In this work, the number of required source driver ICs must be carefully considered and reduced because the bonding design of the source driver ICs on the panel is made difficult by the limited area in the top bezel of the panels for use in high-resolution notebooks. The proposed driving structure with a simple driving waveform yields a larger pixel charging ratio than in other works, halves the cost of source driver ICs, and eliminates

TABLE 2. Design parameters of proposed and conventional pixel circuit.

Proposed pixel circuit			
Parameter	Value	Parameter	Value
$(W/L)_{T1-T3}$ (μm)	2.5/3.5	Vdata (V)	$0 \sim \pm 4.5$
$C_{ST1, ST2}$ (pF)	0.155	V_{COM} (V)	0
$C_{LC1, LC2}$ (pF)	0.023	G[n], GMUX[n] (V)	$10 \sim -6$
Conventional pixel circuit			
Parameter	Value	Parameter	Value
W/L of switch TFTs (μm)	2.5/3.5	Vdata (V)	$0 \sim \pm 4.5$
W/L of Mux TFTs (μm)	80/4.5	V_{COM} (V)	0
C_{ST} (pF)	0.155	Gate[n] (V)	$10 \sim -6$
C_{LC} (pF)	0.023		

gate driver ICs by fully integrating gate drivers on glass, enabling the realization of compact and cost-effective high-resolution displays. A 12.3-inch panel with UHD (3840×2160) and a frame rate of 120 Hz is fabricated and lit up. Experimental results reveal that the color image displayed on the fabricated panel with high image quality, and uniform red, green, and blue monochrome images were provided, confirming the feasibility of the proposed driving structure.

II. ISSUES OF RC LOADINGS ON DATA LINE WITH DE-MUX STRUCTURE

Fig. 2 shows the RC loadings of the conventional driving structure with 1-to-2 De-MUXs, including the RC loadings of MUX bus lines, data lines, and gate lines. The pixel charging ratio is associated with the dynamic current to charge the capacitor of the liquid crystal (C_{LC}) and the storage capacitor (C_{ST}) in the pixel. When an ideal scan pulse is applied to the input of the MUX bus line, the voltage across the capacitor at the gate node of the MUX TFT (V_G) is expressed as

$$V_G(t) = V_{IN} \times (1 - e^{-\frac{t}{R_{MUX} \cdot C_{MUX}}}) \quad (1)$$

where V_{IN} is the input voltage of the MUX scan pulse, R_{MUX} is the resistance of the MUX bus line, C_{MUX} is the capacitance of the MUX bus line, and t is the time for charging.

As the resolution of displays increases, the RC loadings of the MUX bus lines increase, resulting in severely delaying the MUX scan pulse. The available row-line time for charging shrinks because the resolution and the frame rate that is used in the displays are increased. Consequently, the gate node of each MUX TFT fails to be charged to the peak V_{IN} within the limited row-line time of UHD displays, increasing the on-resistance (R_{ON}) of the MUX TFTs. The increase in R_{ON} reduces the dynamic current to charge the C_{LC} and C_{ST} , so the pixel charging ratio of the driving structure with 1-to-2 De-MUXs decreases. The overlapping driving scheme is proposed to improve the pixel charging ratio by extending the charging time for each row of pixels. However, the pixel charging ratio is still insufficient because the dynamic current is limited by the R_{ON} of the MUX TFTs that are connected between the source driver ICs and the data lines. The voltage on the data line will be lower than the input data voltage from

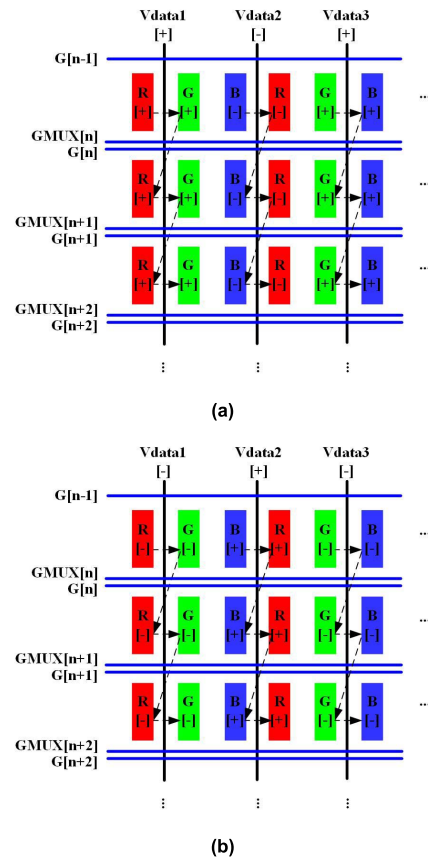


FIGURE 4. Polarity inversion of proposed driving structure when odd columns of data lines are at (a) positive polarity and (b) negative polarity.

the source driver IC, making the charging voltage for pixels incorrect.

Therefore, the proposed new driving structure moves the external TFTs of De-MUXs into pixels to reduce the R_{ON} of MUX TFTs on the data lines, significantly improving the charging ratio of the pixel voltage. The new pixel circuit will be introduced in the following sections.

III. PIXEL CIRCUIT SCHEMATIC AND OPERATION

A. PIXEL CIRCUIT TO ENHANCE PIXEL CHARGING RATIO

Figs. 3(a) and 3(b) show the proposed pixel circuit and its corresponding timing diagram, respectively. The proposed pixel circuit structure of each pair of subpixels comprises three TFTs ($T1$, $T2$, and $T3$), two storage capacitors (C_{ST1} and C_{ST2}), and two capacitors of the liquid crystal (C_{LC1} and C_{LC2}). Vdata is the input data voltage, determining the gray level of each pixel. In the proposed structure, one data line is shared between the two adjacent subpixels to reduce the number of required pins of the source driver ICs. The voltages of nodes A (V_A) and B (V_B) determine the gray level of the subpixels in the even and odd columns, respectively. The operation of the proposed pixel circuit proceeds involving the following steps. In the first period, $G[n]$ and $GMUX[n]$ are set to V_H to turn on $T1$, $T2$, and $T3$. V_A and V_B are pre-charged by the data voltage of the preceding row (V_{D0}).

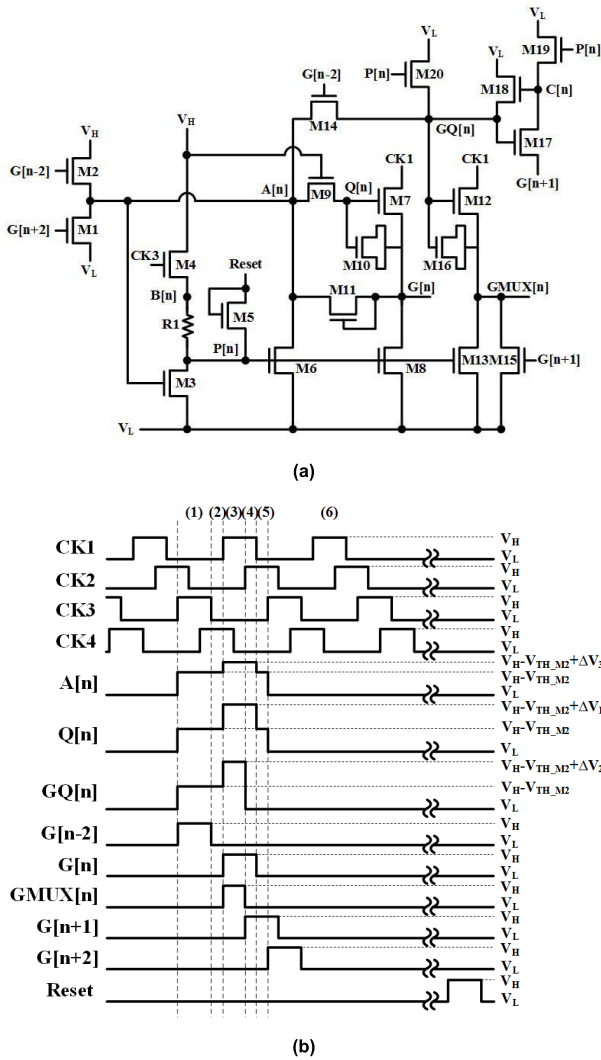


FIGURE 5. (a) Schematic of proposed gate driver circuit and (b) timing diagram.

The voltage difference between V_A and the target voltage for node A (V_{D1}) is shrunk due to the pre-charging. In the second period, $G[n]$ and $GMUX[n]$ remain at V_H , so $T1$, $T2$, and $T3$ are turned on. On account of the pre-charging in the first period, V_A and V_B can be rapidly increased from V_{D0} to V_{D1} , providing a precise pixel voltage of node A. In the third period, $GMUX[n]$ changes from V_H to V_L to turn off $T1$, and $G[n]$ remains at V_H , turning on $T2$ and $T3$. $G[n+1]$ and $GMUX[n+1]$ become V_H , turning on $T4$, $T5$, and $T6$ in the $[n+1]$ th row. Thus, V_A is maintained at V_{D1} by C_{LC1} and C_{ST1} , providing the desired gray level. Moreover, the data voltage for node B (V_{D2}) is applied to node B through $T3$, and the subpixels in the $[n+1]$ th row are pre-charged by V_{D2} to accelerate pixel charging. Operated as described above, the proposed pixel circuit improves the pixel charging ratio by extending the available charging time for the liquid crystal and shrinking the required voltage range of pixel charging, favoring the charging and discharging of pixels in UHD and high-frame-rate displays.

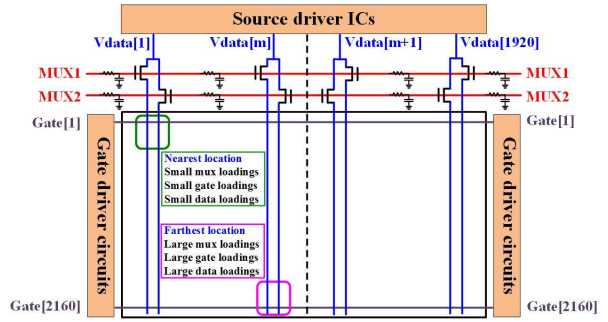


FIGURE 6. Configuration of TFT-LCD panel using conventional 1T2C pixel circuit with 1-to-2 de-multiplexer.

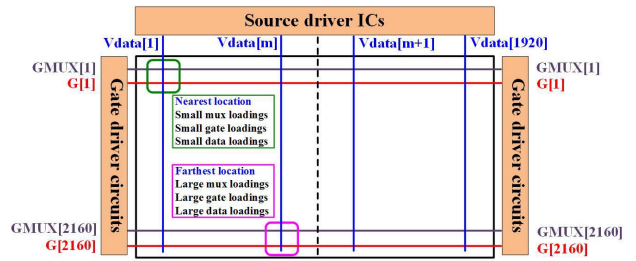


FIGURE 7. Configuration of TFT-LCD panel using proposed driving structure.

B. DRIVING SCHEME OF PROPOSED PIXEL ARRAY

Fig. 3(a) shows the proposed driving structure of a pixel array. To program correctly the pixel voltages of each subpixel, the proposed driving structure is operated as follows. At first, the odd column subpixels are charged, so the subpixel ($P0$) with capacitance $C_{ST0} + C_{LC0}$ is charged to the data voltage of V_{D0} . In the second period, the even-side subpixel ($P1$) with capacitance $C_{ST1} + C_{LC1}$ is charged to V_{D1} , and the odd-side subpixel ($P2$) with capacitance $C_{ST2} + C_{LC2}$ is pre-charged by V_{D1} . In the third period, the subpixel ($P2$) with capacitance $C_{ST2} + C_{LC2}$ is charged to V_{D2} , and the subpixel ($P3$) with capacitance $C_{ST3} + C_{LC3}$ and the subpixel ($P4$) with capacitance $C_{ST4} + C_{LC4}$ is pre-charged by V_{D2} . Subsequently, the even-side subpixel ($P3$) with capacitance $C_{ST3} + C_{LC3}$ is charged to V_{D3} . According to the aforementioned operation, the proposed driving structure firstly operates the odd column subpixels and then operates the even column subpixels, thereby making no need for the additional memory blocks at a source driver circuit for proper operation.

The proposed driving structure uses the column inversion driving method where the polarity of the data voltage is reversed by each frame to prevent deterioration in image quality as a result of the polarization of LC. Figs. 4(a) and 4(b) show the polarity inversion of the proposed pixel array when odd columns of data lines exhibit positive and negative polarities, respectively. In the proposed driving structure, one data line is shared between the two adjacent subpixels, enabling two columns of subpixels that are connected to the same data line to have the same polarity within one frame time. The pixel voltages of each subpixel in the proposed structure are updated in a zigzag manner. Notably, the polarity of the

TABLE 3. RC loadings of proposed and conventional pixel arrays for use in 12.3-inch 4K2K display panel.

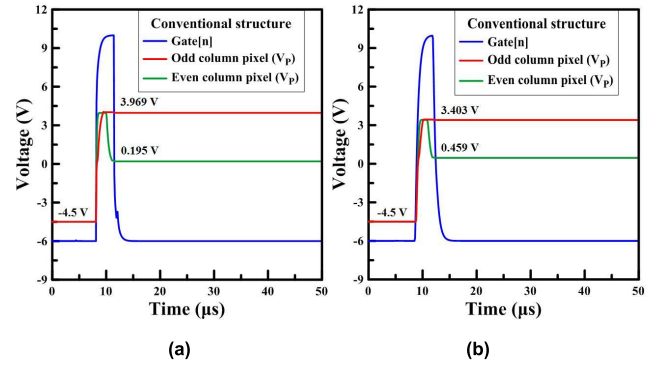
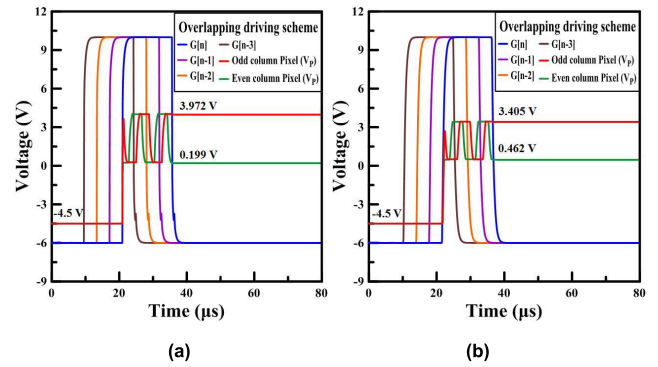
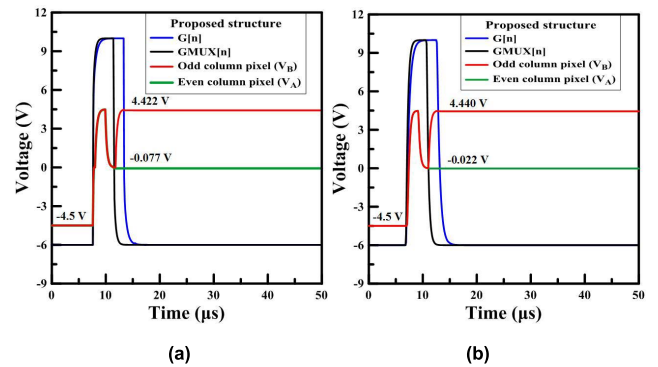
Proposed				Conventional 1T2C pixel circuit with De-MUXs			
G[n]	Rgate	33.25	k Ω	Gate[n]	Rgate	33.25	k Ω
	Cgate	120.6	pF		Cgate	120.6	pF
Vdata	Rdata	5.062	k Ω	Vdata	Rdata	5.062	k Ω
	Cdata	38.2	pF		Cdata	38.2	pF
GMUX[n]	Rmux	33.466	k Ω	MUX1, 2	Rmux	4.18	k Ω
	Cmux	75.537	pF		Cmux	760	pF

data voltage reverses by each frame to reduce the frequency of the polarity change on the data line, reducing the power consumption of the source driver ICs. Although the column flicker may be easily caused by the column inversion method, the flicker can be alleviated by the appropriate design of the panel. A storage capacitor of sufficient size, which is much larger than the parasitic capacitance between the data signal lines and subpixels, is used to help stabilize each pixel voltage that is stored on the storage capacitor and the liquid crystal. Also, by lowering the driving voltage swings of the driver ICs, the pixel voltage difference between the various columns of subpixels as caused by the coupling effect can be reduced, alleviating the flicker. Moreover, the proposed driving structure has none of the external TFTs of the De-MUXs, greatly reducing the RC loadings of the MUX TFTs and data lines, improving the pixel charging ratio in TFT-LCD panels. Therefore, the proposed driving structure can realize high-speed programming and so is suitable for use in UHD displays at a high frame rate.

IV. GATE DRIVER CIRCUIT AND OPERATION

Figs. 5(a) and 5(b) present the proposed gate driver circuit on a glass substrate and its timing diagram, respectively. This circuit generates both GMUX[n] and G[n] signals in a single stage to drive each row of pixels. The proposed gate driver circuit consists of a G[n] generation circuit (M1-M11) and a GMUX[n] generation circuit (M12-M20). M10 and M16 are the capacitors that are formed by the transistor. CK1-CK4 are the clock signals that are used to drive the proposed gate driver circuit. V_H and V_L are the high and low direct current (DC) voltages, respectively. $G[n-2]$ is the output of the $[n-2]$ th stage and applied as a start pulse to activate the $[n]$ th stage. The circuit operation can be divided into the following six steps.

In the first step, $G[n-2]$ is at V_H , turning on M2 and M14 to charge nodes Q[n] and GQ[n] to $V_H - V_{TH_M2}$. Therefore, M7 and M12 are turned on to stabilize nodes G[n] and GMUX[n] at V_L of CK1. Also, M3 is turned on to discharge node P[n] to V_L , turning off M6, M8, and M13. Herein, resistor R1 is used to reduce the large current that flows from V_H to V_L and guarantees that node P[n] can be discharged to a low voltage level to turn off M6, M8, and M13. By introducing resistor R1 in series with M3 and M4, the size of M3 can

**FIGURE 8. Pixel voltages at locations (a) nearest to and (b) farthest from source and gate drivers when Vdata is changed from 0 V to 4.5 V using conventional pixel circuit with 1-to-2 de-multiplexer.****FIGURE 9. Pixel voltages at locations (a) nearest to and (b) farthest from source and gate drivers when Vdata is changed from 0 V to 4.5 V using conventional pixel circuit with 1-to-2 de-multiplexer and overlapping driving scheme.****FIGURE 10. Pixel voltages at locations (a) nearest to and (b) farthest from source and gate drivers when Vdata is changed from 0 V to 4.5 V using proposed pixel circuit.**

be reduced without using an excessively large transistor to discharge node P[n], thereby lowering the large current that flows from V_H to V_L through M3 and M4.

In the second step, $G[n-2]$ and CK3 change from V_H to V_L , so M2, M4, and M14 are turned off. Nodes A[n], Q[n], GQ[n], and P[n] remain as set in the first step, and nodes G[n] and GMUX[n] remain at V_L .

In the third step, when CK1 goes from V_L to V_H , nodes Q[n] and GQ[n] are bootstrapped to $V_H - V_{TH_M2} + \Delta V_1$ and

TABLE 4. Improvements of pixel charging with different sizes of MUX TFT in conventional driving structure.

Pixel voltage at location nearest to source and gate drivers		
W/L (μm)	Pixel voltage of odd column (V)	Pixel voltage of even column (V)
80/4.5	3.969	0.195
160/4.5	4.120	0.101
240/4.5	4.165	0.054
320/4.5	4.184	0.020
400/4.5	4.188	-0.011
Pixel voltage at location farthest from source and gate drivers		
W/L (μm)	Pixel voltage of odd column (V)	Pixel voltage of even column (V)
80/4.5	3.403	0.459
160/4.5	3.672	0.321
240/4.5	3.782	0.257
320/4.5	3.845	0.213
400/4.5	3.882	0.184

$V_H - V_{TH_M2} + \Delta V_2$, respectively, by the capacitive coupling effect of the capacitors that are formed by M10 and M16, to increase the driving capability of M7 and M12. Hence, nodes G[n] and GMUX[n] are charged to V_H by M7 and M12, respectively. Notably, A[n] is charged by the leakage current through M9 to $V_H - V_{TH_M2} + \Delta V_3$, and M11 is used to maintain the high voltage level of node A[n].

In the fourth step, when G[n + 1] changes from V_L to V_H , node C[n] starts increasing to V_C , which is high enough to turn on M18. After M18 is turned on, node GQ[n] is discharged to V_L , turning off M12 and M17. Meanwhile, node GMUX[n] is quickly discharged to V_L through M15. Therefore, the GMUX[n] waveform can be generated.

In the fifth step, CK1 returns to V_L , so node G[n] is discharged to V_L through M7. Node Q[n] is coupled to $V_H - V_{TH_M2}$ by the capacitive coupling effect of the capacitor that is formed by M10. Since M9 is turned on, node A[n] is discharged to $V_H - V_{TH_M2}$ by the charge sharing between nodes A[n] and Q[n].

In the sixth step, G[n + 2] and CK3 become V_H to turn on M1 and M4. Therefore, nodes A[n] and Q[n] are reset to V_L through M1, turning off M3. Then, nodes B[n] and P[n] are charged to $V_H - V_{TH_M4}$ through M4 and activate M6, M8, and M13 to discharge nodes A[n], G[n], and GMUX[n] to V_L . After the operating period, CK3 periodically changes from V_L to V_H to stabilize node P[n] at $V_H - V_{TH_M4}$ to suppress the unexpected fluctuations in the row lines, increasing the stability of the output waveforms of G[n] and GMUX[n]. After the aforementioned main operations, the reset signal changes to V_H at the end of each frame time to turn on M5, discharging nodes G[n] and GMUX[n] of all stages in the gate driver circuits to V_L . According to the above steps, the proposed gate driver circuit generates two different output waveforms by a unit stage to reduce the layout area that is occupied by another required gate driver circuit. Therefore, UHD and narrow-bezel displays can be achieved.

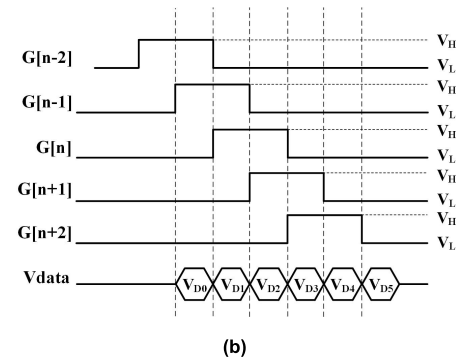
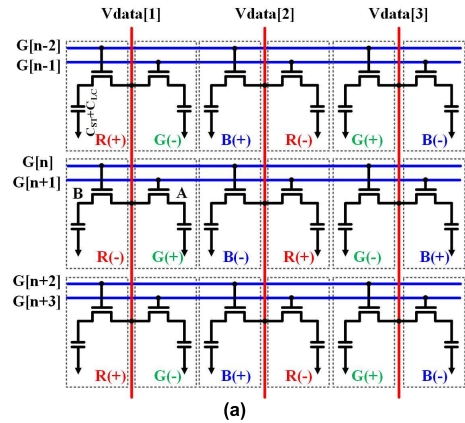


FIGURE 11. (a) Schematic of previously developed driving structure using overlapping gate pulses without 1-to-2 De-MUXs and (b) timing diagram of driving signals.

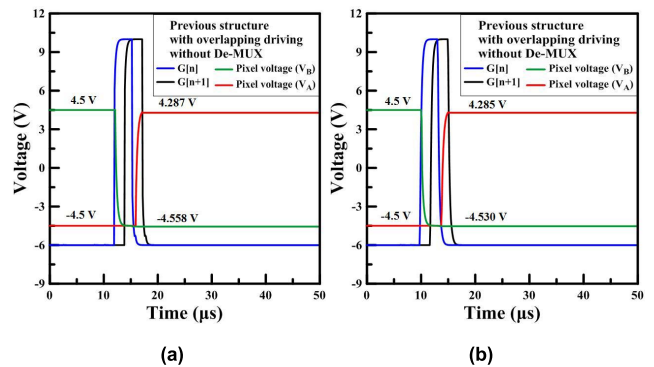


FIGURE 12. Pixel voltages at locations (a) nearest to and (b) farthest from source and gate drivers when Vdata is changed from -4.5 V to 4.5 V using previously developed driving structure with overlapping driving scheme without De-MUX.

V. RESULTS AND DISCUSSION

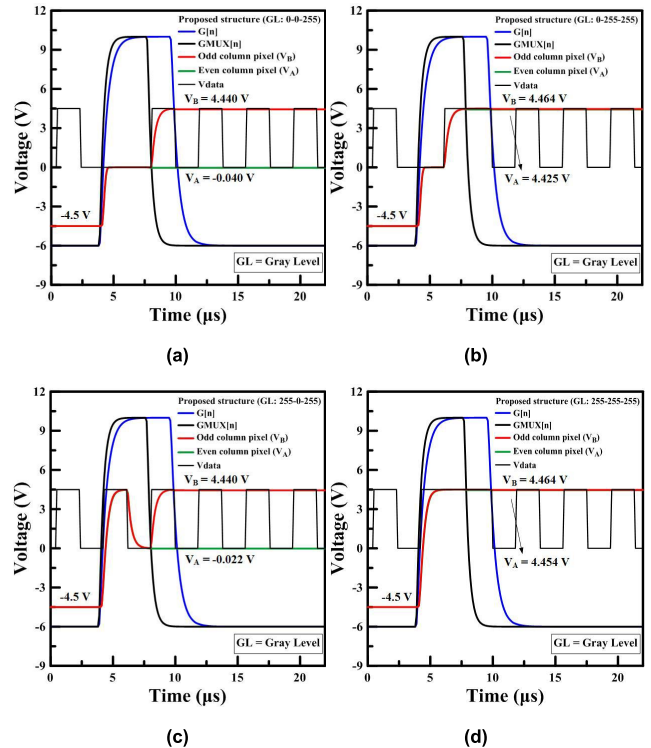
To verify the effectiveness of the proposed driving structure in enhancing the charging ratio of pixels for use in UHD TFT-LCDs, the proposed pixel circuit based on a fabricated 12.3-inch 4K2K display panel is simulated using an HSPICE simulator. Table 2 lists the design parameters of the proposed and conventional pixel circuits. Fig. 6 shows the system diagram of the conventional TFT-LCD panel, which consists of source driver ICs, integrated gate driver circuits, 1-to-2 De-MUXs, and the active area of the panel. Double-side row driving is adopted in UHD displays to reduce scan pulse

TABLE 5. Design parameters of proposed gate driver circuit.

Design parameter	Value
CK1~CK4, Reset	-6 V ~ 10 V
V_H	10 V
V_L	-6 V
(W/L) _{M1, M2, M3, M5, M9, M11, M14, M19}	5.5 μm / 5.5 μm
(W/L) _{M4, M6, M17, M18, M20}	5.5 μm / 5.5+5.5 μm
(W/L) _{M7, M12}	165 μm / 4.5+4.5 μm
(W/L) _{M8, M15}	82.5 μm / 5.5 μm
(W/L) _{M13}	27.5 μm / 5.5 μm
(W/L) _{M10, M16}	13.5 μm / 27 μm
R1	800 k Ω

delay. Herein, the equivalent RC loadings for each pixel depend on the distance from pixel circuit to source driver ICs and gate driver circuits. Therefore, the locations with the smallest RC loadings are nearest the source and gate drivers, in the top-left and top-right corners of the panel, whereas the location with the largest RC loadings is in the bottom-middle of the panel, farthest from both the source and gate drivers. Fig. 7 shows the configuration of TFT-LCD panel using the proposed driving structure. To improve pixel charging, the external TFTs of 1-to-2 De-MUXs are integrated into the pixel circuit for decreasing the RC loadings of the data lines, and thereby accelerate the charging and discharging of the data lines. Table 3 presents the RC loadings of the gate lines, data lines excluding external TFTs, and MUX bus lines in the conventional and proposed driving structures.

To provide a fair comparison, the size of the TFTs and the voltage swings of the driving signals in the conventional and proposed structures are set to be equal. The data voltages range from 0 V to 4.5 V and from 0 V to -4.5 V for positive and negative polarity, respectively. To simulate the circuit with the worst-case pixel charging ratio under a heavy loading pattern, the input data voltage is set to swing between 0 V to 4.5 V. 4.5 V and 0 V are the highest positive voltage and the lowest voltage, respectively, when a voltage of positive polarity is applied. Fig. 8(a) plots the voltage of node P (V_P), which is the pixel voltage of the conventional pixel circuit, at the location nearest to the source and gate drivers. V_P for the subpixel in the odd column is increased from -4.5 V to only 3.969 V within one row line time. Fig. 8(b) shows V_P at the location farthest from the source and gate drivers using the conventional pixel circuit. Ultimately, V_P for the subpixel in the odd column is increased from 0 V to 3.403 V, revealing an insufficient pixel charging ratio of 75.62%, which seriously distorts the pixel voltage. Fig. 9 shows the simulated pixel voltages of the conventional pixel circuit with an overlapping driving scheme under a heavy loading pattern. The subpixel in Fig. 9(a) at the location nearest to the source and gate drivers is charged from -4.5 V to 3.972 V, and that in Fig. 9(b) at the location farthest from the source and gate drivers is charged from -4.5 V to only 3.405 V. Although the pre-charging method uses 3/4 overlapping scan pulses in the conventional driving structure to increase the pixel charging ratio, the pixel

**FIGURE 13.** Pixel voltages farthest from source and gate drivers when pre-charging data sequence of (a) (0-0-255), (b) (0-255-255), (c) (255-0-255), and (d) (255-255-255) is used.

charging ratios under a heavy loading pattern are only 88.27% and 75.67% at the locations nearest to and farthest from the source and gate drivers, respectively. Since the RC loadings of MUX TFTs reduce the current for charging, the pixel charging ratios are too low to satisfy the relevant requirement of high specification displays, causing serious pixel voltage distortion. Fig. 10(a) plots the voltages of nodes A and B (V_A and V_B), representing the pixel voltages of the proposed pixel circuit, at the location nearest to the source and gate drivers. Reducing the huge RC loadings of the TFTs of the De-MUX enables V_B for the subpixel in the odd column at the location nearest to the source and gate drivers to be increased to 4.422 V when a V_{data} of 4.5 V is provided. Fig. 10(b) shows that V_B farthest from the source and gate drivers using the proposed pixel circuit can be increased from 0 V to 4.440 V, significantly improving the pixel charging ratio to 98.67% as opposed to 75.67% for the conventional pixel circuit.

Although enlarging MUX TFTs reduces their on-resistance (R_{on}), doing so cannot efficiently enhance the pixel charging ratio since the huge RC loadings of MUX bus lines still seriously reduce the time available to charge the data lines. Table 4 presents the pixel voltages of odd and even columns as the size of the MUX TFT increases. As the size of MUX TFTs is increased from 80/4.5 ($\mu\text{m}/\mu\text{m}$) to 400/4.5 ($\mu\text{m}/\mu\text{m}$), the pixel voltage at the location nearest to the source and gate drivers is merely increased from 3.969 V to 4.188 V, corresponding to a pixel charging ratio of 93.07%. At the location

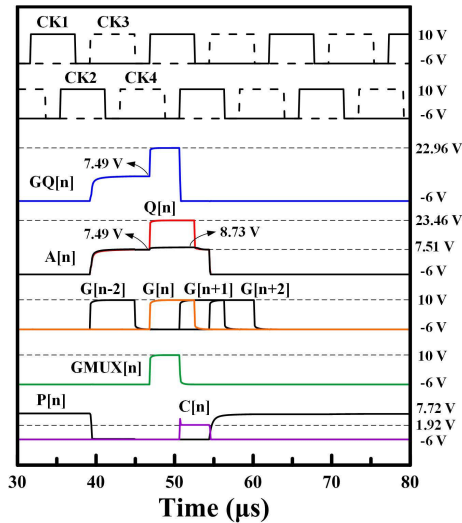


FIGURE 14. Simulated waveforms at internal nodes in proposed gate driver circuit.

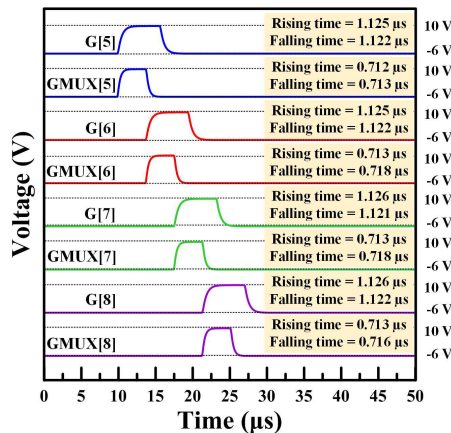


FIGURE 15. Simulated output waveforms of proposed gate driver circuit in four stages.

farthest from the source and gate drivers, as the size of MUX TFTs is increased to 400/4.5 ($\mu\text{m}/\mu\text{m}$), the pixel voltage is increased only to 3.882 V, revealing the insufficient pixel charging ratio of 86.27%.

Figs. 11(a) and 11(b) show the schematic of the previously developed driving structure using the overlapping gate pulses without multiplexing and its timing diagram, respectively. The number of gate lines in the previously developed driving structure with overlapping gate pulses equals that in the proposed driving structure. The previously developed driving structure reverses the polarity of data voltages by the dot inversion method. In contrast, the proposed driving structure applies the column inversion driving method, in which the polarity of the data voltage is reversed by each frame. Thus, the polarities at two adjacent subpixels are the same in the proposed driving structure, accelerating the charging and discharging of pixels by lowering the range of voltages in data lines needing to be charged and discharged. Herein, the TFTs, storage capacitors, and the equivalent capacitor of

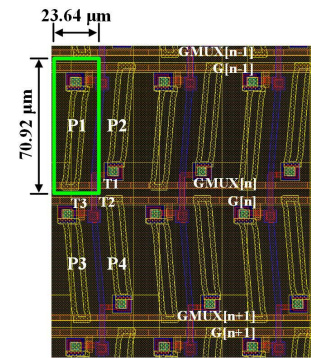


FIGURE 16. Layout of subpixels of proposed driving structure.

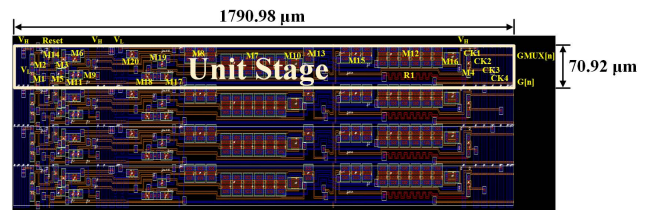


FIGURE 17. Layout of proposed gate driver circuit.

the liquid crystal of the proposed and previously developed driving structures have the same dimensions. The subpixel of the previously developed driving structure with overlapping gate pulses in Fig. 12(a) at the location nearest to the source and gate drivers is charged to 4.287 V when a Vdata of 4.5 V is applied, and that in Fig. 12(b) at the location farthest from the source and gate drivers is charged to 4.285 V. The simulation results verify that the proposed driving structure yields a higher pixel voltage for each subpixel than the previously developed structure with overlapping gate pulses, improving the pixel charging ratio to 98.27% (4.422 V/4.5 V) from 95.22% (4.285 V/4.5 V).

To investigate the charging performance of the proposed driving structure, different sequences of pre-charge data with (0-0-255), (0-255-255), (255-0-255), and (255-255-255) are simulated when the gray levels of 0 and 255 correspond to 0 V and + 4.5 V, respectively. Fig. 13 plots the simulated pixel voltages with different sequences of pre-charge data. The pixel voltages of node B farthest from the gate driver and source driver ICs of the panel are 4.440 V, 4.464 V, 4.440 V, and 4.464 V with pre-charging data sequences of (0-0-255), (0-255-255), (255-0-255), and (255-255-255), respectively. The pre-charge sequence only slightly affects the pixel voltages because the RC loadings of the data lines are greatly decreased by removing the MUX TFTs from the De-MUXs and integrating them into the pixel circuit.

To reduce the bezel of the panel and increase the mechanical reliability of the peripheral circuit, the use of an integrated gate driver circuit on glass is proposed. Table 5 presents the design parameters of the proposed gate driver circuit, including the driving signals, the aspect ratios of the TFTs, and resistance. Fig. 14 plots the simulated waveforms at

each node in the proposed gate driver circuit. When node $G[n-2]$ changes from -6 V to 10 V, the voltages of nodes $Q[n]$ and $GQ[n]$ increase to 7.49 V. Next, $CK1$ changes from -6 V to 10 V, and nodes $Q[n]$ and $GQ[n]$ are bootstrapped to 23.46 V and 22.96 V, respectively by the capacitive coupling effect of the capacitors that are formed by $M10$ and $M16$. Before node $G[n]$ is discharged, node $G[n+1]$ changes from -6 V to 10 V so that node $C[n]$ is charged from -6 V to 1.92 V through $M17$, turning on $M18$ to discharge node $GQ[n]$ to -6 V. Thus, the voltage of $GMUX[n]$ is pulled down by the coupling capacitor of $M16$ as the voltage of $GQ[n]$ is decreased from 22.96 V to -6 V. Meanwhile, $M15$ is turned on by node $G[n+1]$ and rapidly discharges node $GMUX[n]$ to -6 V. Afterward, node $P[n]$ is charged to 7.72 V through $M4$ to activate $M6$, $M8$, $M13$, $M19$, and $M20$ to stabilize nodes $A[n]$, $Q[n]$, $G[n]$, $GMUX[n]$, $C[n]$, and $GQ[n]$ at -6 V. Therefore, highly stable output waveforms of $G[n]$ and $GMUX[n]$ are generated. Fig. 15 plots the simulated output waveforms of the proposed gate driver circuit in four stages. The output waveforms are generated and sequentially transmitted. Also, the rising times of $G[n]$ and $GMUX[n]$ are about $1.13 \mu\text{s}$ and $0.71 \mu\text{s}$, respectively, and the falling times of $G[n]$ and $GMUX[n]$ are about $1.12 \mu\text{s}$ and $0.72 \mu\text{s}$, respectively.

Fig. 16 shows the subpixels of the proposed pixel circuit; the layout area of a single subpixel is $23.64 \mu\text{m} \times 70.92 \mu\text{m}$ based on the fabricated 12.3-inch 4K2K display panel. The layouts of the odd and even pixels are not the same because an odd pixel has one TFT and an even pixel has two TFTs. However, a switching TFT occupies a small layout area in pixels $[(2.5 \mu\text{m} \times 3.5 \mu\text{m}) / (23.64 \mu\text{m} \times 70.92 \mu\text{m}) \approx 0.5\%]$ under the LTPS TFT backplane. The layout slightly lowers the aperture ratio of the odd pixel to equalize it with that of the even pixel; it is evaluated before the tape-out. As the aperture ratio of the odd pixel is reduced, its luminance is decreased, enabling the luminance of an odd pixel with one TFT almost to equal that of the even pixel with two TFTs. Fig. 17 shows the layout area of the proposed gate driver circuit in four stages. The area of a single fabricated stage is $1790.98 \mu\text{m} \times 70.92 \mu\text{m}$. Fig. 18 shows the environment for measuring the luminance of images from the fabricated TFT-LCD panel using the proposed driving structure. The input image information is delivered to the system control board by a computer to generate the driving signals for the fabricated panel. The DC power supply is connected to the system control board to provide stable DC electric power. Then, the system control board delivers the driving waveforms and the determined gray levels to the fabricated panel to display the desired images. Finally, the luminance of various images from the fabricated panel is measured by a display color analyzer (CA-310, Konica Minolta). Fig. 19 shows the actual color image that is displayed by the fabricated 12.3-inch and 4K2K (3840×2160) panel with a frame rate of 120 Hz, indicating that the panel that uses the proposed driving structure can display an image with high quality. Table 6 shows photographs of red, green, and blue monochrome images that are displayed by the fabricated panel. The experimental results reveal that the

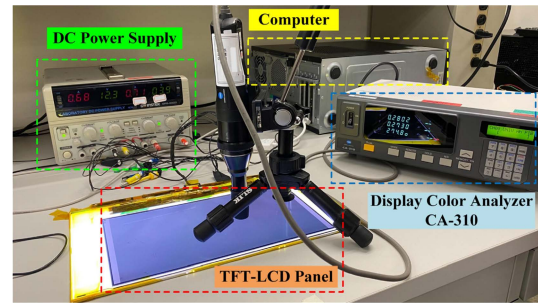





FIGURE 18. Platform system for measuring of fabricated TFT-LCD panel with proposed driving structure.



FIGURE 19. Photograph of image displayed with fabricated 12.3-inch panel.

TABLE 6. Photographs of red, green, and blue images displayed by fabricated panel.

Resolution = 3840×2160 , Frame rate = 120 Hz		
255 Gray level		
Red	Green	Blue
		

fabricated panel can display high-quality images without a serious line, spot, or region defect. For a red, green, blue, and white pattern with both odd and even column subpixels lit up at a gray level of 255, the luminance reaches 49.45 cd/m^2 , 176.8 cd/m^2 , 22.56 cd/m^2 , and 275 cd/m^2 , respectively, so the maximum luminance of white pattern exceeds 250 cd/m^2 . The transmittance of the LC cells can be increased by optimizing the LC cell gaps, improving the maximum luminance of the fabricated panel.

Table 7 presents the measured luminance of the displayed images using the column inversion method when subpixels in only odd or even columns are lit. The luminance values are measured at the bottom end of the fabricated panel where the pixels suffer from the largest RC loadings of the data lines. The maximum luminance deviations between the odd and even column subpixels of the red, green, and blue images at a gray level of 255 are 0.93 cd/m^2 , 3.46 cd/m^2 , and 0.30 cd/m^2 , respectively, where the maximum relative luminance deviations are only 3.61%, 3.95%, and 2.59%, respectively.

TABLE 7. Measured luminance of subpixels in odd and even columns of red, green, and blue images.

Measured luminance of odd subpixels of three different points			
Gray Level	Red images (cd/m ²)		
	1 st point	2 nd point	3 rd point
16	0.32	0.33	0.32
128	5.60	5.08	6.27
255	24.82	24.63	25.55
Gray Level	Green images (cd/m ²)		
	1 st point	2 nd point	3 rd point
16	0.49	0.48	0.51
128	18.55	16.47	20.63
255	91.12	90.82	94.36
Gray Level	Blue images (cd/m ²)		
	1 st point	2 nd point	3 rd point
16	0.30	0.31	0.29
128	2.68	2.50	3.03
255	11.27	11.31	11.80
Measured luminance of even subpixels of three different points			
Gray Level	Red images (cd/m ²)		
	1 st point	2 nd point	3 rd point
16	0.32	0.33	0.32
128	5.36	4.77	5.88
255	25.75	25.45	26.29
Gray Level	Green images (cd/m ²)		
	1 st point	2 nd point	3 rd point
16	0.50	0.51	0.53
128	19.46	17.76	22.11
255	87.66	88.40	91.68
Gray Level	Blue images (cd/m ²)		
	1 st point	2 nd point	3 rd point
16	0.30	0.30	0.29
128	2.54	2.35	2.82
255	11.57	11.57	12.07

The values of luminance of the subpixels in the odd and even columns differ only slightly, demonstrating the absence of any significant relative luminance deviation between odd and even subpixels as caused by column flicker. Thus, the proposed driving structure with the column inversion driving method and an appropriate storage capacitor and driving voltage swings can minimize the flicker and provide high image quality with high luminance uniformity among the columns. Even though each subpixel has a different number of TFTs in the proposed circuit, the asymmetry between the odd and even subpixels causes no serious luminance deviation.

Fig. 20 plots the measured luminance and pixel charging ratios at the bottom end of the fabricated panel for a gray level of 255. Herein, the difference between the highest and lowest luminance in the panel arises mostly from the backlight module rather than the proposed driving structure. By improving the luminance uniformity of the backlight module, the luminance difference of the panel can be decreased. To evaluate the pixel charging ratios under a heavy loading pattern, the subpixel-based vertical stripe patterns of odd or even columns are displayed on the panel since the data voltages swing with the largest amplitude from 0 V to ± 4.5 V. For a full white pattern with both odd and even column subpixels lit up, the data voltages are all fixed at 4.5 V or -4.5 V by frame, so all subpixels are assumed to be fully charged. Measured results show that the luminance of the vertical stripe patterns of odd and even columns is almost identical to half of the luminance of the white pattern where all column subpixels are lit up. The maximum deviation between the luminance of the vertical stripe patterns and the half luminance of the full white

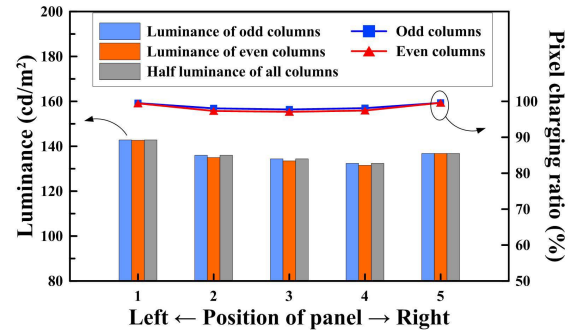


FIGURE 20. Luminance and pixel charging ratios with respect to positions at bottom end of panel when various subpixel columns are lit up.

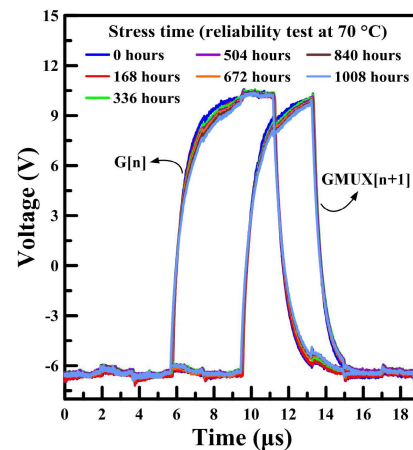


FIGURE 21. Measured waveforms of G[n] and GMUX[n + 1] in proposed gate driver circuit after high-temperature reliability test.

pattern is 4.00 cd/m². Furthermore, if the pixel charging ratio is high enough, then the pre-charging time of odd pixels is not required to be the same as that of even pixels. By reducing the heavy RC loadings of the MUX TFTs and data lines, the pixel charging ratio is greatly increased. The pixel charging ratios of the odd and even pixels at the bottom-middle of the panel with the largest RC loadings are above 97.75% and 97.09%, respectively. The difference in the luminance of the odd and even pixels in the images is very slight because the difference in pixel charging ratio (0.66%) between them is very small; as such, the influence of the difference in pre-charging time can be ignored. Hence, the proposed pixel circuit can increase the pixel charging ratio in an uncomplicated manner with TFT backplane technologies.

To confirm the long-term reliability of the proposed gate driver circuit, Fig. 21 plots the output waveforms of G[n] and GMUX[n + 1] that are measured at 70 °C for 1008 h. The rising and falling times of G[n] are 1.40 μ s and 1.08 μ s, respectively, and those of GMUX[n] are 1.34 μ s and 0.88 μ s, respectively, before stress. After the accelerated lifetime test is performed, the rising times of G[n] and GMUX[n] are increased by only 0.83 μ s and 0.86 μ s, respectively, and the falling times of G[n] and GMUX[n] are increased by only 0.38 μ s and 0.19 μ s, respectively. Also, the output waveforms

can be generated and transmitted sequentially without any malfunction. Therefore, the aforementioned experimental and simulated results demonstrate that the proposed driving structure and gate driver circuit are favorable for use in UHD TFT-LCDs with a frame rate of 120 Hz.

VI. CONCLUSION

This paper presents a new driving structure and a new gate driver circuit that is based on LTPS TFTs to improve the pixel charging ratios of UHD TFT-LCDs at a high frame rate. The proposed driving structure drives two subpixels with one data line to reduce the number of required source driver ICs and improves the pixel charging ratio by reducing the RC loadings of the data lines and prolonging the available pixel charging time. The effects of the RC loadings on pixel charging are analyzed by performing comparative simulations of conventional and proposed driving structures. The measurement made on the proposed driving structure shows that the pixel charging ratio of a heavy loading pattern at a gray level of 255 is higher than 97.09%. The long-term stress test for 1008 h at 70 °C demonstrates the reliability of the proposed gate driver circuit. Therefore, the proposed driving structure and the gate driver circuit are highly promising for use in UHD TFT-LCDs in notebooks with a frame rate of 120 Hz.

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