IEEE Access
Multidisciplinary : Rapid Review : Open Access Journal

Received 28 June 2022, accepted 30 July 2022, date of publication 8 August 2022, date of current version 12 August 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3197171

RESEARCH ARTICLE

Improving Flicker of Low-Refresh-Rate Driven Active-Matrix Organic Light-Emitting Diode Display

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ABSTRACT The brightness of low-temperature polycrystalline silicon and metal-oxide (LTPO) active-matrix organic light-emitting diode (AMOLED) display under low-refresh-rate driving condition tends to increase during pixel voltage holding time of each frame even though there is no critical leakage current path from the storage capacitor. We have found that the main cause of the brightness increase is electron trapping into the gate insulator of driving thin-film transistor (DTFT) which operates in the saturation mode prone to hot carrier injection. We propose a novel driving method to suppress the brightness variation by applying a high voltage to the source and drain of the DTFT during the non-emitting time which is inserted periodically for dimming the organic light-emitting diode (OLED) display. Our experimental results show that the brightness variation can be reduced from 3.7 % to 1.4 % at the 63rd gray level by the proposed DTFT reset scheme.

INDEX TERMS AMOLED, flicker, LTPO, low-refresh-rate driving.

I. INTRODUCTION

In recent years, two thin-film transistor (TFT) technologies have been utilized for AMOLED display. Low Temperature Polycrystalline Silicon (LTPS) TFT has been mainly used for mobile applications such as smart watches and mobile phones while the metal-oxide TFT (oxide TFT) is thought to be suitable for large display applications such as TV. These two technologies have their pros and cons; the LTPS TFT has higher carrier mobility but larger leakage current than the oxide TFT while the oxide TFT has extremely low leakage current but relatively low carrier mobility [1], [2], [3]. In order to compensate for the weaknesses of the LTPS and oxide TFTs, a new concept called LTPO technology has been proposed [4].

The concept of LTPO technology, which combined LTPS TFT and oxide TFT in the same pixel circuit, was first introduced by "Apple Inc." [4]. The LTPO pixel circuit can realize a low-refresh-rate e.g., 1 Hz driving which can reduce the power consumption of the driving circuit considerably. Initially, LTPO was used for smart watches because most of the images displayed on them were still images [4], [5]. Recently, a refresh rate of 120 Hz has been adopted by mobile devices to improve video quality. The high-refresh-rate driving consumes more driving power. In order to reduce the additional power consumption of high-refresh-rate driving, variable-refresh-rate driving combining low-refresh-rate and high-refresh-rate has been proposed [8]. Fig. 1 shows the measurement data of driving power consumption in 6-inch FHD+ (1080 × 2280) AMOLED display panel under the variable-refresh-rate driving.

In an LTPO pixel circuit, LTPS TFTs are used for both the current driving device of an OLED and relatively less important switching devices while oxide TFTs are used as critical switching devices to reduce the leakage current from the storage capacitor [6]. The low-refresh-rate driving method could be a useful solution to enhance the value of OLED display because liquid crystal display (LCD) cannot realize 1 Hz driving [4], [5], [6], [7], [8].

However, in order to take advantages of LTPO, some technical challenges should be taken on. Modified pixel circuits and additional process steps are mandatory. Nevertheless,

The associate editor coordinating the review of this manuscript and approving it for publication was Wen-Sheng Zhao.

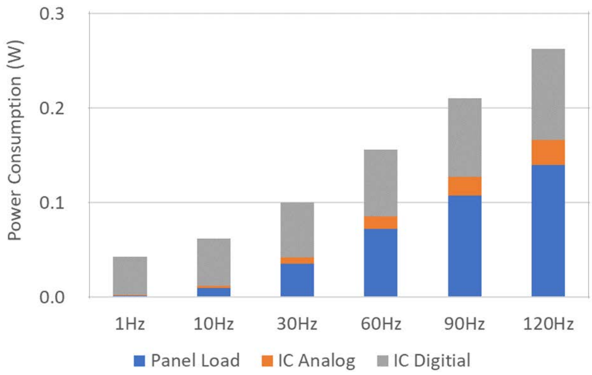

FIGURE 1. Driving power of 6" FHD+ AMOLED display panel for various refresh-rate.

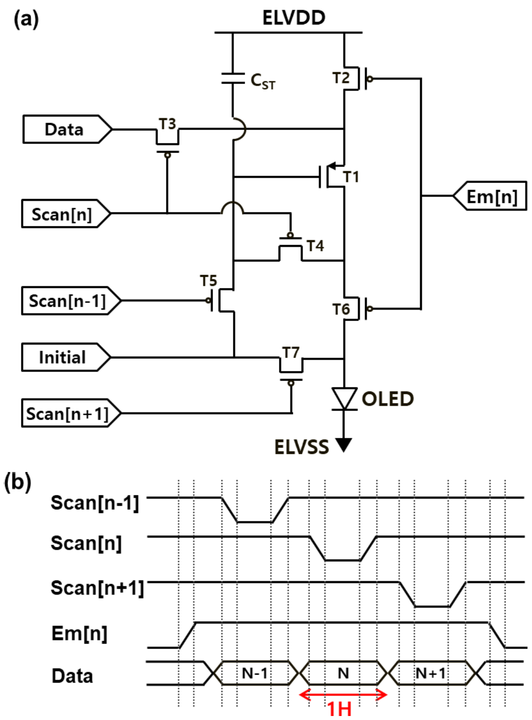

FIGURE 2. Conventional 7T-1C LTPS-TFT AMOLED pixel circuit. (a) Circuit diagram and (b) timing diagram.

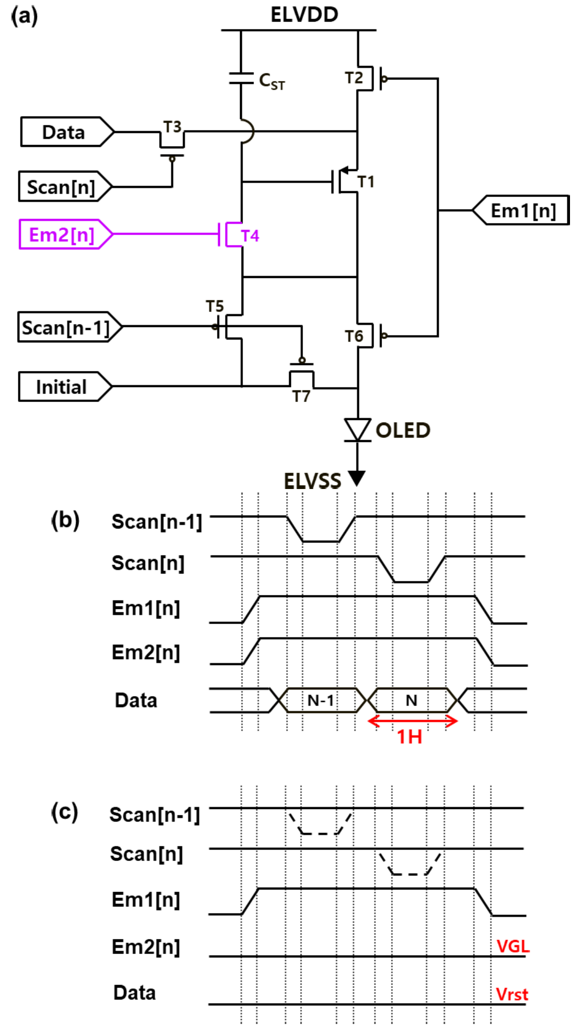

FIGURE 3. New 7T-1C LTPO-TFT AMOLED pixel circuit. (a) Circuit diagram, (b) timing diagram for data writing, (c) timing diagram for non-emitting duration (without or with anode discharging) under low-refresh-rate driving condition.

unknown problems may occur. Especially, brightness stability could become a critical problem because human sensitivity to brightness is increased under lower refresh rate [5], [6], [7], [8]. It has been reported that brightness variation is detected irrespective of charge loss in the storage capacitor even with LTPO [8]. The brightness instability under a low-refresh-rate may result from many unknown causes. Our measurement data show that electron trapping into the gate insulator of the driving TFT is one of the causes of the brightness instability. We propose a novel solution to this problem and report the effects of our solution under the low-refresh-rate driving condition.

II. LTPO AMOLED PIXEL CIRCUIT

Figure 2 shows the conventional 7 TFTs and 1 capacitor (7T-1C) AMOLED pixel circuit structure and its timing diagram [9]. It was invented to compensate for the non-uniform threshold voltage (V_T) of the driving TFT T1. We propose a new 7T-1C pixel circuit suitable for the LTPO technology as shown in Fig. 3. The ΔV_T compensation mechanism is same as the conventional 7T-1C. Only one TFT (T4) is the n-channel oxide TFT, and the others are p-channel LTPS TFTs. The channel length and width (W/L) of T4 is 4.5/4.5 microns and W/L of T1 is 3.0/23.5 microns. W/L of other LTPS switching TFTs is 3.0/3.0 microns. Fig. 4 shows transfer characteristics of the TFTs in the same substrate. Oxide TFT's leakage current is less than 10 fA. This means that the charge in the storage capacitor C_{ST} can be maintained almost constant even for one second.

Em2[n] signal is added to control the oxide TFT (T4) and its frequency is same as the display refresh rate. During data writing, Em2[n] driver circuit generates the same voltage waveform as Em1[n] as shown in Fig. 3 (b). However, Em1[n] pulses are needed not only for data writing but also for OLED anode discharging especially for low-refresh-rate

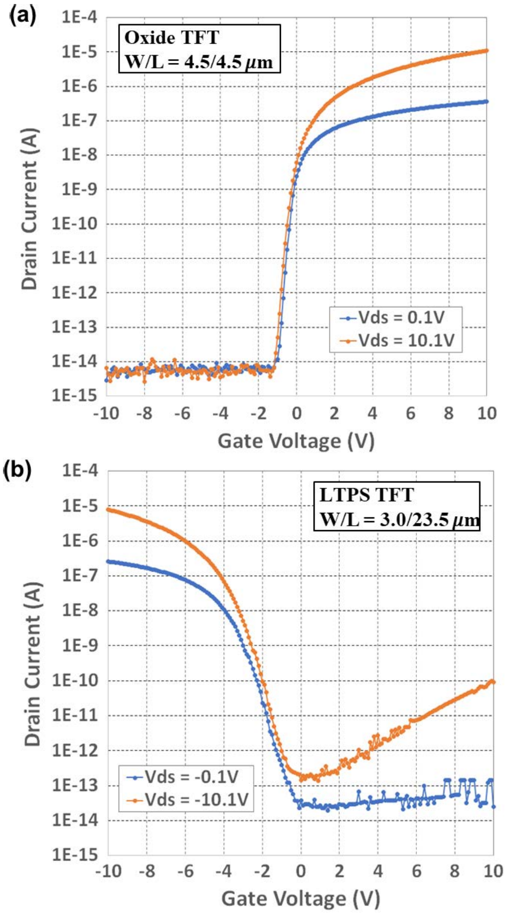

FIGURE 4. Transfer characteristics of TFTs. (a) Oxide TFT W/L = 4.5/4.5 μm, (b) p-channel LTPS TFT W/L = 3.0/23.5 μm.

driving. Without anode discharging, charge accumulation at the OLED anode caused by the leakage current of the driving TFT (T1) may increase the brightness of zero grey level [7].

Em2[n] should be kept low during the OLED anode discharging to maintain the data voltage at the storage capacitor (C_{ST}) as shown in Fig. 3 (c). Periodic Em1[n] pulses are also used for dimming control of the OLED display by modulating the pulse width of Em1[n]. If the discharging during the non-emitting time is not sufficient, Scan[n] pulses are applied additionally at the same frequency as Em1[n] in order to pull the anode voltage down to the initial voltage. The dashed lines in Fig.3 (c) show the Scan[n] waveform for this additional OLED anode discharging.

III. PHENOMENA

We fabricated a 6 inches FHD+ OLED display adopting the new LTPO pixel circuit of Fig. 3. The display panel was fabricated on the polyimide-coated glass substrate. First, LTPS TFTs were prepared on the substrate, and then oxide TFT process was conducted. After completing the TFT fabrication process, OLED was deposited by evaporation. Finally, thin-film encapsulation (TFE) was done to protect the OLED devices.

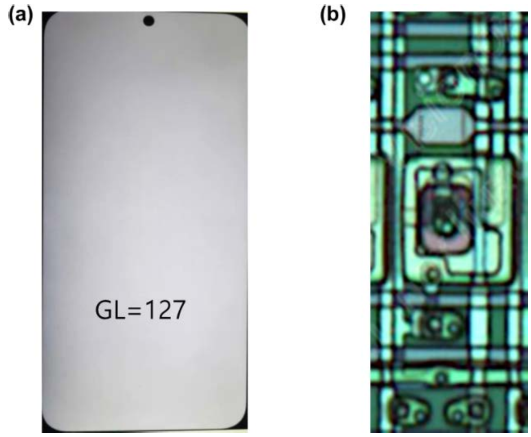

FIGURE 5. (a) Display image of 6″ FHD+ LTPO-TFT AMOLED panel and (b) pixel image.

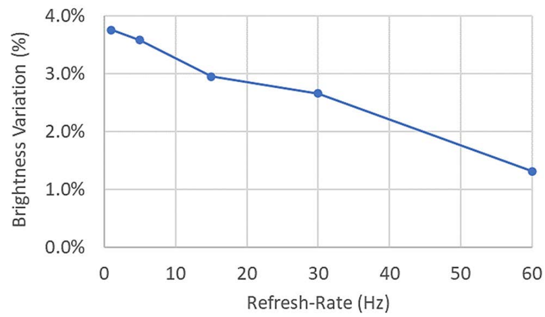

FIGURE 6. Brightness variation of new 7T-1C LTPO-TFT OLED display at 63rd gray level under various refresh-rate driving condition without scan pulses.

We measured the brightness variation of the OLED display under the operation scheme mentioned above. The measurement tool was Minolta CA-P410/V410. First, we measured the brightness with the Scan[n] pulses not applied during the non-emitting time. Fig. 6 shows the measured brightness difference without the Scan[n] pulses for various refresh rate. The brightness variation increases as the refresh rate decreases even with the LTPO pixel circuit. In order to investigate the causes of this variation, we measured the transient brightness variation for the 1 Hz refresh rate. Fig. 7 shows two kinds of brightness variation patterns. One is continuous brightness increase trend for 1 second, i.e. during one frame time and the other is the fast fluctuation within one frame time, which is the result of dimming operation by Em1[n] pulses. We do not recognize this fast brightness fluctuation as a flicker even for the large variation because the frequency is as high as 60 Hz. However, the continuous brightness increase of several percent variation for 1 second can be recognized as a flicker because it repeats at 1 Hz. The amount of slow brightness increase varies depending on the gray levels as shown in Fig. 7. It changes 11.4 nit (1.9 %) at the 255th gray level, 1.06 nit (3.7 %) at the 63rd gray level, and 0.081 nit (5.7 %) at the 15th gray level, respectively.

Since the relative variation is larger for the lower gray level, stronger flicker is perceived at the lower gray levels under the 1 Hz refresh rate condition [5].

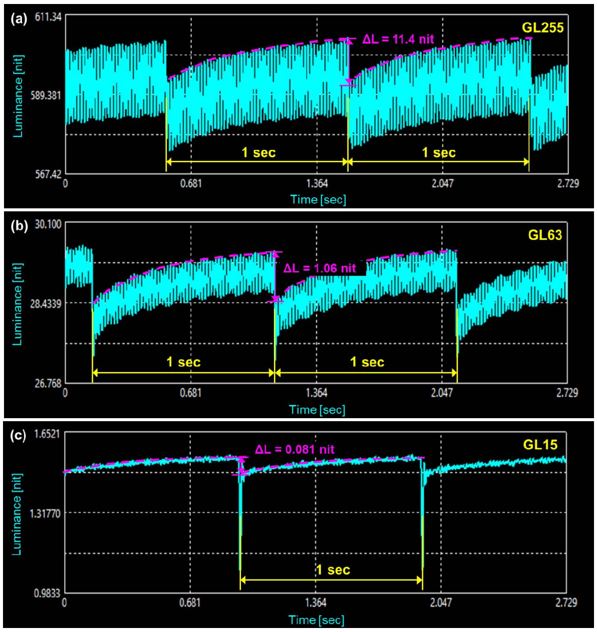

FIGURE 7. Brightness variation of new 7T-1C LTPO-TFT OLED display under 1 Hz driving condition without scan pulses. (a) Gray level: 255, (b) Gray level: 63, (c) Gray level: 15.

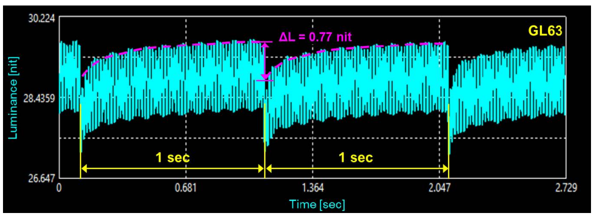

FIGURE 8. Brightness variation of new 7T-1C LTPO-TFT OLED display under 1 Hz driving condition with 60 Hz scan pulses (Vrst = 0 V).

IV. ANALYSIS AND IMPROVEMENT

The Scan[n] pulses for complete anode discharging provide an additional effect of reducing brightness variations. Fig. 8 shows that the brightness change at the 63rd gray level is reduced to 0.77 nit (2.6 %) when the Scan[n] pulses are applied by 60 Hz. The data voltage is 0 V and the initial voltage is −3 V during the data holding period. However, the pattern of brightness variation is similar to the results of Fig. 7 and the flicker is still observed though the anode is completely discharged at 60 Hz. This means that the discharging of anode electrode is not a conclusive solution for the brightness variation of the 1 Hz refresh rate driving.

The charge leakage from C_{ST} to the initial voltage node may be one of the possible reasons for the brightness increase in Fig. 7 and Fig. 8. The leakage current pulls down the gate voltage of T1, which increases the drain current of T1, i.e. the current supply to the OLED. However, the switch TFT T4 in the critical leakage path is an oxide TFT as shown in Fig. 3. The off-state current of our oxide TFT (Indium Gallium Zinc Oxide: IGZO) is lower than 10 fA as shown in Fig.4. Therefore, we exclude the voltage variation in C_{ST} from the causes of the brightness increase and we suspect other causes to increase the current of T1.

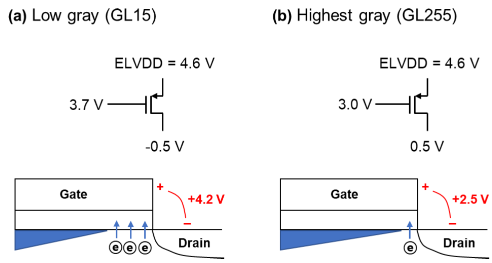

FIGURE 9. Different electron trapping effects in DTFT T1 due to electric field difference according to the gray level.

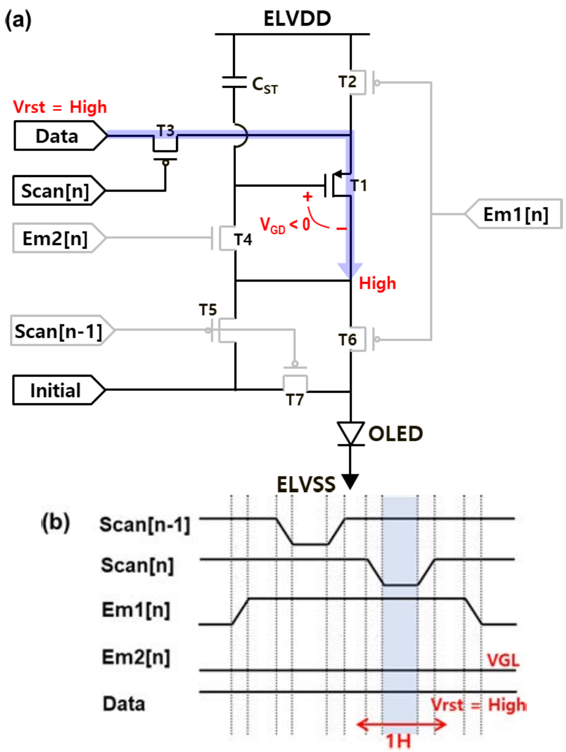

FIGURE 10. Revised low-refresh-rate driving of 7T-1C LTPO-TFT OLED pixel circuit. (a) Application of negative V_{GD} to T1, (b) timing diagram for both discharging anode and resetting T1 with scan pulses under low-refresh-rate driving condition.

The brightness continuously increases but gets back to the previous level after rewriting the data as shown in Fig. 7 and Fig. 8. This phenomenon is similar to the short-term image sticking in p-channel LTPS TFT-based AMOLED, which is known to be the effect of "hysteresis" [10]. It has been reported that the shallow trapped electrons in the gate insulator near drain can be released to recover the initial state by applying a negative gate-to-drain bias (V_{GD}) [10], [11]. The operation sequence of the conventional 7T-1C pixel circuit includes this step–low scan[n-1] pulse–to reset the characteristics of T1 as shown in Fig. 2. When the low initial voltage is input into the gate electrode of T1 through T5, the strong negative V_{GD} restores the characteristics of T1. This process helps to reduce the short-term image sticking and to stabilize the driving current of T1. We thought that the brightness increase under the 1 Hz driving can also be recovered

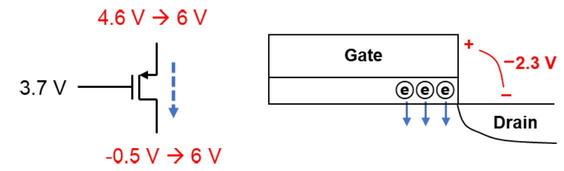

FIGURE 11. Electron de-trapping in T1 by applying positive Vrst (resetting).

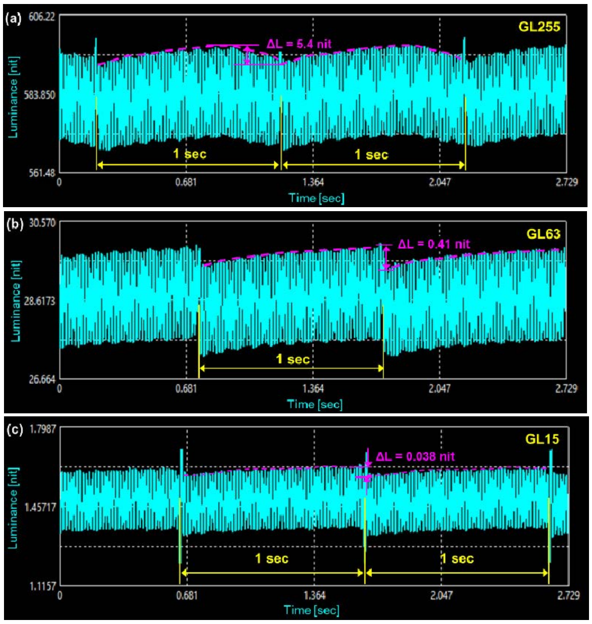

FIGURE 12. Brightness variation of new 7T-1C LTPO-TFT OLED display under 1 Hz driving condition with scan pulses for resetting T1 (Vrst = 6 V). (a) Gray level: 255, (b) Gray level: 63, (c) Gray level: 15.

by adopting this reset process during the data holding period.

It was reported that electron trapping into the gate insulator can appear even in the p-channel LTPS TFT under saturation regime [12]. Lots of electron-hole pairs are generated near the drain by impact ionization under saturation regime. The electrons are easily captured in the shallow traps of the gate insulator when V_{GD} of T1 is sufficiently positive. Fig. 9 illustrates how the effect of electron trapping appears differently in p-channel TFT depending on V_{GD} value under saturation regime. In the case of low gray levels, the gate voltage of T1 is higher and the drain voltage is lower than the high gray level case. Therefore, V_{DS} is larger and V_{GD} is more positive, which generates more electron-hole pairs, and the generated electrons can be more easily trapped into the gate insulator. The electron trapping near drain reduces the effective channel length of T1 and the driving current continuously increases throughout the data holding period [12].

The relatively larger brightness variation at low gray levels is explained by this physical model. In order to prove this physical model and to improve the brightness stability, we attempted to apply a highly positive voltage to the source of T1 at 60 Hz rate under the 1 Hz refresh rate driving condition as shown in Fig. 10. Since the gate voltage of

TABLE 1. Summary of brightness variation at low, middle, and high gray levels under 1 Hz driving condition.

	GL15	GL63	GL255
ΔL (w/o T1 reset)	0.081 nit (5.7 %)	1.06 nit (3.7 %)	11.4 nit (1.9 %)
ΔL (with T1 reset, Vrst = 6 V)	0.038 nit (2.3 %)	0.41 nit (1.4 %)	5.4 nit (0.91 %)

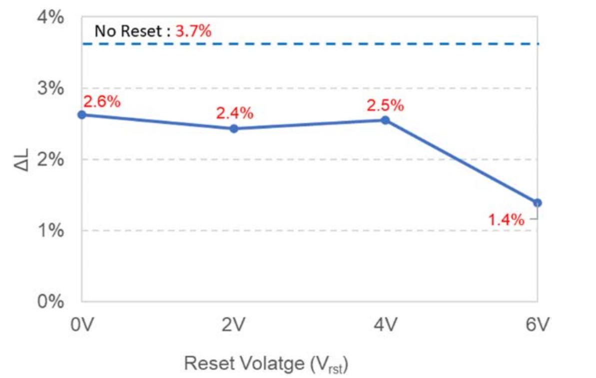

FIGURE 13. Brightness variation at 63rd gray level for various Vrst values under 1 Hz driving condition.

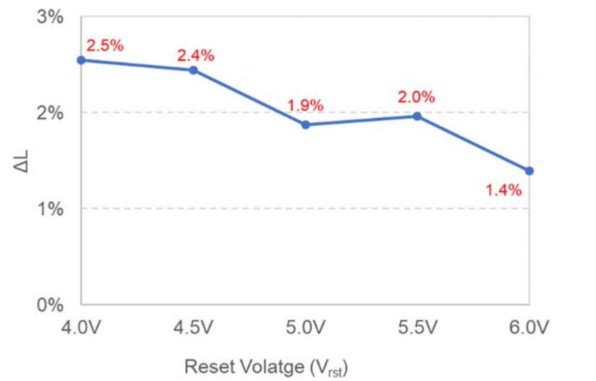

FIGURE 14. Brightness variation at 63rd gray level for Vrst values ranging from 4 V to 6 V under 1 Hz driving condition.

T1 is kept constant by CST, T1 is turned on and negative VGD is implemented by applying the positive data voltage. Accordingly, the trapped electrons near drain can be released by the negative VGD. Fig. 11 illustrates the concept of this mechanism.

In order to investigate the effect of the proposed method for resetting T1, we applied different reset voltages (Vrst) ranging from 0 V to 6 V through the data line. Fig. 12 shows the results of brightness variation when Vrst is 6 V under 1 Hz refresh rate driving condition. The brightness variation at the three different gray levels is reduced to less than half without exception by employing our proposed method. The effects of resetting T1 at the three gray levels are summarized in Table. 1. These results evidently demonstrate that our method improves the brightness variation by de-trapping electrons trapped in the gate insulator of T1.

We also investigated the effect of Vrst variation. Fig. 13 shows the Vrst dependence of brightness variation at the 63rd gray level. The brightness variation is almost constant at about 2.5 % when Vrst is 0 V ∼ 4 V, which indicates that the electron de-trapping is negligible for low Vrst. When Vrst is 6 V, the brightness variation is significantly reduced to 1.4 %. Our SPICE simulation results show that V_{GD} is approximately 0 V when Vrst of 4 V is applied and that more positive Vrst is required for negative V_{GD}. When Vrst of 6 V is input to the source of T1, a sufficiently negative V_{GD} is obtained. We also investigated the effect of Vrst values from 4 V to 6 V in detail. Fig. 14 shows that the brightness variation decreases as Vrst becomes higher.

V. CONCLUSION

The brightness of LTPO AMOLED display unexpectedly increases at the low-refresh-rate of 1 Hz. The brightness variation is relatively large at lower gray levels. The main cause of such brightness variation is electron trapping into the gate insulator near the drain region of the DTFT under the saturation regime. We propose a novel driving method to reduce the brightness variation by de-trapping the electrons with a negative V_{GD}. It is implemented by applying a highly positive voltage to the source of the DTFT at 60 Hz during the data holding period. The brightness variation can be reduced from 3.7 % to 1.4 % at the 63rd gray level by the proposed driving scheme. Our new LTPO AMOLED pixel circuit and its driving scheme provide a requisite solution to the brightness variation problem for comprehensive image quality of low- refresh-rate AMOLED display.

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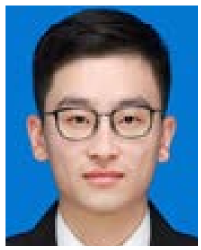

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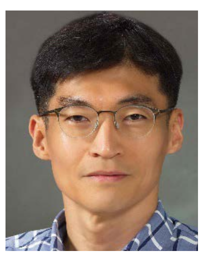

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