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APPLIED RESEARCH

Single-Switch High-Step-Up DC-DC Converter Employing Coupled Inductor and Voltage Multiplier Cell

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ABSTRACT This paper introduces a high-step-up dc-dc converter to provide voltage boosting in low-voltage applications. The circuit contains only a single active switch and is based on the boost-type converter using coupled inductor and voltage multiplier cell. The proposed topology exhibits high efficiency, reduced voltage stress on the semiconductors and requires a low component count. The circuit is intended for applications with rated power in the order of a few hundreds of Watts, which corresponds to the typical level of a single photovoltaic (PV) module. A detailed mathematical description of the circuit operation is carried out, providing the means for the adequate design of the converter. The dynamic analysis is also addressed in the paper, and proper closed-loop operation is demonstrated. A 400 W prototype operating at 90 kHz, with an input voltage range of 24-48 V and output voltage of 400 V was built and tested in laboratory. Experimental results validate the analyses carried out and measurements indicate efficiency levels up to 97.5%, which ratifies the proposed converter as a good solution for typical PV applications.

INDEX TERMS High voltage gain, high step-up, coupled inductor, voltage multiplier cell.

I. INTRODUCTION

Direct current (DC) generation such as photovoltaic power systems has become one of the main sources of electricity supply worldwide. Nevertheless, the energy is produced at relatively low voltage levels, and usually dc-dc converters are required to reach high voltage gain and high efficiency.

It is known that the overall efficiency of a switching converter is strongly affected by switching and conduction losses. Therefore, using circuits with low component count, reduced voltage stress and with the capability of regenerating the leakage energy is key to improving the overall system performance. However, obtaining all these characteristics from a simple dc-dc converter is not an easy task. A good example is the conventional boost converter, which is not appropriate in most applications requiring high voltage conversion ratio because the voltage gain depends solely on the duty cycle [1], [2]. In such case, due to the non-idealities inherent to the elements of the circuit, the efficiency is reduced at high conversion ratio. In this sense, numerous alternative topologies have been proposed to circumvent the conventional step-up converters' drawbacks, as discussed in the reviews presented in [3] and [4]. As it can be observed in these papers, several voltage boosting techniques are used to achieve high voltage gain, such as coupled inductor, voltage multiplier cell and switched capacitor. Among the numerous solutions proposed in the literature, those based on the single-switch boost converter using coupled inductor and capacitor-diode interaction can be highlighted [5], [6].

Considering typical single-module PV applications, in which voltage and power levels are in the order of some tens of Volts and few hundreds of Watts, respectively, the use of simpler topologies is preferrable. In this sense, converters containing a single active switch, one coupled inductor and reduced number of diodes and capacitors have been widely investigated by researchers worldwide. For instance, using

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the conventional boost-flyback topology presented in [7], a larger voltage conversion ratio is achieved by the summing the individual voltage gains of the boost and flyback stages. However, although the voltage stress on the active switch is reduced, an auxiliary snubber circuit is required to limit the voltage spike on the diode contained in the flyback stage. This issue can be addressed by using a voltage doubler associated with the coupled inductor, which also increases the voltage gain of the converter [8]. In [9] and [10], two converters exhibiting a similar voltage gain to that introduced in [8] are proposed. However, although [9] has the advantage of requiring a lower component count, the active switch and the output diode are subjected to the entire value of the output voltage. Circuits operating with higher voltage gains and containing three diodes and three capacitors were introduced in [11]–[14]. A further increase on the voltage gain is achieved by adding more diodes and capacitors to the circuit, as demonstrated in [15] and [16]. In this sense, in [17] and [18], generalized analyses are carried out and demonstrate that the voltage gain can be further increased by employing a higher number of voltage multiplier cells, thus requiring more diodes and capacitors. However, adding more components to the circuit can lead to higher conduction and switching losses, and therefore the overall efficiency of the system would be reduced. Instead of increasing the number of voltage multiplier cells, an alternative approach to achieve a higher voltage gain is to adjust the number of turns ratio or include more windings to the coupled inductor [19]–[24]. However, extreme values for the number of turns ratio can have a negative impact on the efficiency and adding windings would increase the complexity of the coupled inductor design.

Another important concern in high-step-up conversion is the input current ripple. Coupled-inductor-based solutions usually have pulsating input current, and circuits using an input boost inductor were proposed to ensure low input current ripple [22]–[24], but at the cost of requiring a higher component count and increasing the volume of the system. Interleaving techniques were also employed to reduce the input current ripple in high-step-up converters, but a more complex circuit is required and therefore only viable for higher power levels [25]–[30].

This paper introduces a single-switch high-step-up dc-dc converter for applications requiring moderate voltage gains and low component count. These features are key to developing technology for single-module PV systems, especially for integrated DC-AC conversion in AC PV modules. The voltage stresses on all semiconductors contained in the proposed circuit are lower than the output voltage, and thus conduction and switching losses are reduced, which in turn contributes to high efficiency operation. In addition, the voltages on all capacitors are also lower than the output voltage, which reduces the required capacitive energy and potentially leads to volume reduction. Finally, the use of a single coupled inductor with only two windings brings simplicity for the circuit implementation.

II. PROPOSED SINGLE-SWITCH HIGH STEP-UP DC-DC CONVERTER

The proposed single-switch high step-up dc-dc converter composed of a single coupled-inductor and employing voltage multiplier cell is depicted in Fig. 1. The input stage is composed of the primary winding of the coupled inductor and the switch S. The inductances L_m and L_k represent the magnetizing and leakage inductances of the coupled inductor, respectively. The output stage consists of the secondary winding of the coupled inductor, three diodes (D_1-D_3), and three capacitors (C_1-C_3). A closer look at the circuit depicted in Fig. 1 unveils some important operational characteristics of the circuit: (a) the output voltage V_o corresponds to the sum of the voltages on C_2 and C_3; and (b) the pair D_1-C_1 provides an alternative path for i_{Lk} towards the output stage after the switch is turned off, thus the energy stored in L_k is recycled and the blocking voltage of S becomes naturally clamped. It is also demonstrated in this work that the coupled inductor operates both as a conventional transformer and an inductor, because: (a) energy is processed directly from the primary to the secondary winding during some intervals, as a typical transformer; and (b) energy stored in the magnetizing inductance in one stage is transferred to the output at a later interval, as occurs in the flyback converter.

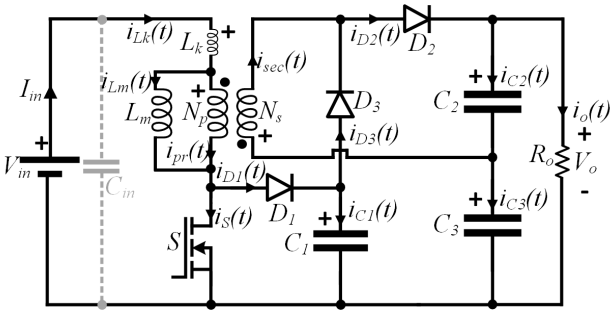


FIGURE 1. Proposed single-switch high step-up dc-dc converter employing coupled inductor and voltage multiplier cell.

III. OPERATION PRINCIPLE IN STEADY STATE

A sequence of five distinct stages characterizes the converter operation in steady state, as depicted in Fig. 2. In this work, a detailed analysis is carried out within a switching period T_s and the following simplifying assumptions are considered:

1) The magnetizing inductance current i_{Lm} is assumed constant and ripple-free;

2) The voltages on the capacitors C_1, C_2 and C_3 are assumed constant and ripple-free;

3) All the semiconductor elements are assumed as ideal;

4) L_k accounts for the total leakage inductance of the primary and secondary windings.

In order to simplify the converter operation within one switching cycle, a general description of the possible five steps is introduced below:

(a) First and third stages, which occur within the respective intervals Δt_1 and Δt_3, start when the switch S is

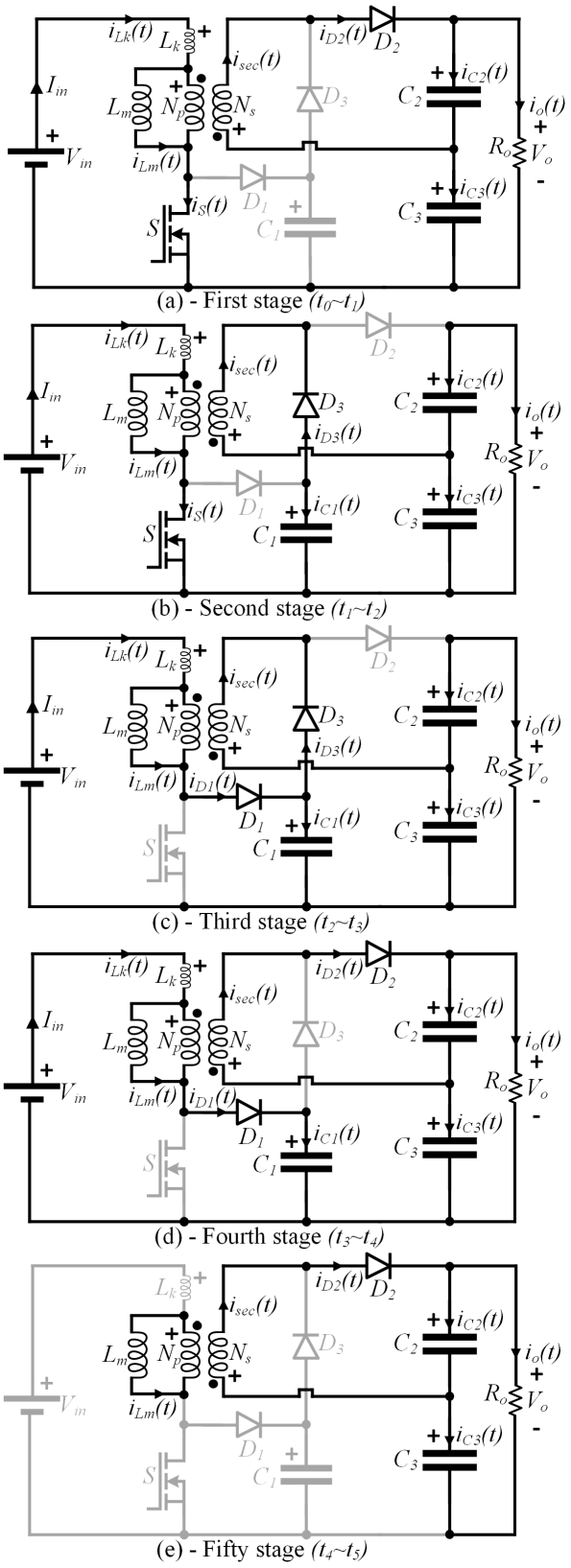


FIGURE 2. Operation stages at steady state.

turned-on and turned-off, respectively. During the interval Δt_3, the energy provided by the leakage inductance L_k is absorbed by C_1, thus avoiding the occurrence of a voltage spike on S. Under ideal operating conditions both Δt_1 and Δt_3 can be neglected, as these intervals are much briefer than those verified for stages 2, 4 and 5. The equivalent circuits of these two operation stages are illustrated in Fig. 2 (a) and Fig. 2 (c).

(b) The second, fourth and fifth operation stages can be considered as the main stages since most of the energy is processed by the converter during the intervals Δt_2, Δt_4 and Δt_5.

During the second stage (c.f., Fig. 2(b)), S is turned on and energy is provided by V_{in} to L_m and also to C_3 via direct energy transfer from the primary to the secondary windings of the coupled inductor (transformer-like operation). Regarding the fourth stage (c.f., Fig. 2 (d)), S is turned off, the leakage energy is diverted to C_1 and the coupled inductor transfer energy to C_2. Finally, during the fifth stage (c.f., Fig. 2 (e)), energy previously stored in L_m is transferred to C_2 via the secondary winding of the coupled inductor (flyback-like operation).

Fig. 3 illustrates the main theoretical waveforms for steady-state operation.

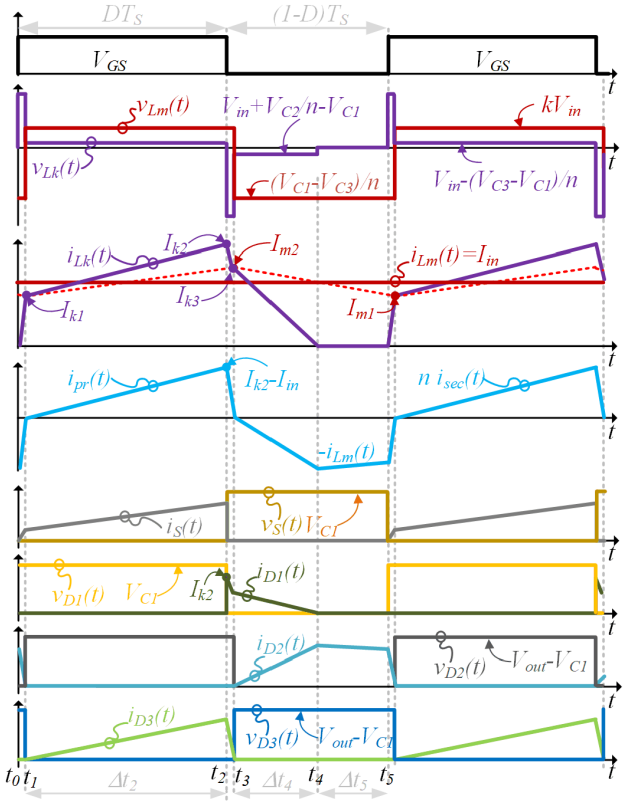


FIGURE 3. Main theoretical waveforms for steady-state operation.

The mathematical description of the converter for steady-state operation is carried out from the analysis of the equivalent circuits generated from stages 2, 4 and 5, and also from the waveforms detailed in Fig. 3. In addition, the following

expressions are considered:

$$\Delta t_i = t_i - t_{i-1}; \quad T_s = \frac{1}{f_s}, \quad n = \frac{N_s}{N_p}; \\ \lambda = \frac{L_k}{L_m}; \quad k = \frac{1}{\lambda + 1}. \tag{1}$$

where: i is the index that defines the time interval of each stage, which starts at t_{i-1} and ends at t_i.

The factor λ defined in (1) represents the ratio between the leakage inductance L_k and the magnetizing inductance L_m. As it is going to be demonstrated in this paper, λ affects the voltage gain of the proposed converter and should be kept as low as possible, which is achieved if the leakage inductance of the coupled inductor is reduced.

IV. STATIC MODEL

A complete mathematical description of the converter operation in steady state is derived in this section. The static model is obtained by the analysis of the equivalent circuits of the operating stages depicted in Fig. 2 and the waveforms shown in Fig. 3. Based on the results of this analysis, the static gain and stresses on the components of the circuit can be computed, thus allowing the adequate design of the converter.

Equations (2)–(5), valid for steady-state operation, can be determined from the analysis of the current on L_k during the first, second, third and fourth stages, respectively.

$$I_{k1} = \left(V_{in} + \frac{V_{C2}}{n}\right) \cdot \frac{\Delta t_1}{\lambda L_m} \tag{2}$$

$$I_{k2} = I_{k1} + \left(V_{in} - \frac{V_{C3} - V_{C1}}{n}\right) \cdot \frac{\Delta t_2}{\lambda L_m} \tag{3}$$

$$I_{k3} = I_{k2} - \left(V_{in} - \frac{V_{C3} - V_{C1}}{n} - V_{C1}\right) \cdot \frac{\Delta t_3}{\lambda L_m} \tag{4}$$

$$I_{k3} = \left(V_{C1} - V_{in} - \frac{V_{C2}}{n}\right) \cdot \frac{\Delta t_4}{\lambda L_m} \tag{5}$$

The equilibrium of the energy processed by L_m can be demonstrated through its Volt-second balance as given in (6). The Volt-second balance in L_k is not necessary since it is already implicitly considered in (2)–(5).

$$(V_{C3} - V_{C1}) \,.\, (\Delta t_2 + \Delta t_3) = V_{C2} \,.\, (\Delta t_4 + \Delta t_5 + \Delta t_1) \tag{6}$$

The analysis of the proposed high gain dc-dc converter unveils that the average current of L_k, which corresponds to the average value of the current provided by the input voltage source, is given by (7).

$$I_{k1} D T_s + I_{k2} \Delta t_2 = (2I_{in} - I_o) T_s \tag{7}$$

The average current on D_1, D_2 and D_3, which must be equal to the average value of the output current I_o, can be computed by (8), (9) and (10), respectively. Equaling (8) and (9), as well as (8) and (10), results in two expressions, which compose the fundamental equations system of the converter.

$$n(I_{k2} + I_{k3})\Delta t_3 + n I_{k3} \Delta t_4 = 2n I_o T_s \tag{8}$$

$$2I_{in}((1 - D)T_S + \Delta t_1) + (I_{k2} + I_{k3})\Delta t_3 + I_{k3}\Delta t_4 = 2n I_o T_s \tag{9}$$

$$(I_{k2} + I_{k1} - 2I_{in})\Delta t_2 + (I_{k2} + I_{k3} - 2I_{in})\Delta t_3 = 2n I_o T_s \tag{10}$$

Equation (11) indicates that the output voltage V_o must be equal to the sum of V_{C2} and V_{C3}.

$$V_{C2} + V_{C3} = V_o \tag{11}$$

From the analysis of the Fig. 2 (b) it is possible to demonstrate that

$$V_{C3} - V_{C1} = n k V_{in}. \tag{12}$$

The modulation strategy adopted for the converter provides the relation between the duty cycle and the intervals of the operating stages, as given by (13) and (14).

$$\Delta t_1 + \Delta t_2 = D \cdot T_s. \tag{13}$$

$$\Delta t_3 + \Delta t_4 + \Delta t_5 = (1 - D) \cdot T_s. \tag{14}$$

The expressions presented in (2)–(14) define the fundamental equations describing the steady-state operation of the converter. However, this system of equations does not have a trivial analytic solution, thus requiring numerical methods to be solved. However, as already mentioned during the description of the operating stages, both Δt_1 and Δt_3 can be neglected because their values are usually much smaller than Δt_2, Δt_4 and Δt_5. Considering this simplifying assumption, an approximate mathematical model can be derived, which provides an adequate description of the converter operation in steady state. On the other hand, the influence of the leakage inductance on the system operation is still represented by the decoupling factor k defined in (1).

Disregarding Δt_1 and Δt_3, it follows that

$$\Delta t_2 = D \cdot T_s, \tag{15}$$

$$\Delta t_4 + \Delta t_5 = (1 - D) \cdot T_s. \tag{16}$$

Replacing (12) and (15) into (3) and (15) into (7), the unknowns I_{k1} and I_{k2} can be determined by (17) and (18), respectively.

$$I_{k1} = \frac{I_{in} - I_o}{D} - \frac{(1 - k) D T_s V_{in}}{2 \lambda L_m} \tag{17}$$

$$I_{k2} = \frac{I_{in} - I_o}{D} + \frac{(1 - k) D T_s V_{in}}{2 \lambda L_m}. \tag{18}$$

At this point, the current gain of the proposed converter can be derived by substituting (15) into (7) and (10), resulting in (19).

$$\frac{I_o}{I_{in}} = \frac{1 - D}{1 + k n}. \tag{19}$$

Considering the power balance between the input and output, it is possible to obtain the static voltage gain M presented in (20), which demonstrates the dependency of the output voltage on the parameters D, k and n.

$$M = \frac{V_o}{V_{in}} = \frac{(1 + k n)}{1 - D}. \tag{20}$$

The voltage level V_{C2} is determined by substituting (12), (15) and (16) into (6), and then the respective result into (20), yielding (21).

$$V_{C2} = \frac{k\,n\,D}{1-D} \cdot V_{in} \tag{21}$$

Fig. 4 depicts the voltage gain M as a function of D for different values of k. It is demonstrated that the decoupling factor k has a low impact on the ideal static gain.

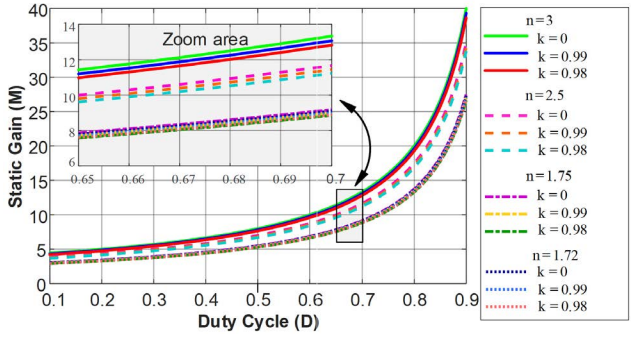


FIGURE 4. Static gain of the converter as function of *D* for different values of *k*.

Isolating V_o in (20) and substituting the result and (21) into (12), it is possible to determine V_{C3} according to (22).

$$V_{C3} = \left(\frac{1}{(1-D)} + k\,n\right) \cdot V_{in} \tag{22}$$

The voltage on capacitor C_1 given in (23) is derived by replacing (22) into (12).

$$V_{C1} = \frac{V_{in}}{1-D} \tag{23}$$

In this work, the duty cycle D is chosen to limit the voltage V_{C1} to some desired value. In this way, the designer is able to ensure that the blocking voltage of S is limited, thus guaranteeing that low voltage rating MOSFETs can be employed, which in turn contributes to reducing the conductions losses.

The current level I_{k3} can be computed from (5) and (8), yielding (24).

$$I_{k3} = \sqrt{\frac{2\,(1-k)}{(1+n\,k)} \cdot \frac{V_{in}\,I_{in}\,T_s\,D}{\lambda\,L_m}} \tag{24}$$

Finally, Δt_4 is determined by substituting (24) into (8), resulting in

$$\Delta t_4 = (1-D)\sqrt{\frac{2}{(1+n\,k)(1-k)} \cdot \frac{\lambda\,L_m\,I_{in}\,T_s}{V_{in}D}}. \tag{25}$$

An important step in the steady-state analysis of the proposed converter is determining the values of the passive elements L_m, C_1, C_2 and C_3. Initially, the value of L_m is chosen to guarantee that the magnetizing current ripple (ΔI_{Lm}) be limited to some prespecified level. The relation between L_m and ΔI_{Lm} can be computed from the waveforms shown in Fig. 3, as given by

$$L_m = \frac{k\,D\,T_s}{\Delta I_{Lm}} \cdot V_{in}. \tag{26}$$

From Fig. 2 it is possible to demonstrate that the capacitances C_1, C_2 and C_3 relate with the respective voltage ripples ΔV_{C1}, ΔV_{C2} and ΔV_{C3} as follows:

$$C_1 = \frac{T_s}{\Delta V_{C1}} \cdot I_o, \tag{27}$$

$$C_2 = \frac{D\,T_s}{\Delta V_{C2}} \cdot I_o, \tag{28}$$

$$C_3 = \frac{(1-D)\,T_s}{\Delta V_{C3}} \cdot I_o. \tag{29}$$

Finally, the voltage stresses on the semiconductor devices can be computed from the analysis of the topological states depicted in Fig. 2. In the proposed converter, the blocking voltage of both S and D_1 are equal to V_{C1} (given in (23)), while D_2 and D_3 are subjected to V_o - V_{C1} (given in (30)).

$$V_{D2} = V_{D3} = \frac{k\,n}{1-D} \cdot V_{in} \tag{30}$$

A. COMPARATIVE ANALYSIS WITH OTHER SINGLE-SWITCH HIGH-STEP-UP DC-DC CONVERTERS

The comparison of the proposed converter with other high-step-up dc-dc converters is summarized in Table 1. This comparative analysis is restricted to circuits containing one single switch, one coupled inductor with only two windings, and the same number of diodes and capacitors as the proposed converter. The efficiency is estimated based on SPICE simulations using the following devices: MOSFET IRFP4668PBF (V_{DSS} = 200 V; R_{DSon} = 8 mΩ) and MUR840 diodes (V_{RRM} = 400 V; V_F = 0.75 V; R_f =11 mΩ). Among all converters, only [7] needs a snubber circuit to prevent the occurrence of voltage spike on the switch. If such snubber is not included, the efficiency of this circuit becomes considerably reduced. Regarding the circuit introduced in [10], which is based on the zeta-type configuration, an isolated gate driver and higher energy on the capacitors are required. In comparison with the topologies presented in [11], [12], [13, and [14], the proposed converter has a lower voltage gain considering the same conditions of D and n. Therefore, the number of turns ratio must be increased to ensure the same voltage gain at a particular duty cycle level. However, in [11], the secondary winding inductance directly influences the converter voltage gain, which has a direct impact on the volume and conduction loss of the coupled inductor, and, in such introduced converters, more energy must be processed by the capacitors under similar operating conditions, which would inevitably increase the cost and size of the circuit. Among all solutions considered, only [8] requires a lower energy on the capacitors. Regarding [13] and [14], the blocking voltages on the active switches are higher than proposed converter, thus their estimated efficiencies are lower than the proposed converter under the same operating conditions.

TABLE 1. Comparation with other single-switch single-coupled-inductor high-step-up dc-dc converters.

Coupled-inductor Based Circuit	Voltage Gain (V_o/V_{in})	Voltage stress on the switch	Voltage stress on the diodes			[2]Estimated efficiency η [%]	[3] $\sum E_c$ [mJ]
			V_{D1}	V_{D2}	V_{D3}		
Proposed Converter	$\frac{1+nk}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{knV_{in}}{1-D}$	$\frac{knV_{in}}{1-D}$	97.6	160
Converter in [7]	$\frac{1+nkD}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	[1] Limited by snubber RCD	[1] Voltage on Diode snubber	96.7	267
Converter in [8]	$\frac{1+nk}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{knV_{in}}{1-D}$	$\frac{knV_{in}}{1-D}$	97.3	150
Converter in [10]	$\frac{1+nk}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{knV_{in}}{1-D}$	$\frac{(n+1)V_{in}}{1-D}$	97.0	343
Converter in [11]	$\frac{2+nk}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{knV_{in}}{1-D}$	$\frac{knV_{in}}{1-D}$	97.6	290
Converter in [12]	$\frac{(2+nk)+(nk-1)D}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{(1+kn)V_{in}}{1-D}$	$\frac{knV_{in}}{1-D}$	$\frac{(1+kn)V_{in}}{1-D}$	97.3	291
Converter in [13]	$\frac{(1+2nk+nkD)}{1-D}$	$\frac{(1+kn)V_{in}}{1-D}$	$\frac{(1+kn)V_{in}}{1-D}$	$\frac{(1+kn)V_{in}}{1-D}$	$\frac{(1+kn)V_{in}}{1-D}$	96.4	280
Converter in [14]	$\frac{(1+nk+2nkD)}{1-D}$	$\frac{(1+kn)V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{(1+kn)V_{in}}{1-D}$	95	325

[1]The voltage stress on the D_2 and D_3 is not informed in the published papers.
[2]Efficiency estimated by the @Orcad 17.2 Lite computing software considering: f_s = 100 kHz, D = 65% and P_o = 400 W. Similar parasitic resistances were included to estimate conduction and magnetic losses on the coupled inductor.
[3]Considering an output voltage ripple of 0.5%.

Based on the results of the comparative analysis, it can be concluded that the proposed circuit shows potential advantages for high-step-up operation, as it exhibits high efficiency and requires a relatively low capacitive energy. An important remark is that, although the proposed circuit does not have the higher voltage gain among all the circuits considered, its estimated performance under operating conditions similar to typical PV modules makes it a good candidate for low power PV applications.

V. DESIGN PROCEDURE

A design procedure is elaborated for the adequate design of the proposed converter using the key results derived in the mathematical analysis carried out in section IV, as detailed in the following steps:

1 – Define the value of the voltage on C_1 according to the desired voltage stress on S;

2 – From (23) compute the duty cycle D;

3 – Assuming a realistic value for λ (typically something in the range 1–5%), compute k using (1) and determine n from the static gain expression given in (20);

4 – Calculate V_{C2} and V_{C3} through (21) and (12), respectively;

5 – Define the current ripple ΔI_{Lm} and calculate L_m using (26);

6 – Define the voltage ripples ΔV_{C1}, ΔV_{C2} and ΔV_{C3} and compute C_1, C_2 and C_3 using (27), (28) and (29), respectively.

TABLE 2. Design specifications for the 400 W prototype.

	Description	Value
V_{in}	Input Voltage	48 V
f_s	Switching frequency	90 kHz
P_o	Output power	400 W
V_o	Output Voltage	400 V
λ	Leakage factor	2 %
V_{C1}	Voltage on C_1	150 V
ΔI_{Lm}	Current ripple in L_m	40 % of I_{in}
ΔV_{C1}	Voltage ripple in C_1	5 % of V_{C1}
ΔV_{C2}	Voltage ripple in C_2	1 % of V_{C2}
ΔV_{C3}	Voltage ripple in C_3	1 % of V_{C3}

TABLE 3. Specified parameters.

Parameter	Value
n	1.72
D	0.68
k	0.98
L_m	80 μH (E42/15) → n_p=14; n_s=24
C_1	1 μF
C_2	4.4 μF
C_3	4.4 μF

Following the previous steps and applying the design specifications presented in Table 2, the converter parameters presented in Table 3 can be found.

VI. DYNAMIC MODEL

In practical applications, the proposed converter must operate in closed loop to ensure that some desired control output (e.g., input current or output voltage) be properly regulated. For instance, in typical grid-tied PV systems, the step-up dc-dc converter is responsible for adjusting its input current (or input voltage) to realize the maximum power point tracking (MPPT) algorithm. Therefore, the behavior of the circuit under transient conditions must be well understood, so the designer is able to determine an adequate compensator for proper closed-loop operation. In this work, a small-signal model is derived based on the operating stages depicted in Fig. 2. The technique used in this analysis is based on the Taylor's series expansion of the non-linear set of equations given in (2)–(14), considering the rated output power condition as the quiescent point. However, since the algebraic solution of the dynamic analysis is very extensive, only the resulting transfer function of the input current versus duty cycle considering the data shown in Tables 2 and 3 is presented, as given in (31).

$$\frac{\widehat{i}_{in}(s)}{\widehat{d}(s)} = \frac{6.5 \times 10^6 s^2 + 7.5 \times 10^{11} s + 1.3 \times 10^{15}}{3.56 s^3 + 4 \times 10^5 s^2 + 9.95 \times 10^8 s + 2.54 \times 10^{13}} \tag{31}$$

In this study, the input current is chosen to be controlled, and the control scheme follows the block diagram depicted in Fig. 5. Here, a simple proportional-integral (PI) compensator is enough to ensure stability and proper response of the system in closed-loop operation. Using the transfer function (31) and considering requirements of an overshoot lower than 20% and a zero-crossing frequency of 1.7 kHz, it is possible to determine the proportional and integral gains of 0.005 and 15, respectively. This yields a controller's transfer function composed of a pole at the origin, a zero at 477.46 Hz and a gain of 15, as given by (32). The controller is implemented using the digital signal processor TMS320F28377S and the current is measured with the Hall effect current transducer LAH 25-NP. Fig. 6 depicts the converter response in closed-loop operation for steps changing the input current reference from 8.4–9.4 A and 9.4–8.4 A

$$C(s) = 15 \cdot \frac{(3.333 \times 10^{-4} s + 1)}{s} \tag{32}$$

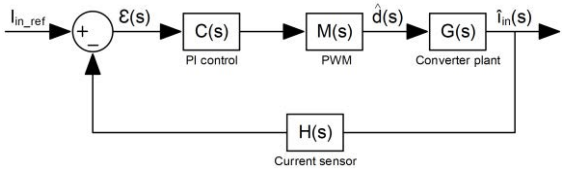


FIGURE 5. Block diagram of the control strategy.

VII. EXPERIMENTAL RESULTS

A 400 W prototype of the proposed converter using the data presented in Tables 2 and 3 was built to verify the feasibility of the proposed converter. A picture of the experimental setup is shown in Fig. 7.

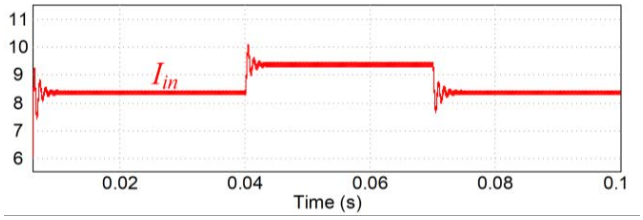


FIGURE 6. Response in closed-loop operation for steps changing the input current reference from 8.4–9.4 A and 9.4–8.4 A.

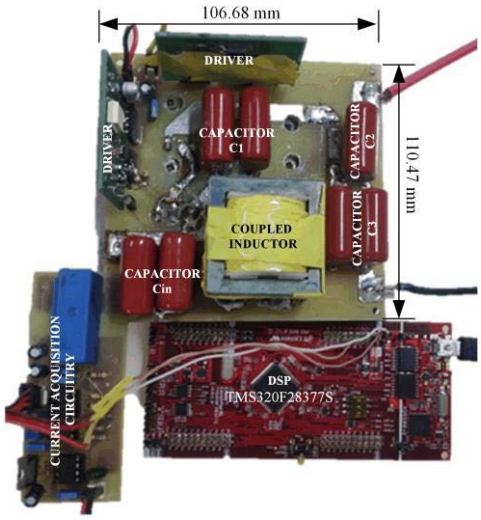


FIGURE 7. Picture of the 400 W prototype built for the experimental tests.

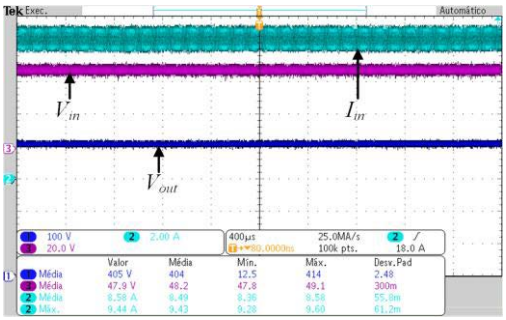


FIGURE 8. Input voltage and current and output voltage. (Scales: CH1 = 100 V / div; CH2 = 2 A / div; CH3 = 20 V / div; t = 400 μs / div.)

Fig. 8 presents the waveforms of the input voltage, input current and output voltage. The input current corresponds to the signal measured before the decoupling capacitor C_{in}, and hence some filtering is achieved.

The voltages on C_1, C_2 and C_3 are shown in Fig. 9. The measurements indicate that the experimental results are in agreement with the theoretical predictions given in (21)–(23). The waveforms of the voltage and current on S are shown in the Fig. 10. As expected, the blocking voltage corresponds to the value of V_{C1} defined by (23). Fig. 11 presents the

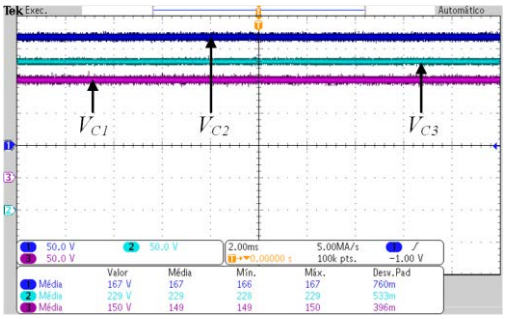


FIGURE 9. Voltages on C_1, C_3 and C_2. (Scales: v = 50 V/div; t = 4 ms/div.)

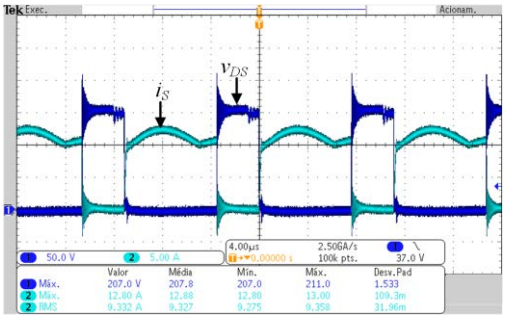


FIGURE 10. Voltage and current on the switch S. (Scales: CH1 = 50 V / div; CH2 = 5 A / div; t = 4 μs / div.)

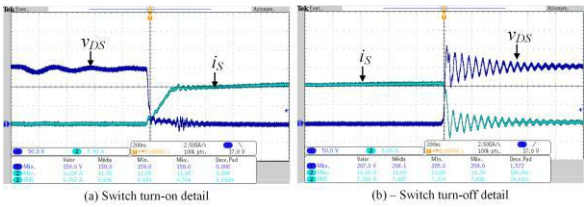
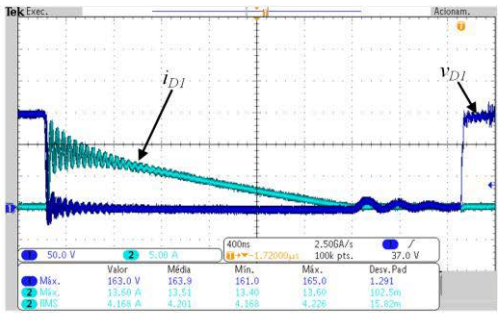
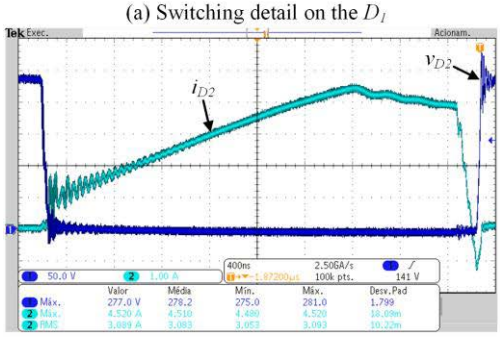


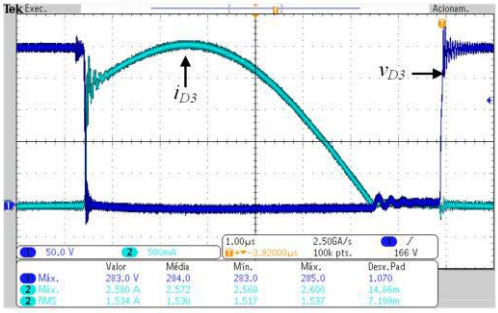
FIGURE 11. Switching intervals for switch S: (a) turn-on; (b) turn-off. (Scales: v = 50 V / div; i: = 5 A / div; t = 200 ns / div.)



(a) Switching detail on the D_1



(b) Switching detail on the D_2



(c) Switching detail on the D_3

FIGURE 12. Voltage and current on D1, D2 and D3. (Scales: on D1 CH1 = 50 V / div; CH2 = 5 A / div; on D2 CH1 = 50 V / div; CH2 = 1 A / div; on D3 CH1 = 50 V / div; CH2 = 500 mA / div t = 1 μs / div.)

turn-on/turn-off transient intervals regarding S. Even though ZVS is not achieved, the turn-on loss is low because there is almost no simultaneous current and voltage during this interval. Fig. 12 shows the waveforms of the voltage and current on D_1, D_2 and D_3, respectively. It can be observed that the blocking voltage values are close to those defined by (23) and (30). In addition, zero-current-switching (ZCS) is verified for D_1 and D_3 and it is noticeable that the turn-on loss on D_2 is low, thus contributing to enhancing the overall converter efficiency.

Fig. 13 presents the system efficiency measured with a Yokogawa WT500 precision power analyzer. Fig. 13 (a) illustrates the efficiency curve as function of the variation of the output power. Values of 96.5% and 97.5% at 100% and 20% of the rated output power, respectively, have been achieved by the proposed high step-up converter.

In applications in which nominal power is maintained while the input voltage is reduced, the proposed converter presents efficiency levels according to Fig. 13 (b). As expected, efficiency is also reduced as the input voltage decreases due to higher current stresses. However, a more realistic condition is to consider that the output power is also reduced for lower input voltage conditions, which leads to a lower efficiency drop at low voltage levels, as shown in Fig. 13 (c).

It is noteworthy that an unusual behavior on the efficiency curve can be observed in Fig. 13 (a) at 20% of rated output power, which is a consequence of better switching conditions due to operation in the discontinuous conduction mode. This improved operating condition can be verified by the drain-to-source (v_{DS}) and gate-to-source (v_{GS}) voltages on the MOSFET at 20% of output power, as shown in Fig. 14. As can be seen, at this particular operating point, the switching occurs at zero voltage (ZVS), which can be explained by the fact the converter enters in the discontinuous conduction mode and the turn-on of the MOSFET occurs at the valley of the resonant transition occurring after L_m is completely discharged.

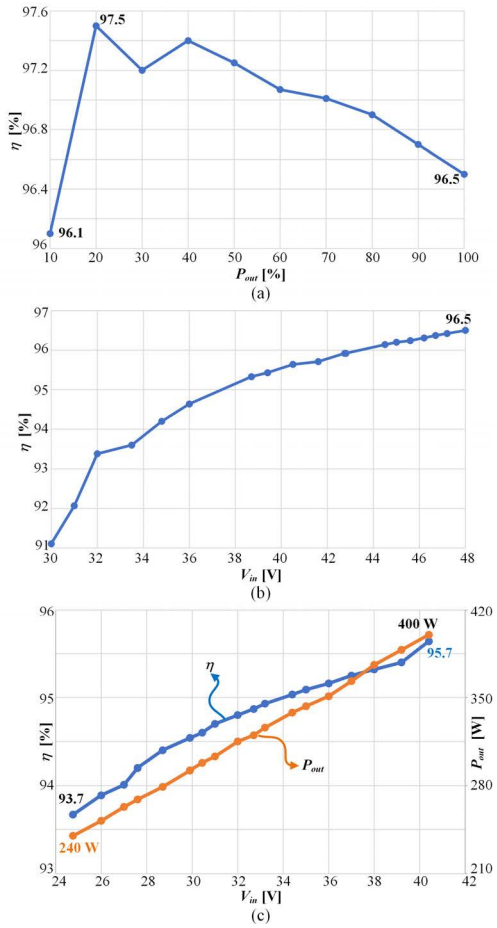


FIGURE 13. Efficiency measurements: (a) as function of output power; (b) as a function of input voltage with Po = 400 W; and (c) as function of input voltage and output power.

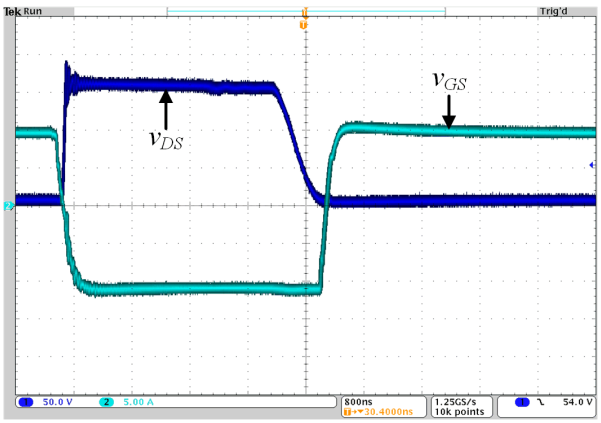


FIGURE 14. Drain-to-source (V_{DS}) and gate-to-source (V_{GS}) voltage on the MOSFET at 20% of rated output power.

Operation at 10% of rated output power was also investigated and the waveforms of voltage and current on S are provided in Fig. 15 for this condition.

Finally, proper closed-loop operation is demonstrated in Fig. 16, which depicts the response of the input current

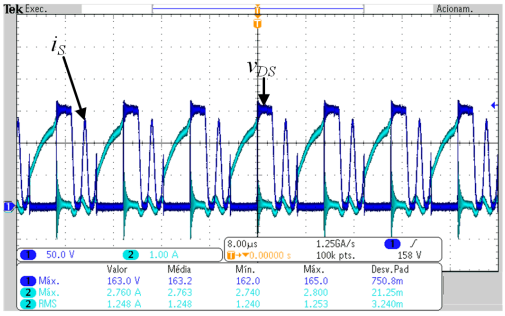


FIGURE 15. Current and voltage on the switch S for 10% of rated output power. (Scales: v = 50 V / div; i: = 1 A / div t = 8 μs / div.)

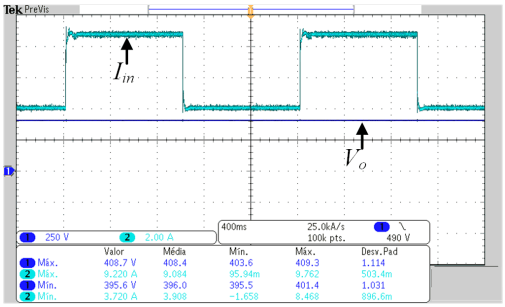


FIGURE 16. Dynamic response of the system for input current disturbances from 4 A to 8.5 A and from 8.5 A to 4 A. (Scales: v = 100 V / div; i: = 5 A / div t = 200 ms / div.)

for 4–8.5 A and 8.5–4 A reference steps with the output voltage fixed at 400 V. For this test, the constant voltage load was implemented using the 4-quadrant ac-load NHR 9430.

VIII. CONCLUSION

This paper introduced a single-switch high-voltage-gain dc-dc converter based on the boost converter employing coupled inductor and voltage multiplier cell. The main advantages of the proposed topology are high efficiency, natural voltage clamping in all semiconductors and reduced component count. Both static and dynamic analyses were detailed in the paper, and a comprehensive design methodology was proposed to ensure proper closed-loop operation. The feasibility of the converter was demonstrated through experimental tests with a 400 W prototype operating with a voltage conversion ratio in the range of 8.33–13.33 and a switching frequency of 90 kHz. Measurements indicated a maximum efficiency of 97.5% at approximately 80 W and an efficiency level of 96.5% at nominal conditions. It is also remarkable that the efficiency is higher than 96% for the entire range of 10–100% of rated output power. Based on the results, the proposed converter shows itself as a good candidate for typical single-module PV applications, in which voltage levels in the order of tens of Volts and power levels up to several hundreds of Watts are usual.

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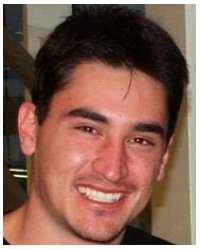

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