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RESEARCH ARTICLE

Benchmark Figure of Merit Extensions for Low Jitter Phase Locked Loops Inspired by New PLL Architectures

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ABSTRACT A conventional figure-of-merit (FOM) for a phase-locked loop (PLL) has served as the most powerful indicator to compare and to normalize performance of different PLL designs. Simply, the conventional FOM is based on the jitter-power trade-off. With a few assumptions, theoretically, it provides a fair comparison. However, as the PLL design techniques have advanced, the assumptions have started breaking. Also, it misses performance impacts from some other important factors other than the jitter and the power. As a result, it is expected that the performance comparison with the conventional FOM is not fair enough for some cases. This work reviews the state-of-the-art PLL design techniques and investigates how those techniques conflict with the assumptions of the conventional FOM. In addition, alternate FOMs which complement the conventional FOM are discussed. To capture complex cross-correlation between various factors, the proposed methodology is to find a correlation between the conventional FOM and other factors from extensive performance surveys, along with quantitative analyses.

INDEX TERMS All-digital PLL, clock-multiplying DLL, figure-of-merit, injection-locked PLL, jitter, PLL, sub-sampling PLL.

I. INTRODUCTION

Figure-of-merit, FOM, is widely used in various fields of engineering, to evaluate the performance of a design and to provide a fair comparison between different designs with a single number. Ever since the FOM of a phase-locked loop (PLL) based on the PLL jitter-power trade-off (FOM_J, or FOM_{jitter}) has been proposed by Gao *et al.* [1], it has widely adopted to evaluate the PLL performance. The FOM_J is simply calculated from the RMS jitter and power consumption of a PLL as

$$FOM_J = 10\log\left(\left(\frac{\sigma_{rms}}{1s}\right)^2\left(\frac{P_{PLL}}{1mW}\right)\right), \quad (1)$$

where σ_{rms} and P_{PLL} are the RMS jitter and power consumption of a PLL, respectively. Note that the RMS jitter is generally obtained by integrating PLL phase noise by 3∼5 decades of frequency range, while the PLL loop bandwidth locates within the range. In fact, FOM_J is based on the following assumptions:

1. reference clock phase noise is negligible,
2. the PLL phase noise is divided to in-band phase noise and voltage-controlled oscillator (VCO) phase noise,
3. the in-band phase noise and the VCO phase noise are inversely proportional to the circuit power consumption,
4. and the PLL loop bandwidth is set to the optimum where the in-band noise and the VCO phase noise are balanced, while the VCO and the other in-band-noise contributors consume equal power.

Due to its simplicity and solid theoretical backgrounds, the FOM_J has been regarded as the most powerful metric to evaluate a PLL performance, as a result almost all PLL papers have advertised their FOM_J ever since the FOM_J was proposed in [1]. In addition, as implied from the survey from *IEEE International Solid-State Circuits Conference* (ISSCC) and *IEEE Symposium on VLSI Circuits* (VLSI) publications

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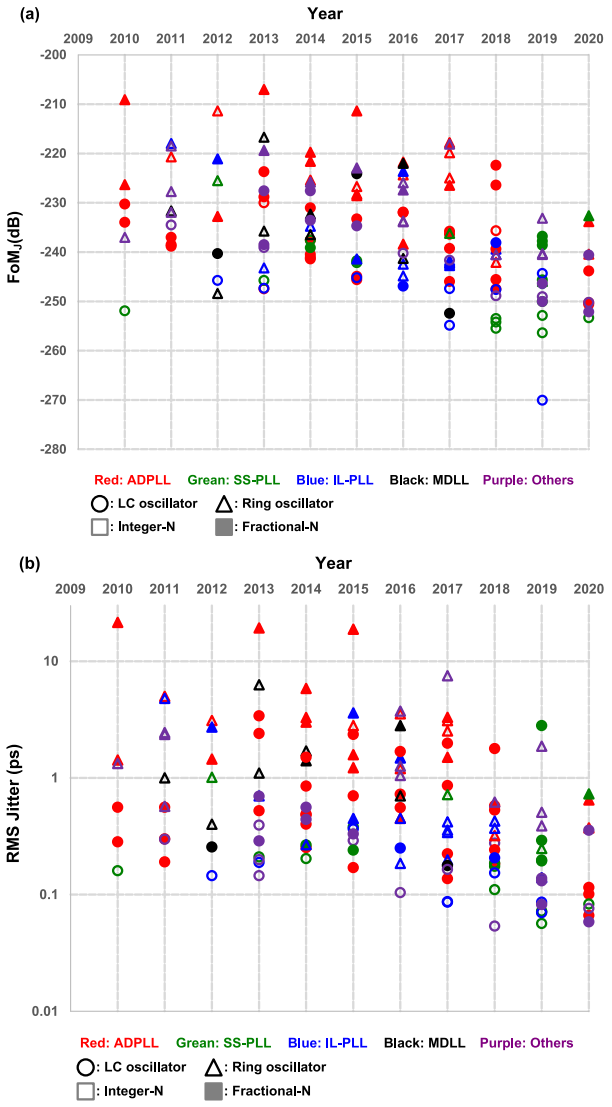

FIGURE 1. (a) Survey of PLL FOM$_J$ over years. (b) Survey of PLL RMS jitter over years.

in 2010–2020 in Fig. 1(a) [2]–[144], where FOM$_J$ survey over the years are presented, achieving a better FOM$_J$ has been one of the most important goals for the PLL designers.

However, although those assumptions used to be reasonable, they have started breaking as PLL design techniques have been evolving. For example, the PLL jitter has been improved down to sub-100-fs$_{rms}$ era, as shown in Fig. 1(b), owing to many advanced circuit techniques to suppress the jitter generation of the PLL building blocks, and therefore the reference phase noise is no longer negligible [145]. In addition, especially for ring-PLLs, the assumption 4 is rarely met because the required bandwidth generally exceeds the stability limit (∼1/10 of the reference frequency) due to the poor phase noise of ring VCOs [146]. That is, for the cases where the assumptions are broken, the FOM$_J$ would be less informative compared to the other cases. In addition to the break of the assumptions, it does not consider other impact from various factors other than jitter and the power consumption, such as

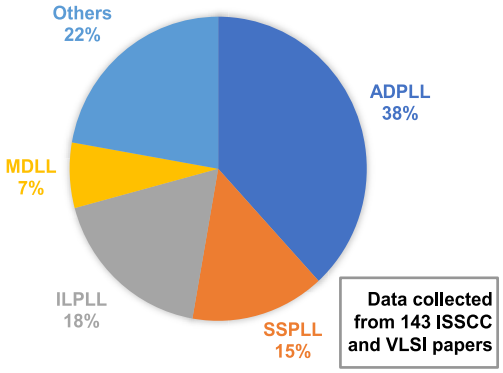

FIGURE 2. Breakdown of state-of-the-art PLL designs.

silicon area or process technology node. As a result, new benchmark FOMs are required to complement the limitations of the FOM$_J$ [147].

The remainder of this paper is organized as follows. Section II briefly reviews the state-of-the-art PLL design techniques for low-jitter performance. Extensive literature surveys are provided in Section III, where we find useful insights and interesting trends. Based on the observations, several alternative FOM candidates are also discussed in Section III. In Section IV, a couple of comprehensive FOM candidates are discussed and validated. Finally, conclusions are provided in Section V.

II. REVIEW OF STATE-OF-THE-ART DEISGN TECHNIQUES

In this section, recent advanced circuit techniques for improving PLL performance will be reviewed. The focus of this section is not to enumerate detailed implementation examples and performance, but to provide an overview of those techniques, e.g., how those techniques reduce the phase noise or what challenges they aim to overcome. In addition, we will discuss why the assumptions of FOM$_J$ break with those techniques. This section introduces the advanced PLL design techniques named all-digital PLL (ADPLL), subsampling PLL (SSPLL), injection-locked PLL (ILPLL), and clock-multiplying DLL (MDLL), which are the most popular PLL design techniques in recent *ISSCC/VLSI* publications, as shown in the survey in Fig. 2 [147].

A. ALL-DIGITAL PLL (ADPLL)

As analog performance of critical building blocks of conventional PLLs has been degrading due to digital-friendly scaled process and reduced voltage headroom, all-digital PLL (ADPLL) where analog components are replaced by digital equivalents has been introduced [148], [149]. Because of their digital-oriented nature, performance of ADPLLs benefits from scaled CMOS process [2], [6], [9].

Fig. 3 briefly illustrates the transformation of a ADPLL from a conventional PLL, where the phase detector (PD), analog loop filter (LF), and VCO are replaced with a time-to-digital converter (TDC), a digital LF, and a digitally-controlled oscillator (DCO), respectively. Simply,

the motivation of ADPLL is to utilize intensive digital logic for information processing and loop control, in order to overcome the drawbacks of analog LFs and to integrate complex functionalities in a small area. As a result, there are analog-to-digital (TDC) and digital-to-analog (DCO) interfaces which bridge the analog signals and the digital processing. However, they introduce quantization noises which are not present in analog PLLs and reduce the benefit of the digital implementation.

B. SUB-SAMPLING PLL (SSPLL)

In conventional PLLs, in-band phase noise (e.g., PD, charge pump, and reference noise) is amplified by 20logN where N is the frequency division ratio [4]. To suppress the in-band phase noise, a SSPLL utilizes a sub-sampling phase detector (SSPD), which is simply a sample-and-hold circuit followed by a V-I converter, to eliminate the frequency divider from the feedback path as shown in Fig. 4. In an equivalent phase-domain linear model, the division factor does not disappear but is placed at the input instead of the feedback path. That is, the noise from the PD or the charge pump does not meet N in its transfer function. Note that the reference phase noise is still amplified by a factor of 20logN. As a result, more than 20-dB in-band noise suppression is generally expected with a SSPLL compared over a conventional PLL with a practical design parameters based on the analysis given in [150]. Therefore, SSPLL techniques are more frequently adopted in LC-based PLLs over ring-based PLLs where the in-band noise is less important due to the dominant ring-VCO noise. For example, the survey shows 17 LC-based SSPLLs [4], [36], [46], [47], [58], [59], [106], [107], [115], [118], [119], [123], [124], [126], [127], [133], [140] but only 4 ring-based SSPLLs [11], [91], [120], [141]. On the other hand, because of the nature of the SSPD, a SSPLL does not distinguish harmonic frequencies, so it needs a separate frequency tracking loop.

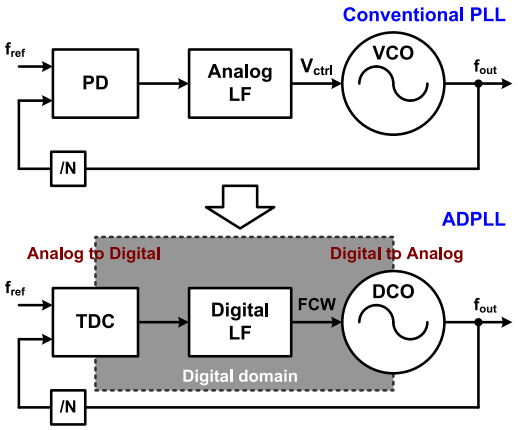

FIGURE 3. All-digital PLL versus conventional PLL.

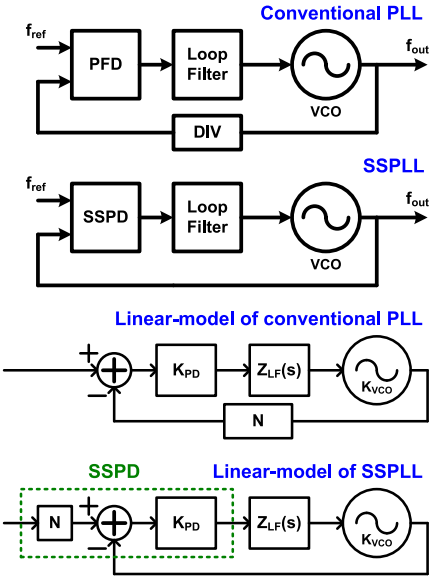

FIGURE 4. Sub-sampling PLL versus conventional PLL.

C. INJECTION-LOCKED PLL (ILPLL)

Injection locked oscillator (ILO) refers to a phenomenon that a periodic charge injection to an oscillator introduces a frequency shift to free-running frequency of the oscillator. In specific, if the offset (f_{off}) between the injection frequency and the free-running frequency (f_{free}) is within a lock range, the oscillator locks to the injected frequency rather than free-running. Because an ILO provides a high jitter-tracking bandwidth (JTB, theoretically up to 1/2 of f_{ref} depending on injection strength [8], [22], [151]) which is much higher than that of a conventional PLL. In other words, its capability to clean up VCO phase noise is much higher than that of a conventional PLL. Reference-clock multiplier techniques can even boost the capability [152], [153]. However, many on-chip variations do not guarantee that a standalone ILO stays in the lock range, and a residual f_{off} degrades jitter performance and causes a huge reference spur [8], [21]. In addition, the first-order filtering of an ILO is not enough to suppress $1/f^3$ phase noise of a VCO [155]. The ILPLL, which combines the ILO technique with a PLL as shown in Fig. 5(a), addresses the issues of the standalone ILO. By introducing a direct injection path to a conventional PLL, it achieves a stronger phase realignment by the reference injection while the PLL loop keeps the frequency in the lock range and provides a better suppression of $1/f^3$ noise thanks to a higher-order loop. On the downside, two separate realignments by the PLL and the injection collides, causing a large reference spur as well as degrading the jitter performance [21], [25]. Therefore, an additional calibration is required to minimize the collision by aligning two paths.

D. CLOCK-MULTIPLYING DLL (MDLL)

Fig. 5(b) shows a simplified block diagram of a MDLL. The reference clock edge is directly fed to a voltage-controlled delay line (VCDL) by the selection logic and multiplexer (MUX). For the time period where there is no reference edge, the selection logic configures the VCDL to a VCO by activating a feedback path of the MUX so that the VCO oscillates

based on the reference edge [14], [17]. The first-order loop controls delay of the VCDL to achieve frequency lock. Contrary to the conventional PLLs and the ILPLLs, the clock edge is fully replaced by the reference edge so that the accumulated jitter of the VCO is completely refreshed. Comparing with the ILPLL, an ILPLL injects the reference edge while VCO keeps running whereas MDLL injects the edge after cutting the oscillator. As a result, an MDLL can be regarded as an ILPLL with an ideal injection strength, and therefore it provides an ultra-high JTB of $f_{ref}/2$. On the other hand, the MDLL loop controls only frequency with the first-order loop, in contrast to a PLL where both phase and frequency are controlled with a proportional-integral loop filter. As a result, any mismatch between the reference path and the feedback path results in a frequency offset, which causes a large reference spur. Therefore, similar to the ILPLLs, additional calibrations are required to compensate the mismatch.

Fig. 5(c) and (d) illustrate the clock jitter comparison of a conventional PLL, an ILPLL, and a MDLL when the reference clock or the VCO is ideal (no jitter), respectively, while neglecting non-idealities (e.g., injection collision, path mismatch) other than the JTB. In the first case, because a VCO keeps accumulating jitter unless there is a realignment by a reference clock edge, the clock jitter increases until the next reference edge rises. In the conventional PLL, the realignment is fully driven by the feedback loop, so the realignment factor is constraint by the loop stability [146]. It leads to a substantial residual jitter. In the ILPLL, there is another direct realignment by the injection, so the realignment is stronger than that of PLLs. However, the reference edge is injected while the VCO is still running, which limits the realignment factor by the relative strength of the injection over the VCO strength. In the MDLL, the realignment is ideal because it happens when the oscillation is disabled, and therefore the accumulated jitter is fully refreshed by the reference edge. On the other hand, if the reference clock is noisy but the VCO is ideal (Fig. 5d), the MDLL provides no filtering on that. The ILPLL offers some depending on the realignment factor, but the PLL gives the strongest filtering.

E. DISCUSSION

Here are a few remarkable observations from the advanced PLL design techniques; first, the reference clock phase noise is no longer negligible to the in-band noise, because the in-band noise generation has been significantly reduced, for example the SSPLLs. Second, from the examples of the ILPLLs and MDLLs, there have been huge efforts to extend the PLL JTB to suppress the VCO phase noise, since the optimum JTB is frequently too high due to excessive VCO noise. That means a higher reference frequency, or a lower division factor can reduce the PLL jitter. Third, the ADPLLs enable a compact loop filter but introduce quantization noise, emphasizing the area-jitter trade-off, which also exists in other PLL designs. From the observations, it can be concluded that the FOM_J would not provide a fair comparison for some cases and would be missing performance impacts from some important factors. Therefore, it is a good time to explore new FOMs which can complement the FOM_J.

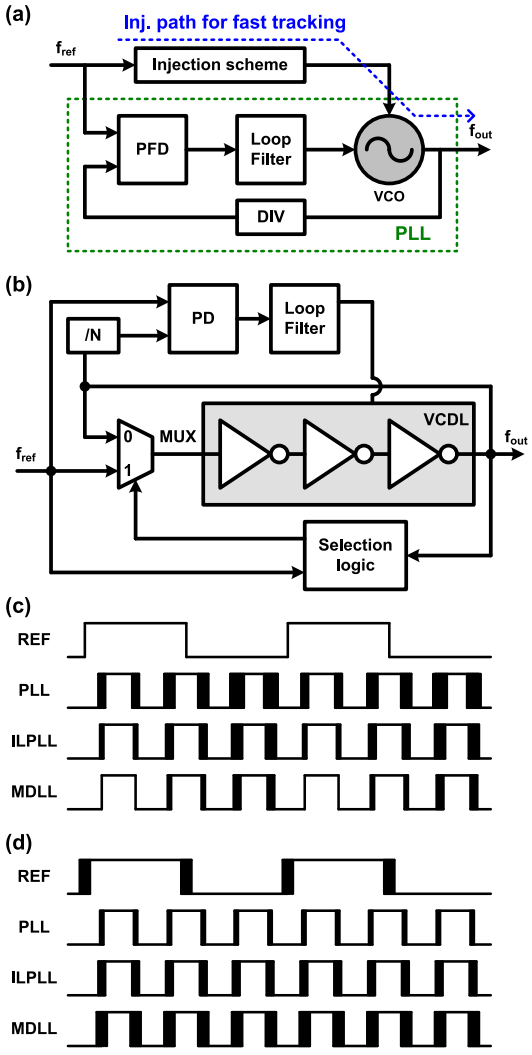

FIGURE 5. (a) Simplified block diagram of ILPLL, (b) simplified block diagram of MDLL, (c) clock jitters of PLL, ILPLL, and MDLL when reference clock is ideal, (d) clock jitters of PLL, ILPLL, and MDLL when oscillator is ideal.

III. PERFORMANCE SURVEY AND TREND, PROPOSALS FOR NEW COMPLEMENTARY FOMS

Basically, a FOM should precisely capture the dependencies on different factors to provide a fair comparison across different designs, for example the FOM_J captures the linear dependency of the PLL power consumption and the square of the RMS jitter. In this section, this work tries to capture various dependencies from extensive survey of state-of-the-art PLL publications in last ten years, since it is generally hard to capture such cross-correlation between various factors only with theoretic approaches. Because the FOM_J already captures the jitter-power trade-off of a PLL, the base approach is to find a correlation between the FOM_J and other factors, in order to capture the dependencies of the jitter/power to other parameters. During the analyses, the dependencies are

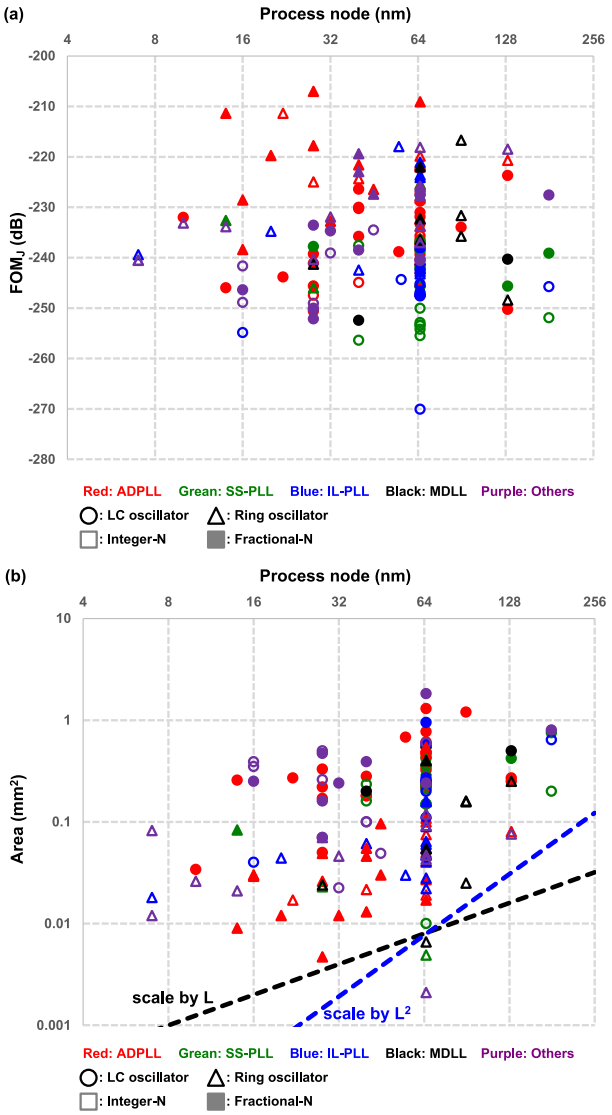

FIGURE 6. (a) Survey of FOM_J versus process node, (b) survey of area versus process node.

extracted among the top-performing designs [154], which are assumed to be less affected by physical constraints (e.g. area [61], [88], [91], [106], [120], [124]). In addition, to avoid use of complex FOM expressions for simplicity, the trends are approximately extracted from a few representative trendlines such as 10 dB/decade or 20 dB/decade slopes.

A. IMPACT OF PROCESS SCALING

Fig. 6(a) shows the FOM_J trend with respect to the process technology scaling. Indeed, the scaling helps to enhance the power consumption and speed. However, at the same time, it has negative impacts on the noise performance of analog building blocks of a PLL. Based on the survey in Fig. 6(a) where no evident trend is observed, such upsides and downsides seem to balance each other. It is also notable that the 65-nm process has been the most popular (70 out of 143 works), and the best FOM_J was also achieved at the 65-nm node [129].

On the other hand, the process scaling does show an impact on the silicon area reduction. Fig. 6(b) shows the survey of PLL area versus process node. Neglecting the data points at the 65-nm where almost half of the efforts have been focused to improve the designs in that node, it shows a trend that the area has been shrunk with the process scaling, regardless of the ring- and the LC-PLLs. In addition, it is also observed that the ring-based ADPLLs are leading the area scaling because they take full advantage of the process scaling.

Some researchers try to normalize the area with the process node to compensate their handicap of using old technology. Because a unit transistor area scales by a factor of L^2 (or λ^2), the factor of L^2 is generally used to normalize the area, where L is the minimum transistor length of the process [78]. However, the scaling of analog circuits is different to that of digital circuits, for example the voltage scaling hurts the analog performance [155], [157]. As a result, the scaling trend observed in Fig. 6(b) is closer to scaling by a factor of L, especially for the process nodes after 65 nm. Therefore, the following formula is suggested to normalize the area with the process node.

$$Area_{norm.} = \frac{Area}{L}. \tag{2}$$

Note that $L^{1.5}$ can be a potential alternate for some special cases depending on the fabrication process and the amount of digital implementation.

B. IMPACT OF SILICON AREA

Silicon area is one of the important resources, however it is not reflected in FOM_J. Evidently if a PLL consumes more resources then it will achieve a better performance, however it is hard to tell theoretically how much the impact is. For example, LC-PLLs provide better performance over ring-PLLs because an LC-VCO exhibits much better phase noise (>20dBc/Hz) at comparable power consumption, whereas LC-PLLs occupy much more silicon area. As a result, the ring-PLLs are generally adopted for area-compact specifications whereas the LC-PLLs are used in high-performance jitter applications [158]–[160]. Therefore, generally the LC-PLLs and the ring-PLLs are not directly compared. However, it is very difficult to theoretically include the impact of area in a FOM, because there are so many factors that affect the area, especially for LC-PLLs. As a result, it is worthwhile to try a survey-based investigation to address the area dependency, which is shown in Fig. 7, where a trend of FOM_J with respect to the silicon area of PLLs is shown. We observe around -10 dB/decade trendline where LC-PLLs and ring-PLLs stand together, when we neglect three outliers under the trendline. It implies that including a linear area dependency on a PLL FOM can be a good alternative to fairly reflect the area consumption.

$$FOM_{JA} = 10\log\left(\left(\frac{\sigma_{rms}}{1s}\right)^2\left(\frac{P_{PLL}}{1mW}\right)\left(\frac{Area}{1mm^2}\right)\right). \tag{3}$$

On the other hand, from Fig. 7 as well as Fig. 6(b), it is observed that ADPLLs are leading the smallest area race although they show relatively worse FOM_J over other techniques, so including area into FOM would reevaluate ADPLLs. Similarly, the ADPLLs that are marking the worst FOM_J in the Fig. 6(a) are leading the area competition in the Fig. 6(b).

C. IMPACT OF DIVISION FACTOR N AND REFERENCE CLOCK FREQUENCY

As discussed, the conventional FOM_J has a limitation that it does not reflect any impact from the reference clock. Because of many advanced design techniques like the SSPLLs, PLL jitter generation keeps improving, so the reference noise becomes no longer negligible. On the other hand, the ILPLLs and the MDLLs pursue a higher tracking of reference noise, so a higher reference frequency offers a higher tracking bandwidth. In other words, the PLL jitter performance starts being constrained by the reference noise, while the reference noise is amplified by 20logN. For example, if the PLL jitter is constrained by the VCO noise, a higher reference frequency is very effective to suppress the noise because the high-pass cut-off frequency is proportional to the reference frequency, either of ILPLL/MDLLs ($f_{ref}/2$) or conventional PLLs ($f_{ref}/10$). In addition, the FOM_J assumes that the noise and power consumption of the divider is negligible.

Fig. 8(a) and (b) show the FOM_J trend of ring-PLLs and LC-PLLs with respect to the division factor, respectively. Since a ring-PLL typically shows ∼20 dB worse FOM_J due to poor phase noise of a ring oscillator, they are depicted in separate plots. For both cases, a slope of ∼10dB/decade is observed, implying that FOM_J has a linear dependency on the division factor N regardless of the oscillator type. Therefore, another FOM metric which includes the impact of N can be introduced as

$$FOM_{JN} = 10\log\left(\left(\frac{\sigma_{rms}}{1s}\right)^2\left(\frac{P_{PLL}}{1mW}\right)\left(\frac{1}{N}\right)\right), \quad (4)$$

which has been already adopted in some of the previous publications [111], [119], [135], [155]. Fig. 9, where a survey of FOM_{JN} with respect to area is shown, supports justifying the use of FOM_{JN} over FOM_J. Comparing to the result in Fig. 7 (FOM_J vs. area) which shows three outliers, it has only one SSPLL outlier with a reduced outlining amount [106]. Considering that the focus of [106] is to minimize the area by placing all building blocks underneath of the inductor, we can conclude that the FOM_{JN} is able to normalize the overestimated FOM_J by a low N.

Similar trend is observed in the f_{ref} dependency survey, because for typical cases, increasing f_{ref} is almost equivalent to decreasing N. For example, if all other parameters are fixed, a higher f_{ref} is identical to a lower N. Even though PLL frequencies are different, they are also identical as long as their bandwidths are at the optimum. For example, when the PLL frequency is doubled while the f_{ref} is doubled, we can assume that the power consumption is also doubled.

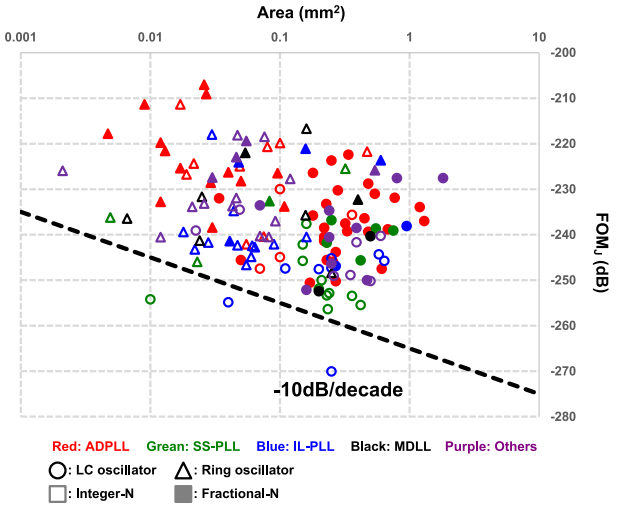

FIGURE 7. Survey of FOM_J with respect to the PLL area.

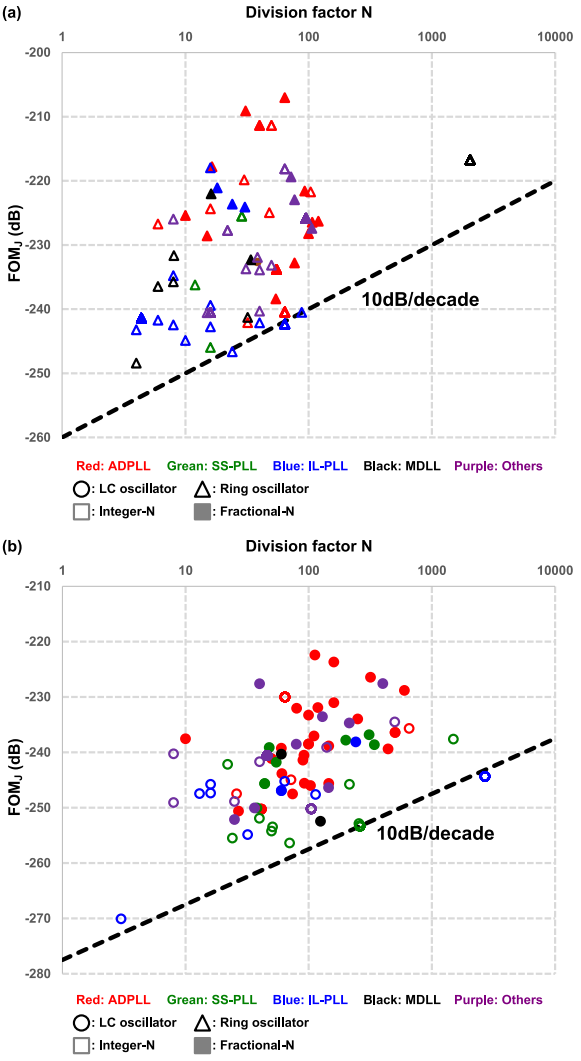

FIGURE 8. Survey of FOM_J with respect to the division factor for (a) ring-PLLs and (b) LC-PLLs.

Of course, the division factor stays the same. Then, both the in-band and VCO phase noises are expected to increase by

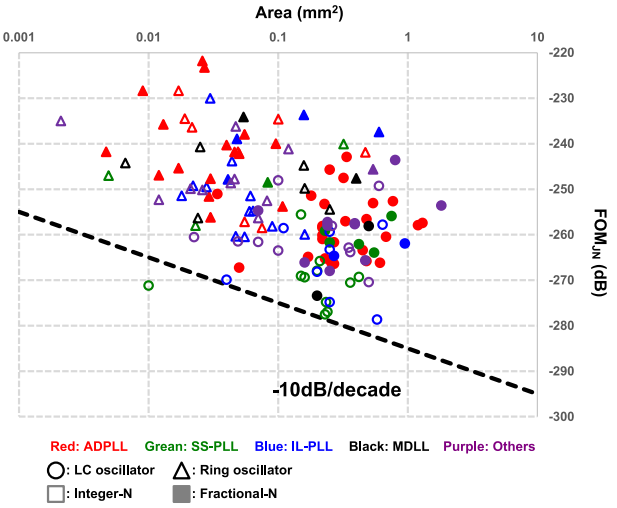

FIGURE 9. Survey of FOM_{JN} versus area.

3 dB, as shown in Fig. 10(a), since they are proportional to the square of the clock frequency and inversely-proportional to the power consumption [1]. As a result, the RMS jitter increases by $\sqrt{2}$, resulting the same FOM_J. On the other hand, however, the FOM_J deviates if the PLL bandwidth is constrained by the f_{ref}. Fig. 10(b) illustrates such case, where a higher f_{ref} helps to suppress the excessive VCO noise. Note that ILPLLs, MDLLs, and some SSPLLs (due to the reduced in-band noise) usually fall into such bandwidth-constrained or dominant-VCO-noise cases. In other words, for the majority of the state-of-the-art PLLs, the f_{ref} dependency would be super-linear, which is supported by the survey results shown in Fig. 11(a) and (b), where the f_{ref} dependency of FOM_J are surveyed for ring-PLLs and LC-PLLs, respectively. Unlike the results in Fig. 8, the trend is closer to -15-dB/decade slope rather than -10-dB/decade which implies that the dependency is more likely super-linear. From the observation, an alternate FOM reflecting the f_{ref} dependency can be suggested as

$$FOM_{JR} = 10\log\left(\left(\frac{\sigma_{rms}}{1s}\right)^2\left(\frac{P_{PLL}}{1mW}\right)\left(\frac{f_{ref}}{1MHz}\right)^{1.5}\right). \quad (5)$$

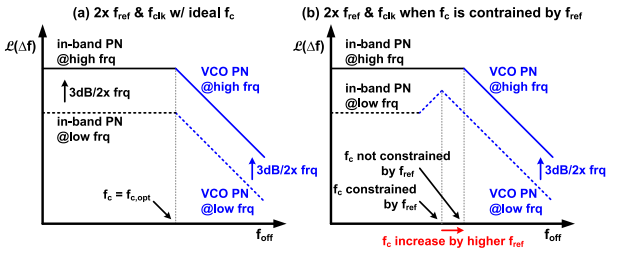

FIGURE 10. Changes in PLL phase noise when the reference frequency and the PLL clock frequency are doubled. (a) When the PLL bandwidths are at optimum, (b) when the PLL bandwidths are constrained by the reference frequency.

D. IMPACT OF REFERENCE SPUR

Another important metric for a PLL is reference spur, which results in a deterministic jitter [148]. Theoretically,

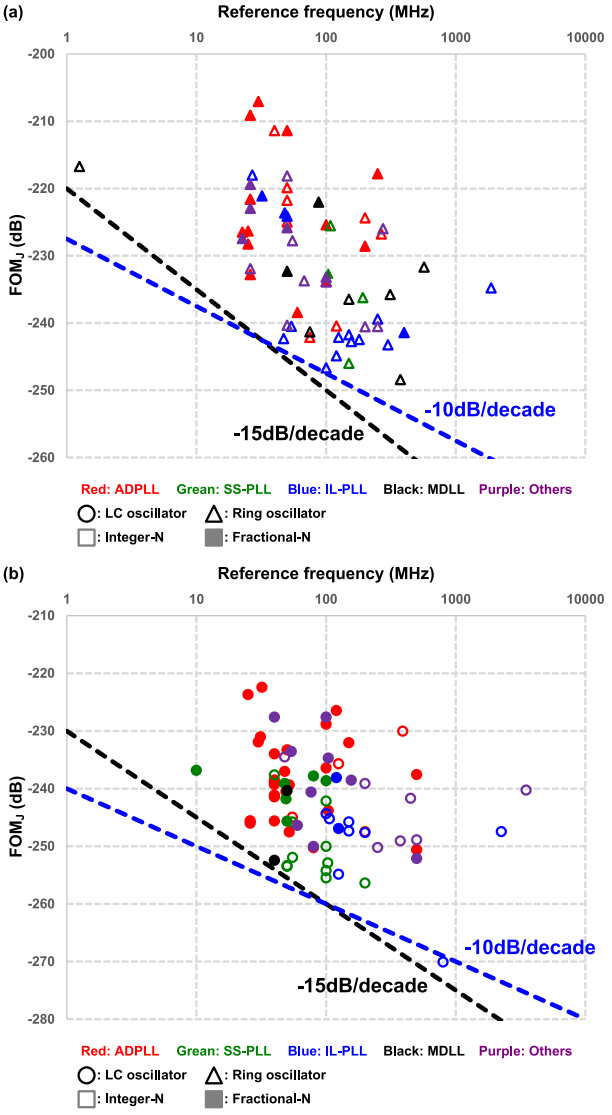

FIGURE 11. Survey of FOM_J with respect to the division factor for (a) ring-PLLs and (b) LC-PLLs.

the reference spur is proportional to $T(f_{ref})$, where T(f) is a frequency-domain open-loop transfer function of a PLL. On the other hand, the closed-loop bandwidth of a PLL, f_c, is approximately locates at the crossing point of the T(f), as shown in Fig. 12. Assuming a second-order PLL for simplicity, the slope of T(f) after f_c is -20 dB/dec because the zero (f_z) must be lower than f_c to stabilize the loop. As a result, we can rephrase that the reference spur is proportional to f_c/f_{ref}. Recalling that a higher f_c/f_{ref} plays a critical role for suppressing VCO noise, a trade-off between the VCO noise suppression and the reference spur is found, which implies that there is a trade-off with FOM_J (or FOM_{JN}). The surveys illustrated in Fig. 13 and Fig. 14 prove such trend. Note that the reference spur is generally not included in the RMS jitter integration. Fig. 13(a) and (b) show the FOM_J versus the reference spur survey for ring-PLLs and LC-PLLs, respectively. The trendline shows slope of around -10dB/20dB (-10-dB FOM_J per 20-dB spur) for both cases, which implies

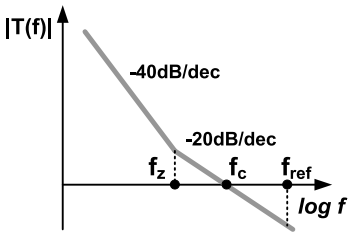

FIGURE 12. Simplified open-loop transfer function of PLL.

a sub-linear dependency. Fig. 14 shows the dependency of FOM_{JN} on the reference spur, and another −10dB/20dB slope is observed. Based on those observations, an alternate FOM can be introduced as

$$FOM_{JS} = FOM_J\ (\ dB) + \frac{Ref\ .Spur(dB)}{2}, \tag{6}$$

or

$$FOM_{JNS} = FOM_{JN}\ (\ dB) + \frac{Ref\ .Spur(dB)}{2}. \tag{7}$$

E. CLOCK FREQUENCY SCALING

For most of wireline and wireless applications, normalized jitter, the ratio of jitter over one clock cycle (or one bit period), is one of the major limiting factors that limiting the bit-error rate (BER) [161], [162]. For example, a 1-GHz clock with 1-ps RMS jitter is equivalent to a 2-GHz clock with 0.5-ps RMS jitter, in terms of BER. Therefore, it is useful to explore how the PLL FOM should scale to secure the same system-level performance, while the required speed keeps increasing.

There are three scenarios for the frequency scaling: (A) scale the frequency while keeping the same power, (B) scale the frequency while keeping the same power efficiency (mW/GHz), (C) scale the frequency while keeping the same normalized jitter. Assuming that FOM_J stays the same while doubling the frequency, the scenarios result in normalized jitter increased by (A) 2x, (B) 1.4x, and (C) 1x, while the power increased by (A) 1x, (B) 2x, and (C) 4x. The survey result provided in Fig. 15 shows a linear dependency, implying that the scaling has followed the scenario A. The assumption of FOM_J independency to the frequency can be supported by the survey shown in Fig. 16, where no evident correlation between the FOM_J and the PLL frequency is found. On the other hand, the FOM_{JN} versus PLL frequency shows a trend that the FOM_{JN} is likely to get better at a higher frequency, which is shown in Fig. 17. In other words, compared to FOM_J, the FOM_{JN} tends to give a higher credit for a higher-speed design.

From a different view, in the previous paragraph and the survey shown in Fig. 15, we observe that the trend follows the scenario A while the FOM_J has not scaled, which means that the system performance (e.g. BER) has been degrading. In order to secure the same system performance without increasing the power efficiency, we should follow the scenario C while the power efficiency stays (2x frequency, 0.5x jitter, 2x power). It is equivalent to 3-dB improvement in

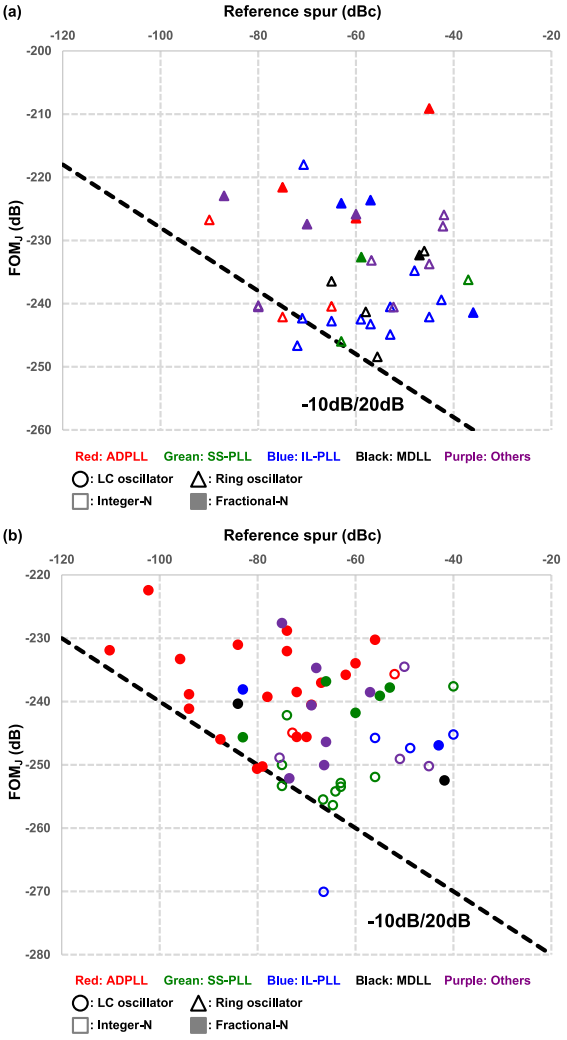

FIGURE 13. Survey of FOM_J with respect to reference spur for (a) ring-PLLs and (b) LC-PLLs.

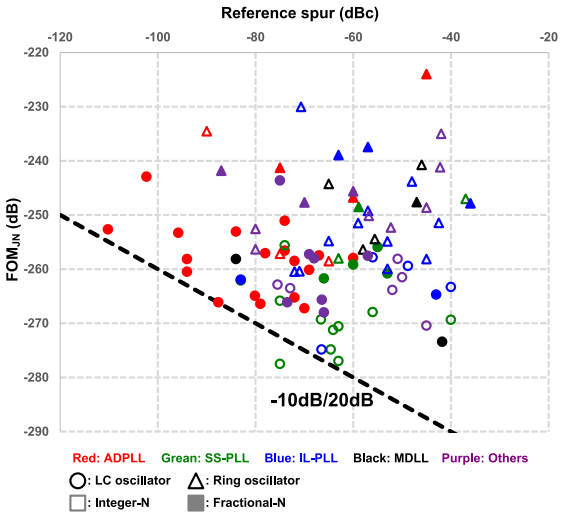

FIGURE 14. Survey of FOM_{JN} with respect to reference spur.

FOM_J while doubling the clock frequency. If we want to keep the same power consumption, it is equivalent to 6-dB

TABLE 1. Summary of section III.

Parameter	Dependent	Dependency	Eq. No.
Process node (L)	Area	$\propto$L	(2)
Area	FOM_J	$\propto 1/Area$	(3)
Division factor (N)	FOM_J	$\propto$N	(4)
Ref. freq. (f_{ref})	FOM_J	$\propto 1/f_{ref}^{1.5}$	(5)
Ref. Spur	FOM_J	-10dB/20dB	(6)

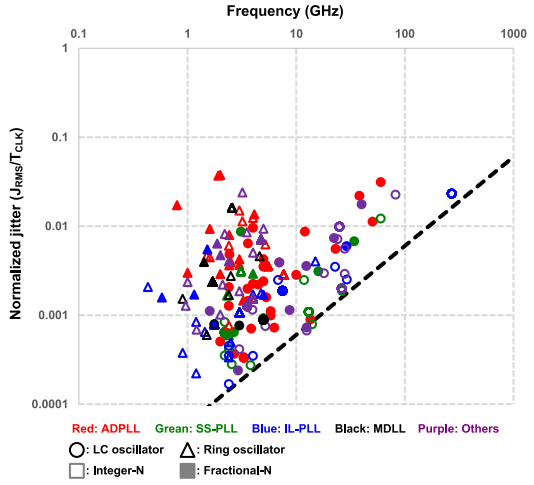

FIGURE 15. Survey of normalized jitter (J_{RMS}/T_{CLK}) with respect to PLL clock frequency.

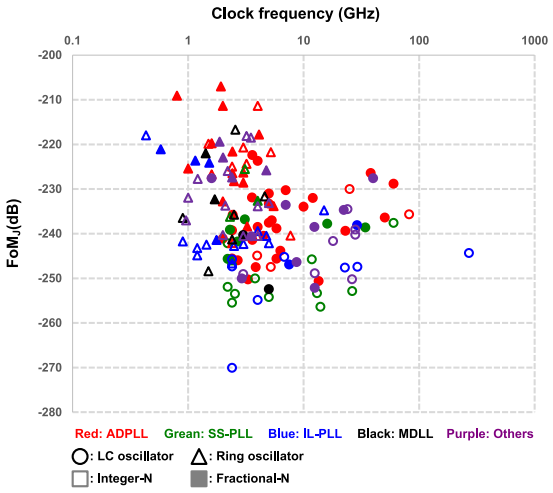

FIGURE 16. Survey of FOM_J with respect to PLL clock frequency.

improvement in FOM_J. To summarize, the PLL FOM should be continuously improved to support the demand for the clock frequency scaling [163].

IV. COMPREHENSIVE FOM AND DISCUSSION

A. PROPOSED COMPREHENSIVE FOMs

In the previous section, various PLL FOM candidates (3)–(7) are discussed based on the dependency studies, which are summarized in Table 1. Again, note that those are not intended to replace the FOM_J, but to complement it because

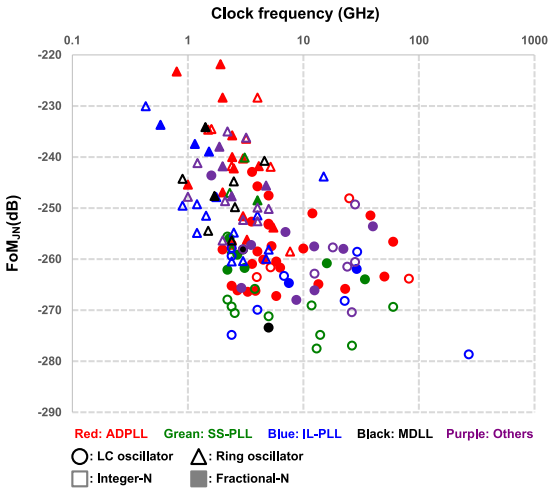

FIGURE 17. Survey of FOM_{JN} with respect to PLL clock frequency.

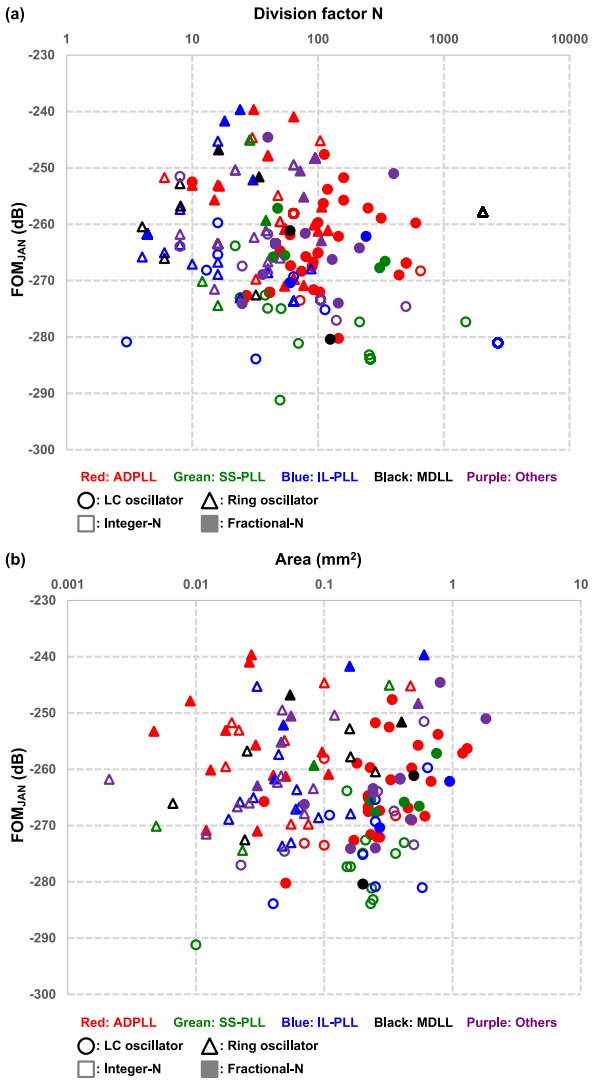

FIGURE 18. Survey of FOM_{JAN} with respect to (a) division factor, (b) PLL area.

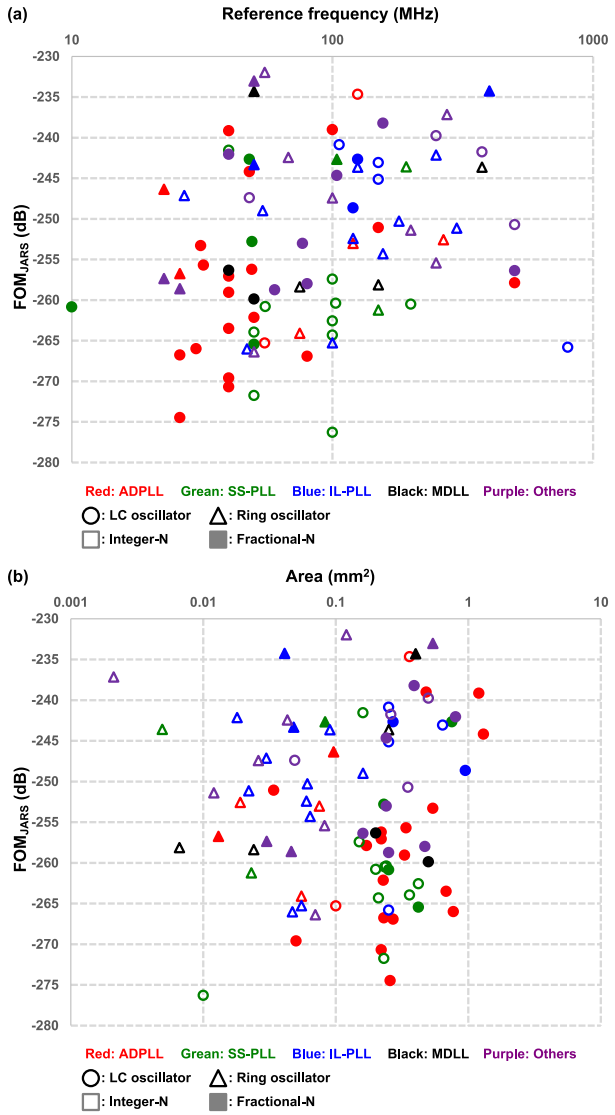

FIGURE 19. Survey of FOM_{JARS} with respect to (a) reference frequency, (b) PLL area.

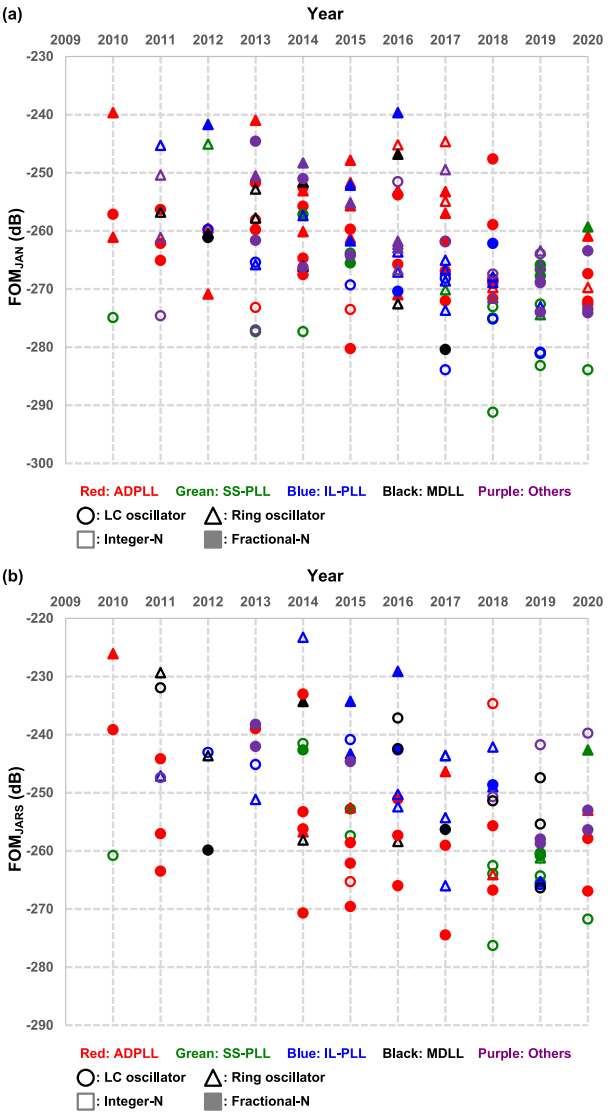

FIGURE 20. (a) Survey of FOM_{JAN} over years, (b) survey of FOM_{JARS} over years.

the FOM_J is still very useful and has solid background. The motivation is not to miss various factors other than the jitter generation and the power consumption of PLL circuits, because there are many others may impact the PLL performance as described in the previous section. PLL designers, who understand the underlying theories of each trends that (3)–(7) and Table 1 imply, can pick one of those complements which is most appropriate for describing their designs. In addition, any combination of (3)–(7) would provide more comprehensive view of a PLL performance. Here are two examples out of many possible combinations, FOM_{JAN} (jitter, area, and N) and FOM_{JARS} (jitter, area, reference frequency, and spur), which are expressed to

$$FOM_{JAN} = 10\log\left(\left(\frac{\sigma_{rms}}{1s}\right)^2\left(\frac{P_{PLL}}{1mW}\right)\left(\frac{Area}{1mm^2}\right)\left(\frac{1}{N}\right)\right), \tag{8}$$

$$FOM_{JARS} = 10\log\left(\left(\frac{\sigma_{rms}}{1s}\right)^2\left(\frac{P_{PLL}}{1mW}\right)\left(\frac{Area}{1mm^2}\right) \times \left(\frac{f_{ref}}{1MHz}\right)^{1.5}\right) + \frac{Ref.Spur}{2}. \tag{9}$$

To validate such comprehensive FOM, FOM_{JAN} is plotted with respect to N and PLL area in Fig. 18(a) and (b), respectively. In those plots, the FOM_{JAN} is scattered relatively randomly, which means it does not show strong correlations with those factors. Similar analyses are presented in Fig. 19(a) and (b), where the FOM_{JARS} is scattered with respect to the reference frequency and the area, respectively. Similarly, no strong correlations are observed from the scatter plots.

B. DISCUSSION

Here is a simple example that provides a comparison of FOM_{JAN} and FOM_{JARS}. Assuming that f_{ref} is doubled while

the other parameters (i.e. output frequency) are held the same. If f_c stays while doubling f_{ref}, the reference spur improves by 6 dB. Therefore, FOM_{JARS} degrades by 1.5 dB whereas FOM_{JAN} degrades by 3 dB. However, as discussed in the section I and II, one of the main motivations of this work is to include many practical cases where fc is constrained by fref. In those cases, we want to raise fc, and then the reference spur improves by 0 to 6 dB depending on fc/fref. As a result, FOM_{JARS} degrades by 1.5∼4.5 dB and agrees with FOM_{JAN}.

Fig. 20(a) and (b) show trend surveys of FOM_{JAN} and FOM_{JARS} over the years. Like the trend of FOM_J presented in Fig. 1(a), they tend to be improved over the years. Here we can revisit the conclusion of [1]; (A) with the comprehensive FOMs, different PLL designs can be compared by using a single number, (B) the FOMs have been improved over the years which we would expect from the state-of-the-art works.

V. CONCLUSION

Conventional PLL FOM (FOM_J) has been widely adopted to compare different PLL designs, thanks to its solid background and simplicity. It is based on a few fundamental assumptions; however, they have started breaking recently, due to the recent advances in PLL design techniques. In addition, some important design factors are missing in FOM_J. This paper reviews the state-of-the-art circuit techniques for low-jitter PLLs and discusses the limitations FOM_J and the needs for introducing complementary FOMs to back-up the FOM_J. In addition, an extensive survey on state-of-the-art PLL designs is provided, to capture FOM_J's dependency on various factors other than jitter and power, since it is hard to capture the exact dependency only with theories. Specifically, we captured the FOM_J dependency on area, division ratio, reference frequency, and reference spur. Based on the trend and dependency study, a few alternative FOMs to complement the legacy FOM_J are discussed. The alternative FOMs are intended to include the performance impacts from those factors. Such comprehensive FOMs are also verified with the PLL performance surveys.

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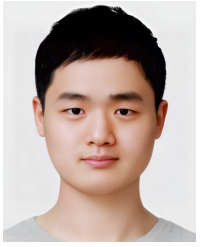

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