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RESEARCH ARTICLE

A Modified Phase Shift Control of the Dual Active Bridge-Based Modular Power Electronic Transformer to Minimize the LVdc Side Voltage Ripples Under Unbalanced Load Conditions

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ABSTRACT Power Electronic Transformers (PETs) are considered as an emerging solution for power conversion due to their benefits over the low frequency power transformers (LFPTs) such as lower size, multi-port structure and different control functionalities. However, unbalanced load conditions may limit the reduction of size due to using bulky capacitors to absorb the resulting 2nd harmonic voltage oscillations. This paper aims to provide a solution to this problem in the Dual Active Bridge (DAB)-based Modular Multilevel Converter Power Electronic Transformers (MMC-PET). In this study, a modified phase shift control strategy for the DAB isolation stage is presented. In this strategy, the duty cycle is allowed to change sinusoidally around the operating point. This consequently transfers the power oscillations to the HV side where their effect is less significant. The system is simulated using Matlab-Simulink under different unbalanced load conditions. Besides, the theoretical analysis and the simulation results are experimentally validated using a laboratory prototype. According to the obtained results, the proposed controller succeeded to reduce the voltage ripples from 7.5% to 0.2% and this helps in replacing large Aluminum electrolytic capacitors with low size film capacitors and consequently reducing the system overall size and volume which is a great benefit.

INDEX TERMS Dual active bridge, modular multilevel converter, power electronic transformer, resonant controller.

I. INTRODUCTION

The Low-Frequency Power Transformer (LFPT) can be considered as the most important element in transmission and distribution of electrical energy. It is a powerful component that interfaces different voltage levels and ensures galvanic isolation with high efficiency, low cost, high reliability and robust structure. Nevertheless, LFPTs are bulky and heavy, that is why it has low power density (0.25 – 0.35 kVA/kg) and this limits its use for applications in which high power density is mandatory such as electrical traction [1], [2]. Also, LFPTs are suffering from some limitations such as no-load losses, high sensitivity to harmonics, and load unbalances which affect its operation in distribution networks.

With the rapid advancement in power converters technology and the emergence of new types of power electronic switches with high power and voltage rating and high switching frequency such as Silicon Carbide (SiC) power devices which can withstand reverse voltage over 15 kV and switching frequency about 10 kHz. This enables the invention of the

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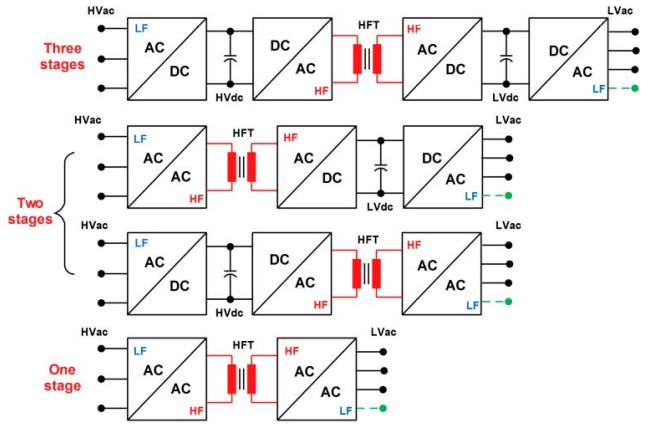


FIGURE 1. PET cell configurations.

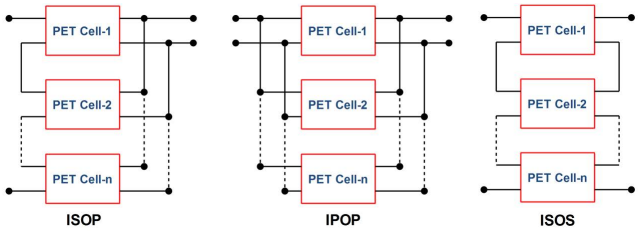


FIGURE 2. PET cell connection methods.

Power Electronic Transformer (PET) or so-called the Solid State Transformer (SST). PET is a promising topology, it is expected to replace the LFPT in the near future. The main idea behind the PET is to increase the frequency of the input voltage from 50/60 Hz to some kilohertz and then (increase / reduce) the voltage using high-frequency transformer (HFT) to achieve galvanic isolation and to reduce the system volume and size, then reduce the frequency back to 50/60 Hz at the output stage [3]. PET has many benefits over LFPT such as high power density (0.5 – 0.75 kVA/kg), relatively higher efficiency (95%–98%), it provides power control, fault current limitations and fault isolation.

Different configurations of PET cell can be found through literature. The substantial difference between these configurations is the number of power conversion stages, this may be one, two or three stages [3], [4]. Fig.1 shows different configurations of PET cell according to the number of power conversion stages. The most popular configuration is the three-stages PET, it converts from HVac to HVdc then from HVdc to LVdc through high frequency DAB converter with HF transformer and finally from LVdc to LVac through VSC, the output can be either three or four wire. This configuration enables HVdc and LVdc ports which could be helpful in integrating Distributed Energy Resources (DER) or Distributed Energy Storage (DES), but the presence of bulky DC link capacitors increase the system size and volume. Also, input and output ports of each PET cell can be connected in different ways, the connection method determines the overall voltage and current rating of the transformer. Input Series Output Parallel (ISOP), Input Parallel Output Parallel (IPOP), Input Series Output Series (ISOS) are the main configurations and are shown in Fig.2 [3], [5], [6].

The main challenge in developing PET is the reduction of the overall size to increase the power density over 1 kVA/kg [1]. The proposed solutions to this problem through literature were focusing on either increasing the operating frequency which consequently leads to higher switching losses and lower efficiency or merging two stages in one stage resulting in the two stages configuration. In this configuration, a direct AC/AC conversion is done either in input or output stages as shown in Fig.1 using direct matrix converter or cycloconverter. This eliminates either HVdc or LVdc ports and reducing the system size. Furthermore, merging two power conversion stages in both input and output stages results in the single stage PET, it converts directly from HVac to LVac and removes both HVdc and LVdc ports. Algthough this will reduce the overall size but this leads to the loss of the ability to connect with Distributed Energy Resources (DER) which is one of the main feature of PET.

Another approach is to minimize the overall size by reducing the LVdc side capacitors size and replacing large Aluminum electrolytic capacitors with small film capacitors. It is well-known that large electrolytic capacitors are always used in DC link to absorb the power oscillations resulting from unbalanced or nonlinear loads. Therefore, minimizing the DC link voltage ripples leads to minimum DC link capacitors.

Many researches have been done to achieve this goal. A ripple cancel DAB circuit has been proposed with additional small capacitors and modified switching pattern to reduce the voltage ripples and voltage stress on the series connected switching devices but with increasing the circuit components [7]. In [8], an Input-parallel Output-series (IPOS-DAB) topology with unbalanced operating points is adopted to compensate the low frequency power oscillations, but the series connection of output cells reduces the current capacity of LVdc side. In [9], a modified control approach for the Cascaded H-Bridge with isolated DAB converters for automotive applications is presented, in which, a low bandwidth PI controller operates in dq reference frame rotating at the ripple frequency is used to maintain the DC voltage level, while, a feed-forward term is added to generate the phase shift required for the motor side H-bridge current ripple control.

In this paper, a modified phase shift controller for the isolation DAB stage is presented to change the phase shift angle between HV and LV H-Bridges sinusoidally around the average operating point. This consequently transfers the power oscillations to the HVdc side and leaves the LVdc link side free of oscillations. This can be done by adding a resonant term with the ripple frequency to the conventional PI controller. As all DAB cells are identical and have the same configuration and control, only one isolation stage is considered in this study to verify the proposed controller which can be easily extended to all other cells.

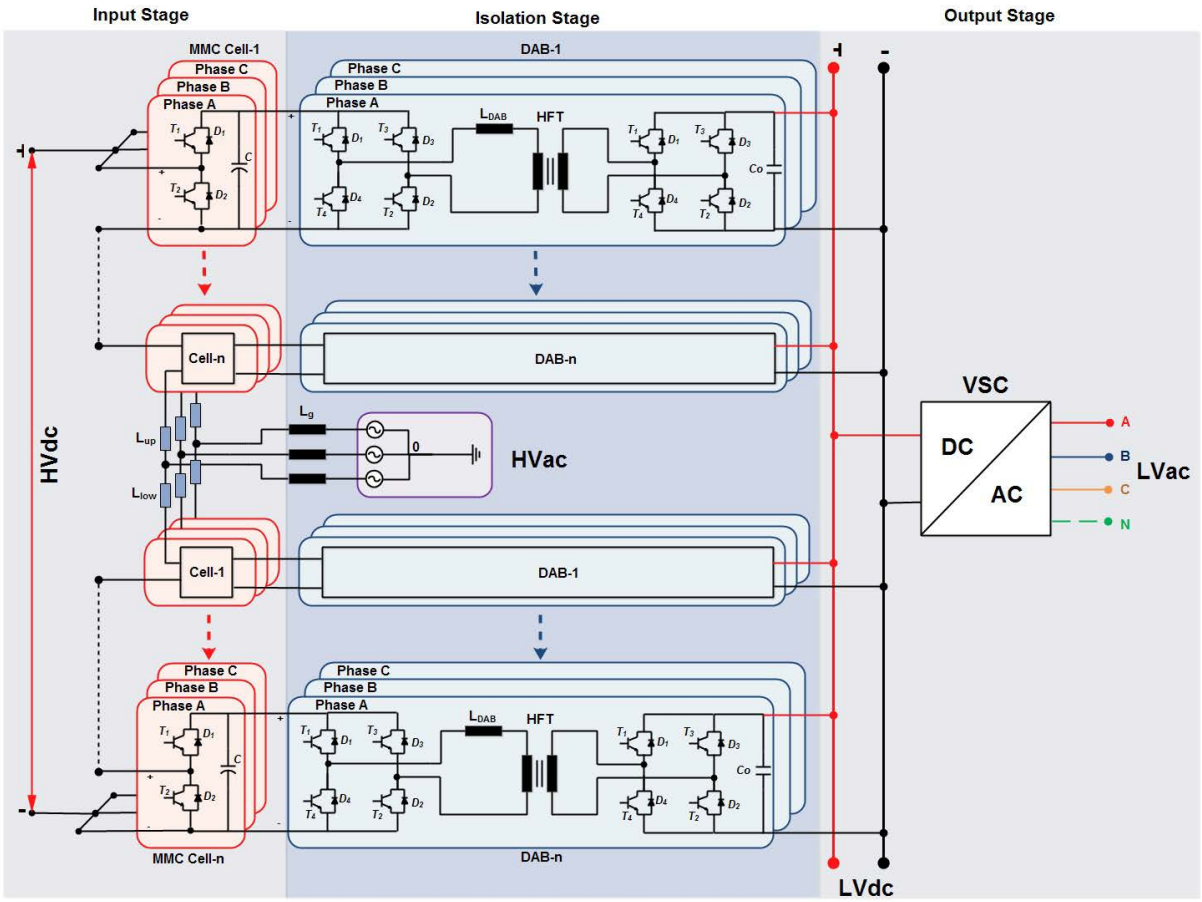


FIGURE 3. Three-phase MMC-PET circuit.

This paper has been organized as follows,the system description is discussed in Sec.II. The control of MMC-PET system is described in Sec.III. The performance of MMC-PET under unbalanced load conditions is presented in Sec.IV. The conventional and proposed phase shift control of the Dual Active Bridge (DAB) are presented in Sec.V. Matlab simulation and the experimental prototype are presented in different loading conditions in Secs.VI,VII respectively. Finally, the results discussion and the main conclusions have been presented in Secs.VIII,IX respectively.

II. MMC-PET SYSTEM DESCRIPTION

The three stages ISOP Modular Multilevel Converter based Power Electronic Transformer (MMC-PET) has been selected for study in this paper because it is suitable for high voltage applications (high input voltage) and can supply large distribution loads (high output current). Fig.3 shows the power circuit of MMC-PET, The system consists of three power conversion stages; the first stage is the Modular Multilevel Converter (MMC) which converts from HVac to HVdc. It consists of six arms (each phase has two arms namely upper and lower arms), each arm consists of N identical chopper cells connected in series and an arm impedance L_{up}, L_{low}. Each chopper cell consists of a capacitor and two complementary switches in half bridge configuration, in this configuration, the submodule capacitor can be inserted or bypassed according to the switches states. When switch T_1 is ON the capacitor is inserted and the cell voltage is equal to the capacitor voltage v_c, while when T_2 is ON the capacitor is bypassed and the submodule voltage is zero [10], [11].

The second stage is the isolation stage which utilizes the Dual Active Bridge (DAB), it is a bidirectional DC-DC converter with galvanic isolation. It consists of two H-Bridges and high-frequency transformer to provide galvanic isolation. Each bridge operates with square pulses with 50% duty cycle, the average current that flows through the converter depends on the phase shift between the primary and the secondary bridges. The third stage is the DC/AC inverter which converts from LVdc to LVac, the output of this stage can be connected to a load or to the utility grid.

III. MMC-PET CONTROL SYSTEM

As the MMC-PET consists of different power stages, each stage has its own control system. Different control targets should be achieved simultaneously, the power transferred between power stages should be balanced [12], [13]. MMC

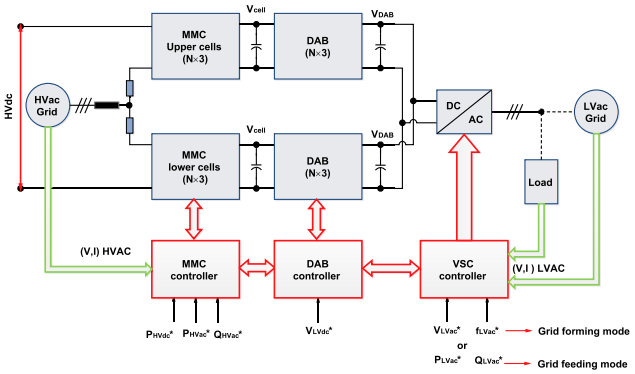


FIGURE 4. MMC-PET control system.

controller achieves different tasks internally such as keeping the cell voltage at a certain level and regulates the circulating currents flowing between the three phases. Externally, it matches the power between HVac and HVdc sides [14]–[17]. DAB controller regulates the LVdc capacitor voltage by regulating the power flow between the transformer sides. Finally, the 2L-VSC controller has two configurations, it depends on its operating mode, when the converter works in grid feeding mode then the controller should control active and reactive power. While, when it operates in grid forming mode (supplies a passive network), it controls the output voltage magnitude and frequency. Fig.4 shows the overall control system of MMC-PET. As mentioned earlier this paper focuses on the control of DAB converters, so the control of input and output stages is out of the scope of this paper.

IV. MMC-PET UNDER UNBALANCED LOAD CONDITIONS

The output stage of MMC-PET is the three-phase VSC that supplies a load, which is often unbalanced loads. In balanced three phase system the AC voltages and currents can be written as in (1):

$$v_{abc} = \begin{cases} v_a(t) = V_0 cos(\omega t) \\ v_b(t) = V_0 cos(\omega t - \frac{2\pi}{3}) \\ v_c(t) = V_0 cos(\omega t + \frac{2\pi}{3}), \end{cases}$$
$$i_{abc} = \begin{cases} i_a(t) = I_0 cos(\omega t - \phi) \\ i_b(t) = I_0 cos(\omega t - \frac{2\pi}{3} - \phi) \\ i_c(t) = I_0 cos(\omega t + \frac{2\pi}{3} - \phi) \end{cases} \quad (1)$$

The DC side current can be calculated as in (2)

$$i_{dc}(t) = i_{dc}^{+}(t) - i_{dc}^{-}(t) = \sum \frac{1 + m_x(t)}{2} i_x(t) - \sum \frac{1 - m_x(t)}{2} i_x(t), x \in \{a, b, c\} \quad (2)$$

where i_{dc} is the converter DC side current, i_{dc}^{+}, i_{dc}^{-} are the positive and negative pole currents respectively, m_x, i_x are the modulation index and the current of phase (x). In (2), the summation of the three phase balanced currents is zero then the DC current is constant while in unbalanced load conditions it consists of DC and AC components, the DC components equal to the average current and the AC component is a 2^{nd} harmonic. Fig.5 shows the VSC input and output currents under balanced and unbalanced load conditions. Neglecting the switching losses, the input DC and output AC instantaneous power are equal and can be calculated as:

$$\begin{aligned} p_{dc}(t) &= v_{dc}(t) i_{dc}(t) \\ &= v_a(t) i_a(t) + v_b(t) i_b(t) + v_c(t) i_c(t) \\ &= (V_a I_a + V_b I_b + V_c I_c) cos(\phi) \\ &\quad - \begin{bmatrix} V_a I_a cos(2\omega t) \\ + V_b I_b cos(2\omega t + \frac{2\pi}{3}) \\ + V_c I_c cos(2\omega t - \frac{2\pi}{3}) \end{bmatrix} \end{aligned} \quad (3)$$

In balanced system the sum of the 2^{nd} harmonics terms is zero and the total power is equal to the average power. While in case of unbalanced load conditions the instantaneous power oscillates around the average value with double the fundamental frequency [18]. Fig.6a shows the power flow from the DAB to the three-phase load across the VSC, as the DAB is a current controlled converter it can be represented as a controlled current source depends on the phase shift angle ϕ. In conventional control method using PI controller, the controller can only process the DC power (red line). Hence, the capacitor contributes in supplying the load with the 2^{nd} harmonic power term (blue line).

According to [19], the minimum DC link capacitor required to absorb power ripples can be calculated by (4), where P_0 is the average power, f_0 is the output frequency, V_{dc} is the DC link voltage and Δv_{ripple} is the peak to peak ripple voltage magnitude.

$$C_o = \frac{P_0}{2\pi f_0 V_{dc} \Delta v_{ripple}} \quad (4)$$

Therefore, large capacitors are needed to absorb power oscillations in unbalanced or single phase operation. However, in case of modular PET, enlarging LVdc link capacitor in each DAB is not a proper solution because this will increase the size and the volume of the whole system remembering that PET has been invented basically to replace LFPT due to its large size. So, increasing the power density is a major requirement in designing PET as well as the use of large electrolytic capacitors will affect the system reliability due to their high failure rate.

The proposed method is to modify the DAB controller to process both DC and 2^{nd} harmonic power terms and leave the capacitor free of oscillations as shown in Fig.6b. So, there is no need to use large capacitors in LVdc side. Modeling and control of DAB stage with the conventional and proposed controller are presented in the next section.

V. DAB CONTROL SYSTEM

Fig.7 shows DAB circuit diagram, it consists of two identical H-bridges and high-frequency transformer in between to provide voltage level variation and galvanic isolation. L_{DAB}, R_{DAB} represent the equivalent leakage inductance and internal resistance of the transformer respectively. Each H-bridge

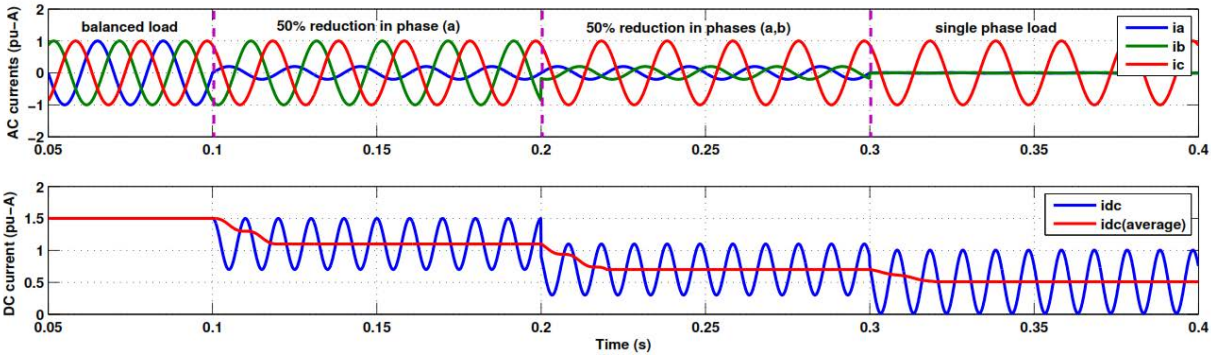


FIGURE 5. Input and output currents of VSC under balanced and unbalanced load conditions.

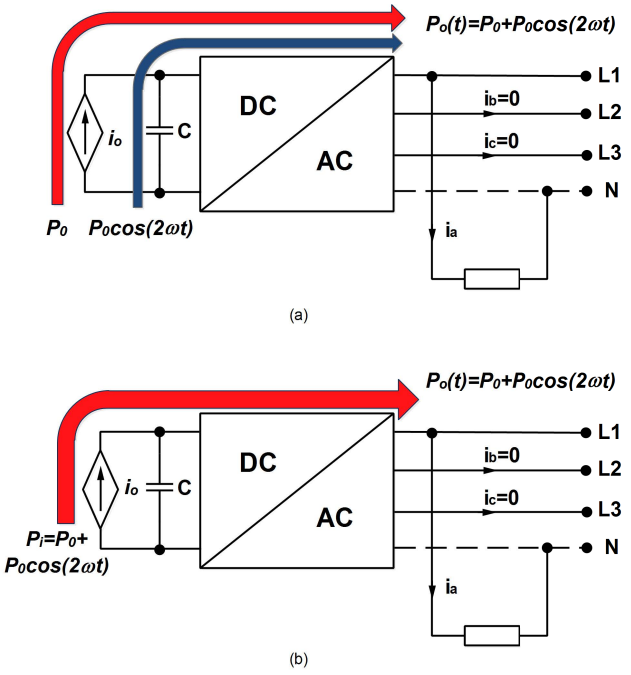


FIGURE 6. Power flow from DAB to load under single phase load condition: (a) conventional method, (b) proposed method.

operates by a high-frequency square wave pulse width modulated signals with 50% duty cycle. The power transferred can be regulated by changing the phase shift between input and output bridges switching states, this method is called phase shift modulation [20]–[22].

A. THE CONVENTIONAL PHASE SHIFT CONTROL

As shown in Fig.8, the input and output bridges provide a high-frequency square wave voltage at the primary and the secondary winding of the transformer respectively. The leakage inductance current $i_{L_{DAB}}(t)$ depends on the difference between the primary voltage $v_1(t)$ and the secondary voltage referred to primary side $v_2(t)/n$ where n is the transformer turns ratio. Figs.8a,b show the leakage inductance voltage and current when the input bridge leads and lags the output bridge by an angle ϕ respectively. The power flows from the leading bridge to the lagging bridge depends on the phase shift ratio $d = \phi/\pi$. Analyzing the leakage inductance current waveform, the average power that can be delivered by the DAB can be calculated as in (5) [23]–[25].

$$P_{DAB} = \frac{nV_iV_oD(1-D)}{2f_sL_{DAB}} \tag{5}$$

where V_i, V_o and D are the average input and output voltages and the average phase shift ratio respectively, f_s is the switching frequency. Neglecting the switching losses, the power balance equation can be written as

$$P_i = P_o = P_{DAB} = V_iI_i = V_oI_o \tag{6}$$

where P_i,P_o are input and output average power respectively and P_{DAB} is the average power transferred across the DAB. Also, I_i, I_o are the average input and output current respectively.

$$I_o = \frac{nV_iD(1-D)}{2f_sL_{DAB}}, \quad I_i = \frac{nV_oD(1-D)}{2f_sL_{DAB}} \tag{7}$$

According to [20], [26] the control to output current transfer function $G_{di}(s)$ and the output current to output voltage transfer function $G_{iv}(s)$ can be derived as in (8),(9) respectively.

$$G_{di}(s) = \frac{I_o(s)}{d(s)} = \frac{2V_o}{sL_{DAB} + R_{DAB}} \tag{8}$$

$$G_{iv}(s) = \frac{V_o(s)}{I_o(s)} = \frac{R_l(1-2D)}{R_lC_os + 1} \tag{9}$$

The main target of the DAB control system is to regulate the output capacitor voltage by regulating the power transferred between the HV and LV sides. The control system consists of two cascaded control loops, the outer loop controls the output voltage and generates the reference output current i_o^*. The inner loop regulates the current by adjusting the phase shift d between the primary and secondary bridges as shown in Fig.9. Both inner and outer loops use PI controllers as the reference and measured signals are dc values.

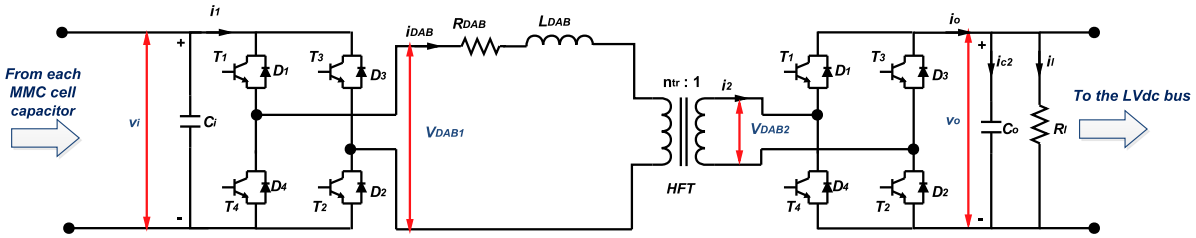


FIGURE 7. Dual Active Bridge (DAB) circuit.

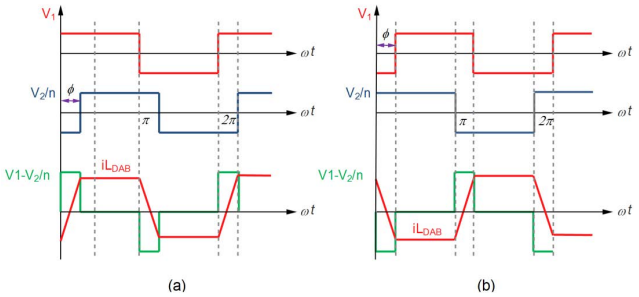


FIGURE 8. DAB phase shift control: (a) $\phi > 0$, (b) $\phi < 0$.

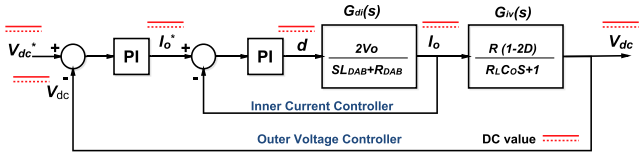


FIGURE 9. Conventional DAB control system.

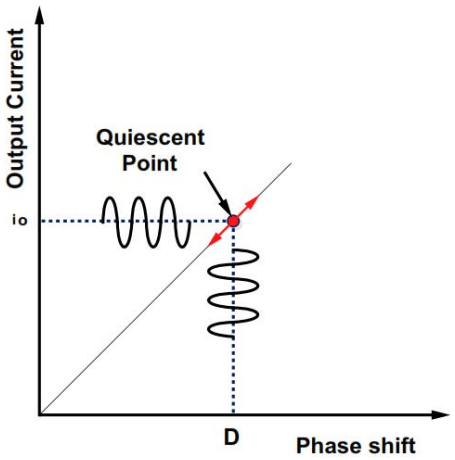


FIGURE 10. The relation between DAB phase shift and output current.

B. THE PROPOSED PHASE SHIFT CONTROL

As discussed earlier, the control target of the DAB controller is to regulate the output voltage according to the power transferred between input and output sides. This can be achieved by changing the phase shift between the switching states of input and output H-bridges. In steady state, the converter operates at a quiescent point (D, I_o) at which the average output current I_o depends on the average phase shift ratio D as shown in Fig.10.

The proposed control method depends on changing the phase shift ratio (d) sinusoidally with double fundamental frequency. This can be done using the Proportional Integral Resonant (PIR) controller instead of the conventional PI controller. The Proportional-Integral (PI) part is responsible to generate the average phase shift ratio (D) according to the average output current (I_o). While the resonant part (R) allows the phase shift ratio to oscillate with double fundamental frequency around the quiescent point, this consequently makes the output current oscillates at this frequency as shown in Fig.10.

Resonant controller is a type of control actions which is suitable for AC current regulation, the main difference between the conventional PI current controller and the most famous type of resonant controllers Proportional Resonant (PR) controller is the response to a sinusoidal input. PI controller cannot achieve zero steady state error in case of sinusoidal references while PR controller has infinite gain and zero phase shift at the resonant frequency ω_r which results in a good tracking and zero steady state error [27].

Equation (10) shows the transfer function of the ideal PR controller $G_{PR}(s)$, where k_p, k_r are the proportional and resonant gains respectively and ω_r is the resonant frequency, the ideal resonant controller gives an infinite gain at the resonant frequency. In fact, it is impossible to have an infinite gain in practical implementation. Therefore, it is preferable to use the modified PR formula $G'_{PR}(s)$ described in (11). Where $\omega_c = 2\pi f_c$ is the controller cut-off frequency, Fig.11 shows the difference between the ideal and modified resonant controller frequency response [28]–[30].

$$G_{PR}(s) = k_p + \frac{2k_r s}{s^2 + \omega_r^2} \tag{10}$$

$$G'_{PR}(s) = k_p + \frac{2\omega_c k_r s}{s^2 + 2\omega_c s + \omega_r^2} \tag{11}$$

In some cases the reference signal contains both DC and AC components. Unfortunately, neither PI nor PR controllers can fulfill zero steady state error in such cases. So, the Proportional Integral Resonant (PIR) controller has been introduced. PIR controller consists of both PI and R parts as indicated by its transfer function $G_{PIR}(s)$ in (12). Fig.12 shows a

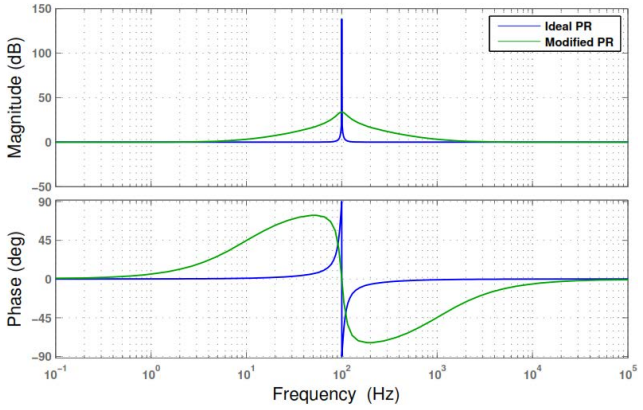


FIGURE 11. Frequency response of ideal and modified PR controller.

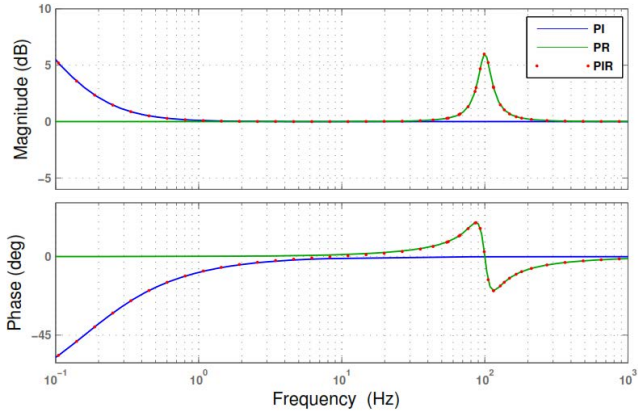


FIGURE 12. Comparison between PI, PR and PIR controller frequency response.

comparison between PI, PR and PIR controller frequency response, it is obvious that PI controller can only achieve good tracking with DC references while it has no effect at the resonant frequency. On the contrary, PR controller cannot achieve high gain at low frequencies while it has high gain at the resonant frequency. PIR controller has the benefits of both PI and PR controllers where it has high gain at low frequencies such as PI and also it has high gain with zero phase shift at the resonant frequency like PR controller which means perfect reference tracking at both low and resonant frequencies.

$$G_{PIR}(s) = k_p + \frac{k_i}{s} + \frac{2\omega_c k_r s}{s^2 + 2\omega_c s + \omega_r^2} \tag{12}$$

Under unbalanced load conditions, the output current of each DAB unit is required to track a mixed reference signal that contains both the DC component relative to the DC power transferred to the load and an AC (2^{nd} harmonic) component to cancel the capacitor voltage fluctuations. To achieve this task, two PIR controllers have been used, the first one is used in the outer voltage controller to inject the 2^{nd} harmonic component in the reference current while the other has been

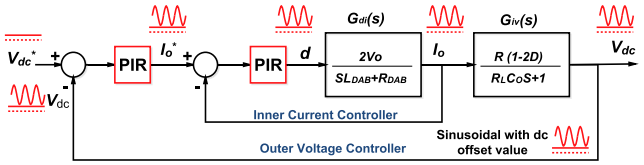


FIGURE 13. Modified DAB control system.

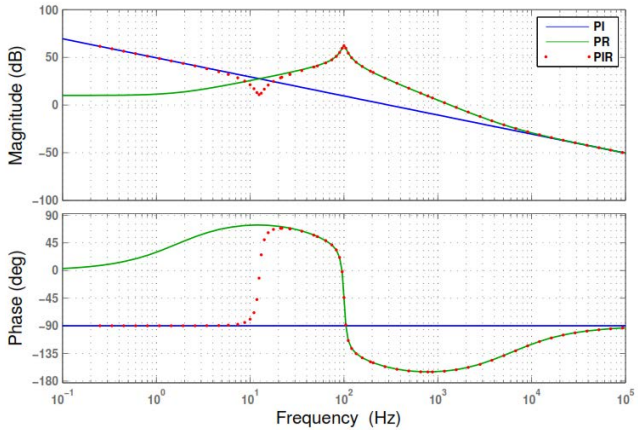


FIGURE 14. Comparison between PI, PR and PIR controller frequency response (open loop T.F).

used in the inner current controller to track the new reference signal perfectly as shown in Fig.13.

Fig.14 shows the Bode diagram of the open loop transfer function of the inner current loop using PI, PR and PIR controller, it is obvious that the PIR controller acts like PI controller at low frequencies while it behaves like the PR controller at the resonant frequency $f_r = 100$ Hz, this results in perfect tracking for both DC and AC reference signal components. On the other hand, the PIR controller can reject the disturbances at the low and resonant frequencies compared to the PI and PR controllers as indicated from the frequency response of the output to disturbance transfer function of the outer voltage loop shown in Fig.15.

C. IMPACT OF THE PROPOSED METHOD ON MMC INPUT STAGE

It is worth mentioning that the proposed method transfers the 2^{nd} harmonic power ripples to the HV side. This causes voltage fluctuations at the MMC cell capacitors. Fortunately, the three phase MMC-PET has a self protection property thanks to the circuit topology, it limits this effect especially that the connection of DAB cells is Input Series Output Parallel (ISOP). In this configuration, all DAB cells in the three phases of the PET are connected in parallel to the same LVdc bus and they are subjected to the same amount of power oscillations. Therefore, the LVdc current ripples will be divided by the number of DAB units (at least 24 units (4 modules × 6 arms)). Furthermore, in each DAB cell the current drawn from the input capacitor (MMC cell capacitor) equals the DAB output current divided by the voltage conversion ratio

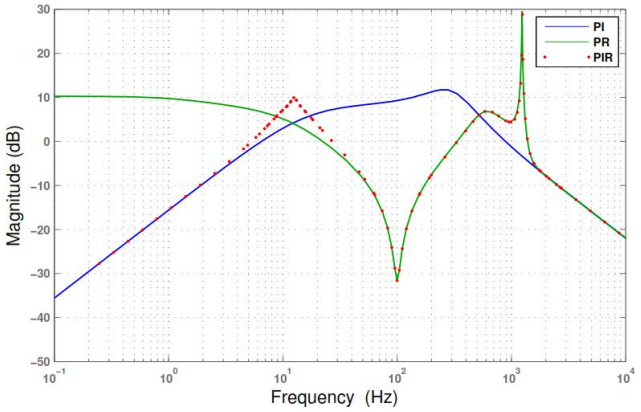


FIGURE 15. Comparison between PI, PR and PIR controller frequency response (output to disturbance T.F).

TABLE 1. Simulation parameters.

Parameter	Symbol	Value
Input voltage	V_{in}	1000 V
Output voltage	V_o	500 V
Output power	P_o	7.5 kW
Switching frequency	f_s	20 kHz
Output capacitance	C_o	320 μF
Load resistance	R_l	17 Ω
HFT equivalent leakage inductance	L_{DAB}	170 μH
HFT equivalent resistance	R_{DAB}	0.1 Ω
HFT turns ratio	n	2:1
Resonant frequency	ω_r	628.32 rad/s

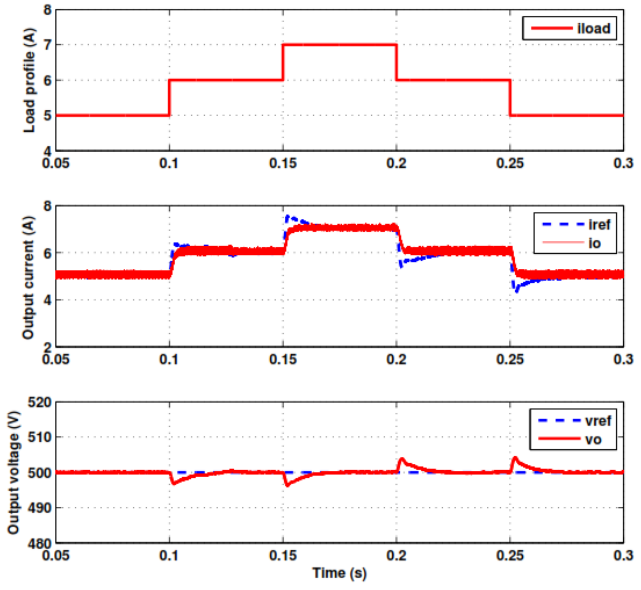


FIGURE 16. System response against step load disturbances.

(as the power transferred is constant). Equation (13) shows the relation between the input (HV side) and output (LV side) voltages and currents. For example, if the peak to peak current ripples at LV side are about 100 A, $N = 24$ is the total number of DAB units and the transformer ratio $n = 0.5$ then, the

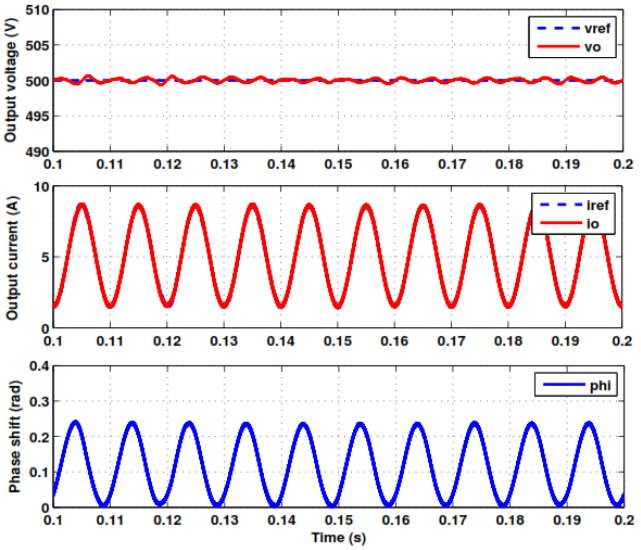


FIGURE 17. System response against single phase AC load.

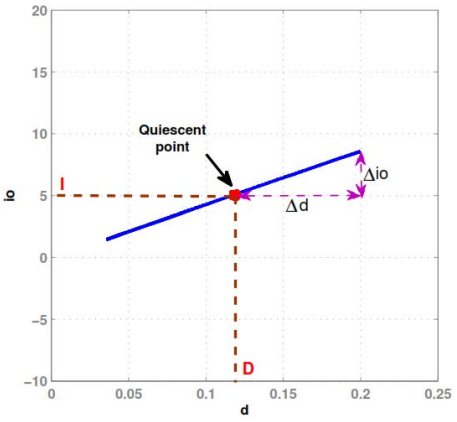


FIGURE 18. The relation between phase shift and output current (simulation).

TABLE 2. Experimental setup parameters.

DAB parameters	
Parameter	**Value**
Input voltage	240 V
Output voltage	120 V
Rated power	500 W
Switching frequency	20 kHz
LVdc capacitor	220 μF
HFT equivalent leakage inductance	207 μH
HFT turns ratio	2:1
Resonant frequency	628.32 rad/s
Single phase inverter parameters	
SPWM switching frequency	240 kHz
Modulation index	0.8
Ac Inductance filter	1.2 mH

peak to peak current ripples at HV side will be about 2 A and this will not affect the MMC capacitor voltage. On the other

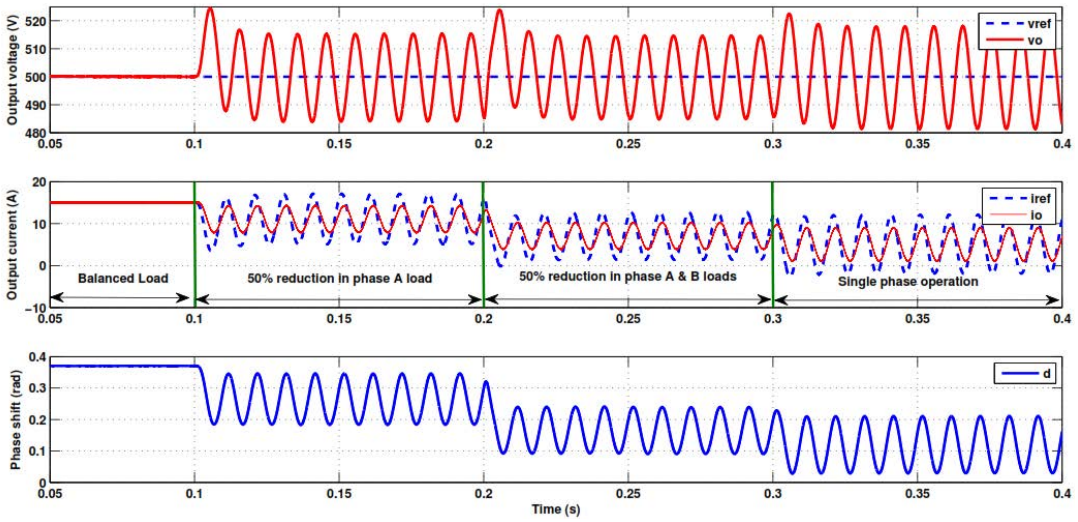


FIGURE 19. The conventional PI controller response under different unbalanced load conditions.

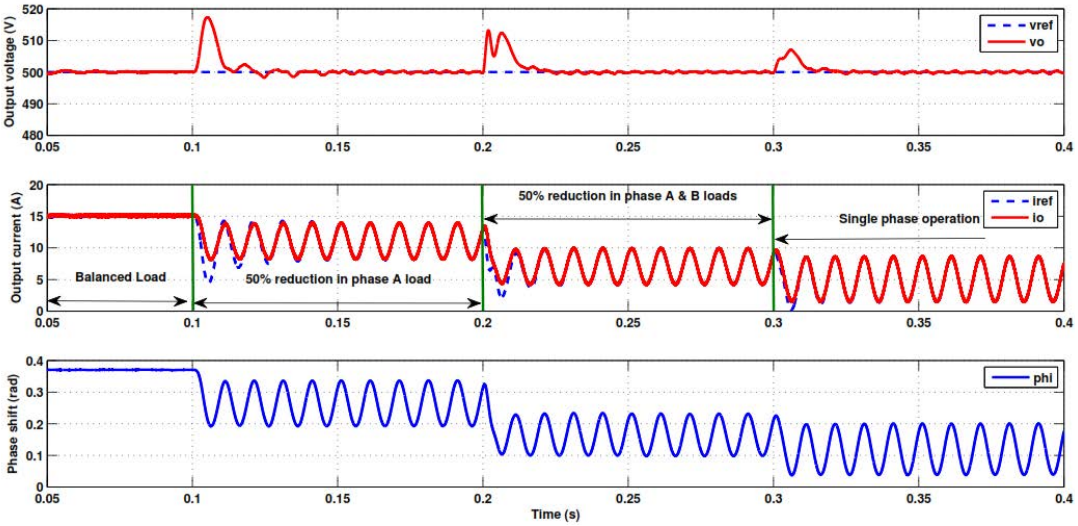


FIGURE 20. The proposed PIR controller response under different unbalanced load conditions.

hand, as the power oscillations are transferred to the HV side, in case of large unbalanced loads the HVAC side currents will be unbalanced but this unbalance can be compensated using different unbalance control techniques as the MMC is connected to the HVAC grid, some of these techniques are presented in [31]–[33].

$$I_{hv} = I_{lv} \frac{V_{lv}}{V_{hv} \times N} \tag{13}$$

VI. SIMULATION RESULTS

A single isolation stage has been simulated using Matlab-Simulink, the simulation parameters are listed in Table 1. Firstly, the system has been subjected to a DC load step disturbances as shown in Fig.16. The load profile is shown (top view), the load changes every 50 millisecond with 1 A step magnitude increasing and decreasing, the current controller tracks the current reference (middle view) and the output voltage tracks the voltage command (500 V) and rejects the load disturbances correctly in about 12 millisecond (bottom view).

Secondly, the system has been tested to supply a single phase AC load drawing a current of $5 + 5sin2\omega t$ A. Fig.17 shows the results in this case, the output current tracks the mixed reference thanks to the PIR current controller (middle view), this removes the voltage pulsations from the output capacitor voltage (top view) and the phase shift changed sinusoidally with double fundamental frequency (bottom view).

The relation between the output current (i_o) and the phase shift ratio (d) is shown in Fig.18, the red point in the middle of the figure represents the quiescent (equilibrium point) where the system operates at the average phase shift ratio (D) and average output current (I) at steady state. While the blue

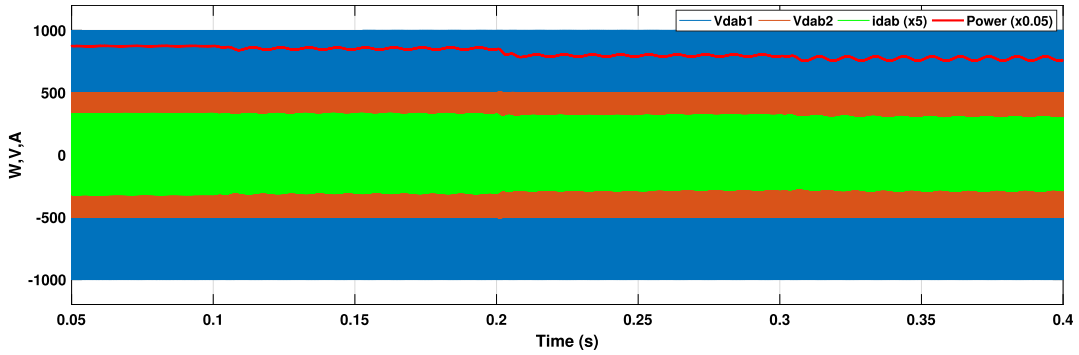
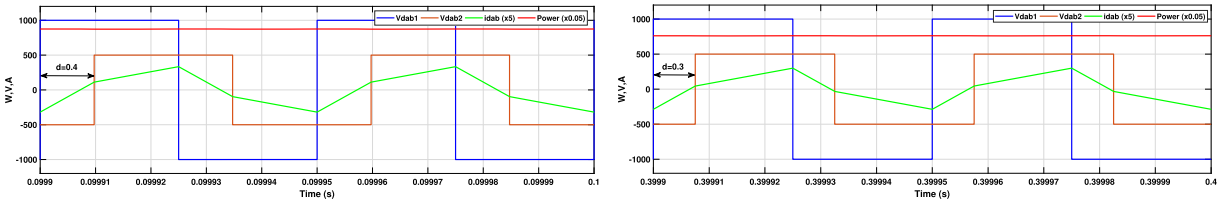


FIGURE 21. DAB power, input and output bridge voltages and leakage inductance current.



(a) (b)

FIGURE 22. Zoomed view of Fig.21 (a) at balanced load, (b) at single phase load.

line represents the current locus against the phase shift under single phase load with PIR controller allows the phase shift ratio and the output current to oscillate sinusoidally around the quiescent point with $\pm\Delta d$ and $\pm\Delta i_o$ respectively.

Finally, the system has been subjected to unbalanced three phase load at the output of the three-phase inverter. The proposed control algorithm is tested under the worst case scenario of unbalanced load, which is a single phase load to verify how the controller will work under such severe unbalance. Although the loads are usually distributed on the three phases to guarantee the power balance, but the severe unbalanced conditions cannot be avoided due to sudden change in loads, asymmetrical faults or maintenance in the LV network. The simulation starts with a three-phase balanced load, then at t =0.1 s, the load of phase (a) has been reduced to 50%, then at t=0.2 s, the load of phase (b) has been reduced to 50% and finally at t=0.3 s, the system operates in single phase mode (phases (a,b) at no load and phase (c) is full loaded). Figs.19, 20 show the system response with PI and PIR controller respectively. In each figure, the top view shows the DC link voltage and its reference signal, the middle view shows the filtered output current and its reference signal and the bottom view shows the phase shift signal generated from the DAB controller. It is clear that the proposed controller keeps the output capacitor voltage constant and removes the voltage ripples successfully. Considering the capacitor voltage ripples, it is shown that the proposed controller reduces the 2^{nd} harmonic ripples from 7.5% to 0.2% without increasing the output capacitor.

Also, the DAB input and output bridge voltages, the HF transformer leakage inductance current scaled (5:1) and the

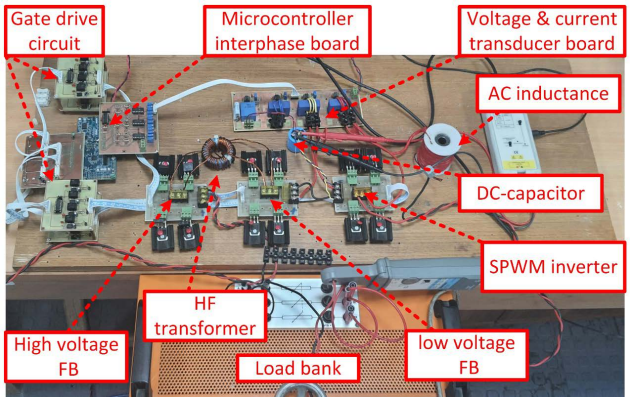


FIGURE 23. Experimental test setup.

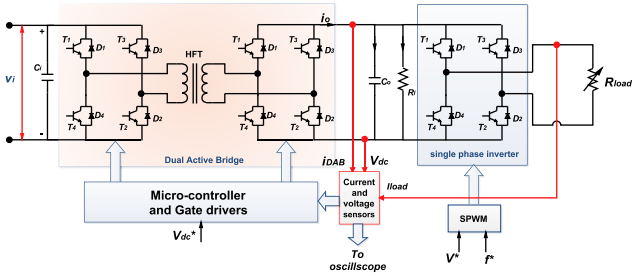


FIGURE 24. Experimental test setup schematic diagram.

power transferred through the DAB scaled (1:20) are shown in Fig.21. It is clear that the proposed controller is working successfully, as the 100 Hz envelope is observable in the

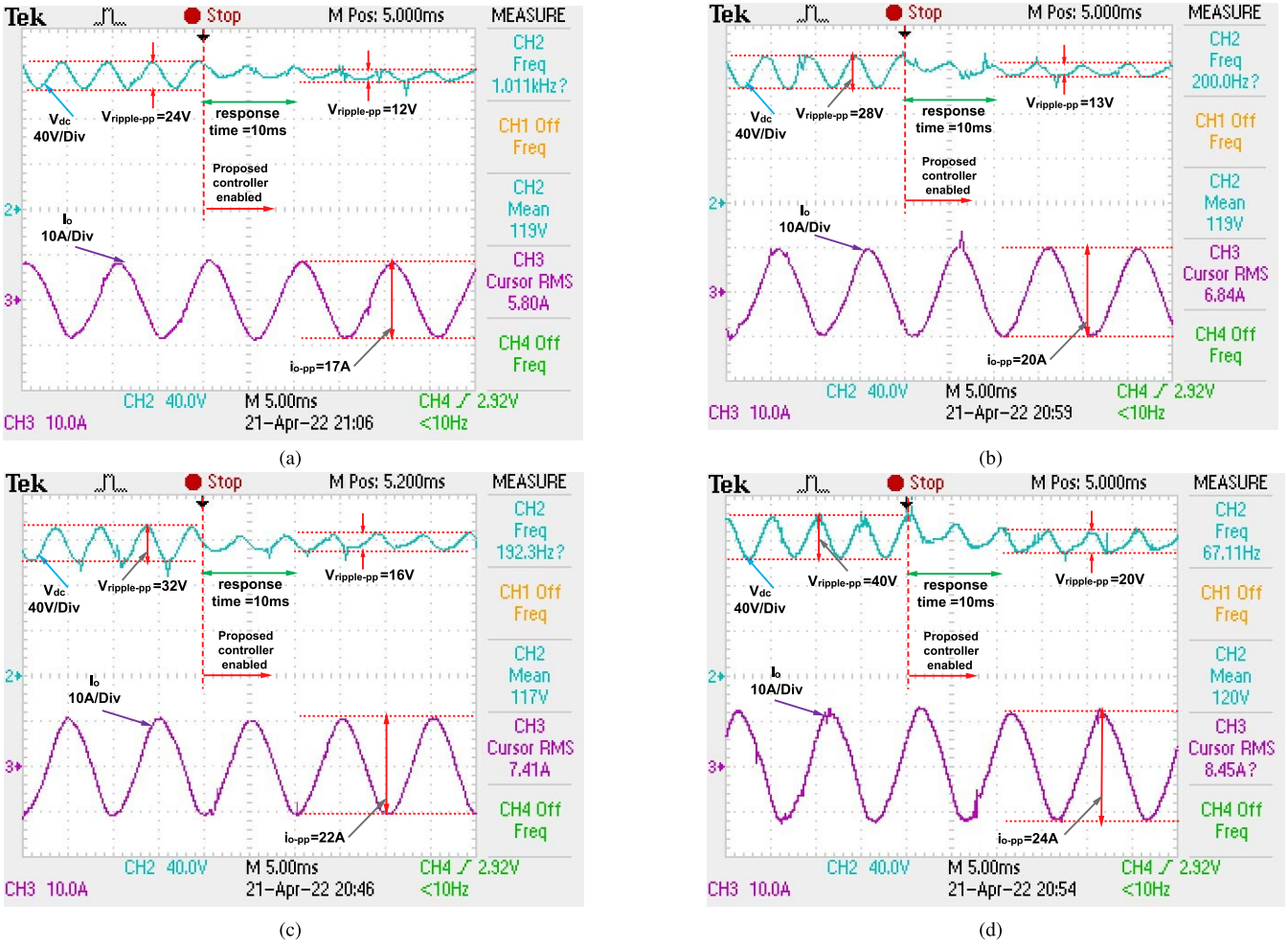


FIGURE 25. Experimental results with different load resistance values: (a) 10 Ω, (b) 9 Ω,(c) 8 Ω,(d) 7 Ω.

transformer current. This means that the phase shift ratio tracks the output power oscillations successfully. A zoomed views of Fig.21 are shown in Figs.22a,22b at two different simulation periods (under balanced loads and single phase load) respectively, to show the relation between input and output bridge voltages and transformer inductance current under different load conditions.

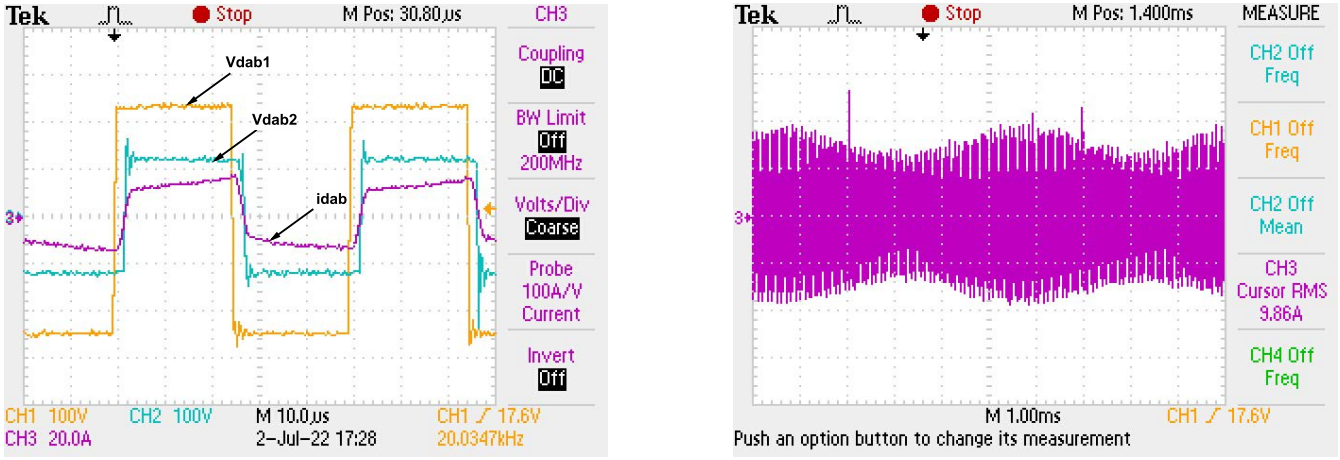
VII. EXPERIMENTAL RESULTS

An experimental test setup has been built to validate the theoretical analysis as shown in Fig.23 with the parameter listed in Table 2. A low scaled single isolation stage has been considered. Fig.24 shows the schematic diagram of the experimental setup, it consists of a DAB unit supplies a single phase inverter as a source of 2nd harmonic oscillations.

Fig.25 from (a) to (d) show the experimental results before and after the proposed strategy is enabled at different load resistance values (Rload=10,9,8,7 Ω) respectively. In each figure, the top view is the DAB output DC voltage and the bottom view is the output load current. The obtained results show that the proposed control strategy reduces the DC voltage ripples to about 50% without increasing the DC link capacitor. Increasing the load current, increases the ripple magnitude but the proposed controller still able to reduce the ripple voltage successfully. After enabling the proposed strategy, the system reaches the steady state within 10ms. Also, Fig.26a shows the DAB input and output bridge voltages and the HF transformer leakage inductance current and Fig.26b shows the transformer leakage inductance current for two fundamental cycles. It is clear that the 100 Hz current envelope is now observable and the power oscillations are transferred successfully through the DAB.

VIII. DISCUSSION

From the theoretical analysis, it is found that in balanced load conditions, according to (4) and with the system ratings listed in Table 1, the minimum required DC link capacitor for 5% allowable voltage ripple is 640 μF. Therefore, under unbalanced or single phase load the ripple magnitude will be higher and need larger capacitor (may be thousands of microfarads) to be absorbed. It is obvious from simulation results that with the proposed control strategy only 100 μF was sufficient to



(a) (b)

FIGURE 26. Experimental results: (a) input and output bridge voltages and the HF transformer current, (b) two fundamental cycles of the HF transformer current.

TABLE 3. Experimental test results.

load resistance **Rload** (Ohm)	load current **Iload-pp** (A)	**Vripple-pp** with the conventional controller (V)	**Vripple-pp** with the proposed controller (V)	Minimization ratio (%)
10	17	24	12	50
9	20	28	13	53
8	22	32	16	50
7	24	40	20	50

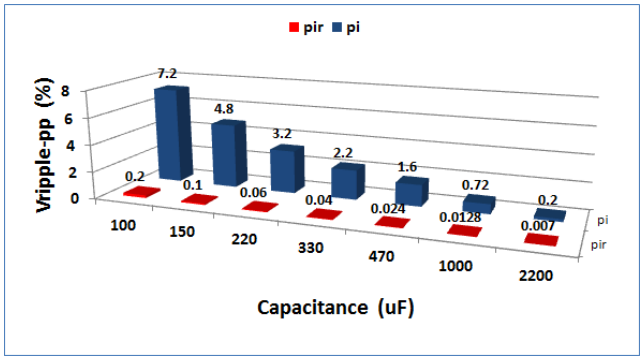


FIGURE 27. Voltage ripple magnitude using the conventional and the proposed control methods.

reduce the voltage ripple to very low value (0.2%). Fig.27 shows a comparison between the simulation results obtained with the conventional and the proposed controller according to the amount of voltage ripples as a percentage of the DC voltage using different capacitor values ranged from 100 to 2200 μF. It is clear that the capacitor voltage ripples obtained using 2200 μF capacitor can be obtained with only 100 μF using the proposed method.

Table 3 summarizes the results obtained from the experimental test setup. It is obvious that the proposed strategy is capable of minimizing the voltage ripples about 50% with different load current magnitudes using only a relatively low capacitor (220 μF).

IX. CONCLUSION

In this paper, a modified phase shift control algorithm of the Dual Active Bridge (DAB) based Modular Multilevel Converter Power Electronic Transformer (MMC-PET) has been presented. The main objective of this control strategy is to reduce the LVdc link capacitor voltage ripples resulting from unbalanced or single phase operation which consequently reduces the capacitor size and improves the power density. The proposed modification is to force the phase shift between DAB bridges to oscillate sinusoidally with the ripple frequency around fixed operating value. This modification makes the 2^{nd} harmonic power oscillations to be transferred across each DAB to the HVdc side. This helps in minimizing the LVdc side voltage ripples and consequently reduces the LVdc capacitor size and eventually increasing the power density.

The proposed phase shift controller is implemented by replacing the conventional PI controller with the Proportional Integral Resonant (PIR) controller. With this controller the output current is forced to track both the DC and the 2^{nd} harmonic command signals, then the capacitor current will be free of these oscillations. A comparison between PI, PR and PIR controllers has been done in terms of transient and frequency response to show the benefits of PIR controller over PI and PR controllers. It is concluded that PIR controller combines the advantages of both types, It is able to track reference signal when it contains both DC and AC components. Also it can rejects the sinusoidal load current disturbances resulting from unbalanced load conditions.

Different configurations of PET systems have been described. The system has been analyzed under unbalanced or single phase load conditions. The conventional and proposed DAB controller are discussed. A detailed switching model

of a single stage DAB unit is built on Matlab/Simulink to test the controller performance in different operating conditions. In balanced conditions, the simulation results gave a fast response against step load disturbances. Under unbalanced and single phase loads, the dc link capacitor voltage ripples have been reduced from 7.5% to 0.2% with only 100 μF capacitor thanks to the proposed controller. An experimental test setup is built to validated the theoretical analysis and the simulation results. The system performance has been tested with different load resistance values. It is found that, the proposed strategy reduces the LVdc side voltage ripples about 50% successfully with no need to increase the DC link capacitor. Therefore, it can be concluded that using the proposed controller allows to use low size film capacitor instead of large Aluminum electrolytic capacitors, consequently reduces the LVdc link capacitor size in each DAB unit and eventually reduces the whole system size.

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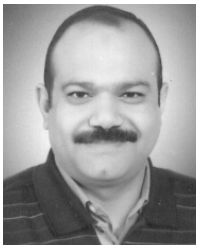

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