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RESEARCH ARTICLE

Combined Optimizer for Automatic Design of Machine Learning-Based Fault Classifier for Multilevel Inverters

V. SUDHA[1], K. VIJAYAREKHA[1], RAKESH KUMAR SIDHARTHAN[2], AND NATARAJAN PRABAHARAN[1], (Member, IEEE)

[1]Department of EEE, SASTRA Deemed to be University, Thanjavur, Tamil Nadu 613401, India
[2]Technical Manager, Engineering Research and Development Services (ERS), HCL Technologies Pvt. Ltd., Chennai, Tamil Nadu 600119, India

Corresponding author: K. Vijayarekha (vijayarekha@eee.sastra.edu)

ABSTRACT Fault detection and classification are fundamental requirements of multilevel inverters (MLIs) to ensure constant operation and improved reliability. Nowadays, the machine learning (ML) technique is utilized for fault diagnosis in MLIs due to its inherent features such as high accuracy, reduced computation time, and complexity. However, the rich availability of parts and classifiers in ML techniques demands a tedious investigation of every combination to design an optimal fault classifier. To overcome this problem, a combined optimiser is proposed to automate the ML-based classifier design, which involves selecting optimal features and classifier. Mean, total harmonic distortion, root mean square, and different harmonic orders (upto 12^{th} order) of the output voltage of MLI are considered as features and four different ML techniques like K-nearest neighborhood, decision tree, Naive Bayesian classifier, and support vector machines are considered. Ant Colony Optimization (ACO) is used to formulate a combinatorial optimization routine to maximize classification accuracy by optimal selection of features and classifier. The proposed technique is used to design a fault classifier for two different MLIs, such as Cascaded H-bridge MLI (CHBMLI) and Packed U cell inverter (PUC), during the fault conditions (open circuit and short circuit) to check the feasibility. Simulation results illustrate classification accuracy of 97.84% and 98.61% for CHBMLI and PUC, respectively. Experimental validation of the designed classifier on the inverter prototype is also carried out and illustrates 95.56% and 94.28% classification accuracy for CHBMLI and PUC, respectively.

INDEX TERMS Ant colony optimization, combined optimizer, fault classification, inverters, machine learning, multiple signal classification.

I. INTRODUCTION

Multilevel inverters (MLIs) have been utilized in high-power renewable energy sources [1] like windmills, photovoltaic [2]–[4] and fuel cells. Easy integration and fewer harmonics encourage their applications in many industries [5]. Among several topologies of MLIs, the cascaded H-bridge Multilevel inverter (CHBMLI) exhibits reliable performance in variable speed applications [6], [7] and renewable energy source integration [8]. Harmonic reduction in CHBMLI is achieved by increasing the levels, which leads to an increase in power semiconductor switches [9]. It increases the complexity and reduces reliability [10].

In CHBMLI, 38% of faults are occurred due to the malfunction of power semiconductor devices like IGBTs or MOSFETs [11]. Open circuits, short circuits, and gate misfires are common failures in power semiconductor devices that occur due to excess thermal and electric stress. Continuous operation of CHBMLI under such failure conditions leads to additional failures and causes serious effects [12].

For instance, failures in switching devices of CHBMLI supplying a traction motor in a hybrid electric vehicle will affect the speed control operation [13]. Downtime associated with inverter failures in industries affects the production

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cycle and causes a massive loss of cost per hour. Shielding circuits have been used in inverters to safeguard and decrease the impact of power semiconductor device failures. However, they may fail due to abnormal use, complicated circuit arrangement, disturbance in load, power system disturbance, and electromagnetic interference [14]. In recent times, a Packed U-Cell (PUC) type inverter has been preferred [15], which integrates the merits of a flying capacitor (F.C.) and CHBMLI inverter. PUC topology contains the minimum number of switches compared to the CHBMLI, making the system compact, more efficient, and cost-effective [16]. The compact PUC inverters have been utilized in critical applications like motor control, grid interfaces, and Flexible A.C. transmission system (FACTS). In variable speed drive, the fault occurs often owing to power semiconductor device failure. Therefore, the detection and classification of faults are essential. Reduction in switching components demands more reliability [17], and it necessitates fault diagnosis and tolerant strategies. Hence, a combined optimizer is developed in the proposed work to automate the design of ML-based classifier by selecting the optimal features and classification technique for both CHBMLI and PUC inverters.

Fault diagnosis technique based on output voltage or current is widely used and reliable for inverters. It enables the detection of fault location and identification of fault type [18]. Type of faults and its location are essential to plan mitigation procedures to overcome the failure [19]. Three types of fault diagnostics techniques, namely (i) model-based [20], (ii) knowledge-based [21], and (iii) data-driven based, have been discussed in the literature. An exact mathematical model has been required for defining the fault mechanisms in a model-based approach. Developing such a mathematical model for the complex structured inverter circuit is a tedious task. Moreover, these mathematical models are limited in solving particular fault problems [22].

Unlike the model-based method, the knowledge-based approach is widely applied in complex inverters, which does not depend on a precise mathematical model. It needs a complete knowledge (fault type and location) and interference engine. This method depends highly on the practical knowledge of the professionals, and the diagnosis accuracy relies on the significant amount of professional expertise available in the knowledge base [23]. Fuzzy-based support vector machine (SVM) has been reported [24] for higher accuracy than other approaches. However, this method takes more computing time to diagnose the fault and requires expert knowledge to tune the rules manually.

The availability of rich data encourages the usage of data-driven methods like machine learning (ML) approaches. Predominant of the ML techniques, namely Support vector machine (SVM) [8], Artificial Neural Network (ANN) [25], and K-nearest neighbor (KNN) [26], belong to the data-driven approach. Fault diagnosis using intelligent data-driven algorithms has turned out to be a research hotspot in recent years [27], [28]. Fault diagnosis technique fundamentally demands in-depth knowledge about the operations of the inverters to understand its working under normal conditions. Any deviations from its normal operations have to be analyzed to determine the fault type and severity. Hence, the inverter design-specific nature of fault detection systems demands significant effort and expert knowledge. ML technique emerges as the mitigation strategy to automatically learn the correlation between the features and faults. ML tends to eliminate the need for expert knowledge on inverter operations.

These ML techniques have been incorporated into feature extraction procedures to increase fault diagnosis performances. Statistical techniques, Fast Fourier Transform (FFT),wavelet transforms [29], [30], and Principal Component Analysis (PCA) has been used to extract the features for fault detection. The number of fault classes may increase depending on the number of switches utilized in developed multilevel inverter for generating the required output voltage level. Due to the increase in fault classes, more features may require for fault classification.

A complex neural network with 40 input (features) neurons has been utilized to detect open circuit fault in MLI using FFT signals [31]. Genetic algorithm (GA) and PCA has been used to reduce the required features and complexity of the classifiers. A fault diagnosis approach based on the FFT-PCA-multiclass relevance vector machine has been developed to diagnose the open circuit faults in CHBMLI [32]. Operator knowledge has also been used to select the required features using PCA [31], [32]. Limiting the number of fault classes is another approach to reducing the classifier complexity. Open and short circuit faults were classified using FFT-based features [33].

The availability of vast features and classifiers in ML enables a large number of combinations which need to be investigated to design the best fault classifier. Though techniques like GA., PCA, and random forest algorithm have been used for optimal feature selection, the choice of classifiers remains biased. The lesser training time of shallow ML-based classifiers like SVM, KNN, NBC, and decision trees allows the use of an optimization routine for the combined selection of features and classifier. Hence, a combined optimizer is proposed in this work to simultaneously select both the features and classifier, which is required to design a fault classification method for CHBMLI and PUC. A search space comprising static and harmonic features extracted from the output voltage along with several ML-based classifiers is formulated. Ant colony optimization (ACO) is also used to select the unique combination of features and classifier from the search space to maximize the classification accuracy.

Major contributions of the proposed work are as follows

(i) Design of combined optimizer using ACO to select the optimal features and classifier without manual interventions.

(ii) Formulate the cost function to provide better classification accuracy.

(iii) The proposed method is suitable for fault diagnosis in open circuit and short circuit fault conditions to any MLI configuration.

(iv) Simulation has been carried out during healthy and faulty conditions (open circuit and short circuit) of CHBMLI and PUC.

(v) Experimental validation of the proposed design procedure to design a classifier for fault classification in CHBMLI and PUC type inverter.

The rest of the paper is organized as follows: Section 2 describes the related background required for problem formulation. It explains the operation and fault characteristics of CHBMLI and PUC inverters. Section 3 provides a brief introduction to feature extraction and the classifier considered in this study. Section 4 explains the proposed design of an ACO-based combined optimizer for selecting features and classifiers. Section 5 shows the experimental results and comparative analysis, and Section 6 concludes this work with future direction.

II. RELATED BACKGROUND

Multilevel inverters are widely used in A.C. drives, non-pollutant renewable energy integration, and active power filters. In Multilevel inverter families, cascaded H-bridge Multilevel inverters have gained significant attention because they satisfy the medium voltage and high-power requirements in industries but require more semiconductor devices. This drawback is overcome in the PUC inverter. PUC inverters need lesser semiconductor switches to attain the same voltage level as CHBMLI. CHBMLI and PUC inverters are chosen in the proposed work due to their distinct features.

A. ARCHITECTURE OF CHBMLI

A single-phase CHBMLI is connected to the motor load, as illustrated in Figure 1. It generates a five-level output voltage by combining the two H-bridge inverter modules in series with the separate D.C. source in symmetric conditions. Each H-bridge inverter module consists of 4 IGBT switches marked as T_1, T_2, T_3, T_4, and T_5, T_6, T_7, and T_8. The output voltage of CHBMLI is produced by the combination of voltage generated in the two modules.

The switching pulses necessary for IGBT switches are generated by using the Alternative Phase Opposition Disposition (APOD) technique, as shown in Figure 2. The carrier frequency and modulation index of a sinusoidal signal are set as 3 kHz and 0.8, respectively. In this technique, each triangular waveform is out of phase by 180^o with its alternate waveform, and a sinusoidal signal is kept as a reference. To generate an output voltage with x levels, the MLI uses $x - 1$ triangular waveforms. The switching scheme of the CHBMLI is shown in Table 1. The number of H-bridge (N_H) used in the MLI determines the output voltage level (L_v) as in (1), which in turn describes the smoothness of the generated A.C. voltage. The increase in the number of H-bridge and their associated switching components necessitates the need for fault-tolerant systems in MLI.

$$L_v = 2N_H + 1 \tag{1}$$

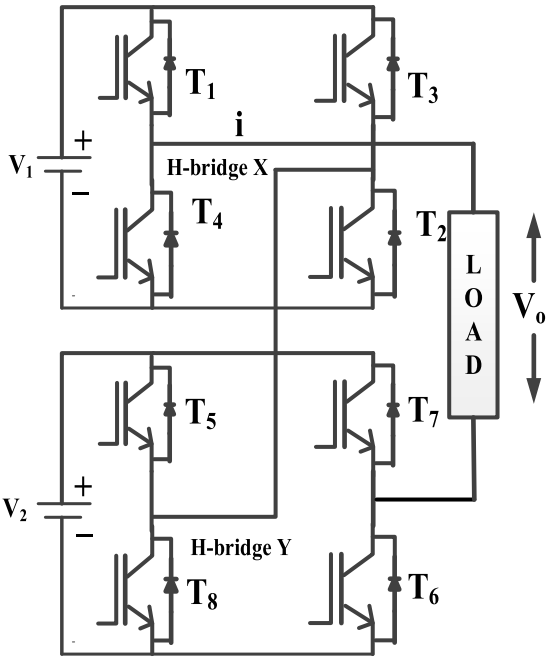

FIGURE 1. Structure of single-phase 5-level CHBMLI.

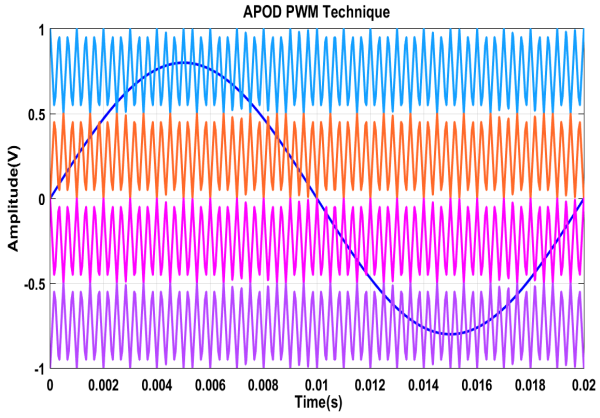

FIGURE 2. APOD PWM scheme.

TABLE 1. Switching scheme for the proposed topology.

Conducting devices	0V	V	2V	-V	-2V
T_1	1	1	1	0	0
T_2	0	1	1	0	0
T_3	1	0	0	1	1
T_4	0	0	0	1	1
T_5	1	1	1	1	0
T_6	0	0	1	0	0
T_7	1	1	0	1	1
T_8	0	0	0	0	1

The operating modes of the CHBMLI are discussed in [34]. Initially, switches T_1, T_2, T_5, and T_6 are turned ON and the other four switches T_3, T_4, T_7, and T_8 are turned OFF, to get an output voltage level of $+2V_{dc}$. To get the $+V_{dc}$

level at output voltage, the switches T_1, T_2, T_8, and T_6 are turned ON and the other switches namely T_3, T_4, T_7, and T_5 are set to OFF. Finally, switches T_2, T_4, T_6, and T_8 are turned ON and all the other switches are turned OFF. So that no current will flow in the power circuit creating a level of zero output voltage. Thus, all the switches in the CHBMLI play a vital role in determining the waveshape of the output voltage. It necessitates a need to diagnose and ensure the health of these switches for reliable power delivery using the CHBMLI.

B. ARCHITECTURE OF PUC INVERTER

The main merits of the PUC inverter are the minimum number of active switches and the minimum requirement of gate drivers. The component count of the PUC inverter is compared with other popular inverters like CHB, NPC, and F.C., and the component count comparison is shown in Table 2 [35].

A single-phase 5-level PUC inverter is shown in figure 3. It consists of two dc sources in symmetric condition and 6 power semiconductor switches. It is worth mentioning that T_4, T_5 and T_6 are the complementary switches of T_1, T_2 and T_3, respectively. The operating modes and the advantage of this topology are discussed in [36]. The switching states of this topology for generating the five-level output voltage are shown in table 3.

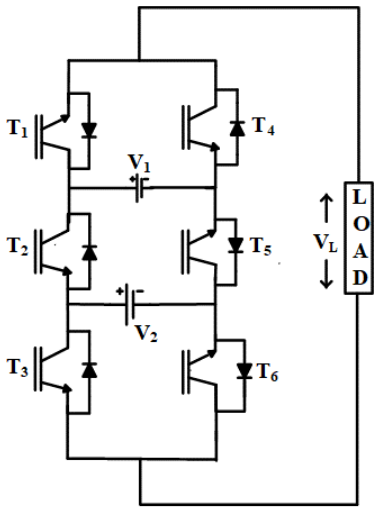

FIGURE 3. Structure of the PUC5 level inverter.

TABLE 2. Components counts of single-phase multilevel inverter.

Multilevel inverter type	DC source	Flying capacitor	Clamped diode	Active switch	Total Component
CHBMLI	2	0	0	8	10
NPC MLI	1	4	6	8	19
FC	1	3	0	8	12
PUC	2	0	0	6	8

PUC inverter turns ON the switches T_1, T_5, and T_6, and switches T_2, T_3, T_4, and T_8 are turned OFF to get an output voltage level of $+2V_{dc}$. A $+V_{dc}$ is obtained by turning ON the switches T_1, T_5, and T_3, and all the other switches like T_2, T_4, and T_6 are set to be OFF. The current in the power circuit is made as zero by turning ON switches T_1, T_2, and, T_3, and all the other switches T_4, T_5, and T_6 are turned OFF. It enables to have the output voltage at level zero.

TABLE 3. Switching states of puc 5 level inverter.

Conducting Devices	2V	V	0	-V	-2V
T_1	1	1	1	0	0
T_2	0	0	1	0	1
T_3	0	1	1	1	1
T_4	0	0	0	1	1
T_5	1	1	0	1	0
T_6	1	0	0	0	0

The structure of the generalized fault diagnosis approach [32] for inverters is illustrated in Figure 4. MLI tends to provide a smooth sinusoidal waveform using multiple D.C. sources by generating a periodic switching pattern. In a fault diagnosis approach, the output voltage signal of MLI is measured because these signals consist of reliable information and are independent of load variations. The measured signals are preprocessed and the required features are extracted. Statistical features like % THD, RMS, Mean, and frequency domain features like harmonic distortions are extracted from the measured voltage signal. These features are extracted from MLI and given as input to the fault classifier. A fault classifier uses these extracted features to determine the fault class.

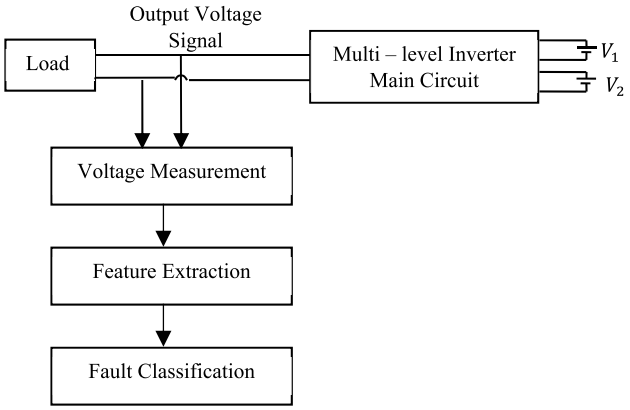

FIGURE 4. Structure of the generalized Fault diagnosis approach.

III. METHODOLOGY

The design of an ML-based fault classifier involves various steps, as described in Figure 5. The ML-based classifier requires a data set describing various fault conditions in the inverter. Hence, various faults are induced into the inverter, and the corresponding output voltages are acquired. Features are extracted from the acquired output voltage signal, and

the data set is prepared with the corresponding fault class. A training dataset is used to train the ML-classifier, and another set of datasets are used to test the trained classifier. The testing performance is evaluated using standard performance metrics and deployed. The choice of features and classifier plays a vital role in designing an efficient fault classifier, which has been investigated in this work.

A. DATASET PREPARATION

The output voltage waveform is considered a diagnostic parameter to diagnose the fault in the proposed technique, whereas the output current changes with respect to the different loads. Faults are induced in each switch of the inverter and its corresponding output voltage waveform is acquired.

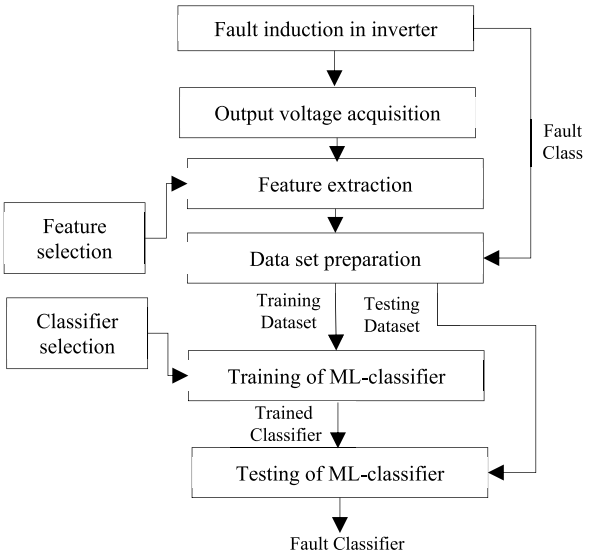

FIGURE 5. Design process for ML-based fault classifier.

Healthy condition, open-circuit, and short-circuit faults are induced with varying modulation indexes. For instance, at a certain value of modulation index ($m = 0.8$), the output voltage waveforms for healthy conditions, open-circuit faults of switches T_1 to T_4 and short-circuit faults of T_5 to T_8 in CHBMLI are observed as in Figure 6. A distinctive pattern of the output voltage waveforms is observed for different switch fault conditions, which serve as a reliable marker for fault classification. Similarly, the open-circuit and short circuit faults are created in each switch of the PUC topology, and the corresponding output voltage waveforms are observed as in Figure 7. The voltage waveforms observed during healthy and faulty conditions of each switch have unique characteristics that provide a reliable marker for fault classification. It is observed that the positive half cycle and the negative half cycle are completely diminished due to the open circuit fault of T_1 and T_3 respectively. Hence the failure in these switches greatly affects the performance of the PUC which needs to be diagnosed quickly to avoid serious failures.

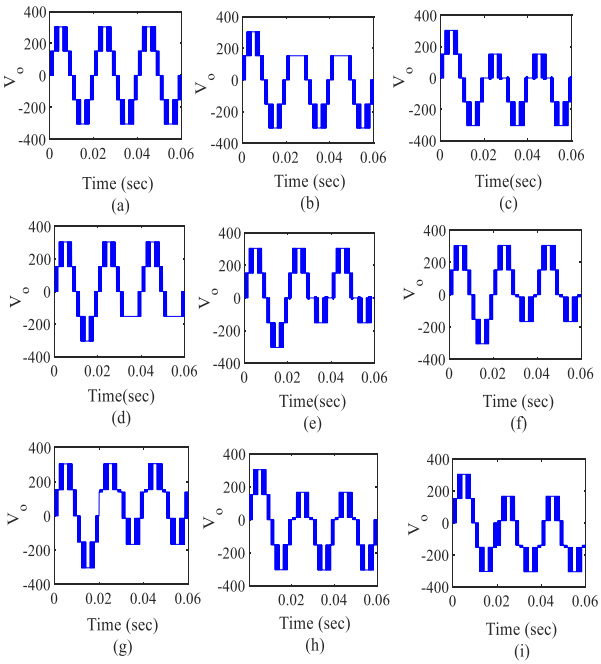

FIGURE 6. Output voltage waveforms of CHBMLI: (a) Healthy state (b) Open circuit fault in T_1 (c) Open circuit fault in T_2 (d) Open circuit fault in T_3 (e) Open circuit fault in T_4 (f) Short circuit fault in T_5 (g) Short circuit fault in T_6 (h) Short circuit fault in T_7 (i) Short circuit fault in T_8.

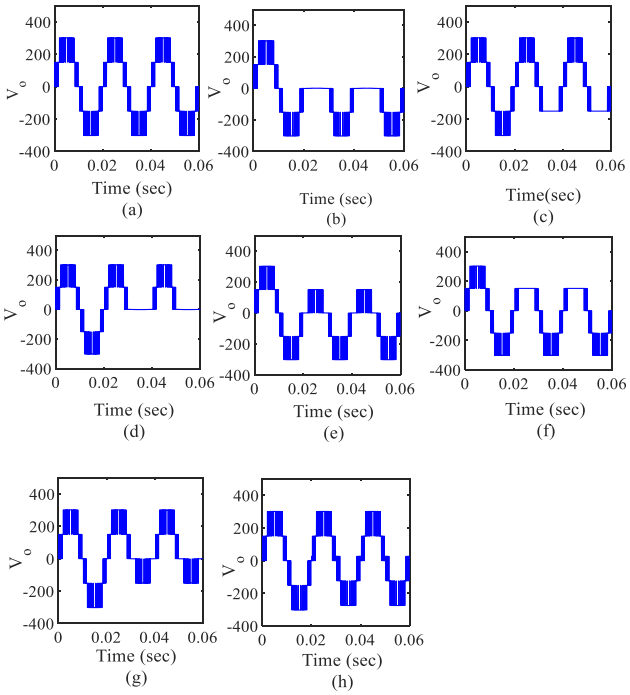

FIGURE 7. Output voltage waveforms of PUC: (a) Healthy state (b) Open circuit fault in T_1 (c) Open circuit fault in T_2 (d) Open circuit fault in T_3 (e) Open circuit fault in T_4 (f) Open circuit fault in T_5 (g) Open circuit fault in T_6 (h) Short circuit fault in T_1.

B. FAULT CLASS DESCRIPTION

This section describes the various faults considered in this study. The main reason for malfunction in CHBMLI and PUC is the failure of the power semiconductor devices.

It may lead to open or short circuit faults. Hence, both open circuit and short circuit faults in CHBMLI and PUC are analyzed. The current supplied to the load is interrupted during open-circuit (O.C.) faults and leads to significant distortion in the output load waveforms. A high current flow is induced with a short-circuit (S.C.) fault by making zero voltage drop across the switch. Unlike open circuit faults, short circuit faults cause catastrophic failure in the inverter even in a shorter time.

All the switches in the CHBMLI (8 switches) and PUC (6 switches) are considered in the proposed work. Each switch is subjected to O.C. and S.C. conditions to simulate various fault classes along with normal operating conditions as one class, as in Table 4 for CHBMLI and Table 5 for PUC.

TABLE 4. Ault and category labels of CHBMLI.

Type of fault	Labels
Normal	1
T_1 XO.C. fault	2
T_2 X O.C. fault	3
T_3X O.C. fault	4
T_4X O.C. fault	5
T_5 X O.C. fault	6
T_6 X O.C. fault	7
T_7 X O.C. fault	8
T_8 X O.C. fault	9
T_1X S.C. fault	10
T_2 X S.C. fault	11
T_3 X S.C. fault	12
T_4 X S.C. fault	13
T_5 Y S.C. fault	14
T_6 Y S.C. fault	15
T_7 Y S.C. fault	16
T_8 Y S.C. fault	17

TABLE 5. Fault and category labels of PUC.

Type of fault	Labels
Normal	1
T_1 XO.C. fault	2
T_2 X O.C. fault	3
T_3X O.C. fault	4
T_4X O.C. fault	5
T_5 X O.C. fault	6
T_6 X O.C. fault	7
T_1X S.C. fault	8
T_2 X S.C. fault	9
T_3 X S.C. fault	10
T_4 X S.C. fault	11
T_5 Y S.C. fault	12
T_6 Y S.C. fault	13

C. FEATURE EXTRACTION

Any ML-based classification consists of two steps, namely, feature extraction and classification. In the feature extraction step, the feature required for classification is extracted from the measurement signal. Features define the abstraction of the measurement signal and convey reliable information used for classification. A unique combination of features for a particular class is often preferred, which enables an accurate classification. Hence, the choice of features plays a vital role in determining the classification performance of the ML-based fault classifier.

In this work, three static features (Mean, % THD, VRMS) and eleven harmonic features (individual harmonic order up to 12th order) are extracted from the output voltage as described in Table 6. These features have a higher degree of detectable variations during the faulty conditions and contain reliable markers on the fault type. Mean value provides a D.C. shift encountered and loss of symmetrical pattern during the faulty conditions of MLI.

TABLE 6. Features used for fault classification.

Feature	Formula
THD	$THD = \sqrt{\left(\frac{V_{rms}}{V_{1rms}}\right)^2 - 1}$
V_{RMS}	$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} V_s^2 \, d(\omega t)}$
Harmonics	$f(\omega t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} (a_n cos n\omega t + b_n sin n\omega t)$

The RMS value detects the peak value of distortions in the output voltage. Noise introduced by the switching faults provides significant variations in % THD. The first 11 harmonic orders (H_{2-12}) of the output voltage are also extracted using FFT analysis and used as features. If the dominant harmonics are present in the lower order, it affects the system performance and also, the designing of filters is difficult. Therefore, the individual harmonic orders up to the 12^{th} order are considered in this work.

D. ML-BASED CLASSIFIER

In the proposed work, four different classifiers, namely, decision tree (D.T.), K-nearest neighbor (KNN), Naive Bayesian classifier (NBC), and support vector machines (SVM) are considered in this work. The choice of these classifiers is strongly encouraged by the literature for fault classification applications.

KNN is a supervised learning algorithm widely used for regression and classification applications. This algorithm tends to cluster the identical data that are near in proximity. During learning, the rule for partition of the whole training data is carried out and allots a particular label for the cluster. For unknown data, the distance between the unknown and the training data set is computed. The unknown data is classified using the minimum distance criterion. KNN exhibits a higher level of accuracy and excellent stability [37]. It is used to identify the O.C. faults in a cascaded Multilevel inverter [26]. It tends to select features that are close neighbors and forms a cluster corresponding to the fault type. Its non-parametric approach makes it a preferred choice for data-driven classifier design.

The decision tree (D.T.) algorithm has a top to bottom approach that searches the features to decide on the fault type. It has a tree-like structure, where the features of the data set are represented by an internal node, decision rules are represented by branches, and the outcome is represented by a leaf node. This tree is mainly preferred for resolving classification problems. D.T. has a successive model that unites a sequence of the basic test proficiently and cohesively [38]. An optimal classification tree is constructed to detect and diagnose the fault. It is similar to a flowchart but has a tree-like structure.

SVM uses statistical learning theory to construct classifiers. It tends to divide the features in a hyperplane to understand their fault specific characteristics. Hyperplane is created with extreme vectors, which describes the variations across features. It is a supervised learning model with accompanying learning algorithms that are used to examine features and recognize patterns across each fault type. It is widely used in applications like classification, regression models, and pattern recognition. It can overcome the limitations in data dimensionality and inadequate samples. This makes it ideal for fault classification in inverters, where wider range of fault class is encountered. SVM is use to diagnose the O.C. faults in cascaded Multilevel inverters [8].

Naïve Bayesian classifier (NBC) is one of the quickest learning algorithms and able to handle larger number of classes. Simple in construction, efficient classification and immune to noise in data sets are some of the metrics that encourages the used of NBC for fault classification. It is a supervised probabilistic classifier predominantly used for classification [39]. Knowledge-based nature of NBC encourages its usage for both binary and multiclass pattern classification. It estimates the fault class based on the likelihood of the features. It is used to decide the possibility of a premise with previous information extracted from the training set. It relies on conditional probability estimated using the Bayes theorem is given as in (2).

$$\mathrm{P(A|B)} = \mathrm{P(A|B)P(A))/P(B)} \tag{2}$$

NBC is used for image classification in [40] due to its greater classification accuracy and fast computing time, which makes it dependable in real-time applications [41], [42].

E. PROPOSED COMBINED OPTIMIZER FOR ML-BASED FAULT CLASSIFIER DESIGN

The design of an ML-based fault classifier involves the selection of optimal features and classification technique, which has been investigated in this work using a combined optimizer as in Figure 8. The combined optimizer tends to select the optimal features from the set of features described in Section C. These features are extracted from the output measured voltage (V_m) acquired from the faulty inverter. It also selects one ML classifier from the given set of classifiers as described in Section D. The optimal selection of features and classifier is governed by evaluating the classification accuracy using confusion matrix analysis. The proposed combined optimizer is designed using ACO based combinatorial optimization technique.

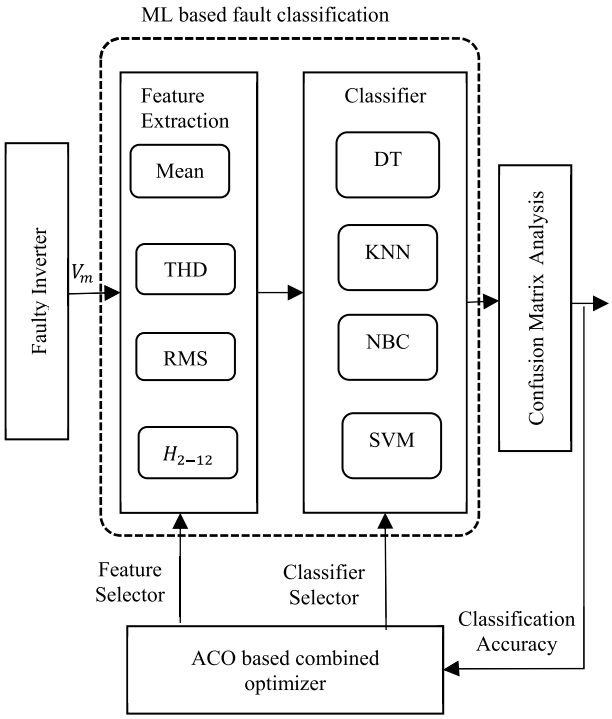

FIGURE 8. Proposed combined optimizer.

ACO is one of the popular and reliable techniques for solving combinatorial optimization problems [43]. It is a metaheuristic technique that was inspired by the communicative and navigation behavior of ants to solve their path planning problems. Ants tend to define an optimal path that can be traced to bring in the food to their nest. They define the shortest path by avoiding obstacles through their collaborative nature. Ants deposits pheromone (a scented chemical substance) on their navigation path, which leaves traces for other ants to recognize. This deposited pheromone is used by the ants to determine the optimal path by their foraging behavior. This natural-inspired technique is mathematically formulated as ACO for solving various applications.

In the proposed work, an ACO-based combinatorial optimization problem is used to determine the optimal selector ant, which can minimize the cost function. The cost function is formulated in terms of classification accuracy, which is evaluated using a confusion matrix and as a function of selector ant, as illustrated in Figure 9.

The selector ant has information to select the optimal features (F_S) and classifier (c_S) from the given set of features (F) and classifiers (C), respectively. In the proposed work, about fourteen features ($M = 14$) and five classifiers ($N = 5$) are considered as in (3) and (4), respectively. Each selector ant (A_S) has the mask formulated using '1s' and '0s' of length ($N + m$) as in (5). It is used as a gating signal for feature and classifier selection. For feature selection, a '1' indicates

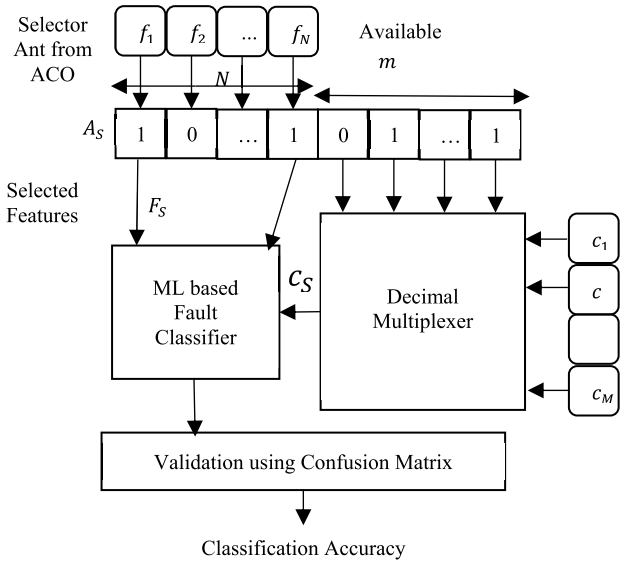

FIGURE 9. Objective function of combined optimizer.

the closure of the gate, which allows the particular feature to be used for training the classifier, and a '0' opens the gate restricting the features as in (6). Unlike features, only one classifier is selected using the (m) gating signals from the selector ant. The classifier gating signals ($m = \lceil log_2 M \rceil$) is used by the decimal decoder to select one classifier from the available classifier set (M). The decimal decoder tends to convert the binary gating signal into a corresponding decimal to select the classifier as in (7). The selected classifier (c_s) is trained using the training data of the selected features (F_S^{tr}) to design an ML-based fault classifier (Fc) as in (8).

$$F = \{f_1, f_2, \ldots\ldots, f_N\} \tag{3}$$

$$C = \{c_1, c_2, \ldots\ldots, c_M\} \tag{4}$$

$$A_s = \{a_1, a_2, \ldots, a_N, \ldots, a_{N+m}\} \tag{5}$$

$$F_S = \{f_i | a_i = 1, i \leq N, f_i \in F\} \tag{6}$$

$$c_s = \left\{ c_i | i = \sum_{j=N+1}^{N+m} a_j 2^{j-1}, \; N+1 < i \leq N+m, c_i \in C \right\} \tag{7}$$

The classification performance of the trained classifier is evaluated in terms of classification accuracy to formulate the cost function. The predicted fault class (Cl_P^i) for the given feature set is determined using the trained classifier as in (9). Then, the predicted class is compared with the actual fault class (Cl_A^i) to determine the classification accuracy (CA_t) in percentage as in (10). The classification accuracy for training (CA_{tr}) and testing data (CA_{te}) are calculated, and weights added. The weights provide the importance of each classification accuracy in evaluating the cost function (CF) as in (11). Thus, the objective of the proposed combined optimizer is to determine the selector ant (A_f), which can minimize the cost function with the choice of features and classifier as in (12).

$$Fc = Train(c_s, F_s^{tr}) \tag{8}$$

$$\mathrm{Cl_P^i} = Predict(Fc, F_S^i) \tag{9}$$

$$\mathrm{CA_t} = \frac{1}{N_t} \sum_{i=1}^{N_t} \left\{ 1 | Cl_A^i = Cl_P^i \right\} \times 100\% \tag{10}$$

$$\mathrm{CF} = w_{tr}(100 - CA_{tr}) + w_{te}(100 - CA_{te}) \tag{11}$$

$$\mathrm{A_f} = argmin_A \, (CF | F_s \subseteq F, c_s \in C) \tag{12}$$

IV. RESULTS AND DISCUSSION

The proposed work aims to formulate an automated technique to design an ML-based fault classifier. It majorly involves the choice of features and the classifier, which are determined using a multi-objective ACO algorithm. It tends to choose the optimal features and the ML classifier that maximizes the classification accuracy for fault classification.

The performance of the proposed design technique is evaluated using two types of Multilevel inverters (CHBMLI and PUC). The switches in the Multilevel inverter are subjected to O.C. and S.C. faults, which need to be identified to provide proper mitigation. Features like Mean value, RMS value, Harmonic order, and %THD of the output voltage signal under healthy, O.C., and S.C. faulty circumstances are extracted. The extracted features are labeled to create the data set required for training the ML classifier. The data set is segregated to have 80% of data for training and 20% of data for testing the classifier, as in Table 7.

TABLE 7. Dataset preparation.

Name	CHBMLI	PUC
Total No. of labels	17	13
Healthy condition	1	1
OC fault condition	8	6
SC fault condition	8	6
Dataset Size	697	533
Training data size	558	426
Testing data size	139	107
Type of data set	Balanced	Balanced
Data size per class	41	41

Four widely used ML-based classifiers, namely D.T., KNN, NBC, and SVM, are considered in this study, and the ACO is responsible for choosing any one optimal classifier out of them. The choice in features and classifier across various iterations of the proposed combined optimizer are acquired as in Figures 10 to 13, respectively. The actual choice of features and classifier of all the ants and choice of best ant is observed. It is indicated that the fault classifier of CHBMLI uses a higher number of features at initial iterations and settles at seven optimal features. Similarly, among the four classifiers, a close competition exists between the choice of NBC and KNN classifiers. However, KNN is chosen to be the optimal classifier to detect faults in CHBMLI.

During the automatic design of the fault classifier for PUC, a minimal number of features are selected during initial

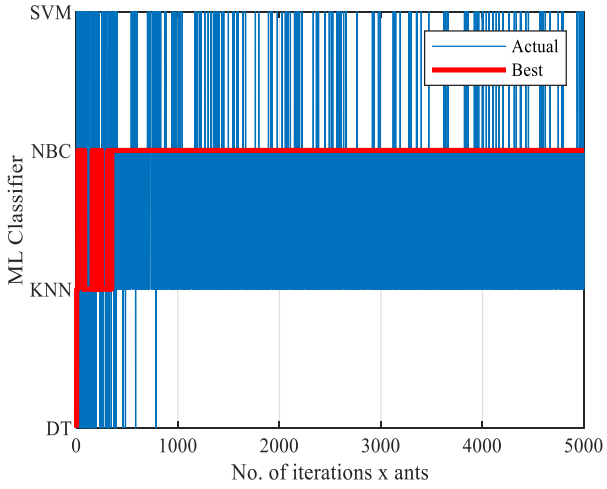

FIGURE 10. Selection of classifier for CHBMLI.

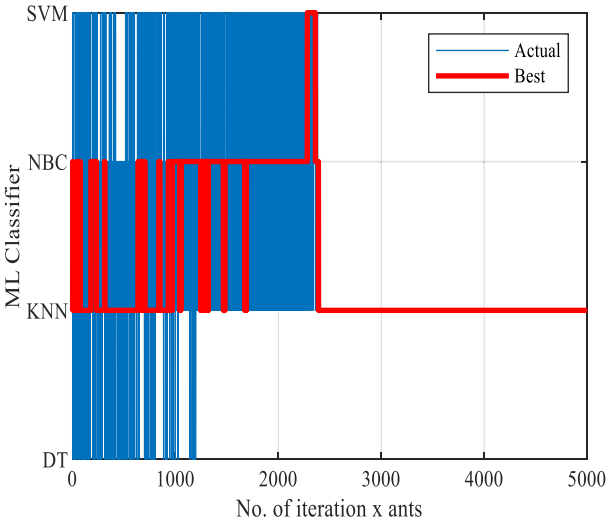

FIGURE 11. Selection of classifier for PUC.

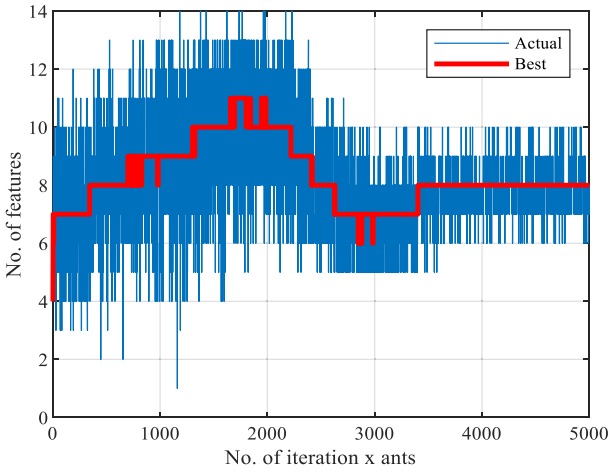

FIGURE 12. Optimal feature selection for CHBMLI.

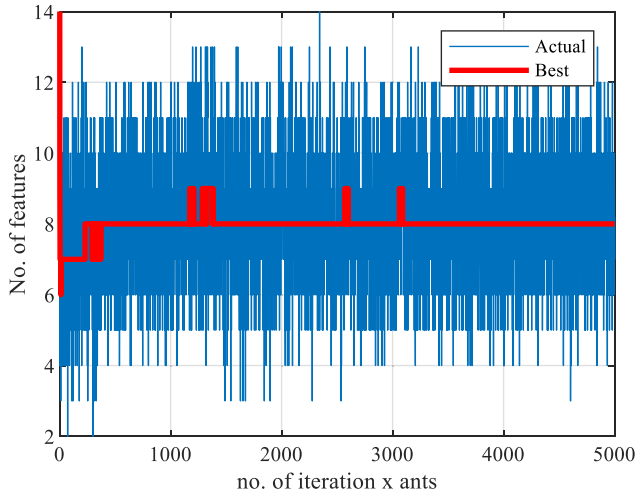

FIGURE 13. Optimal feature selection for PUC.

TABLE 8. High-level confusion matrix for CHBMLI.

Labels		Predicted Class		
Actual Class	NO Fault	33 (8)	0(0)	0(0)
	OC Fault	0(3)	264(64)	0(0)
	SC Fault	0(0)	0(0)	264(64)
Classification Accuracy in %		100(100)	100	100(100)

*( ) – Testing data

iterations, and features are increased to maximize the classification accuracy. Finally, optimal eight features are selected. NBC is selected as the fault classifier, which provides maximum classification accuracy.

The designed ML-based classifier with optimal selected features is evaluated using a confusion matrix at various levels. Initially, the fault classes are grouped as no faults indicating a health inverter, O.C. faults, and S.C. faults. It is observed that the KNN-based fault classifier used in CHBMLI is capable of classifying the fault type accurately without any error, as indicated by the confusion matrix in Table 8. Whereas in PUC, the NBC-based fault classifier misclassifies one O.C. fault as an S.C. fault leading to the classification accuracy of 98.6%, for testing data, as indicated by the confusion matrix in Table 9.

The switch-specific fault classification performance is also evaluated in Tables 10 and 11, which tend to identify the type of fault and the corresponding faulty switch. The data responsible for the misclassification and its classification accuracy is also tabulated. It is observed that in one instance, the S.C. fault occurred in T_9 switch of PUC is predicted as it occurred in T_{10}. Similarly, in three instances of testing data, the fault classifier failed to detect the faulty switch in the CHBMLI inverter.

A. COMPARISON WITH CONVENTIONAL TECHNIQUE

The performance of the ML-based classifier designed using the proposed combined optimizer is compared with the

TABLE 9. High-level confusion matrix for PUC.

Labels		Predicted Class		
		NO Fault	O.C. Fault	SC Fault
Actual Class	NO Fault	29 (12)	0(0)	0(0)
	OC Fault	0(0)	174(72)	0(0)
	SC Fault	0(0)	0(1)	174(71)
Classification Accuracy in %		100(100)	100(100)	100(98.6)

TABLE 10. Performance analysis of CHBMLI fault classifier.

Type of data	Actual Class	Predicted Class	No of misclassification data	%Accuracy
Training Data	--	--	0	100%
Testing Data	T4[OC]	T5 [OC]	1	97.80%
	T6[OC]	T2[OC]	1	
	T8[OC]	T7 [OC]	1	

TABLE 11. Performance analysis of PUC fault classifier.

Type of data	Actual Class	Predicted class	No of misclassification Data	% Accuracy
Training Data	--	--	0	100%
Testing Data	T_9 [SC]	T_{10} [SC]	1	98.6

conventional classifier designed with no feature and classifier selection. With no feature selection procedure available, all features are used to design the conventional classifier. Four ML classifiers considered in this study are used individually to design the fault classifier for both the inverters as described in Tables 12 & 13. The training and testing classification accuracy is evaluated and is considered as performance metrics. It is observed that the proposed combined optimizer is capable of selecting optimal features and a classifier that can significantly improve the classification accuracy as compared with the conventional classifier design.

It is observed that the D.T. and SVM have a lesser level of classification accuracy with the use of conventional design techniques. KNN suffers overfitting with higher classification accuracy on the training dataset. But fails to classify the testing dataset accurately. NBC provides higher performance to detect the fault in CHBMLI. However, with the use of optimal features selected by the proposed design, NBC exhibits a significantly higher performance as compared with other conventional techniques as described in Table 12. Similarly, KNN is capable of detecting the fault in the PUC inverter accurately with the use of all features in conventional design. The proposed design tends to select KNN with eight optimal features enabling it to have a higher level of accurate fault detection as described in Table 13.

TABLE 12. Performance comparison of CHBMLI fault classifier.

Type of classifier design	Features	ML classifier	% Classification Accuracy Training Dataset	Testing Dataset
Conventional design	All	DT	91.5	90.3
	All	SVM	94.8	92.8
	All	KNN	100	92.6
	All	NBC	96.2	93.8
Proposed design	8	NBC	100	97.8

TABLE 13. Performance comparison of PUC fault classifier.

Type of classifier design	Features	ML classifier	% Classification Accuracy Training Dataset	Testing Dataset
Conventional design	All	DT	97.8	96.5
	All	SVM	96.9	95.8
	All	KNN	98.4	94.2
	All	NBC	97.8	95.1
Proposed design	8	KNN	100	98.6

B. EXPERIMENTAL ANALYSIS

A laboratory-scaled prototype is developed for the selected MLIs such as CHBMLI and PUC separately, as in Figure 14. The MLIs are constructed using IGBT switches, a TPL350 driver, and two D.C. sources. These MLIs are capable of generating a five-level output voltage. The switching signals are generated using a real-time controller (FPGA) by incorporating the APOD PWM technique. The prototype is equipped with a voltage sensor to acquire the output voltage for the various modulation indices. It also has a 3196-power quality analyzer to extract the features from the acquired output voltage.

In the experimental setup, healthy and O.C. faults are only investigated due to the practical difficulties in realizing S.C. faults. The O.C. fault is created by disconnecting the gate signal from the corresponding switch and the output voltage is measured at various modulation indices ranging from 0.6 to 1. The output voltage acquired from the experimental setup during healthy and O.C. faulty conditions indicates observable changes as in Figure 15 for the modulation index 0.8. The O.C. fault in the switch T_1 causes the voltage to lose its positive peak value making it biased towards the negative cycle and vice versa during O.C. fault at the switch T_2 of CHBMLI. A similar change in output voltage is observed in the PUC inverter also, as in Figure 16.

Table 14 represents the accuracy of experimental dataset values for CHBMLI and PUC using a confusion matrix. The experimental results illustrate a reliable classification accuracy of 95.56% and 94.31% for CHBMLI and PUC respectively.

Further, the experimental setup is compared with the simulation studies in terms of feature extraction and fault classification. The quality of voltage measurement and the

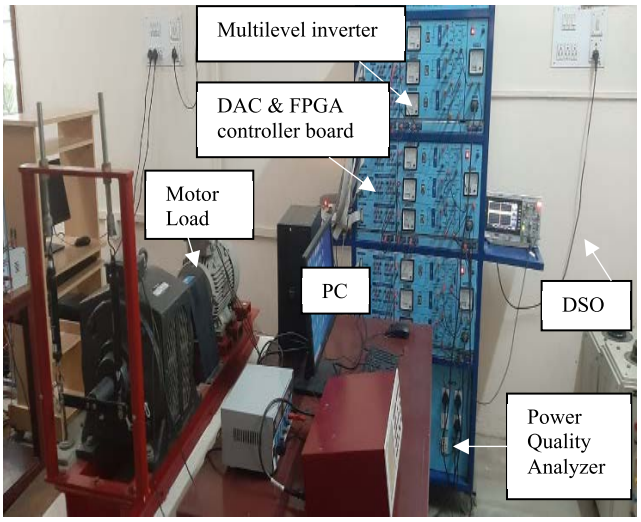

FIGURE 14. Experimental setup of MLIs.

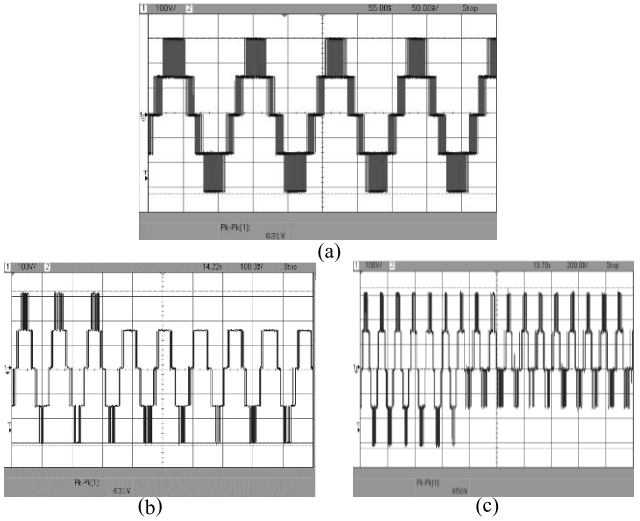

FIGURE 15. Output voltage waveforms of CHBMLI: (a) Healthy state (b) Open circuit fault in T_1 (c) Open circuit fault in T_2.

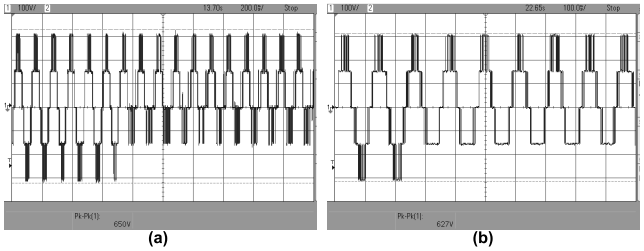

FIGURE 16. Output voltage waveforms of PUC: (a) Open circuit fault in T_2 (b) Open circuit fault T_6.

corresponding features extracted during experimental implementation are evaluated by comparing with simulation. Mean absolute error (MAE) as described in (13) is used as a performance metric for comparison. It tends to calculate the deviation between the features extracted from the simulated

TABLE 14. Performance analysis in the experimental setup.

Inverter	Actual Class	Predicted Class	No. of data	% Accuracy
CHBMLI	T_2 [O.C.]	T_8 [O.C.]	1	95.56 %
	T_7[O.C.]	T_1 [O.C.]	1	
PUC	T6[OC]	T2 OC]	1	94.28%
		T3[OC]	1	

TABLE 15. Comparative analysis of features.

Feature	MAE in %	
	CHBMLI	PUC Inverter
THD	0.82	0.74
V_{RMS}	0.34	0.26
Harmonics Order - H_2	1.32	1.05
Harmonics Order – H_3	0.98	1.21
Harmonics Order – H_4	2.06	1.65
Harmonics Order – H_5	1.21	0.98
Harmonics Order – H_6	2.24	2.11
Harmonics Order - H_7	2.43	2.05
Harmonics Order – H_8	1.98	1.76
Harmonics Order – H_9	2.86	2.24
Harmonics Order – H_{10}	3.04	2.78
Harmonics Order – H_{11}	3.16	3.02
Harmonics Order – H_{12}	3.78	3.32

TABLE 16. Comparative analysis of classifier.

	% Classification Accuracy	
	CHBMLI	PUC Inverter
Simulation	97.84	98.61
Experimental Setup	95.56	94.28

inverter ($F^{i,j}_{s\_sim}$) and the experimental setup ($F^{i,j}_{s\_exp}$). The MAE is expressed in terms of percentage for all the available features (N_f – number of features) as listed in Table 15. It is observed that the THD and RMS feature have lesser deviations. The harmonic order will have increased deviations at higher orders. The classification accuracy for the experimental setup is compared with the simulation as described in Table 16. Minor deviation in classification accuracy is observed due to the noise associated with the measurement signal and features extracted from the experimental setup. Analysis indicates a significant detection accuracy making the proposed design ideal for real-time implementation.

$$MAE_j = \frac{1}{N_d^j} \sum_{i=1} {N_d}^j \frac{\left| F^{i,j}_{s\_sim} - F^{i,j}_{s\_exp} \right|}{F^{i,j}_{s\_sim}} \times 100\% | j \in \left[1, N_f\right] \tag{13}$$

V. CONCLUSION

In this paper, a fully automated methodology to design a machine learning-based classifier is proposed using a combined optimizer. A combined optimizer tends to select optimal features and classifiers using the ACO-based Combinatorial optimization technique. A multi-objective ACO is formulated using classification accuracy as the

performance metric. The different features such as mean, % THD, RMS, and harmonic orders (upto 12^{th} order) from the output voltage of the selected MLI have been considered as features for the proposed ML technique. The proposed combined optimizer is used to design a fault classifier for Multilevel inverters. Two widely used inverters, namely CHBMLI and PUC, are selected. Open circuit and short circuit faults are detected based on the features extracted from the output voltage of the selected MLI.

About 7 features with the KNN classifier are selected to design an optimal fault classifier for CHBMLI. Similarly, NBC with 8 features is selected for PUC. The proposed fault diagnosis technique has improved accuracy which will decrease the operating time of electrical equipment's and also increase the working life span of equipment under abnormal circumstances. The experimental results have been taken for CHBMLI and PUC with the implementation of proposed technique to corroborate their performance. Simulation results illustrate a reliable classification accuracy of 97.84% and 98.56% for CHBMLI and PUC inverters, respectively. In addition, the designed classifiers are also subjected to detect the fault in the laboratory-scale prototype of MLIs with the classification accuracy 95.56% and 94.28% for CHBMLI and PUC respectively. Reliable performance with significant classification accuracy is observed to make the proposed combined optimizer a reliable tool for designing ML-based classifiers.

The proposed automated design methodology can be used to design classifiers for other power converters. The designed classifier can be integrated with fault isolation and mitigation systems to ensure operational continuity.

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V. SUDHA is currently pursuing the Ph.D. degree with SASTRA Deemed to be University, Thanjavur, India. Her current research interests include power electronics and fault diagnosis in multilevel inverters.

K. VIJAYAREKHA received the bachelor's degree in electrical and electronics engineering from the Alagappa Chettiar College of Engineering and Technology, Karaikudi, in 1990, the M.E. degree in power systems from the NIT, Trichy, in 1992, and the Ph.D. degree from SASTRA University, in 2008. She has teaching experience of 26 years. She has published more than 72 research papers in reputed national and international journals and conferences in the area of image processing, power converters, non destructive testing, interharmonics, and FACTS. Under her guidance three candidates completed and six are doing their Ph.D. in SASTRA Deemed to be University.

RAKESH KUMAR SIDHARTHAN received the Ph.D. degree in autonomous navigation for mobile robots. He is currently working as a Technical Manager with the ERS Division, HCL Technologies Ltd. He has been working on the development of AI and ML-based solutions for robotics and automation applications. He has also developed a vision-enabled robot control framework for automated device testing applications. He has also published more than 50 research papers in various peer-reviewed journals and conferences. His research interests include robotics, deep learning, and MPC.

NATARAJAN PRABAHARAN (Member, IEEE) received the B.E. degree in electrical and electronics engineering from the Affiliated College of Anna University, Chennai, India, in 2012, the M.E. degree in power electronics and drives from Anna University, in 2014, and the Ph.D. degree in energy and power electronics from VIT University, Vellore, India, in 2017. He is currently an Assistant Professor with the Department of Electrical and Electronics Engineering, SASTRA Deemed University, Thanjavur, Tamil Nadu, India. His research interests include power electronics, new topologies for multilevel inverter and converters, electric vehicle, grid integration of renewable energy sources and its controllers, microgrid, demand side management, and energy trading. He received the two prestigious travel grants under the category of Young Scientist from the Science and Engineering Research Board (SERB) and Asian Development Bank (ADB) in 2015 and 2016. He obtained the University Merit Ranker Award in 2014. He serves as an Associate Editor for *IET Renewable Power Generation*, *International Transactions on Electrical Energy Systems*, IEEE Access, and few other journals. He is a technical program committee member for many reputed international conferences.