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RESEARCH ARTICLE

# CMOS Injection-Locked Frequency Quadrupler/Quintupler

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**ABSTRACT** This paper designs a C-band single-stage *LC*-tank injection locked frequency quintupler (ILFQ) fabricated in 0.18 $\mu$m CMOS process. The differential input/output ILFQ circuit is made of a first-harmonic injection-locked frequency oscillator (ILO) and a frequency quadrupler/quintupler. The free-running oscillation frequency of the ILFQ is around 7.6 GHz. At the dc power consumption of 9.9 mW and at the incident power of 0 dBm, the input locking range is from the incident frequency 1.456 GHz to 1.644 GHz to provide an output signal source from the frequency 7.28 GHz to 8.22 GHz. The whole chip occupies a die area of $1.114 \times 1.060$ mm$^2$. The designed circuit is also used as a new X-band single-stage *LC*-tank injection locked frequency quadrupler, which shows measured $\times 4$ output locking range from 7.82 GHz to 8.6 GHz.

**INDEX TERMS** Frequency quadrupler, injection-locked frequency quintupler, LC-tank, locking range, 0.18 $\mu$m CMOS.

## I. INTRODUCTION

Frequency multipliers (FM's) and/or injection-locked frequency multipliers (ILFM's) are often used in wireless transceivers or radar systems, converting a low frequency signal into a high frequency local (LO) signal. Their applications include: (a) a single-PLL-based LO generator supports multiple frequency bands by using post-PLL ILFM's [1], a sub-THz frequency synthesizer uses many ILFM's to boost the output frequency [2] and ILFM chain is used in the PLL circuit [3]. High-multiplication factor FM's are used to simplify the circuit design. A $\times$ 5 FM [4] is designed by using a self-generated 4$^{th}$ harmonic of a circuit to mix with the input signal in a mixer. A $\times$ 5 FM [5] is designed by using an amplifier stage operated in strongly non-linear regime to generate an output signal with a rich harmonic content and a narrowband filter with the purpose of filtering all the harmonics different from the desired one. A $\times$ 5 FM [6] is designed by combining a frequency tripler, frequency divider and mixer. Other passive frequency quintupler uses varactors [7].

Combining an active frequency quintupler as shown in Fig. 1(a) and an injection-locked oscillator (ILO) forms an injection-locked frequency quintupler ($\times$5 ILFQ) as shown in Fig. 1(b). The 5$^{th}$ harmonic is generated by either the direct harmonic generation and/or the mixing upconversion. The ILFQ has the advantage of low phase noise signal at low injection power and amplifying the harmonic signal. Injection locking forces the ILFQ to follow the low phase noise reference frequency thus attenuating the ILFQ output phase-noise. An ILFQ has been proposed [8], it uses a series direct harmonic injection approach and it shows that the output frequency is higher than the transition frequency $f_T$. The circuit is not fully characterized because it is integrated with the VCO in the PLL loop. A multiply-by-10 ILFM [9] with a multiply-by-5 ILFM locked to the output of a multiply-by-2 ILFM was designed with a VCO in a PLL loop. The multiply-by-5 ILFM uses the direct injection method and has not been fully characterized. A recent $\times$5 ILFM [10] is designed, it uses a pre-generator realized by chopping

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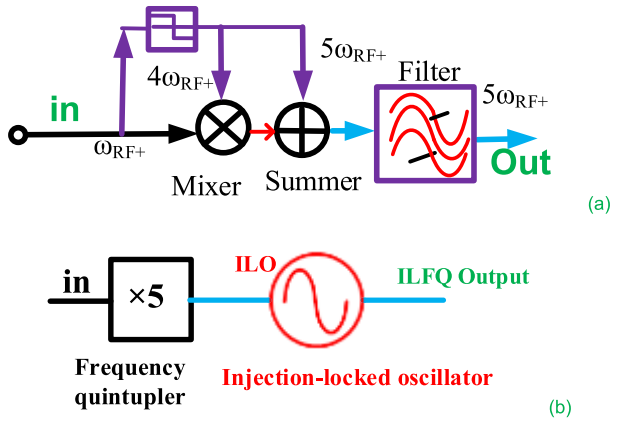



**FIGURE 1.** Block-diagrams of (a) the frequency quintupler and (b) the injection-locked frequency quintupler.

the drain current controlled by the biasing voltage, an ILO suppressing the harmonic spurs, and the tunable fourth-order resonator to select the desired harmonic. No phase noise performance is reported and cascaded stages are used to achieve the harmonic filtering. In addition, two MOSFETs stacked in series leads to higher supply voltage. A multiply-by-5 ILFM can't be designed with low-division-factor as a ×4 FM with two cascaded ×2 FM's. It normally has smaller locking range than a multiply-by-3 ILFM, and enhancement of the ×5 locking range becomes an important issue. This can be achieved by increasing the output strength of the frequency quintupler and/or the input sensitivity in Fig. 1(b). The latter often uses a tunable multi-resonance resonator. This tends to increase the circuit complexity and the cost of system control.

This paper proposes a new single-stage ILFQ, which intends to increase the output strength of the active frequency quintupler, and it combines an injection-locked frequency oscillator (ILO) and a frequency quintupler (×5 FQ), the designed ×5 ILFM use a shunt injection approach. The ILFQ is aided by a self-generated 4$^{th}$ harmonic and a buffer is used to extract the 4$^{th}$ harmonic to verify the theoretical inference. As by-product of this ×5 ILFM design, a single-stage ×4 ILFM is found with a simpler circuit structure than the existing ×4 ILFM's.

One ×4 frequency quadrupler [11] consists of cascaded frequency doublers with intermediate power amplifiers to increase the output power. The single-stage frequency quadrupler [12] is based on a balanced topology. At the output, the odd-order harmonics are suppressed by connecting the collectors. The unwanted 2$^{nd}$ harmonic is short-circuited by a λ/4 thin-film MS-line. The frequency quadrupler [10] uses the phase-controlled circuit. The frequency quadrupler (FQ) [13] based on stacked double bootstrapped Gilbert cell. These FQs are not easy to integrate with the present circuit to form a frequency quintupler. Injection-locked frequency quadruplers are easy to configure with one first-harmonic injection-locked oscillator and two frequency doublers [14] as shown in Fig. 2(a). The injection locked frequency

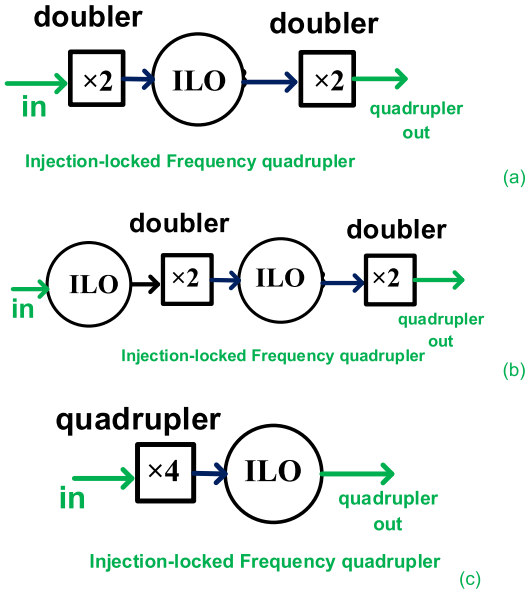



**FIGURE 2.** Block-diagrams of the injection-locked frequency quadrupler. (a) One ILO between two doublers. (b) Two pairs of ILO and doubler. (c) One quadrupler and one ILO.

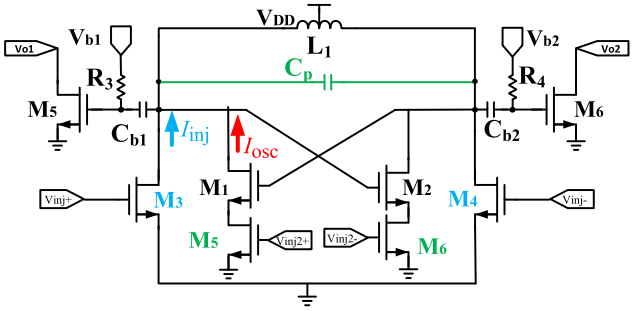



**FIGURE 3.** Circuit diagram of the ILFQ using the series and shunt injection.

quadrupler with quadrature outputs [15] shows rather limited locking range. The injection locked frequency quadrupler [16] as shown in Fig. 2(b) cascades two injection-locked frequency doublers. These ×4 ILFM's use multi-stage approach. The designed circuit used as a single-stage ×4 ILFM simplifies the circuit topology. Fig. 2(c) shows a ×4 ILFM with one 4$^{th}$ harmonic pregenerator.

## II. CIRCUIT DESIGN

Fig. 3 shows the circuit diagram of a possible ILFQ using a cross-coupled ILO with both the series injection FETs ($M_5$, $M_6$) and shunt injection FETs ($M_3$, $M_4$). These injection FETs are nonlinear amplifiers to supply the 5$^{th}$ harmonic current of the injection signal to the cross-coupled oscillator. The generation is a low efficiency conversion yielding small locking range. Fig. 4(a) shows the circuit diagram of the proposed ILFQ using an ILO and an active frequency quintupler (FQ) to improve the conversion efficiency. Fig. 4(b) shows the block diagram of the ILFQ using the concept of linear mixer. In Fig. 4(a), $M_1$, $M_2$, $C_1$, $C_2$

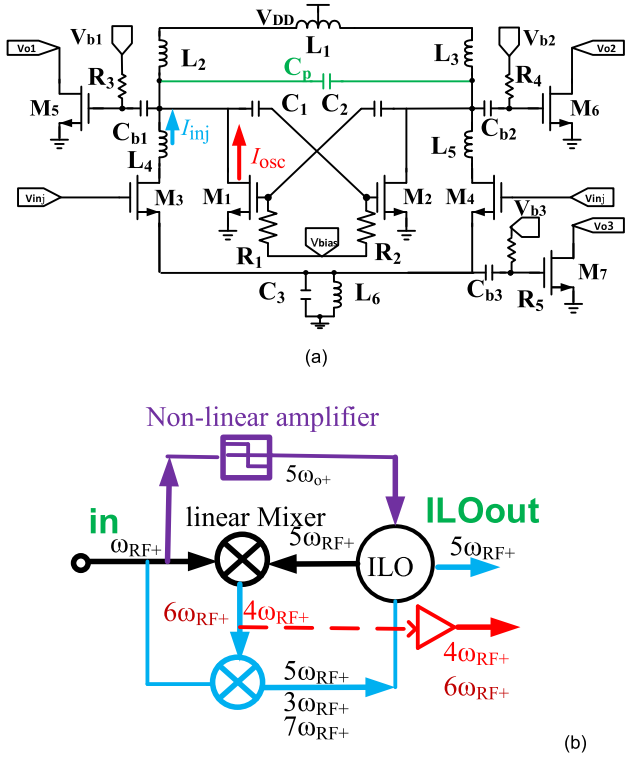



**FIGURE 4.** (a) Circuit diagram of an injection-locked frequency quintupler. (b) Simplified block-diagram of the injection-locked frequency quintupler.

and $R_1$, $R_2$ act as a negative resistance generator, which forms the ILO with the resonator composed of $L_1$, $L_2$ and $L_3$ and parasitic capacitor $C_p$, which is bias-dependent. $L_1$, $L_2$ and $L_3$ are chosen so that it can resonate with the net capacitance at the drain of $M_1/M_2$ at the 5$^{th}$-order harmonic frequency of the injection frequency. $M_5$ and $M_6$ are output buffers with dc blocking and dc gate bias for the 5$^{th}$ harmonic extraction. The frequency quintupler is formed with $C_3$, $L_6$, $M_3$, $M_4$, $L_4$ and $L_5$. Bias-tees are used for buffer drains.

Under the injection locking condition, $M_3$ and $M_4$ plays the role of mixer to generate the 4$^{th}$/6$^{th}$ harmonic at the common node of $L_6$ and $M_3$ by mixing the 5$^{th}$ harmonic voltage from the drain and the injection signal from the gate. The source 4$^{th}$ and 6$^{th}$ harmonics then mix with the gate input signal of injection FET $M_3$ to generate 3$^{rd}$, 5$^{th}$, and 7$^{th}$ to the ILO $LC$-tank, which suppresses the 3$^{rd}$ and 7$^{th}$ frequency components. Consequently, the ×5 ILFM locks at five times the input frequency. Output buffer $M_7$ with dc gate bias and ac-coupled input is used to evaluate the 4$^{th}$/6$^{th}$ harmonic output signal. As a large input signal is applied to the gates of injection devices, $M_3$ and $M_4$ switch between the cutoff and linear region to generate harmonic drain currents. For the direct injection method [9], the drain and source of injection FET are biased at zero voltage. The 4$^{th}$ and 6$^{th}$ harmonics are yielded at the common source of two injection FETs as a result of mixing the injection signal with the self-oscillation frequency of the ×5 ILFM-core. The strengths of 4$^{th}$ and 6$^{th}$ harmonics are small as the zero drain-source voltage is applied and this circuit relies on ac drain-source voltage to create harmonic components. In Fig. 4(b), two linear mixers model the net effect of $M_3$ ($M_4$). The top mixer takes the input signals from the injection port and ILO output to create the mixing output products at 4$^{th}$ and 6$^{th}$ harmonics measurable at buffer output. The bottom mixer takes the input signals from the injection port and injection-induced mixer output to create the mixing product at 5$^{th}$ harmonic for driving the ILO. Additionally, $M_3$ plays the 2$^{nd}$ role as a 5$^{th}$ harmonic generator. Fig. 4(b) distinguishes the operation function of the designed ILFQ from the ILFQ using Fig. 1 in the mixing strategy. Inductors $L_4$ and $L_5$ increase the drain voltage swing of injection FET and locking range.

Under the locking case, the drain voltage of $M_3$ ($M_4$) will self-generate 4$^{th}$ and 6$^{th}$ harmonics by mixing the drain voltage and gate voltage, and the harmonics concurrently mix with the injection signal to supply the 5$^{th}$ harmonic current to the $LC$ tank. The locking range model is simplified as follows. The drain current of injection MOSFET $M_3$ ($M_4$) is often formulated as

$$I_{ds} = \frac{\mu W C_{ox}}{L}([V_{GS} - V_{TH}]V_{ds} - \mathrm{V}_{ds}^2/2) \tag{1a}$$

The ac drain-to-source and gate-to-source voltages are given by

$$v_{ds} = v_{da}\cos(5\omega_o t + 5\phi), \quad v_{gs} = v_{GS+}\cos(\omega_{RF} t + \theta) \tag{1b}$$

where $v_{da+}/v_{GS+}$ is the amplitude of the voltage, $5\phi$ and $\theta$ are phases and $\omega_{RF}/5\omega_o$ is the frequency of injection source/FQ output. The above equation yields a mixing dynamic drain current given by

$$i_{ds} = \frac{\mu W C_{ox}}{L} v_{da} v_{GS+}\cos(\omega_{RF} t + \theta)\cos(5\omega_o t + 5\phi) \tag{1c}$$

The self-generated source voltage of $M_3$ ($M_4$) is given by

$$v_s = \frac{\mu W C_{ox}}{L} v_{da} v_{GS+}\cos(\omega_{RF} t + \theta)\cos(5\omega_o t + 5\phi) Z_s \tag{2}$$

where $Z_s$ is the source impedance. Under the locking condition, $\varphi = \theta$ and $\omega_{RF} = \omega_o$, the new self-consistent injection drain current is given by

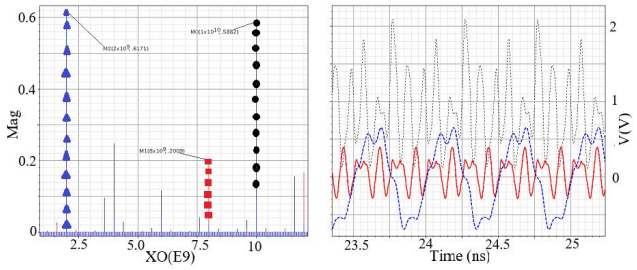
$$i_{ds} = [\frac{\mu W C_{ox}}{2L}]^2 v_{da} v_{GS+}^2 Z_s \cos(5\omega_{RF} t + 5\theta) \tag{3}$$

The prefactor of (3) is $I_{inj}$. The output locking range of a $RLC$-tank ILO around the resonant frequency is derived as [17]:

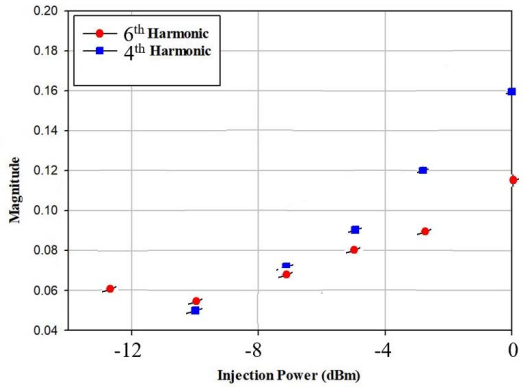
$$\Delta\omega_{RFLR} = (5\omega_{RF} - 5\omega_o) = \frac{5\omega_o I_{inj}}{2QI_{osc}} \tag{4}$$

$Q$ is the tank quality-factor. The current $I_{inj}$ to the $LC$ tank is from injection mixer, and the fundamental oscillation current $I_{osc}$ comes from the switching FET to the tank.

Combination of (3) and (4) shows that high-impedance tail resonator of pregenator enhances the locking range. If $Z_s = 0$, then $I_{inj} = 0$, the locking range due to injection mixing is equal to zero. Without $Z_s$ the circuit relies on other injection mechanisms to generate the fifth harmonic current. The




(a)




(b)

**FIGURE 5.** (a) Pre-layout simulated DFT and voltage waveforms of an ILFQ. $V_{DD}$ = 1 V, $V_{bias}$ = 0.9 V, $V_{inj}$ = 0.51 V, $V_{O1}$ = $V_{O2}$ = 0.6 V, $V_{OUT3}$ = 1.14 V, $V_{B1}$ = $V_{B2}$ = 0.54 V, $V_{B3}$ = 0.76 V. $f_{inj}$ = 2.0 GHz, $P_{inj}$ = 0 dBm. Black dotted: Drain voltage of $M_5$, $M_6$. Red solid: source voltage of $M_3$, $M_4$. Blue dashed: injection signal. (b) Pre-layout simulated strength of the 4th and 6th harmonics at mixer source.

**TABLE 1.** (a) Passive parameters (b) Performance of 2 simulated ×5 ILFM's.

(a)

| | | | |
|---|---|---|---|
| L1 | 0.238 nH | L4 | 0.544 nH |
| L2 | 0.397 nH | L5 | 0.544 nH |
| L3 | 0.397 nH | L6 | 0.202 nH |
| Cb1~ Cb3 | 951 fF | C1~ C3 | 951 fF |

(b)

| | Proposed ×5 ILFM | Reference ×5 ILFM |
|---|---|---|
| Free-run frequency | 1.02GHz | 9.6 GHz |
| Lock Range (GHz) | 9.7~11.5(16.98%) | 9.4~9.65(2.62%) |

circuit uses an *LC* resonator at the tail node, therefore the tail resonator increases the locking range.

The chopping current ×5 ILFM [10] doesn't use this injection mixing technique. The ×5 ILFM is operable at various bias conditions. Fig. 5(a) shows simulated DFT and voltage waveforms of frequency quintupler. The injection FETs are biased in the class-C mode. In the free-run mode, the oscillation frequency is 10.2 GHz and the gate and source voltages of $M_3$ ($M_4$) are small. In the locked mode, injection FET switches between on and off-state, and the source voltage increases because the injection FETs are turned-on. The drain voltage of $M_3$ ($M_4$) contains primarily the 5th harmonic and the source voltage contains the 4th/6th harmonic while the injection signal to the gate is the fundamental. For the circuit with parameters shown in Table 1A, at $V_{DD}$ = 1 V, $V_{bias}$ = 0.9 V, $V_{in1}$ = $V_{in2}$ = 0.51 V, the simulated ×5 input (output) locking range at $P_{inj}$ = 0 dBm is from

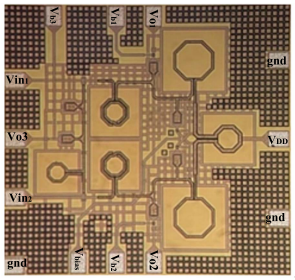



**FIGURE 6.** Chip micrograph for the ×5 ILFM.

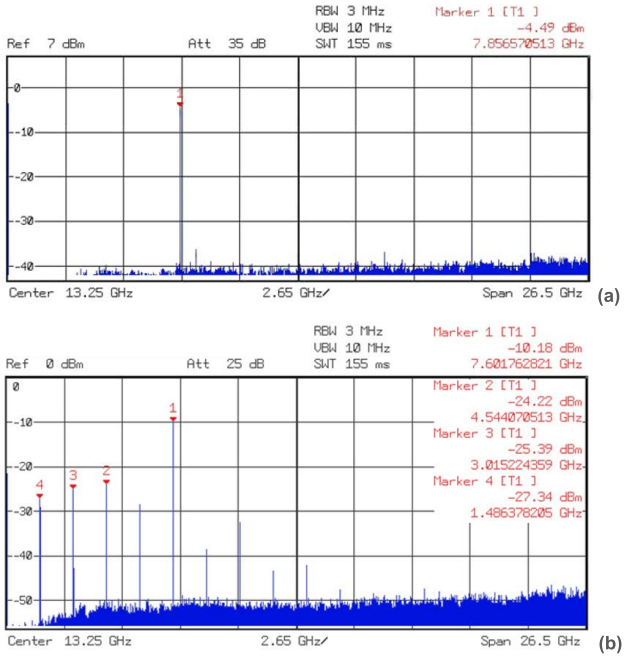



**FIGURE 7.** (a) Measured ×5 free-run full spectrum. (b) Measured ×5 locking full spectrum. $V_{DD}$ = 0.5 V, $V_{bias}$ = 1 V, $V_{inj}$ = 0.16 V, $V_{O1}$ = $V_{O2}$ = 1 V. $V_{b1}$ = $V_{b2}$ = 0.97 V, $V_{O3}$ = $V_{b3}$ = 0 V. $f_{inj}$ = 1.524 GHz, $P_{inj}$ = 0 dBm.

1.94 (9.7) GHz to 2.31 (11.55) GHz. Under the same bias and device parameters, the reference ×5 ILFM without $C_3$, $L_6$, $L_4$ and $L_5$ shows much smaller locking range. Table 1B shows the comparison of two ILFM's. Fig. 5(b) shows simulated strength of the 4th and 6th harmonics at mixer $M_3$ source. The harmonics increases with injection power and the 4th harmonic is larger.

## III. MEASUREMENT RESULTS

### A. MEASUREMENT OF THE MULTIPLY-BY-5 ILFQ

The ×5 ILFM has been designed and fabricated in the TSMC 0.18 $\mu$m 1P6M CMOS technology. The die micrograph occupying an area of 1.114 × 1.060 mm$^2$ is shown in Fig. 6. Dies have been glued on PCB for experimental characterization. The chip input/output pads are wired to the PCB input signal through bond-wires. The open-drain buffers are supplied off-chip with bias-tees through bond-wires.

Fig. 7(a) shows the measured free-run spectrum of ILFQ buffer output, the carrier is at 7.86 GHz and with output power of −4.49 dBm. Fig. 7(b) shows the measured locked spectrum

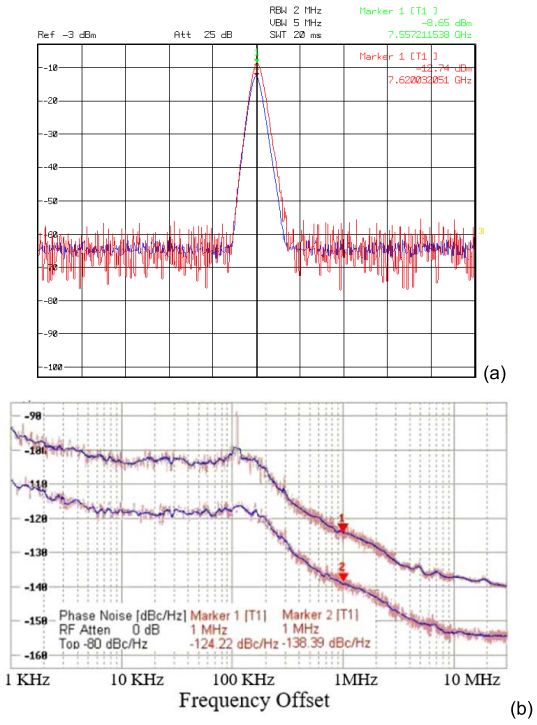



**FIGURE 8.** (a) Measured spectra of the free-run and the locked frequency quintupler. (b) Measured phase noises of the locked quintupler and injection source. The injection signal, $f_{inj}$ = 1.573 GHz, $P_{inj}$ = 0 dBm.

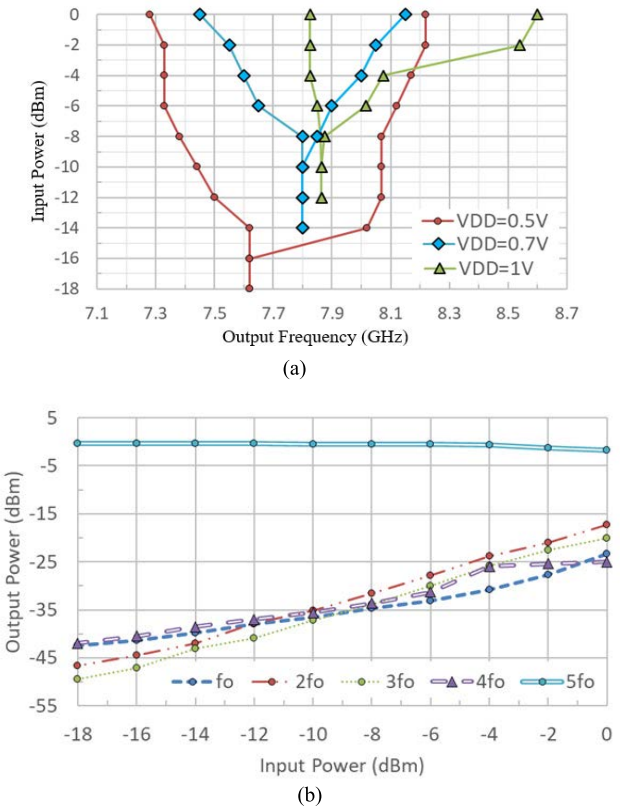



**FIGURE 9.** (a) Measured ×5 output sensitivity. (b) Measured ×5 harmonic output power levels. $V_{DD}$ = 0.5 V, $V_{bias}$ = 1 V, $V_{inj}$ = 0.16 V, $V_{O1}$ = 1 V, $V_{b1}$ = $V_{b2}$ =0.97 V, $V_{O3}$ = $V_{b3}$ = 0 V. $f_{inj}$ = 1.524 GHz.

of ILFQ buffer output. The locked carrier is at 7.6 GHz and with output power of −10.18 dBm. The 5th harmonic is larger than the 3rd harmonic by 14.12 dBm.

Fig. 8(a) shows the superposed measured spectra of free-run and locked quintupler. Fig. 8(b) shows the measured phase noises of the locked quintupler and injection source. The data are from the ILFQ buffer $M_5$ output. The locked phase noise at 1MHz offset frequency is −124.22 dBc/Hz and the phase noise difference between the two phase noises is 14.17 dBc/Hz. Under the bias used in Fig. 7, the pre-layout simulated carrier is at 9.28 GHz. Layout interconnect parasitic decreases the carrier frequency.

Fig. 9(a) shows the ×5 output sensitivity measured from $V_{o1}$. At 0 dBm input power and $V_{DD}$ = 0.5 V, the output locking range is from 7.3 GHz to 8.2 GHz. Locking range increases with increasing injection power $P_{inj}$ due to the increasing injection current to the *LC* resonator. The sensitivity plots at $V_{DD}$ = 0.7 and 1 V are not measured at optimum gate bias as that at $V_{DD}$ = 0.5 V. Fig. 9(b) shows measured harmonic output power levels versus injection power at the input frequency $f_{inj}$ of 1.524 GHz, the harmonic injection suppression improves as injection power decreases.

### B. MEASUREMENT OF THE MULTIPLY-BY-4 ILFM

In the past, many ×4 ILFM's have been implemented. [15], [16], [18]. One ×4 ILFM consists of a cross-coupled injection-locked oscillator [19], [20]. Once injection-locked, the ILO oscillation frequency is exactly the same as its input. By extracting the 4th harmonic at the output push-push node, frequency quadrupling can be realized. However, the signal strength of push-push 4th harmonic is small and signal amplification of the 4th harmonic is important for the successful usage of this technique.

The proposed circuit offers a new way to implement a ×4 ILFM. The proposed ×4 ILFM and the proposed ×5 ILFM use the same circuit with different goals. The ×4 ILFM output requires harmonic suppression and high harmonic contents in the ILO output are tolerable. Fig. 10(a) shows the measured free-run spectrum of ×4 ILFM output buffer and Fig. 10(b) shows the measured locked spectrum of ×4 ILFM buffer output. The 4th harmonic at 8.49 GHz is larger than the 1st harmonic at 1.23 GHz by 5.27 dBm, the 1st harmonic is caused by the unbalanced layout and is easily separated from the 4th harmonic by an output filter.

Fig. 11(a) shows the superposed measured spectra of free-run and locked quadrupler. Fig. 11(b) shows measured phase noises of the locked quadrupler output and injection source. The data are from the $M_7$ buffer output. The locked phase noise at 1MHz is larger than the injection signal by 16.54 dBc/Hz at 1 MHz offset frequency. Fig. 12 shows the measured ×4 output sensitivity measured from $V_{o3}$. At 0 dBm input power and $V_{DD}$ = 0.5 V, the output locking range is from 7.82 GHz to 8.6 GHz. The sensitivity plots at $V_{DD}$ = 0.6 and 0.7 V are measured at the same gate bias for that at $V_{DD}$ = 0.5 V, and they are not measured at optimum

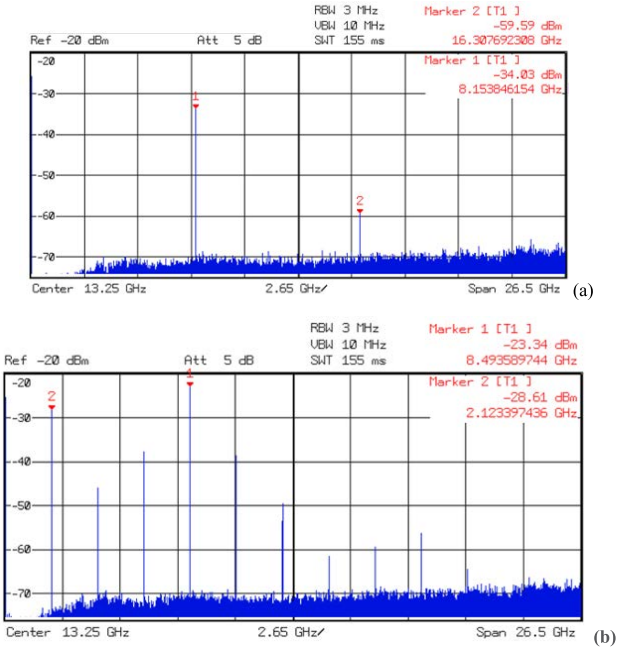



**FIGURE 10.** (a) Measured ×4 free-run spectrum. (b) Measured ×4 locking full spectrum. $V_{DD} = 0.7$ V, $V_{bias} = 0.6$ V, $V_{inj} = 0.25$ V, $V_{O3} = 1.3$ V, $V_{b3} = 1$ V, $V_{O1} = V_{b1} = V_{b2} = 0$ V. $f_{inj} = 2.123$ GHz, $P_{inj} = 0$ dBm.

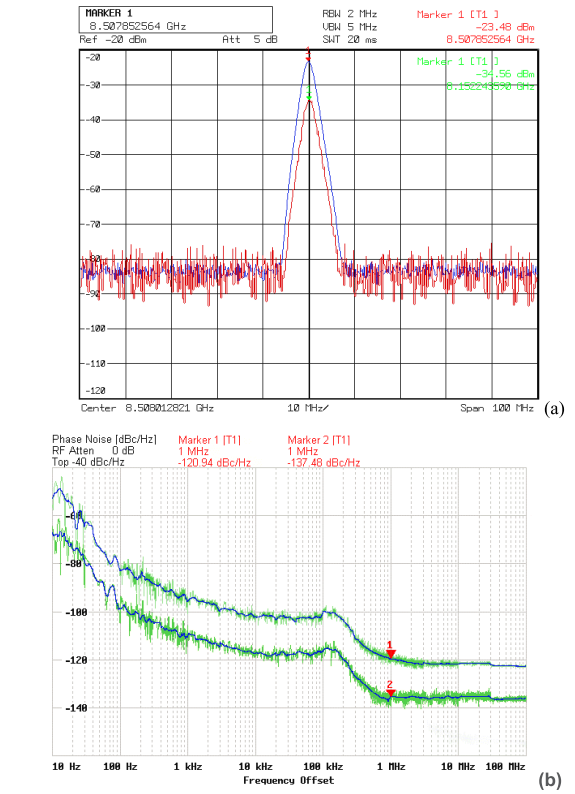



**FIGURE 11.** (a) Measured spectra of free-run and locked quadrupler. (b) Measured phase noises of the locked quadrupler and injection source. Injection signal $f_{inj} = 1.524$ GHz, $P_{inj} = 0$ dBm. $V_{DD} = 0.7$ V, $V_{bias} = 0.6$ V, $V_{in1} = V_{in2} = 0.25$ V. $V_{OUT3} = 1.3$ V, $V_{b3} = 1$ V, $V_{OUT01} = V_{OUT02} = V_{b1} = V_{b2} = 0$ V.

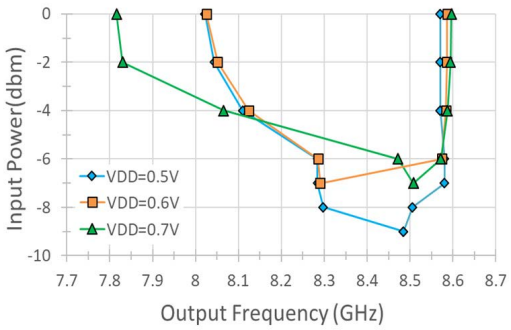



**FIGURE 12.** Measured ×4 output sensitivity. The green triangle is the widest locking range of 0.78 GHz at $V_{DD} = 0.7$ V. The blue diamond and the orange square represent the range equal to 0.5484 GHz at $V_{DD} = 0.5$ V, and 0.5608 GHz at $V_{DD} = 0.6$ V.

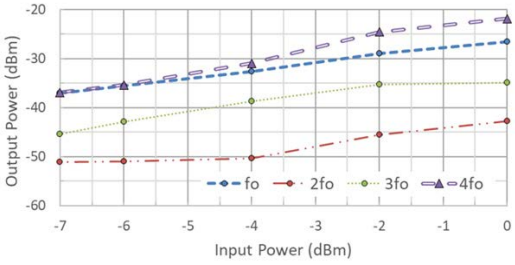



**FIGURE 13.** Measured harmonic output power levels of ×4 frequency multiplier output. $V_{DD} = 0.7$ V, $V_{bias} = 0.6$ V, $V_{in1} = V_{in2} = 0.25$ V, $V_{OUT3} = 1.3$ V, $V_{b3} = 1$ V, $V_{OUT01} = V_{OUT02} = V_{b1} = V_{b2} = 0$ V. $f_{inj} = 2.123$ GHz.

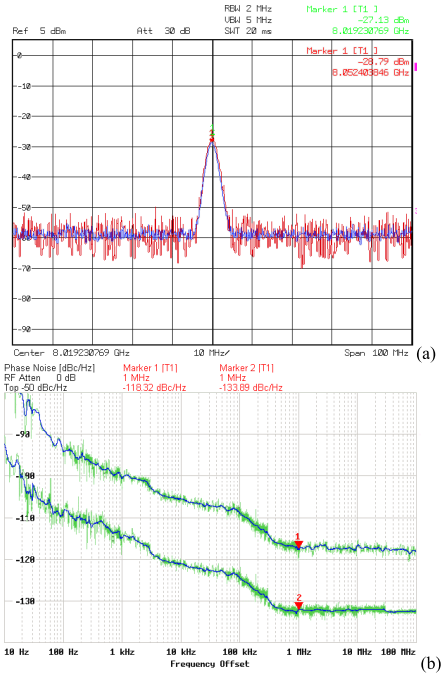



**FIGURE 14.** (a) Measured spectra of free-run and locked sixtupler. (b) Measured phase noises of the locked sixtupler and injection source. Injection signal, $f_{inj} = 1.336$ GHz, $P_{inj} = 0$ dBm. $V_{DD} = 0.5$ V, $V_{bias} = 0.72$ V, $V_{in1} = V_{in2} = 0.23$ V. $V_{OUT3} = 1.15$ V, $V_{b3} = 1.1$ V, $V_{OUT01} = V_{OUT02} = V_{b1} = V_{b2} = 0$ V.

gate bias. Fig. 13 shows the measured harmonic output power levels versus injection power at $f_{inj}$ of 2.123 GHz, the 1st harmonic leakage is large but it can be easily filtered by a post-buffer filter because large frequency separation

**TABLE 2.** Performance comparison of CMOS *LC* ×5/4 ILFMs.

| Ref | Tech. (μm) | $P_{inj}$ (dBm) | *Stages* | $V_{DD}$ (V) | $P_{dis}$ (mW) | FOM | Die area ($mm^2$) | Locking Range (GHz) |
|---|---|---|---|---|---|---|---|---|
| [15]×4 ILFM | 0.09 | 0 | 3 | 0.7 | 9.1 | 2.48 | 0.70×0.89 | 24.0~29.6 (22.6%) |
| [16]×4 ILFM | 0.065 | - | 2 | 0.6 | 3.1 | 0.0427 | 0.16×0.11 | 60.36~60.4(0.13%) |
| [18]×4 ILFM | 0.055 | 0 | 4 | 1.8 | 39.0 | 0.667 | 0.76×0.88 | 30.8~40.0 (26.0%) |
| This (mea) ×4 ILFM | 0.18 | 0 | 1 | 0.5 | 8.9 | 0.533 | 1.114×1.06 | 7.82~8.6 (4.75%) |
| [10]×5 ILFM | 0.065 | 0 | 3 | 1.0 | 10 | 5.77 | 0.48 × 0.45 | 22.4~40.6 (57.7%) |
| This (mea) ×5 ILFM | 0.18 | 0 | 1 | 0.5 | 8.9 | 1.3 | 1.114×1.06 | 7.3~8.2(11.61%) |

between 4th and 1st harmonic signals. The circuit in Fig. 4(a) can be used as a ×6 ILFM as the data are measured from the ×6 ILFM buffer $M_7$ output. Fig. 14(a) shows measured spectrum of free-run and locked ×6 ILFM with smaller locking range than the ×4 ILFM. Fig. 14(b) shows measured phase noises of the locked frequency sixtupler and injection source. Difference of the measured phase noises between the locked sixtupler and injection source is 15.57 dBc/Hz. Table 2 lists the performance of CMOS ILFMs. Figure of merit (FOM) is equal to the locking range percentage over power consumption in mW, the reference circuit uses operation range to replace the locking range in the FOM calculation. The FOM is not good enough because the designed circuit is simpler than other circuit [10], which uses three stages and switch control.

## IV. CONCLUSION

This paper presents a single-stage fully integrated n-core CMOS *LC*-tank injection-locked frequency quintupler that combines an injection-locked oscillator and a shunt-injection frequency quintupler. The C-band injection-locked frequency quintupler in the 0.18-$\mu$m standard CMOS shows good measured phase noise performance. As the proof of concept of using the self-induced 4th harmonic to aid the injection mixing, experimental 4th harmonic is measured. Experimental data shows the circuit uses a frequency quadrupler signal for the mixer to form a ×5 frequency pre-generator. The designed circuit is also used as a new X-band injection-locked frequency quadrupler showing possible good phase noise and simpler circuit architecture. The circuit with new circuit physics is extendable to higher operation frequency.

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