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RESEARCH ARTICLE

A Low-Power Passive UHF Tag With High-Precision Temperature Sensor for Human Body Application

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ABSTRACT Radio frequency identification (RFID) tags are widely used in various electronic devices due to their low cost, simple structure, and convenient data reading. This topic aims to study the key technologies of ultra-high frequency (UHF) RFID tags and high-precision temperature sensors, and how to reduce the power consumption of the temperature sensor and the overall circuits while maintaining minimal loss of performance. Combined with the biomedicine, an innovative high-precision human UHF RFID chip for body temperature monitoring is designed. In this study, a ring oscillator whose output frequency is linearly related to temperature is designed and proposed as a temperature-sensing circuit by innovatively combining auxiliary calibration technology. Then, a binary counter is used to count the pulses, and the temperature is ultimately calculated. This topic designed a relaxation oscillator independent of voltage and current. The various types of resistors were used to offset the temperature deviation. A current mirror array calibration circuit is used to calibrate the process corner deviation of the clock circuit with a self-calibration algorithm. This study mainly contributes to reducing power consumption and improving accuracy. The total power consumption of the RF/analog front-end and temperature sensor is 7.65μW. The measurement error of the temperature sensor in the range of 0 to 60°C is less than $\pm$0.1%, and the accuracy of the output frequency of the clock circuit is $\pm$2.5%.

INDEX TERMS Demodulation circuit, RFID, rectifier, Relaxor, temperature sensor.

I. INTRODUCTION

With the development and progress of society, embedded processors [1]–[6] have become widely used in image processing, networks, system logic, and other fields as an open communication source. Low-power sensors are increasingly used in everyday activities [7]–[9]. In addition, radio frequency identification (RFID) tags are widely used due to their low cost, simple structure, and convenient data reading. Nowadays, the use of RFID in various applications such as supply chain management [10], public transportation [11]–[13], and access control [14] has become an unstoppable trend [15]. Recently, the combination of RFID and sensing systems have expanded the application of RFID to environmental monitoring [16]–[23] and healthcare [24], [25]. For example, the sensors mentioned in the work of Shafiq *et al.* and Camera *et al.* [26], [27] are generally designed for temperature measurement. Zhu *et al.* [28] proposes the use of a passive RFID temperature sensor using a bimetallic coil as the temperature sensing unit. Jain *et al.* [29] proposes a high-performance, low-power temperature sensor suitable for wireless Internet of Things (IoT) devices/RFID

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tags. Implemented in a 65nm CMOS process, the sensor consumes 310nW in a 10ms conversion time. Tan *et al.* [30] proposes a fully passive 13.56MHz RFID temperature sensor system-on-chip, with a two-point calibration, the SoC achieves a 3σ sensing accuracy of ± 0.4°C from 0°C to 125°C. However, the limitation of these sensors is limited in reading range and high costs. Wang *et al.* [31] proposes the RF-Thermometer, a remote temperature-sensing system with commercial ultra-high frequency (UHF) RFID tags. To alleviate the precision deterioration caused by missing phase measurements, a tensor completion method is proposed to restore missing phases and a Gaussian process model is leveraged to construct a phase-temperature map in the offline stage. Therefore, W. Yang *et al.* [32] presents a complementary metal–oxide–semiconductor (CMOS) ultra-low power temperature sensor chip for cold chain applications with temperatures down to −60°C.

To ensure low power consumption, the most popular research direction is to continuously study higher-precision sensors. Therefore, this topic will focus on the key technologies of UHF RFID tags and high-precision temperature sensors, and how to reduce the power consumption of the temperature sensor and the overall tag chip while ensuring the performance as much as possible.

According to the index requirements of passive UHF RFID system and the measurement accuracy of human body temperature in health monitoring equipment, this study designs a fully passive UHF tag for human body temperature monitoring based on the 0.18μm CMOS mixed signal 1P4M process. The energy and data transmission principles in RFID are analyzed, the ISO/IEC 18000-6C protocol is examined, and the design index of the system is proposed. Combined with the overall structure block diagram of passive UHF RFID, the RF/analog circuit in the RFID system is analyzed and designed. In the design of the rectifier circuit, the steady state and output of the Dixon rectifier are analyzed emphatically. In the design of the voltage regulator circuit, a reference power circuit suitable for passive UHF RFID system is created. In the RFID system, the digital baseband module has very high requirements in clock stability. A relaxation oscillator, which is independent of the power supply voltage and the reference current, is designed. An amplitude shift keying (ASK) demodulation circuit with a feedback voltage divider adjustment structure is designed. The feedback voltage divider adjustment circuit can adjust the amplitude of the input signal after voltage doubling in percentage, which increases the flexibility of the electronic label. The interaction process of the temperature data measurement between the reader and the tag is analyzed, and the flow chart is used for further analysis. Based on the in-depth analysis of the temperature sensor, a temperature sensor suitable for passive UHF RFID is designed.

The rest of this paper is organized as follows: Section II introduces the overall structure block diagram of passive UHF RFID, and makes a simple analysis of the overall circuit. Section III presents the design and analysis of key circuit modules, including Rectifier, Relaxor, Demodulation Circuit and Modulation Circuit. Section IV provides the simulation results and analysis. Section V posted a discussion.

II. RFID SENSOR ARCHITECTURE

The block diagram of the RFID system is shown in Figure 1 [33], including the RF/Analog front end module, the digital baseband module, and the sensor readout module. The RF front end includes an energy conversion circuit, a modulation circuit and a demodulation circuit, a clock circuit power circuit and a supply module circuit. Sensor readout module contains temperature-sensing circuit and analog-to-digital conversion circuit.

A. ANALOG FRONT END

The design of the RF/Analog front end considers the system limitations [34]. Therefore, all modules have been optimized for low power consumption to maximize the communication range. Native MOSFET are used to realize a 60% efficiency Dickson voltage multiplier [35]. The module rectifies the input signal and stores the energy required for operation in the power capacitor. Three voltage-stabilizing circuits are provided, including digital baseband, self-calibration clock generator, modulation circuit, demodulation circuit and power on reset circuit, as well as temperature sensor and electrically erasable programmable read only memory (EEPROM) to provide stable voltage. A voltage limiter has been installed to avoid possible damage to the circuit due to voltage surges when the reader and the tag are very close to each other [36].

Three regulators are also implemented, namely, 1V, 1V and 1.8V. The first 1V provides a stable voltage to the digital baseband. The second 1V provides a stable voltage to the self-calibration clock generator circuit, modulation circuit, demodulation circuit, and power on reset circuit. Lastly, the third 1.8V power the temperature sensor.

B. RF FRONT END AND SENSOR READOUT CIRCUITS

In the UHF RFID chips, the rectifier circuit converts radio frequency waves to DC voltage, which powers the system in turn. To improve output voltage and efficiency, the Schottky diode with a low barrier is used. The relaxation oscillator calibrates the circuit through the current mirror array, the self-calibration algorithm is used to calibrate the process corner deviation of the clock circuit. An ASK demodulation circuit with a feedback voltage divider adjustment structure is designed, and the feedback voltage divider adjustment circuit can adjust the amplitude of the input signal after being doubled by a percentage. Therefore, the working distance of the electronic tag is not limited, which increases its flexibility.

C. DIGITAL CORE

The digital core follows the electronic product code second-generation communication protocol to control the communication flow with the reader. Its structure is shown in Figure 1. The input signal from the analog front end is detected and demodulated in the digital demodulator. The decoder obtains

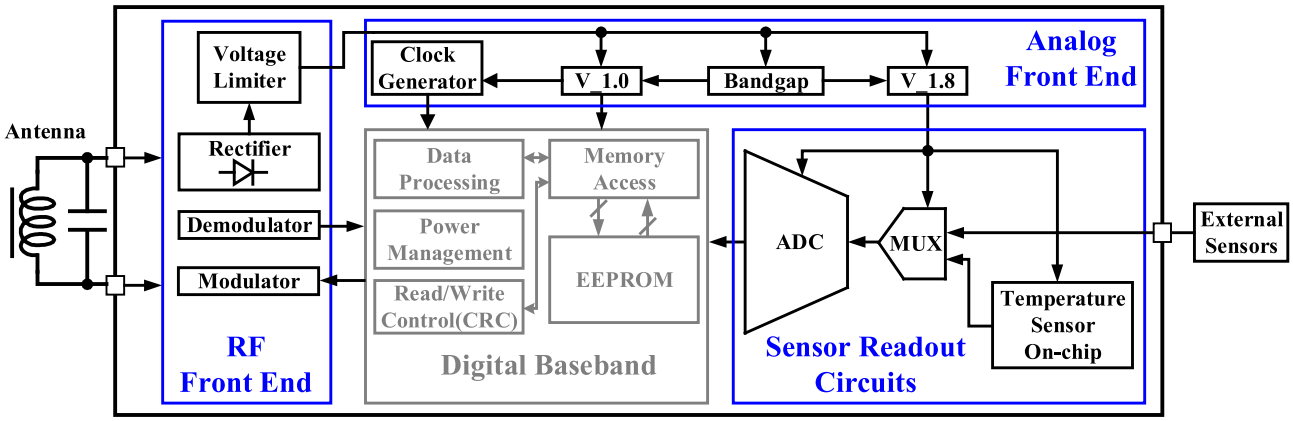

FIGURE 1. Simplified block diagram of proposed RFID sensor.

the opcode and parameters of the instruction. The control module uses a finite state machine to control the system. It performs necessary operations by accessing memory and register banks. Finally, the transmitter modulates the answer. Access to the EEPROM is handled by the memory access module circuit. In this study, a power management module that controls the state of each block is implemented. The digital baseband module is not designed in this study.

III. CIRCUIT DESIGN

A. RECTIFIER

In the passive UHF RFID chip, the rectifier circuit converts the radio frequency waves into a direct current voltage to power the system. As the sensor or RFID tag works at a long distance from the transmitter, the input voltage of the tag is usually very small, approximately 200mV or even lower [37]–[40]. A low-resistance Schottky diode is used to improve the efficiency of output voltage.

The rectifier circuit is realized by a MOS transistor with an external threshold voltage compensator [41]. The MOS tube has a low volt threshold voltage and a zero-volt threshold voltage. The threshold voltage is as low as 150mV and 20mV, which can be used for passive Labels [42]. As the input voltage is equivalent to the threshold voltage, a multi-stage rectifier must be used. The analysis and optimization of alternating to current (AC-DC) rectifiers are similar to the direct-to-current (DC-DC) rectifiers discussed by [43]. With a 3MHz input, the opto-coupled dynamic gate-control rectifier can achieve more than 80% power conversion efficiency (PCE) at an input power down to 0.55mW and achieve a forward voltage drop less than 0.1V. More than 20% PCE improvement is achieved compared with the PCE of bootstrapping rectifier (BSR) [44].

Figure 2 shows an N-stage rectifier consisting of N MOS transistors and N capacitors. All transistors have the same size value, and since the bottom plate of the capacitor has a larger parasitic capacitance than the top plate, the bottom plate can be connected to the input or ground to reduce losses. The two inputs (RF_IN+ and RF_IN-) are directly connected to

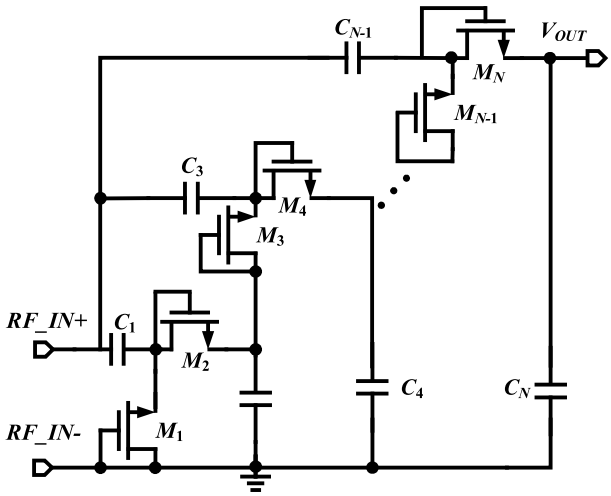

FIGURE 2. N-stages rectifier circuit.

the UHF antenna through an impedance matching network. RF_IN- is arbitrarily designated as the ground node of the rectifier, and assuming that the input to the rectifier is a sinusoidal signal, there is RF_{IN+}- RF_{IN-}=Vacosωt, where Va is the amplitude and f= $\omega/2\pi$=1/T is the frequency. The load capacitance (C_L=C_N) needs to be large to store enough charge to complete the signal processing tasks and reduce the output ripple voltage.

B. RELAXOR

1) WORKING PRINCIPLE

The charge-discharge module is the core of the relaxation oscillator, as shown in Figure 3. The DC current source charges the capacitor, and the capacitor voltage rises in a ramp. The comparator's output state changes when this voltage exceeds the reference level of the input end as a comparator. This results leads to changes in the status of the Reset Set flip-flop, so that the current switch of the capacitor is charged, and the charging mode of the capacitor is changed

to the discharge state. The voltage level of the formation of the trigger output is oscillated in a cycle.

Given a reference current source to charge capacitor, the charging process can be represented by the formula (1):

$$I_{REF} = C\frac{dV_{REF}}{dt}, \tag{1}$$

where C is the capacity, I_{REF} is a reference current source, and V_{REF} is a reference level, which can be simplified to the formula (2):

$$dV_{REF} = \frac{I_{REF}}{C}dt, \tag{2}$$

The circuit is a total of two capacitance turntables, so the charge and discharge cycle of each capacitor is half the entire clock cycle. Formula (2) is integrated in [0, T/2]

$$V_{REF} = \int_0^{\frac{T}{2}} \frac{I_{REF}}{C}dt = \frac{I_{REF}}{C} \bullet \frac{T}{2}, \tag{3}$$

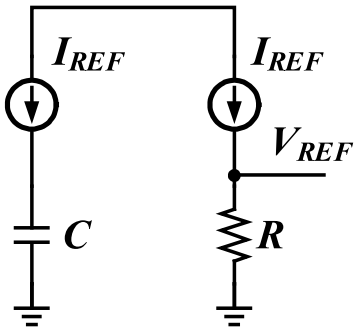

FIGURE 3. Simplified block of slope circuit.

Due to the non-ideality of the comparator, the jump of the comparator output required to input the difference mode signal has a certain amplitude and require a response time. Thus, the voltage across the capacitor inevitably compares the circuit state to change the circuit state than the reference level of the comparator.

The calculation formula is as follows:

$$f = \frac{I_{REF}}{2V_{REF}C} = \frac{1}{2RC}. \tag{4}$$

For higher accuracy, the oscillator needs to be calibrated.

C. CALIBRATION PRINCIPLE AND CIRCUIT IMPLEMENTATION

At the beginning of the calibration process, the electronic tag antenna receives a square wave modulation signal of 38.4 kHz. Then, the square wave signal is demodulated by the demodulator and input to the digital baseband module, and becomes the enabling signal of the counter. The output clock of the oscillator is measured at a high voltage level to judge whether the output of the counter can meet the set value at a low voltage level. If the count meets the set value, then calibration is stopped. Otherwise, the charging current of the relaxation oscillator is increased or decreased. Then, the next cycle also repeats the previous operation until the output clock frequency of the oscillator reaches the expected accuracy. The flowchart of the calibration algorithm is shown in Figure 4.

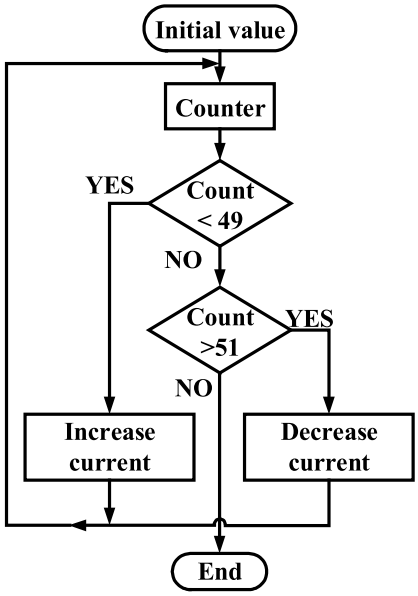

FIGURE 4. Simplified block of slope circuit.

Theoretically, the output clock frequency of the relaxation oscillator is only related to the capacitance and resistance, and has nothing to do with the power supply voltage and reference current. The deviation in values of the capacitance and resistance values are shown at different process corners, in which the 0.18μm process has approximately 30% deviation, which can lead to a large deviation in the output clock frequency of the oscillator. And this study use two types of resistors (i.e., rhrpo and rpdifsab), the first-order temperature coefficients of the two resistors can be found in the process library, and the total temperature coefficients can be achieved by calculation to zero. Through simulation verification, the digital baseband can still work normally when the clock deviation is $\pm$10%. To ensure the yield of the electronic tag chip, this topic has to calibrate the clock and the system clock frequency to $\pm$2.5% required by ISO/IEC 18000-6C protocol.

The Clock calibration consists of two methods [45]: current mirror array calibration and capacitive (or resistive) array calibration. The latter is unrelated to the magnitude or fluctuation of bias current and related only to the proportion of current. Correct calibration cannot be guaranteed if a capacitor or resistor array is used for calibration. Thus, this study adopts the current mirror-array calibration method. Compared with the capacitance or resistance array calibration method, this method has the advantages of simple structure, high linearity and high precision, and the layout and wiring are relatively simple.

This study assume that the current flowing through the capacitor C is I_{REF} during normal operation. As shown in Figure 5, the currents flowing through the resistor and

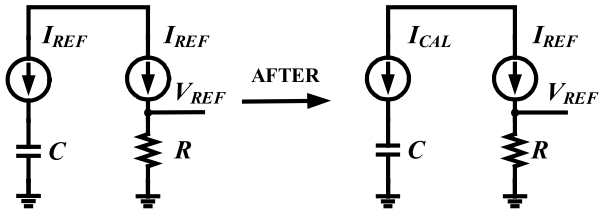

FIGURE 5. Circuit comparison before and after clock calibration.

capacitor in the clock circuit before calibration are both I_{REF}. When a deviation of the current I_{REF} occurs, the deviation of the two currents cancel each other out. However, because the deviation of the capacitor and the resistor at different process corners is not the same, the output clock frequency and set value of the oscillator are different, and the clock calibration needs to be performed at this time. By adjusting the current flowing through the capacitor, this topic can obtain the charging current I_{CAL}.

$$\alpha = \frac{I_{CAL}}{I_{REF}}, \tag{5}$$

Based on the assumption that the deviation of resistance is m and the deviation of capacitance is n, larger is positive, and less is negative, the following formula (6) can be obtained by combining formulas (4) and (5):

$$\begin{aligned} f &= \frac{I_{CAL}}{2V_{REF}C}, \\ &= \frac{I_{CAL}}{2I_{REF}R(1+m)C(1+n)}, \\ &= \frac{\alpha}{2RC(1+m)(1+n)}, \end{aligned} \tag{6}$$

To consistently keep the clock output frequency at f = 1.92MHz all the time, the following formula can be obtained:

$$\alpha = (1+m)(1+n), \tag{7}$$

The reference level V_{REF} is generated by a constant current source flowing through the resistor, and its current value is $17I_0$. The current I_{CAL} that charges the capacitor is obtained after calibration by the current mirror array. The current mirror array calibration analysis diagram is shown in the Figure 6.

By querying the parameters of the process library and simulation, it can be concluded that under different process corners, the maximum deviation of the resistance is 20% and the maximum deviation of the capacitance is 30%. If the clock is not calibrated and combined with formula (6), the maximum and minimum output frequency value of the clocks are shown as follows:

$$f_{\max} = \frac{1}{0.8 \times 0.7} f_0 = 1.79 f_0, \tag{8}$$

$$f_{\min} = \frac{1}{1.2 \times 1.3} f_0 = 0.64 f_0, \tag{9}$$

where f_0 is the clock output frequency value of this design, which is 1.92MHz.

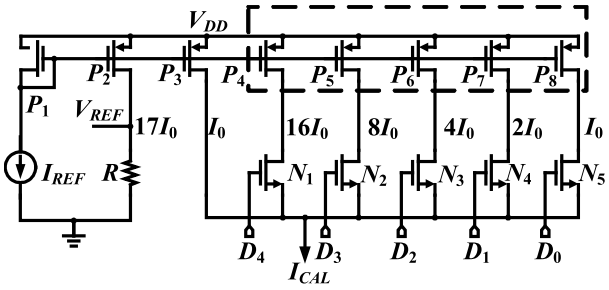

FIGURE 6. Current mirror array.

As shown in Figure 6, transistors (P_4, P_5, P_6, P_7, P_8) constitute the current mirror array, and its aspect ratio is set at 16:8:4:2:1. The ports (D_4, D_3, D_2, D_1) of the digital baseband module to calibrate the signal to the current mirror array. To enable the clock calibration circuit to conduct both positive calibration (increase the output frequency) and negative calibration (reduce the output frequency), setting the calibration ports (D_4, D_3, D_2, D_1) to (10000) by default. The current flowing through P_8 is I_0, which is the minimum branch current of the current mirror array. Then, the calibration range of the current mirror array is $16I_0$-$15I_0$. To avoid the situation where the calibration ports (D_4, D_3, D_2, D_1) are 0 and the charging current I_{CAL} is 0, the P_3 branch solves the situation in which the clock circuit does not oscillate at this time. The current flowing through the resistor R is used to generate the reference level V_{REF}, which is set to $17I_0$. When the default value is input for clock calibration, $I_{REF} = I_{CAL}$.

The calibration range of this circuit is as follows:

$$f_{CAL\_\max} = \frac{32}{17} f_0 \approx 1.88 f_0, \tag{10}$$

$$f_{CAL\_\min} = \frac{1}{17} f_0 \approx 0.06 f_0, \tag{11}$$

The calibration accuracy is calculated as follows:

$$\Delta f_{CAL} = \frac{1}{32} \times f_0 = 0.06\text{MHz}. \tag{12}$$

This result ensures that the clock calibration circuit can calibrate the clock output frequency within the requirements specified in the protocol.

The block diagram of the relaxation oscillator is shown in Figure 7, and the relaxation oscillator consists of the following four modules [46], [47]. The first is the reference power supply. The second is the charging and discharging circuit, which is composed of two sets of inverters. Third is the charging and discharging control logic, which is used to control the charging and discharging of the capacitor. Last is the clock calibration module, which calibrates the oscillator due to the process, voltage, temperature, and frequency deviation [48].

(1) The flip-flop is in the state of Q = 1 when the input voltage gradually increases. At this time, the P_2 tube of the right inverter is switched on, and the N_2 tube is switched off, so the current I_{CAL} charges the capacitor C_2 through the P_2 tube of the right inverter.

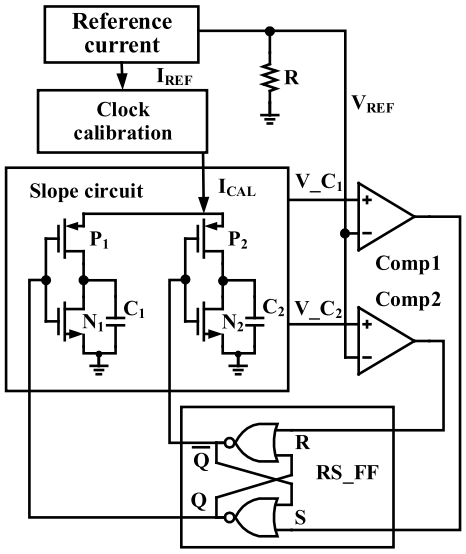

FIGURE 7. Clock circuit structure of relaxation oscillator structure.

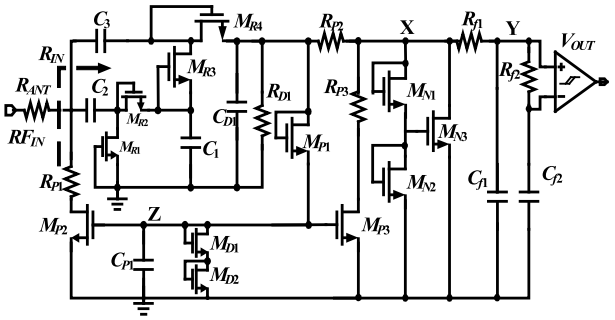

FIGURE 8. Improved demodulation circuit structure.

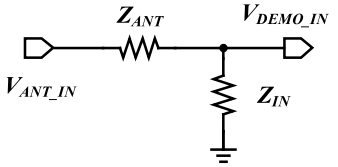

FIGURE 9. Equivalent impedance model.

The voltage V_C_2 on C_2 gradually increases as the charging time increases, the P_1 tube of the left inverter is turned off, and the N_1 tube is turned on. C_1 is discharged to the ground through the N_1 tube of the left inverter. The level of V_C_1 decreases rapidly because the discharge current is much larger than the charging current.

(2) When V_C_2 slowly rises to V_{REF}, the output state of Comp2 changes and the output of flip-flop is $Q = 0$. At this time, the P_1 tube is turned on, and the N_1 tube is turned off. Thus, the current I_{CAL} charges C_1 through the P_1 tube, and the voltage V_C_1 on C_1 slowly rises. The P_2 tube is turned off, the N_2 tube is turned on, and C_2 is discharged to the ground through the N_2 tube, so the level of V_C_2 drops rapidly.

(3) When V_C_1 rises to the reference level V_{REF} of the comparator, the output state of Comp1 changes, and the output of the flip-flop is Q=1. Then, returning to the initial state, so roll on occurs in cycles and the output of Q generates periodic pulses. After shaping and improving the driving capability, a rectangular output pulse is formed, which meets the needs of the digital baseband.

D. DEMODULATION CIRCUIT

The improved demodulator structure is shown in Figure 8. In Figure 9, the RF signal RF_{IN} received by the antenna passes through the voltage doubling rectifier circuit composed of M_{R1}, M_{R2}, M_{R3}, M_{R4} and C_1, C_2, C_3 to obtain the amplified positive half cycle signal [49], [50]. Then, the signal recovers the envelope of the data signal through the envelope detector composed of M_{R4}, C_{D1}, and R_{D1} connected by diodes. The leakage protection circuit does not work when the input signal amplitude in the far-field area is low, and opens the shunt when the input voltage amplitude in the near-field area is high, to keep the voltage at point X stable. R_{f1}, C_{F1}, R_{F2}, and C_{F2} form a second order low pass filter. When it works, it can be regarded as two first order low pass filters in series; The first-order envelope filter R_{F1} is mainly used to remove the residual components of the high frequency carrier; The low-pass filter composed of R_{F2} and C_{F2} mainly completes the average filtering. Due to the large noise interference in wireless communication, the data decision comparator adopts a hysteretic comparator with certain anti interference ability. The internal output buffer stage of the comparator is a two-stage inverter, which is mainly used to complete the function of waveform shaping.

M_{P1}, M_{P2}, M_{P3}, R_{P1}, R_{P1}, R_{P3}, C_{P1}, M_{D1}, and M_{D2} form a limiting circuit, which is called the feedback partial voltage regulating circuit in this paper. The obtained energy expression is shown in formula (13), and the equivalent diagram of energy acquisition is shown in Figure 9.

$$V_{DEMO\_IN} = \frac{Z_{IN}}{Z_{ANT} + Z_{IN}} V_{ANT\_IN}, \tag{13}$$

When the input signal RF_{IN} is extremely small, Z_{ANT} and Z_{IN} should be conjugate matched to ensure the maximum transmission of energy. At this time, V_{DEMO_IN}=0.5V_{ANT_IN}; when the input signal RF_{IN} is large and the matching is not very strict, V_{DEMO_IN}<0.5V_{ANT_IN}. The feedback voltage division regulation structure mainly limits the voltage at point X by adjusting the input resistance R_{IN} of the demodulator.

The working principle of the feedback partial voltage regulation structure is shown as follows: when the input signal energy received by the antenna is small, the voltage at point X is low and does not reach the opening voltage of the feedback partial voltage regulation structure. At this time, M_{P1} is cut off; the voltage at point Z is very low; M_{P1}, M_{P2}, and M_{P3} are cut off; and the feedback partial voltage regulation

structure does not work. When the signal energy received by the antenna is high, the input signal after voltage doubling rectification makes the voltage at point X higher, reaching the opening voltage of the feedback voltage division regulation structure, M_{P1} starts to charge the capacitor C_{P1}, and the voltage at point Z increases. When the voltage at point Z is greater than the threshold voltage of M_{P2}, M_{P2} is switched on. With the increase of the drain current of M_{P2}, the drain output resistance becomes smaller so that the input resistance R_{IN} of the demodulator decreases, and the input signal V_{DEMO_IN} of the demodulator also decreases.

The main function of the capacitor C_{P1} is to keep the voltage at point Z basically constant during the data ASK_0, so that the voltage divider ratio of V_{ANT_IN} and V_{DEMO_IN} during the data ASK_1 and ASK_0 remains unchanged basically. At the same time, the tag chip may move from the near-field area to the far-field area during operation, and the charge stored on C_{P1} should be discharged at this time. M_{D1}, M_{D2} mainly form a discharge circuit, and then form a slow decay circuit with C_{P1}. After the feedback voltage divider adjustment, the amplitudes of the data signals ASK_1 and ASK_0 are attenuated in equal proportions. The role of M_{P3}, R_{P2}, and R_{P3} is to further reduce the common mode voltage of the input data envelope signal.

The aforementioned feedback partial voltage regulation structure can achieve demodulation better in a high dynamic range when the antenna impedance is large, such as $|Z_{ANT}| = 630\Omega$. However, the impedance of the general dipole antenna is 73Ω. Formula (13) shows that the effect of feedback adjustment is not very good. To solve this problem, the improved method in this study aims to add parallel voltage stabilizing and current relief regulating MOS tubes M_{N1}, M_{N2}, and M_{N3} after feedback of the partial pressure regulation.

In the traditional demodulator, the parallel voltage stabilizing and hard limiting protection circuit makes the modulation depth shallow and increases the difficulty of demodulation. The improved feedback parallel voltage regulation circuit can attenuate the signal without reducing the modulation depth, so it has a larger dynamic working range.

E. MODULATION CIRCUIT

The modulation mode of passive UHF RFID is backscattered energy [51]. The principle of ASK backscatter modulation is to control the internal impedance of the electronic tag chip, so that the mismatch between the chip and the antenna indirectly changes the reflection coefficient. The reader senses RF signals with various amplitudes and demodulates them according to the protocol to obtain the correct signal.

In the signal modulation, impedance mismatch increases the reflection coefficient, and a large amount of RF energy is reflected at this time. The reflection coefficient can be obtained from the load impedance (Z_L) and the characteristic impedance (Z_A) of the transmission line. It is shown in the following formula:

$$\Gamma = \frac{Z_L - Z_A}{Z_L + Z_A}. \tag{14}$$

As shown in Figure 10, by adding capacitance or resistance to the modulation circuit to change the internal impedance, the modulation methods are divided into two categories.

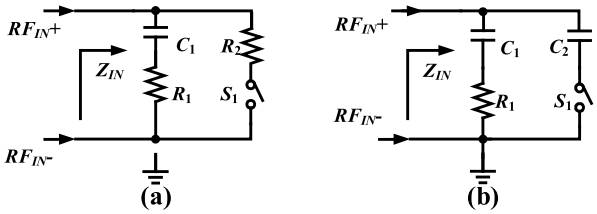

FIGURE 10. (a) Resistance load modulation circuit and (b) Capacitive load modulation circuit.

When the data "1" is returned, the switch is closed to adjust the mismatch between the internal impedance of the electronic tag chip and the antenna impedance. At this time, the electronic tag chip backscatters the most of the RF signals. When the data "0" is returned, the switch is disconnected, so the internal impedance of the electronic tag chip completely matches the antenna impedance. At this time, the electronic tag chip absorbs most of the RF signals and reflects a few back so that the data "0" and "1" can be distinguished. As shown in Figure 11, the level conversion circuit converts the low level of the digital baseband signal to the high level so that the resistance becomes smaller when the switch N_6 is turned on. At the same time, an enable tube N_5 controlled by the digital signal is added. The modulation circuit can be modulated normally only after the digital baseband is enabled. When EN is at a low level and the enable tube N_5 is not on, the gate source voltage of the switch tube N_6 is zero, the switch tube N_6 is not on and the modulation does not work. When EN is high, the gate source voltage of the enable tube N_5 is high, the gate source voltage of the switch tube N_6 is also high, the switch tube N_6 is turned on, and the modulation circuit works normally. The level conversion circuit and N_5 greatly improve the efficiency of the circuit.

F. TEMPERATURE SENSOR

Figure 12 shows the block diagram of the temperature sensor [52]. The digital control logic module (CTRL LOGIC) controls the oscillator (OSC) and binary counter. The digital control logic module controls the on-off status of the oscillator and whether the binary counter counts. The output frequency of the oscillator depends on the detected temperature. Finally, the binary counter counts the number of pulses sent by the oscillator in a fixed time interval.

The measurement process starts from the rising edge of the "start" signal sent by the digital baseband. Then, the control logic module generates three binary signals to control the working time of other modules. First, the "OSC_EN" signal

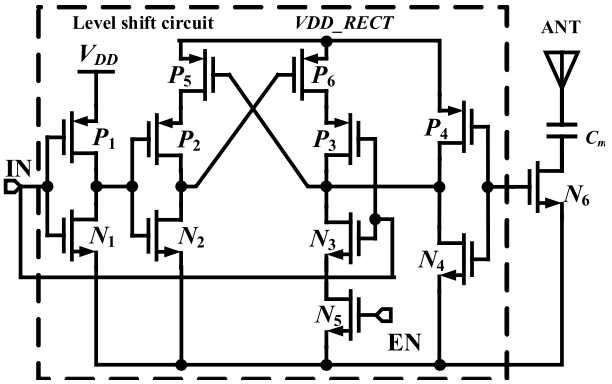

FIGURE 11. Circuit diagram of realizing backscatter modulation.

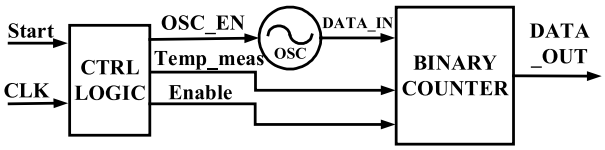

FIGURE 12. Block diagram of temperature sensor.

connects the oscillator to the power supply. After the frequency of the oscillator has stabilized, the "Temp_meas" signal determines the fixed time interval, so the binary counter counts the pulses. The control logic module uses the given 1.92MHz clock generator module with temperature compensation as a reference time. Finally, the falling edge of the "Enable" signal indicates the end of the measurement and resets the counter.

Figure 13 shows the circuit diagram of a ring oscillator whose output frequency changes with temperature. The output frequency is adjusted by the power supply current I. The frequency expression of the pulse generator is shown in formula (15), C_L is the load capacitance, N_S is the number of delay stages, and V_H–V_L is the output voltage swing. Each stage delay gate has two states of opening and closing, so burrs occur in current I, and C_1 is the filter capacitance of current I. C_2 and R_4 adjust the lower voltage limit of the oscillator to adjust the oscillation frequency. At the same time, a pole is introduced to filter out the tip pulse. The pole frequency is shown in formula (16).

$$f = \frac{I}{N_S C_L (V_H - V_L)}, \tag{15}$$

$$f_{p0} = \frac{1}{2\pi R_4 C_2}, \tag{16}$$

The self-biased cascode current source generates the temperature-dependent power supply current required by the pulse generator. As shown in formulas (17) and (18), the power supply current I can be expressed as a function of the threshold voltage V_{TH}, the transconductance K_N and the aspect ratio W/L of transistor N_6, and the resistance R_3.

$$I = k_N \left(\frac{W}{L}\right)_6 (V_{GS6} - V_{TH})^2, \tag{17}$$

$$V_{GS6} = I \bullet R_3, \tag{18}$$

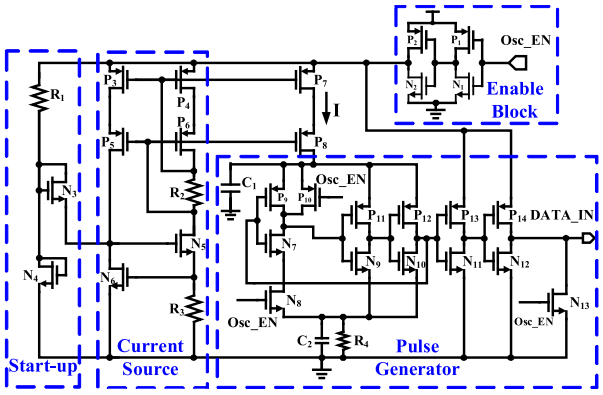

FIGURE 13. Circuit diagram of temperature dependent oscillator module.

Formula (19) can be obtained by simplification as follows:

$$I = \frac{V_{TH}}{R_3} + \frac{1}{k_N \left(\frac{W}{L}\right)_{N_6} R_3^2} + \frac{1}{R_3}\sqrt{\frac{2V_{TH}}{k_N \left(\frac{W}{L}\right)_{N_6} R_3} + \frac{1}{\left[k_N \left(\frac{W}{L}\right)_{N_6} R_3\right]^2}} \tag{19}$$

If R_3 and $(W/L)_{N6}$ are large, current I can be expressed as follows:

$$I \approx \frac{V_{TH}}{R_3}, \tag{20}$$

The relationship between the threshold voltage V_{TH} and the temperature change of resistance R_3 is shown in the following formulas:

$$V_{TH}(T) = V_{TH}(T_0)\left[1 + TC_{V_{TH}}(\Delta T)\right], \tag{21}$$

$$R_3(T) = R_3(T_0)\left[1 + TC1_{R_3}(\Delta T) + TC2_{R_3}(\Delta T)^2\right], \tag{22}$$

TC_{VTH} and TC1 are negative temperature coefficients, $\Delta T = T\text{-}T_0$. Formulas (21) and (22) are replaced into formula (23). Current I can be expressed as a function of temperature T and expanded by Taylor series as follows:

$$I = \frac{V_{TH}(T_0)}{R_3(T_0)}[1 + (TC_{V_{TH}} - TC1_{R_3})(\Delta T) + (TC1_{R_3}^2 - TC_{V_{TH}} TC1_{R_3})(\Delta T)^2 - TC1_{R_3}^3(\Delta T)^3 + \cdots], \tag{23}$$

The variation range of the human body temperature is small. When $|\Delta T| < 20°C$, the contribution of higher-order terms is very small, so it can be ignored. At this time, the dependence of current I and temperature T is

$$\frac{\partial I}{\partial T} = \frac{V_{TH}(T_0)}{R_3(T_0)}(TC_{V_{TH}} - TC1_{R_3}). \tag{24}$$

Therefore, the oscillation frequency is expected to change linearly with temperature from 25°C to 45°C, and its temperature characteristics are mainly provided by the change of V_{TH} of resistor R_3 and transistor N_6 with temperature. The output frequency sensitivity of the oscillator is 58.3kHz/°C.

Transistors (P_3, P_4, P_5, P_6, P_7, P_8) form a large swing PMOS cascode current mirror to provide a high-power rejection ratio for the temperature sensor. Within the V_{DD} variation range of ±20%, the change of the temperature sensor is less than 0.1°C. The pulse generator subcircuit is basically a ring oscillator composed of an odd number of current controlled inverter units and a feedback loop. The two sets of inverters (N_{11}, P_{13} and N_{12}, P_{14}) shape the output of the ring oscillator and shift the pulse level to the digital logic level.

The power supply current of the ring oscillator varies with temperature. Therefore, as shown in formula (20), the output frequency varies in proportion to the temperature. Therefore, the number of pulses N that the binary counter will count within a controlled time interval fixed by the signal ''Temp_meas'' depends on the temperature. To correct the process variation error, the calibration points N_1 and N_2 at two different temperatures T_1 and T_2 are stored in the memory of the RFID tag chip. Then, the sensor does not need to send the three values when the reader needs to measure the temperature in T_3. However, it needs to send the difference between the measured value at T_3, the calibration value at T_1, and the difference between the calibration value at T_2, T_1. In this way, the number of bits to be sent back to the reader is reduced with the minimum additional cost of the digital baseband part, thereby reducing the power consumption. By knowing Y_2 and the calibrated temperature of the sensor in advance, the reader can obtain the sensor characteristic formula. Finally, the reader can determine the temperature T_3 of the sensor by the value of Y_3.

IV. SIMULATION RESULTS

A. RELAXOR

For reference, the current changes as follows:

As shown in Table 1, the maximum deviation of the output frequency of the clock is 0.019MHz (0.99%), which meets the standard requirement of ±2.5%. The circuit designed can suppress the fluctuation and deviation of the reference current to a great extent and allow the deviation of the reference current within a certain range (±20%).

TABLE 1. Clock simulation for different reference current deviations.

Input	V_{DD} = 1V	$D_4D_3D_2D_1D_0$= "10000"
I_{REF} (nA)	f (MHz)	*Jitter* (ns)
80	1.901	0.9
90	1.915	0.4
100	1.920	0.1
110	1.927	0.7
120	1.932	0.9

As shown in Table 2, when the power supply voltage deviation is 200 mV (20%), the maximum deviation of the output frequency of the clock is 0.021 MHz (1.09%), which meets the standard requirement of ±2.5% and leaves a large margin. From the preceding simulation results, it can be concluded that the output frequency of the clock remains basically unchanged when the power supply voltage ripple amplitude, ripple frequency, and deviation are different. The circuit designed this time can suppress the fluctuation and deviation of the power supply voltage to a great extent and allow the deviation of the power supply voltage within a certain range (±20%), which reduces the design difficulty of the voltage regulator circuit.

TABLE 2. Clock simulation for different supply voltage deviations.

Input	I_{REF} =100nA	$D_4D_3D_2D_1D_0$= "10000"
V_{DD} (V)	f (MHz)	*Jitter*(ns)
0.8	1.899	0.9
0.9	1.910	0.9
1.0	1.920	0.3
1.1	1.928	0.7
1.2	1.935	1.2

After the clock calibration is turned on and the simulation environment remains unchanged, the relaxation oscillator circuit is simulated under the TT, SS, and FF process corners. The results are shown in Figure 14.

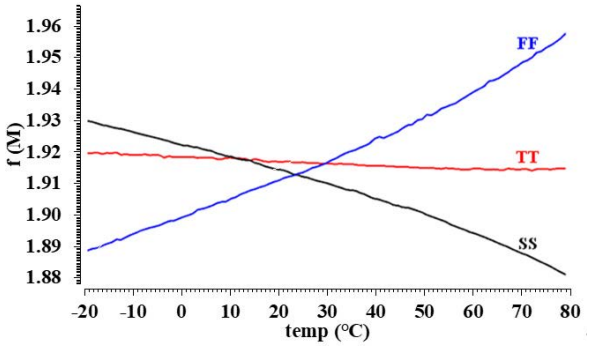

FIGURE 14. Clock circuit process simulation of corner and temperature.

The figure shows that the temperature characteristics of the clock circuit are good. The temperature change has a great influence on the output frequency at the SS and FF process corners. The maximum frequency is 1.96MHz, the minimum frequency is 1.89MHz, and the error range is 1.56% to 2.08%, meeting the requirement of ±2.5% specified in the agreement. The power consumption simulation value of the clock circuit is 1.8μW.

B. DEMODULATION AND MODULATION

The input and output simulation diagrams of the demodulator in the far-field, mid-field and near-field areas are shown in Figure 15, Figure 16, and Figure 17, respectively. Among them, the amplitude of the input ASK modulation signal in these areas are 100mV, 300mV, and 5V, respectively. The modulation depth is 80% and noisy signals occur.

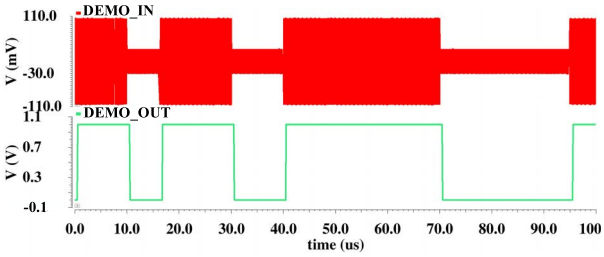

FIGURE 15. Input and output of demodulator in far-field area.

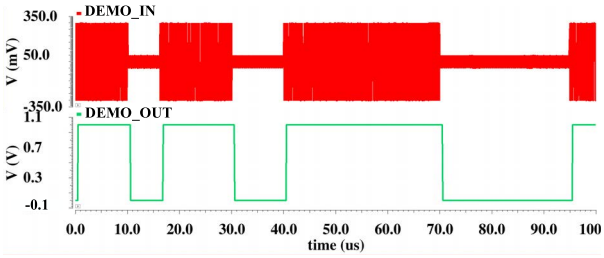

FIGURE 16. Input and output of demodulator in mid-field area.

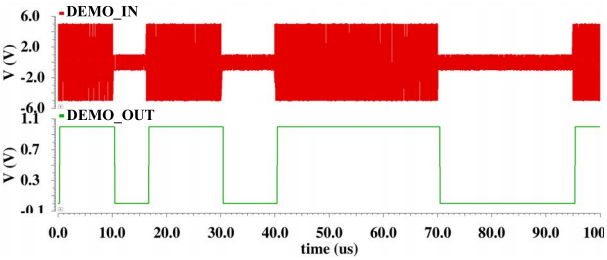

FIGURE 17. The input and output of the demodulator in the near-field area.

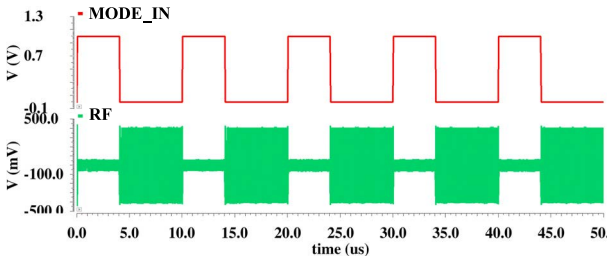

FIGURE 18. Simulation diagram of backscatter modulation circuit.

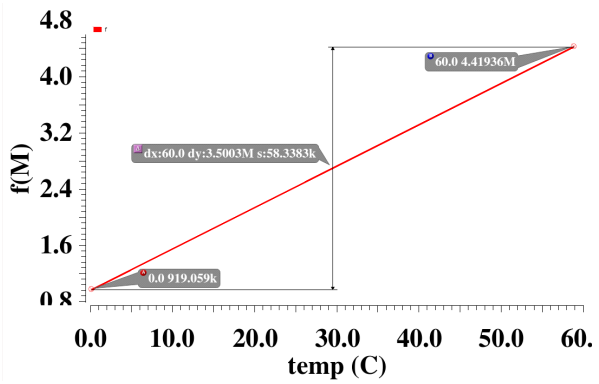

FIGURE 19. Simulation diagram of output frequency of temperature sensing circuit.

TABLE 3. Performance summary.

Parameters	[28]	[48]	[49]	This Work
Technology (nm)	130	40	22	180
Area(mm^2)	0.002	0.001	0.005	0.04
Inaccuracy (°C)	2	0.9	1.07	0.1
Temp range (°C)	-60~40	0~100	-5~85	0~60
Power (μW)	0.15	530	56	7.65

The low-level duration is 6.25, 10, and 5μs, which correspond to the bit rate of 160, 100, and 40 kbps, respectively.

The low-voltage input modulation signal of the circuit can be correctly demodulated, the high level is 1V, and the low level is 0V. The power consumption simulation value of the demodulation circuit is 2μW.

The simulation result of the modulation circuit is shown in Figure 18. In the picture, MOD_IN is the digital signal given by the digital baseband, and RF is the radio frequency signal received by the electronic tag chip. When the digital signal is at a high level, most of the radio frequency energy is backscattered, and the signal amplitude received by the electronic tag chip is at this time. The value is small; when the digital signal is at a low level, because the impedance is completely matched, almost all the energy is captured by the chip at this time, and the signal amplitude is large. The power consumption simulation value of the modulation circuit is 100nW.

C. TEMPERATURE SENSOR SIMULATION

The output frequency simulation diagram of the temperature sensing circuit is shown in Figure 19, which shows that the output frequency of the ring oscillator is proportional to the temperature. The output frequency of the ring oscillator has very stable characteristics with temperature in the entire temperature range, and changes linearly. For every degree of temperature increase, the output frequency of the ring oscillator increases by approximately 58.3383kHz.

When the temperature is 0 °C, the output of the binary counter is 11b'00101101111, which is converted to a decimal number of 367. Similarly, when the temperature is 60 °C, the output of the counter is converted to a decimal number of 1767.

The quantitative results of the temperature sensor at different temperatures are shown in Table 3. When the temperature is 0°C, the output of the binary counter is 11b'00101101111, which is converted to a decimal number of 367. Similarly,

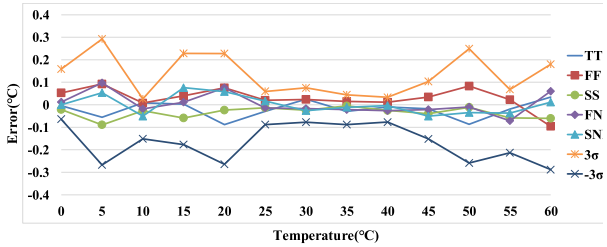

FIGURE 20. Temperature sensor measurement error under different process corners.

when the temperature is 60°C, the output of the counter is converted to a decimal number of 1767.

Simulations are performed under the TT, FF, SS, FNSP, and SNFP process corners. The simulation data are exported to MATLAB for processing, and error calculation is performed on all data within the temperature range of 0 to 60°C. Finally, the results are calculated. Fitting is performed in a line graph, and the error result is shown in Figure 20. The figure shows that the measurement error of the temperature sensor is very small from 25°C to 40°C, $|3\sigma|<0.1$°C, except for the range $|3\sigma|<0.3$°C, which meets the expected index requirements. The power consumption simulation value of the temperature sensor is 900nW.

The performance of the presented temperature sensor chip is summarized and compared to other state-of-the-art designs in Table 3. Compared to other designs, the presented chip shows the lowest measurement temperature with the smallest chip area and the lowest power consumption, by using the proposed nonlinear error calibration. However, the power consumption reduction is actually at the cost of a narrowed measurement range at the high temperature end, which is presented in Table 3.

V. DISCUSSION

According to the index requirements of passive UHF RFID system and the measurement accuracy of human body temperature in health monitoring equipment, this paper designs a fully passive UHF tag applied to human body temperature monitoring. The total power consumption of the designed RFID tag RF/analog front end and temperature sensor is 7.65μW, the measurement error of the temperature sensor in the range of 0 to 60°C is less than ±0.1°C, and the accuracy of the output frequency of the clock circuit is ±2.5%.

Compared with the traditional temperature sensor, the new temperature sensor in this study uses a ring oscillator whose output frequency is linearly related to the temperature as the temperature-sensing circuit. Compared with the quantization method, it does not need to consume static power consumption and is easy to integrate into the RFID system. And the temperature sensor is calibrated to improve the accuracy of the temperature sensor. Aparicio *et al.* [53] introduces a sensor topology specifically tailored for these requirements. Targeting the 40 nm CMOS technology node, the proposed sensor uses both bipolar and CMOS transistors, benefiting from the stable thermal characteristics of the former and the compactness and speed of the latter. The sensor has been fully characterized through extensive post-layout simulations for a temperature range of 0 to 100°C, achieving a maximum error of ±0.9°C, considering 3σ yield and a resolution of 0.5°C.

Unlike the proposed CMOS temperature sensor [54] for use in cold chain applications down to −60°C, the nonlinear error in the conventional PTAT current-based sensor circuit was characterized for the first time. A two-point calibration method was proposed to compensate for the nonlinear error in addition to the traditional linear error calibration.

VI. CONCLUSION

According to the index requirements of the passive UHF RFID system and the measurement accuracy of human body temperature in health monitoring equipment, a ring oscillator whose output frequency is linearly related to temperature is designed. This ring oscillator is proposed as a temperature-sensing circuit by innovatively combining auxiliary calibration technology. The present study designs a fully passive UHF tag for human body temperature monitoring. The total power consumption of the designed RFID tag RF/analog front end and temperature sensor is 7.65μW, the stimulation error of the temperature sensor is less than ±0.1% from 0 °C to 60°C and the accuracy of the output frequency of the clock circuit is ±2.5%. This design only completes the pre-imitation, layout, and post-imitation of the analog front-end, RF front-end, and temperature sensor in the RFID system. Except for the circuit modules that have been designed, the digital baseband and memory have not been designed. Combining the RFID tags with temperature sensors can sense and transmit the ambient temperature, and at the same time identify items, which have more practical functions than general tags. The RFID tag chip with integrated temperature sensor can be widely used in the medical and healthcare field, and combined with portable medical electronic equipment. This development will greatly promote the further improvement of the global medical service level and the level of disease prevention.

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