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RESEARCH ARTICLE

Design and Implementation of Single-Input-Multi-Output DC-DC Converter Topology for Auxiliary Power Modules of Electric Vehicle

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ABSTRACT A compact DC-DC converter is required as an auxiliary power module in Electric Vehicles (EVs) to power the onboard electric motor and other auxiliaries. Most of the existing multi-port converters have limitations on duty ratio, charging currents of the inductor ($i_{L1}>i_{L2}$ or $i_{L1}<i_{L2}$), output voltages ($V_{01}>V_{02}$ or $V_{01}<V_{02}$), and the issue of cross-regulation during load variation. This paper presents a multi-port DC-DC converter with Single-Input Multiple-Output (SIMO) to circumvent all these limitations. The proposed topology generates independent outputs without affecting the other loads during the operation. It is observed that cross-regulation is effectively eliminated while controlling the loads. The control of the converter is simple without any duty ratio and inductor current charging constraints. The validity of the proposed converter has been verified by using a prototype with a 100W rating and delivers two output voltages of 24V and 14.4V at duty ratios of 50% and 30% with an input voltage of 48V. It can be extended to multiple outputs. The simulation and experimental results are analyzed to prove the effectiveness of this auxiliary power module for EV applications.

INDEX TERMS Auxiliary power module, cross-regulation, DC-DC converter, electric vehicle, single-input-dual-output converter.

NOMENCLATURE

V_{DC}	Input voltage.
I_{DC}	Input current.
D_1, D_2	Duty ratio of switches.
S_1, S_2	Switches.
D_{1D}, D_{2D}	Diodes.
L_1, L_2	Inductors.
C_1, C_2	Capacitors.
V_{01}, V_{02}	Output voltages.
I_{01}, I_{02}	Output currents.
i_{L1}, i_{L2}	Inductor currents.
V_{C1}, V_{C2}	Voltage across capacitors.
i_{D1D}, i_{D2D}	Current through the diodes.
V_{S1}, VS2	Voltage across the switches.
i_{D1D}, i_{D2D}	Current through the diodes.
V_{S1}, V_{S2}	Voltage across the switches.
c_{1-8}	Initial values.
t	Time period.
M_{VDC1}	Voltage gain at load-1.
M_{VDC2}	Voltage gain at load-2.
T_S	Time period in one switching cycle.
f	Switching frequency.
Δi_{L1}	Inductor (L_1) ripple current.
Δi_{L2}	Inductor (L_2) ripple current.
CCM	Continuous conduction mode.
DCM	Discontinuous conduction mode.

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D_M	Duty ratio between CCM and DCM.
x, u	State and input vectors.
B, C, E, F	Matrices of appropriate size.
y	Output vector.
G_{vd1}	Transfer function at load-1.
G_{vd2}	Transfer function at load-2.
V_{Smax}	Maximum voltage stress across switch.
D_{1min}, D_{2min}	Minimum duty ratios.
D_{1min}, D_{2min}	Maximum duty ratios.
L_{1min}, L_{2min}	Minimum inductance.
L_{1max}, L_{2max}	Maximum inductance.
R_{L1max}, R_{L2max}	Maximum load resistance.
D_{max}	Maximum duty ratio.
Δi_{L1max}	Maximum inductor (L_1) ripple current.
Δi_{L2max}	Maximum inductor (L_2) ripple current.
C_{1min}, C_{2min}	Minimum capacitance of capacitors.
r_C	ESR of the filter capacitor.
V_{cpp}	Peak-to-peak ripple output voltage.
$i_{F,}$	Forward current of the switch.
V_F	Threshold voltage of the switch.
r_{DS}	On-state resistance of the switch.
P_O	Output power.
Vr	Ripple voltage.
S_{V_Sttess}	Switch voltage stress.
D_{V_Sttess}	Diode voltage stress.
S_{I_Sttess}	Switch current stress.
D_{I_Sttess}	Diode current stress.
N_S	Number of switches.
N_D	Number of diodes.
N_L	Number of inductors.
N_C	Number of capacitors.
$N_{component}$	Number of components.
N_{input}	Number of inputs.
N_{output}	Number of outputs.
t_{on}	Switch on-time.
t_{off}	Switch off-time.
P_D	Diode conduction loss.
R_F	diode forward resistance.
I_D	Average value of the diode current.
I_{Drms}	RMS value of the diode current.
P_{RFD}	Diode conduction loss due to RF.
R_{FD}	Diode forward voltage.
P_{VFD}	Diode conduction loss due to VF.
P_{rL}	Power loss in the inductor ESR.
r_L	Effective resistance of an inductor.
i_{rms}	RMS value of the switch current.
I_0	Load current.
Δi_L	Maximum inductor ripple current.
r_C	Effective resistance of the capacitor.
P_{rC}	Power loss in the capacitor ESR.
P_I	Input power.
M_{IDC}	Current gain.

I. INTRODUCTION

The depletion of fossil fuels has an extreme impact on the automobile industry, influenced by environmental issues, including global warming and increment in the carbon footprint. These issues are effortlessly addressed by integrating power converters with renewable energy sources like photovoltaic (PV) and fuel cells. However, the variety of renewable energy sources and varied power converters complicates their penetration. The DC-DC converters are usually application-specific and suitable for low to high-power applications in Electric Vehicles (EVs) and grid-tied converters [1], [2]. The automotive industry, as well as many national governments, have recently promoted and invested significant resources in developing EVs and hybrid electric vehicles (HEVs) to reduce dependency on fossil fuels while providing users with energy-efficient, environmentally-friendly transportation. The sales growth of EVs and HEVs is not yet equivalent to that of traditional internal combustion engine vehicles, owing to parts design problems and the cost of such intermediate devices. A critical challenge in designing an energy-efficient electric powertrain that utilizes numerous integrated power electronics subcomponents while meeting the component expenditure, power density, and volume objectives.

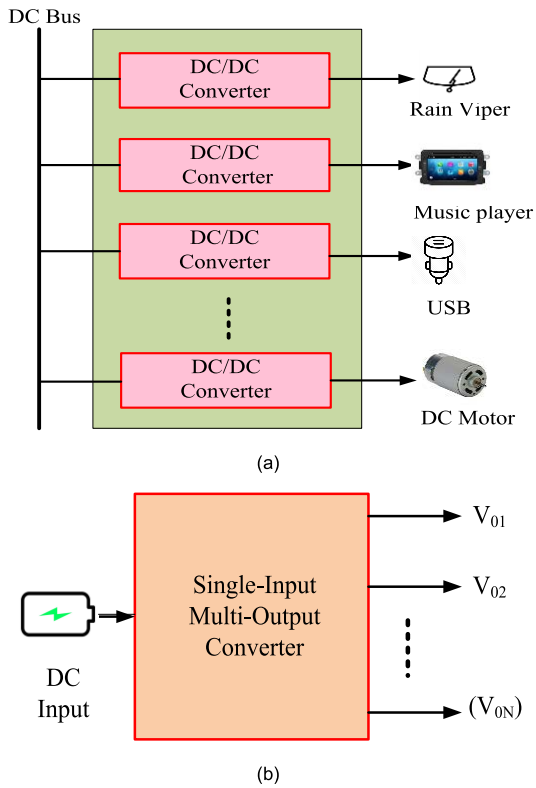

FIGURE 1. (a) Auxiliary power modules, (b) SIMO converter.

A conventional powertrain comprises several power electronic converter modules, each with different power ratings, as shown in Figure 1(a). In the powertrain, a DC-DC converter, also known as an auxiliary power module, is critical because it supplies power to vehicle accessories, such as power steering, wiper blade motors, music systems, headlamps, and other modules. Moreover, it functions continuously throughout the vehicle's operation.

Multi-output DC-DC converters are required in various applications, including standby power supplies, LED drivers, and communication systems. Multiple outputs can be generated with multiple windings in the flyback converter to obtain simple circuitry and simplify the design. EVs with auxiliary power modules using Single-Input-Multi-Output (SIMO) DC-DC converters are illustrated in Figure 1(b). However, due to the severe cross-regulation, it is impossible to adjust the output voltages independently, reducing their overall efficiency. SIMO converters have been developed to attain higher efficiency; nonetheless, the cross-regulation problem still is present with these converters.

The topology in [3] and [4] has the potential to operate as buck/boost simultaneously using a single inductor. However, the multiple RC networks cause slow steady-state response. The topology reported in [5] and [6] is a Single-Input Multiple-Outputs (SIMO) and Single Input-Dual Output (SIDO) converter and provides buck operation. However, both these topologies use coupled inductors which is feasible for only low-power applications. A single inductor SIMO with buck/boost operation is reported in [7]. However, the estimation and design of the current predictor for the controller are complex. Most SIMO DC converters are prone to cross-regulation, as reported in [8]. The deadbeat control offers an effective solution to this problem. Nevertheless, an additional current observer is needed from multiple output channels. Eventually, the control strategy gets complex. A novel unidirectional and bidirectional DC-DC converter for buck operation is reported in [9]. This topology is designed using more inductors, which ultimately reduces efficiency. The topology in [10] presents a generalized integrated dual output converter with a wide range of buck action and better steady-state performance. However, the conduction loss for this converter is higher as both the switches operate to yield the different dc outputs. An interleaved synchronous buck converter is reported in [11]. It has a constraint on inductor currents viz. $i_{L1} > i_{L2}$, which reduces converter utilization. Synthesis of Multiple-Input Multiple-Outputs (MIMO) topologies is derived using network theory in [12] with optimized components. However, port voltage restriction and duty ratio may reduce the source voltage utilization and converter operation. A dual output DC converter for step operation is reported in [13] based on the coupled inductor and voltage-lift techniques. The advantage of this topology is high voltage boosting and low voltage stress. Synthesis of single inductor multi-port SIDO and Dual-Input Single-Output (DISO) converters is presented in [14]. However, due to the operating duty ratios, their working conditions will limit the source utilization. Super-lift LUO and buck converter are integrated to develop the SIDO converter in [15] to provide both boost and buck output voltages. The operational constraint on duty ratios, i.e., $D_2 < D_1$, limits the operation range of D_1 when D_2 increases. The topology in [16] has a feature that uses a single switch to enhance the power density by reducing the size. It has high current stress for the generalized structure.

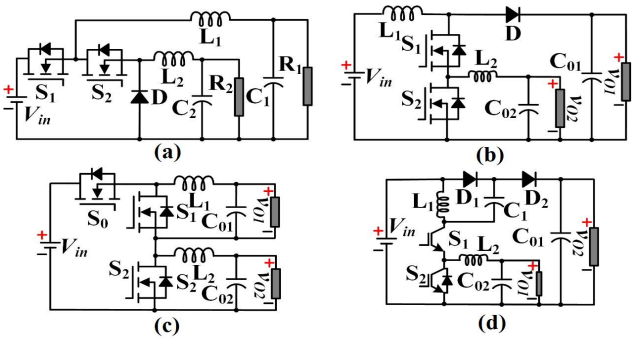

FIGURE 2. SIDO converters; (a) proposed in [9], (b) proposed in [10], (c) proposed in [11], and (d) proposed in [16].

A novel switched ladder network comprising two capacitors and inductors is presented in [17]. Even though this topology yields high voltage gain, the moderately high current stress and the inrush current on switches are problems with this converter, making it suitable for low power applications. A SIDO topology with three-level and multi-port structure features is presented in [18]. The reduction in the component and high efficiency are advantages. However, the current stress on switches and inductors is very high, limiting the topology feasibility for low-power applications. A multi-port switched-capacitor based on differential input buck topology for power management architecture is reported in [19]. It has a high inrush current and capacitor charging current ripples for achieving a substantial voltage boost.

A step-up SIMO architecture using the coupled inductor-based interleaved converter with high efficiency is presented in [20]. The coupled inductor reduces the size of the converter. However, this topology is feasible for very low-power applications. The topology reported in [21] is an interleaved architecture of SEPIC and CUK converters. This topology adds merits to handle adequate power without high voltage and current stress. The synchronous and interleaved mode of operation has high efficiency and a high-power advantage [22]. Various SIDO DC-DC converters are available in the literature for EVs application, and a few converters are depicted in Figure 2. The converters shown in Figure 2 in the recent literature have a high voltage gain and continuous current. However, it has some constraints on converter operation.

A new SIDO DC-DC converter topology for auxiliary power module applications is proposed in this paper to overcome the cross-regulation problem and other limitations of existing SIMO converters in the literature. The benefits of the proposed converter are, (i) the converter can produce different output voltages with independent or simultaneous control of two loads, (ii) there are no duty cycle constraints ($D_1 > D_2$ or $D_2 < D_1$ or $D_1 = D_2$), and port voltage restriction ($V_{01} > V_{02}$ or $V_{01} < V_{02}$) during control, and it enhances the battery utilization, and (iii) Avoid the cross-regulation problems. The main contributions of the paper are as follows.

- Design of a new SIDO DC-DC converter topology
- Possible extension of the proposed converter to multiple outputs

- Small-signal analysis of the proposed SIDO converter
- Stress analysis, power loss calculations, and controller design
- Simulation and experimental investigations

This paper is organized as follows: Section II describes the proposed SIDO topology and different operating modes. In Section III, a small-signal analysis is presented. Semiconductor stress analysis, design parameters, analysis of power loss, performance comparison, and controller design are dealt with in Section IV. The results and discussions are presented in Section V. Finally conclusion is presented in Section VI.

II. PROPOSED SINGLE-INPUT-DOUBLE-OUTPUT DC-DC CONVERTER TOPOLOGY

The proposed converter operation for Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) is elaborated here. The proposed SIDO converter structure is portrayed in Figure 3(a). It has two switches (S_1, S_2), two diodes (D_{1D}, D_{2D}), two inductors (L_1, L_2), two capacitors (C_1, C_2), and load (R_1, R_2). In this topology, output voltages are independently regulated at different voltage levels by the duty cycle $D_1 - D_2$. The extended version of the proposed SIMO converter with multiple outputs is illustrated in Figure 3(b). It requires N switches, N-inductors, and N-capacitors for N-outputs. The proposed N-output version configuration can generate the independent outputs and avoid the ground problems between the outputs during their control.

The advantages of the proposed converter are:

- It is a simple structure, without using any operational constraint on duty ratio ($D_1 > D_2$ or $D_2 < D_1$ or $D_1 = D_2$)
- It can generate independent output voltages.
- No assumptions are made on inductor currents like $i_{L1} < i_{L2}$ or $i_{L1} > i_{L2}$ during control.
- Loads are isolated during real-time control of the loads, which avoids the issue of cross-regulation
- The circuit configuration can also be extended to N-outputs

It is observed that a buck mode of operation is required for EVs' auxiliary power system application. In the proposed configuration, as shown in Figure 3(b), the outputs $V_{01} - V_{0N}$ are less than V_{DC}, and they can be regulated simultaneously and individually. The converter presented in this paper is suitable to handle the loads on present and future load requirements of an EV.

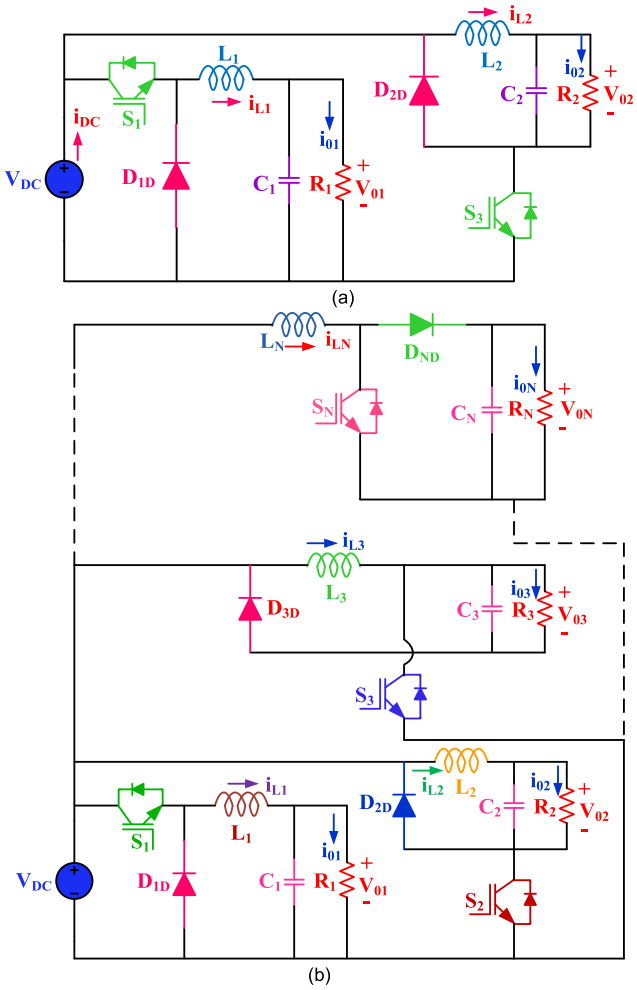

FIGURE 3. Proposed configuration: (a) Dual output version, (b) N-output version.

A. CONTINUOUS CONDUCTION MODE (CCM)

1) SWITCHING STATE 1

Power semiconductor switches S_1 and S_2 are kept ON in this state. The current flow path is depicted in Figure 4(a). In state 1, L_1 and L_2 are magnetized by the energy port V_{DC} and supply energy to the loads (R_1 and R_2). The current through inductors and voltage across capacitors are given in equations (1)-(4).

$$i_{L1}(t) = \frac{V_{DC}}{R_1} + e^{-\alpha_1 t}\left[c_1 \cos\omega_1 t + c_2 \sin\omega_1 t\right] \tag{1}$$

$$v_{C1}(t) = V_{DC} - \frac{L_1}{2C_1} e^{-\alpha_1 t}\begin{bmatrix} \cos\omega_1 t\left(\frac{\alpha_1 c_1}{R_1} + \omega_1 c_2\right) \\ + \sin\omega_1 t\left(-\alpha_1 c_2 + \frac{\omega_1 c_1}{R_1}\right)\end{bmatrix} \tag{2}$$

$$i_{L2}(t) = \frac{V_{DC}}{R_2} + e^{-\alpha_2 t}\left[c_3 \cos\omega_2 t + c_4 \sin\omega_2 t\right] \tag{3}$$

$$v_{C2}(t) = V_{DC} - \frac{L_2}{2C_2} e^{-\alpha_2 t}\begin{bmatrix} \cos\omega_2 t\left(\frac{\alpha_2 c_3}{R_2} + \omega_2 c_4\right) \\ + \sin\omega_2 t\left(-\alpha_2 c_4 + \frac{\omega_2 c_3}{R_2}\right)\end{bmatrix} \tag{4}$$

2) SWITCHING STATE 2

In this state, the L_1 and L_2 are de-magnetized and deliver their stored energy to load R_1 and R_2 through D_{1D} and D_{2D}, as shown in Figure 4(b). The current through inductors and voltage across capacitors are given in equations (5)-(9) during this mode.

$$i_{L1}(t) = e^{-\alpha_1 t}\left[c_5 \cos\omega_1 t + c_6 \sin\omega_1 t\right] \tag{5}$$

$$v_{C1}(t) = -L_1 e^{-\alpha_1 t}\begin{bmatrix} (-\alpha_1 c_5 + \omega_1 c_6)\cos\omega_1 t \\ + (\omega_1 c_5 - \alpha_1 c_6)\sin\omega_1 t\end{bmatrix} \tag{6}$$

$$i_{L2}(t) = e^{-\alpha_2 t}\left[c_7 \cos\omega_2 t + c_8 \sin\omega_2 t\right] \tag{7}$$

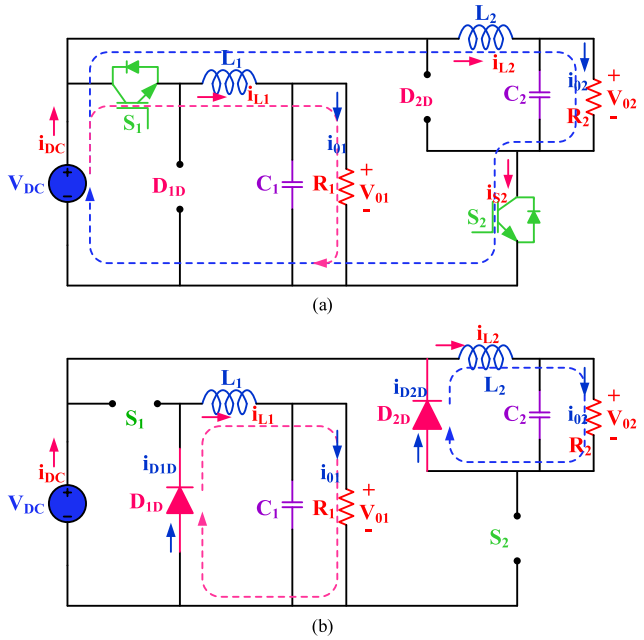

FIGURE 4. Modes of operation: (a) Switching state 1, (b) Switching state 2.

$$v_{C2}(t) = -L_2 e^{-\alpha_2 t}\begin{bmatrix}(-\alpha_2 c_7 + \omega_2 c_8)\cos\omega_2 t \\ +(\omega_2 c_7 - \alpha_2 c_8)\sin\omega_2 t\end{bmatrix} \quad (8)$$

where

$$\alpha_1 = \frac{1}{2R_1C_1}, \quad \omega_1 = \frac{1}{2}\sqrt{\left(\frac{1}{R_1^2C_1^2} - \frac{4}{L_1C_1}\right)},$$
$$\alpha_2 = \frac{1}{2R_1C_1} \text{ and } \omega_2 = \frac{1}{2}\sqrt{\left(\frac{1}{R_2^2C_2^2} - \frac{4}{L_2C_2}\right)} \quad (9)$$

The key component waveforms of circuit elements in the proposed configuration are illustrated in Figure 5 for CCM. In mode-1, when S_1 and S_2 are turned on, the voltage across inductor $L_1(V_{L1})$ is subjected to $V_{DC} - V_{01}$. The current is raised with the positive slope of $(V_{DC} - V_{01})/L_1$. Consequently, the voltage across inductor $L_2(V_{L2})$ is subjected to $V_{DC} - V_{02}$, and the current is raised with the positive slope of $(V_{DC} - V_{02})/L_2$. In mode-2, when S_1 and S_2 are turned off, the voltage across inductor $L_1(V_{L1})$ is subjected to $-V_{01}$. Now the current is decreased with the negative slope of $-V_{01}/L_1$. At the same time, the voltage across inductor $L_2(V_{L2})$ is subjected to $-V_{02}$. Consequently, the current decreases with a negative $-V_{02}/L_2$ slope. It is observed that during mode-2, the source current is zero as the source is open-circuited when S_1 and S_2 switches are turned off. This process is repeated for every cycle of control.

From the CCM, the output voltage equations for the duty ratios are given (10) for the proposed converter.

$$V_{01} = D_1V_{DC},$$
$$V_{02} = D_2V_{DC} \quad (10)$$

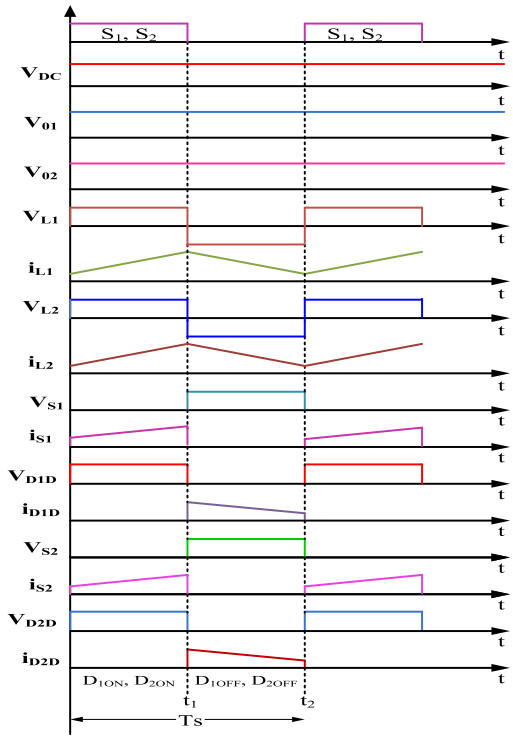

FIGURE 5. Theoretical waveforms of the proposed converter in CCM.

From the above discussions, it is observed that change in one load would not influence the other. Hence, the issue of cross-regulation is eliminated, and the circuit configuration facilitates that the inductor stored energy is limited to one particular load only. So, the converter allows independent control and operation of loads. More importantly, the control of this converter is simple and has no control and operational constraints on duty ratio and inductor currents.

B. DISCONTINUOUS CONDUCTION MODE (DCM)

This section elaborates on the converter operation during DCM, and corresponding equivalent circuits are given in Figure 6(a-c). The respective current and the voltage plots are shown in Figure 7 for ideal conditions.

In DCM, there are three modes of operation. In mode-1, when S_1 and S_2 are turned on, the voltage across inductor L_1 (V_{L1}) is subjected to $V_{DC} - V_{01}$. The current is raised with the positive slope of $(V_{DC} - V_{01})/L_1$. Consequently, the voltage across inductor $L_2(V_{L2})$ is subjected to $V_{DC} - V_{02}$, and the current is raised with the positive slope of $(V_{DC} - V_{02})/L_2$. In mode-2, when S_1 and S_2 are turned off, the voltage across inductor L_1 (V_{L1}) is subjected to $-V_{01}$. Now the current is decreased with the negative slope of $-V_{01}/L_1$. At the same time, the voltage across inductor $L_2(V_{L2})$ is subjected to $-V_{02}$. Consequently, the current decreases with a negative $-V_{02}/L_2$ slope. This process is repeated for every cycle of control. In mode-3, due to the lower current magnitude, it would become zero during t_2 to t_3,

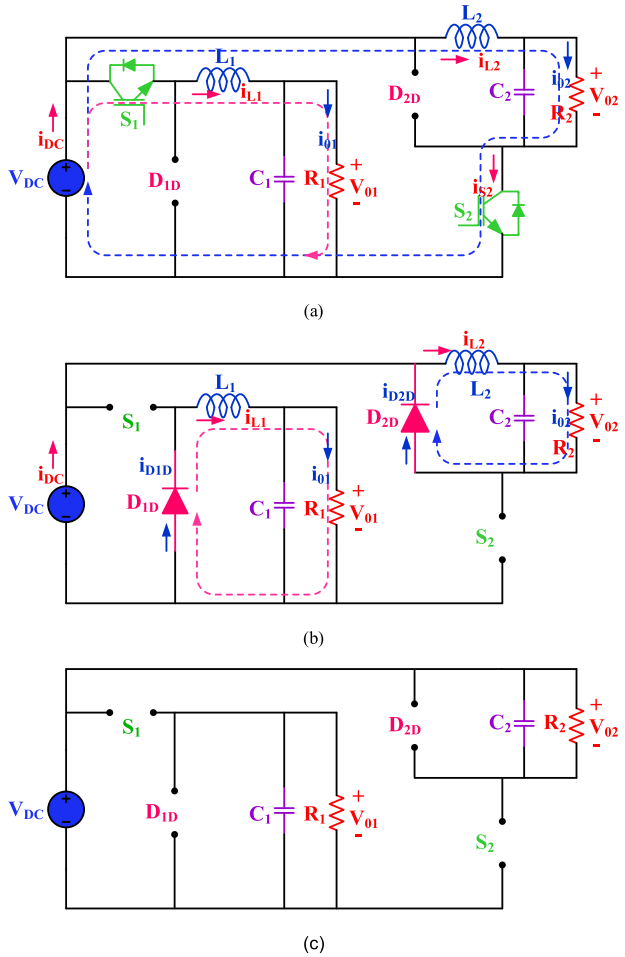

FIGURE 6. Modes of operation in DCM: (a) Switching state 1-Switches are ON, (b) Switching state 2- Switches are OFF, diodes are forward biased, and (c) Switching state 2- Switches are OFF, diodes are reverse biased.

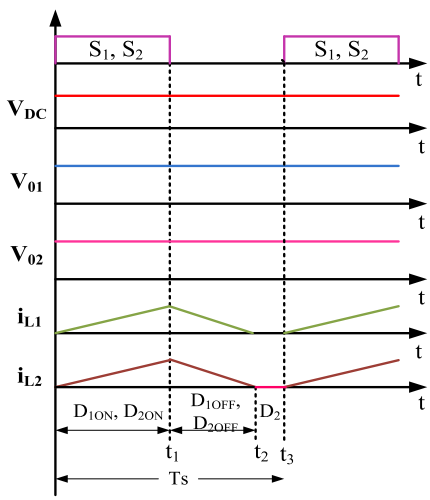

FIGURE 7. Theoretical waveforms of the proposed converter in DCM.

as shown in Figure. 7, just before the S_1 and S_2 are turned ON in the next cycle.

The output voltage equation expressions are written using the volt-sec balance for load-1 as given in (11).

$$(V_{DC} - V_{01})D_{1ON}T_S = V_{01}D_{1OFF}T_S \tag{11}$$

The output current equation (12) is written as follows.

$$I_{01} = \frac{1}{T}\int_0^{T_S} i_{L1}dt = \frac{(D_{1ON} + D_{1OFF})\Delta i_{L1}}{2} \tag{12}$$

The peak-to-peak inductor current is expressed in (13) as follows.

$$\Delta i_{L1} = \frac{(V_{DC} - V_{01})D_{1ON}}{L_1} = \frac{V_{01}D_{1ON}(1 - M_{VDC1})}{fL_1M_{VDC}} \tag{13}$$

$$I_{01} = \frac{V_{01}D_1^2(1 - M_{VDC1})}{2fL_1M_{VDC1}^2} \tag{14}$$

$$D_{1ON} = \sqrt{\frac{2fL_1M_{VDC1}}{R_{01}(1 - M_{VDC1})}} \tag{15}$$

$$\text{for } D_{1ON} = 1 - \frac{2fL_1}{R_1} \tag{16}$$

$$D_{1ON} = 1 - \frac{2fL_1I_{01}}{V_{01}} \tag{17}$$

The boundary between CCM and DCM is expressed as follows.

$$M_{VDC1} = D_B = \sqrt{\frac{2fL_1M_{VDC1}^2}{R_{01}(1 - M_{VDC1})}} \tag{18}$$

Rearranging eq. 15, one obtains,

$$\frac{2fL_1}{D_{1OFF}R_1}M_{VDC1}^2 + M_{VDC1} - 1 = 0 \tag{19}$$

By solving the above equation, the voltage gain under DCM is

$$M_{VDC1} = \frac{2}{1 + \sqrt{1 + \frac{8fL_1}{D_{1ON}^2R_1}}} \tag{20}$$

The duty ratio, D_{1OFF}, can be derived in terms of D_{1ON}, L_1, f, and R_{01} as follows.

$$D_{1OFF} = D_{10N}\left(\frac{1}{M_{VDC1}} - 1\right) \tag{21}$$

$$D_{10FF} = \left(\sqrt{1 + \frac{8fL_1}{D_{1ON}^2R_1}} - 1\right) \tag{22}$$

The above procedure is the same for the derivation of D_{2ON}, D_{2OFF}, and voltage gain-2 (M_{VDC2}) at load-2.

III. SMALL-SIGNAL MODELING

The converter is derived based on the description in [11], [22]. The general forms of dynamic equations in the state-space form are as in (10)-(27).

$$\frac{dx}{dt} = Bx + Cu \tag{23}$$

$$y = Ex + Fu \tag{24}$$

where 'x' and 'u' state and input vectors and 'y' denotes the output vector. The above equations are applicable for one

switching cycle, and the state equation and output equations are expressed as,

$$\dot{x} = B_n x + C_n u \tag{25}$$
$$y = E_n x + F_n u \tag{26}$$

where n = 1, 2 based on the mode of operation. The state equations are expressed as follows.

$$\dot{x} = dB_1 x + (1-d)B_2 x + dC_1 u + (1-d)C_2 \tag{27}$$
$$y = dE_1 x + (1-d)E_2 x + dF_1 u + (1-d)F_2 u \tag{28}$$

The perturbations are added in voltage, current, and duty ratio for linearizing the above state equation and expressed in (29)-(34) as follows.

$$d = D + \hat{d} \tag{29}$$
$$U = U + \hat{u} \tag{30}$$
$$X = X + \hat{x} \tag{31}$$
$$Y = Y + \hat{y} \tag{32}$$

The average model given in matrix form for the suggested converter is as follows.

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} = B \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + CV_{DC} \tag{33}$$

where

$$B = \begin{bmatrix} 0 & 0 & \frac{-(1-D_1)}{L_1} & 0 \\ 0 & 0 & 0 & \frac{(1-D_2)}{L_2} \\ \frac{(1-D_1)}{C_1} & 0 & \frac{-1}{R_1C_1} & 0 \\ 0 & \frac{(1-D_2)}{C_2} & 0 & \frac{-1}{R_2C_2} \end{bmatrix} \tag{34}$$

$$C = \begin{bmatrix} \frac{1}{L_1} \\ \frac{D_2}{L_2} \\ 0 \\ 0 \end{bmatrix}, \quad E = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{35}$$

The derived output voltages $\hat{v}_{01}$, $\hat{v}_{02}$, $\hat{d}_1$, $\hat{d}_2$ expressions are in (36) and (37).

$$\hat{v}_{01}(s) = G_{vd1}\hat{d}_1(s) \tag{36}$$
$$\hat{v}_{02}(s) = G_{vd2}\hat{d}_2(s) \tag{37}$$

The transfer function model for the converter is given in (38)-(39) below.

$$\frac{\hat{v}_{01}(s)}{\hat{d}_1(s)} = \frac{V_{DC}}{R_1}\left[\frac{1 + sC_1R_1}{1 + s\frac{L_1}{R_1} + s^2L_1C_1}\right] \tag{38}$$
$$\frac{\hat{v}_{02}(s)}{\hat{d}_2(s)} = \frac{V_{DC}}{R_2}\left[\frac{1 + sC_2R_2}{1 + s\frac{L_2}{R_2} + s^2L_2C_2}\right] \tag{39}$$

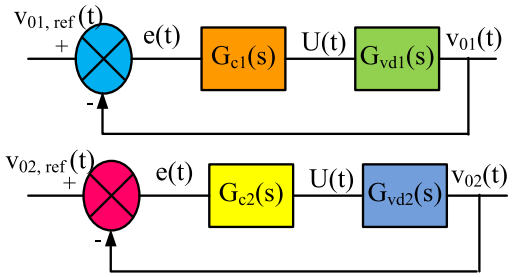

FIGURE 8. Control block diagram of the proposed converter.

A. CONTROLLER DESIGN

The closed-loop control design for the suggested converter is illustrated in Figure 8. The transfer function model of the converter is controlled using the PID controller. The gains selected using Ziegler-Nichols thumb rules and adequately tuning the gains produced desired output voltages across the loads. The effectiveness of the controller is also tested at sudden variations of the loads.

The output voltages $\hat{v}_{01}\hat{v}_{02}$ are determined by $\hat{d}_1$ and $\hat{d}_2$, as given in (40).

$$\hat{v}_{01}(s) = G_{vd1}\,\hat{d}_1(s), \quad \hat{v}_{02}(s) = G_{vd2}\,\hat{d}_2(s) \tag{40}$$

The proportional gain $(Kp_1) = 0.002$, integral gain $(K_{i1}) = 0.21$, and differential gain $(K_{d1}) = 0$ are used during the control of the load-1 output voltage. Similarly, proportional gain $(Kp_2) = 0.083$, integral gain $(K_{i2}) = 1.614$ and differential gain $(K_{d2}) = 0$ are used for control the load-2 output voltage.

The bode plot of the open-loop transfer is shown in Figure 9(a-b), with the gain margins of 0.979dB and 1.05dB, and the phase margins are 127° and 144° for the derived open-loop transfer functions. The bode plot of the suggested converter with closed is depicted in Figure 9(c-d). The gain margins of 3.17dB and 1.49dB, and the phase margins are 113° and 134°, respectively. It is noticed that the closed-loop control is stable for the converter.

IV. PERFORMANCE ANALYSIS AND COMPARATIVE ASSESSMENT

This section describes the current and voltage stresses of the power semiconductor switches, the design procedure, the power loss calculations and their distributions, and the performance comparison.

A. VOLTAGE AND CURRENT STRESS ANALYSIS

The voltage and current stress analysis for the proposed converter are given from (41)-(43) based on the literature given in [22].

The voltage stress across the power semiconductor switch and diodes are expressed as follows.

$$V_{S1} = V_{S2} = V_{DC}, \quad V_{D1D} = V_{D2D} = V_{DC} \tag{41}$$

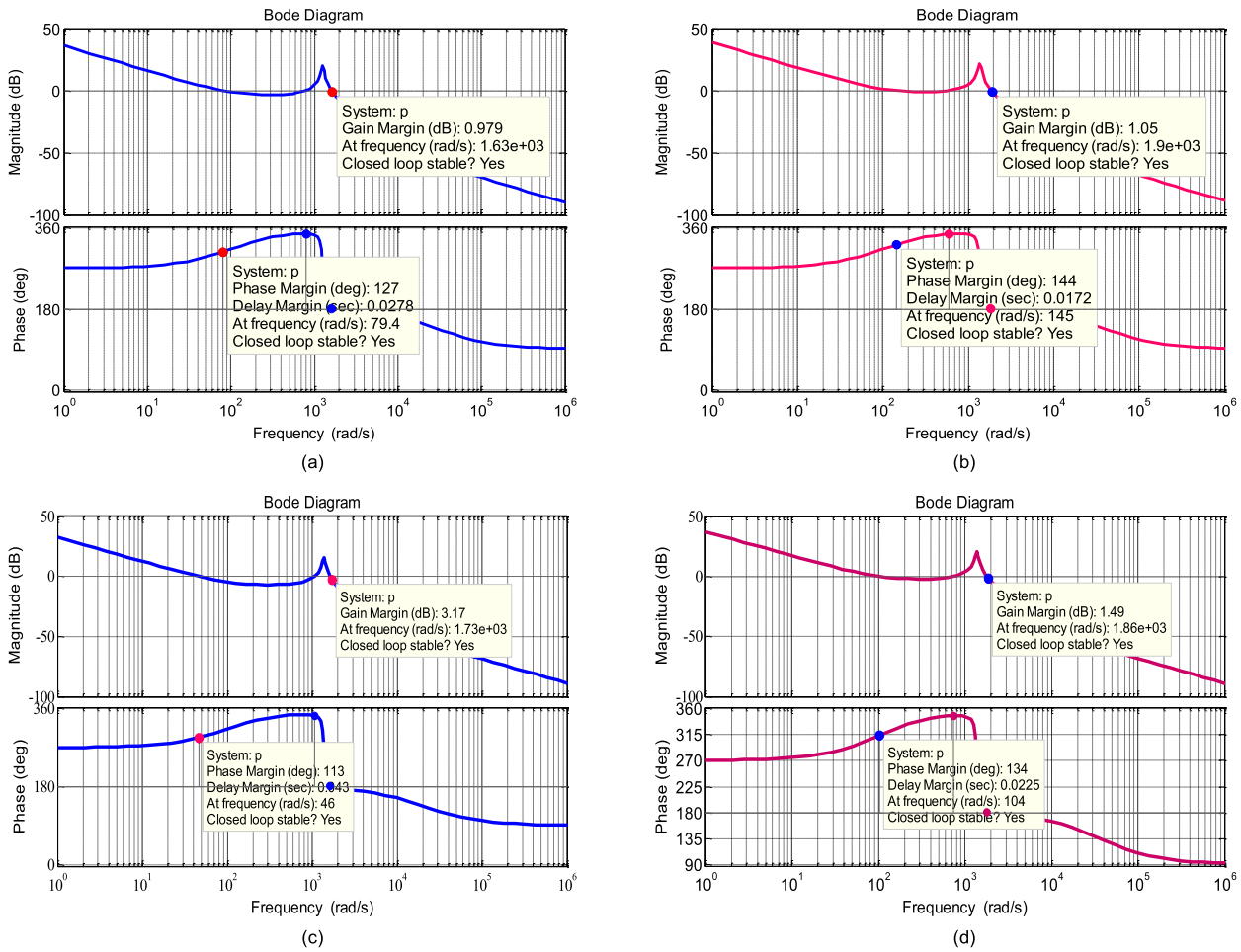

FIGURE 9. Bode plot analysis of the proposed converter: (a) without controller for G_{vd1}, (b) without controller for G_{vd2}, (c) with controller for G_{vd1}, and (d) with controller for G_{vd2}.

Similarly, the current stresses on the power switches and diodes are expressed as follows.

Mode 1:

$$\begin{aligned} i_{S1} &= i_{L1}, \quad i_{D1D} = 0 \\ i_{S2} &= i_{L2}, \quad i_{D2D} = 0 \end{aligned} \tag{42}$$

Mode 2:

$$\begin{aligned} i_{S1} &= 0, \quad i_{D1D} = i_{L1} \\ i_{S2} &= 0, \quad i_{D2D} = i_{L2} \end{aligned} \tag{43}$$

B. PARAMETER DESIGN

The parameter design for the proposed converter is given in equations from (44)-(47) and is derived based on literature given in [22]. The designs of inductors are given in (44).

$$\begin{aligned} L_{1min} &= \frac{R_{L1max}(1 - D_{1min})}{2f} \\ L_{2min} &= \frac{R_{L2max}(1 - D_{2min})}{2f} \end{aligned} \tag{44}$$

The inductor ripple current can be calculated as in (45).

$$\begin{aligned} \Delta i_{L1\,max} &= \frac{V_{01}(1 - D_{1min})}{fL_1} \\ \Delta i_{L2\,max} &= \frac{V_{02}(1 - D_{2min})}{fL_2} \end{aligned} \tag{45}$$

The output filter capacitance is calculated as in (46).

$$C_{1min} = C_{2min} = \frac{D_{max}}{2r_c f_s} \tag{46}$$

The V_{cpp} denotes the peak-to-peak output ripple voltage, calculated as in (47).

$$V_{cpp} = \frac{V_r}{2} \tag{47}$$

The complete electrical specifications of the proposed converter are provided in Table 1.

C. POWER LOSS CALCULATION

The calculation of power losses helps to determine the efficiency of converter operation, and they are based on the

TABLE 1. Parameter specifications.

Parameter	Simulation	Experimental
Input voltage (V_{DC})	48 V	48 V
Switching frequency (f)	10 kHz	10 kHz
Capacitor (C_1/C_2)	360/200 uF	470/200 uF
Output current (I_{01}/ I_{02})	4.1/3 A	4.1/3 A
Output voltage (V_{01}/V_{02})	24/14.4 V	24/14.4 V
Inductors (L_1/L_2)	0.6/0.4 mH	1/0.5 mH

description given in [23]–[25] and are shown in Eq. (48)-(51).

$$P_{loss\_IGBT} = P_c + P_s \tag{48}$$

The IGBT conduction losses (P_c) are calculated as follows.

$$P_C = \frac{1}{T}\int_0^T (R_{don} i_F + V_{Fo}) i_F dt \tag{49}$$

The switching losses (P_s) are calculated using (50) and expressed as follows.

$$P_S = (E_{OFF,j} + E_{ON,j}) \times f \tag{50}$$

where $E_{OFF/ON}$ is the energy distribution during the respective OFF/ON time of the switch and switching frequency. The efficiency (η) of the converter operation can be calculated as in (51).

$$\eta = \frac{P_O}{P_O + P_S + P_C} \tag{51}$$

D. COMPARATIVE ASSESSMENT

A performance comparison of the proposed converter is presented based on several components, reactive elements, voltage gain, and stresses on the device using recently developed SIMO converters, as presented in Table 2 and Table 3.

The proposed structure is tested at a different set of duty ratios, the corresponding output voltage vs. duty ratio plot is depicted in Figure 10(a). Similarly, output voltage vs. load is illustrated in Figure 10(b). Figure 10(a)-(b) shows that it can produce various output voltages without any duty cycle limitation and independently regulate the outputs. Moreover, irrespective of load variations, the output voltages are not influenced. Hence, one can conclude that the cross-regulation problems do not appear during the control of the proposed converter.

The proposed topology is simple and, without any operational constraints, can generate two different output voltages and independently be regulated. The proposed configuration has less voltage and current stress. Therefore, the converter is appropriate for auxiliary power module applications of EVs

E. EFFECT OF PARASITIC ELEMENTS

Analysis of the converter with parasitic parameters is also presented to know the effectiveness of the converter in real-time operation. Figure 11 shows the converter configuration with the parasitic resistances. The term r_{DS} denotes the

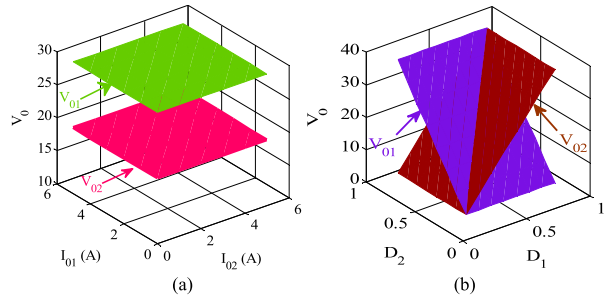

FIGURE 10. Output voltage variation as a function of load current and duty cycle; (a) Output voltage vs. load current, (b) Output voltage vs. duty cycle.

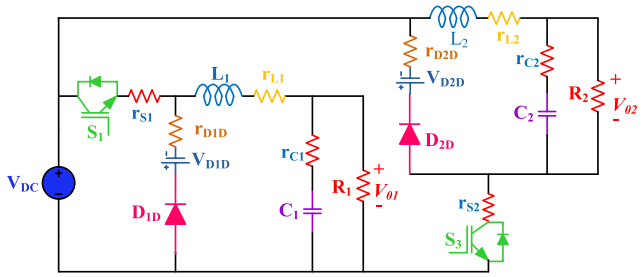

FIGURE 11. The proposed converter circuit with parasitic elements.

on-state resistance of the switch, r_{D1D}, r_{D2D}, and r_{D3D} are the forward resistance of the D_{1-3D}, respectively. r_{L1-2} is the ESR of the inductor $L_1 - L_2$. The mathematical analysis with parasitic elements for different modes of operation as in (52)-(70) is based on the description given in [22].

$$P_C = \frac{r_{DS} D P_0}{(1-D)^2 R_L} \tag{52}$$

R_L is the load resistance and D duty ratio of the switch

The switching loss is expressed as follows.

$$P_S = \frac{1}{6} R_L f\,(t_{on} + t_{off})\,P_0 \tag{53}$$

The total power dissipation in the switch is calculated as follows.

$$P_{loss\_IGBT} = P_C + P_S \tag{54}$$

$$P_{loss\_IGBT} = \left[\frac{r_{DS} D P_0}{(1-D)^2 R_L} + \frac{1}{6} R_L f (t_{on} + t_{off}) P_0\right] \tag{55}$$

The diode conduction loss is calculated as follows.

$$P_D = P_{VFD} + P_{RFD} \tag{56}$$

$$P_{VFD} = V_{FD} I_D = (1-D)\,V_{FD} I_0 = \frac{(1-D)V_{FD}}{V_0} P_0 \tag{57}$$

$$P_{RFD} = R_{FD} I_{Drms}^2 = (1-D)\,R_{FD} I_0^2 = \frac{(1-D)R_{FD}}{R_L} P_0 \tag{58}$$

$$P_D = (1-D)\left[\frac{V_{FD}}{V_0} + \frac{R_{FD}}{R_L}\right] P_0 \tag{59}$$

TABLE 2. Performance comparison for various SIMO converters.

Ref.	Gain	$S_{V\_Stress}/S_{I\_Stress}$	$D_{V\_Stress}/D_{I\_Stress}$	N_S	N_D	N_L	N_C	$N_{component}$	N_{input}	N_{output}	Load Isolation
[10]	$V_{01} = \frac{1}{(1-D_1)}$, $V_{02} = \frac{D_2}{(1-D_1)}$ $D_1 + D_2 = 1$	$V_{Smax} = V_{02}$ $i_S = i_{L1}$	-	2	0	2	2	6	1	2	No
[15]	$V_{01} = D_1 V_{in}$ $V_{02} = (D_2 - D_1)V_b$ $D < 1$	$V_{Smax} = V_{in}$	$V_{Dmax} = V_{in}$	3	3	1	3	10	1	2	No
[16]	$V_{01} = \frac{D}{(1-D)}$ $V_{02} = \frac{1}{(1-D)}$ $D < 1$	$V_{Smax} = \left(\frac{V_g}{1-D}\right)$ $i_S = i_{L1}$	$V_{D_1} = V_g + V_{01}$ $V_{D_2} = V_{02}$ $i_{D_1} = i_{L2}, i_{D_2} = i_{L1}$	1	2	2	3	8	1	2	No
[18]	$v_{01} = \frac{v_{in}}{(2-d_1-d_2)}$, $v_{02} = \frac{v_{in}(1-d_2)}{(2-d_1-d_2)}$ $0.5 < d_1 \,\&\, d_2 < 1$	$V_{Smax} = \frac{V_{01}}{2}$ $V_{S_{1\text{-}6}} = \frac{V_{01}}{2}$ $i_{Smax} = i_{L1}$	-	6	-	2	3	11	1	2	No
[19]	$V_{01} = \frac{2+D}{3}$, $V_{02} = \frac{1+D}{3}, V_{03} = \frac{D}{3}$ $0 < D < 1$	$V_{Smax} = V_{01}$ $i_{Smax} = i_{L1}$	-	12	-	3	8	23	1	3	No
Proposed	$V_{01} = D_1 V_{DC}$ $V_{02} = D_2 V_{DC}$ $0 < D_1 < 1, 0 < D_2 < 1$	$V_{Smax} = V_{01}$, $V_{S1} = V_{01}, V_{S2} = V_{02}$ $i_{S1} = i_{L1}, i_{S2} = i_{L2}$	$V_{D1D} = V_{01}, V_{D2D} = V_{02}$ $i_{D1D} = i_{L1}, i_{D2D} = i_{L2}$	2	2	2	2	8	1	2	Yes

TABLE 3. Performance comparison on SIDO buck topologies.

Ref.	Power Switches and diodes	L	C	Maximum voltage stress	Control Constraint	Load isolation
[1]	6	1	3	$V_{Smax} = V_i$	-	No
[9]	3	2	2	$V_{Smax} = V_i$	$V_{01} > V_{02}$	No
[11]	3	2	2	$V_{Smax} = V_i$	$i_{L1} > i_{L2}$	No
Proposed	4	2	2	$V_{Smax} = V_{DC}$	No assumptions on the inductor charging currents and output voltages	Yes

The inductor loss is given by in (60)

$$P_{rL} = r_L I_{rms}^2 = r_L I_0^2 = \frac{r_L}{R_L} P_0 \tag{60}$$

The capacitor loss is given as follows.

$$P_{rC} = r_C \frac{\Delta i_L^2}{12} \tag{61}$$

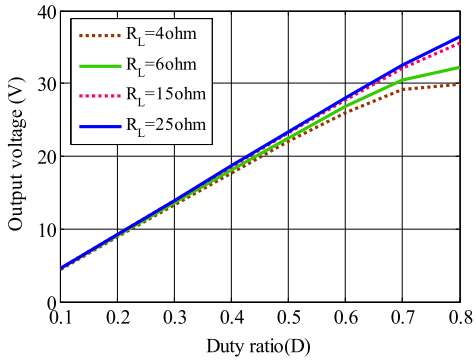

FIGURE 12. Output voltage vs. duty ratio with parasitic elements.

$$P_{rC} = \frac{r_C P_0 (1-D)^2}{12 f^2 L^2} \tag{62}$$

The overall power loss (P_{LS}) of the proposed converter is calculated using (63).

$$P_{LS} = P_C + P_S + P_D + P_{rL} + P_{rC} \tag{63}$$

$$P_{LS} = \left[\frac{r_{DS} D P_0}{(1-D)^2 R_L} + \frac{1}{6} R_L f(t_{on} + t_{off}) P_0\right] + (1-D)\left[\frac{V_{FD}}{V_0} + \frac{R_{FD}}{R_L}\right] P_0 + \frac{r_L}{R_L} P_0 + \frac{r_C P_0 (1-D)^2}{12 f^2 L^2} \tag{64}$$

$$\eta = \frac{P_0}{P_0 + P_{LS}} \tag{65}$$

$$\eta = \frac{1}{1 + \left[\begin{array}{c}\left[\frac{r_{DS} D}{(1-D)^2 R_L} + \frac{1}{6} R_L f(t_{on} + t_{off})\right] \\ + (1-D)\left[\frac{V_{FD}}{V_0} + \frac{R_{FD}}{R_L}\right] + \frac{r_L}{R_L} + \frac{r_C (1-D)^2}{12 f^2 L^2}\end{array}\right]} \tag{66}$$

The voltage gain of the lossy buck converter is as follows.

$$\eta = \frac{P_0}{P_I} = \frac{V_0 I_0}{V_{DC} I_{DC}} = M_{VDC} M_{IDC} \tag{67}$$

$$M_{IDC} = \frac{I_0}{I_{DC}} \tag{68}$$

$$I_{DC} = D I_0 \tag{69}$$

$$M_{VDC} = \frac{D}{1 + \left[\begin{array}{c}\left[\frac{r_{DS} D}{(1-D)^2 R_L} + \frac{1}{6} R_L f(t_{on} + t_{off})\right] \\ + (1-D)\left[\frac{V_{FD}}{V_0} + \frac{R_{FD}}{R_L}\right] + \frac{r_L}{R_L} + \frac{r_C (1-D)^2}{12 f^2 L^2}\end{array}\right]} \tag{70}$$

The above equations (52)-(70) are used to plot the output voltage1 versus duty ratio at different loads by considering the parasitic elements depicted in Figure 12.

V. RESULTS AND DISCUSSIONS

A. SIMULATION RESULTS

This section comprehensively explains the simulation and experimental analysis of the proposed SIDO converter. The electrical specification of the converter is provided in Table. I. Firstly, the proposed converter circuit is simulated in MATLAB/Simulink environment with the parameters described in Table 1 to validate and confirm the theoretical performance of the converter under various conditions. Figure 13 shows the output voltages and inductor currents during open-loop control at fixed duty ratios of $D_1 = 50\%$ and $D_2 = 30\%$. The resultant output voltage V_{01} is 24 volts, and V_{02} is 14.4 volts as the converter operates in buck mode with an input DC voltage of 48 volts. The efficacy of the converter during closed-loop control is shown in Figures 14-17. Figure14 shows the output voltage across load-1 and load-2 for sudden decrement at load-1 at t = 0.5 sec. Similarly, output voltages of the two loads at sudden increment in load-1 are displayed in Figure15. Further, the effect of load-2 variation on the output voltages is also tested, and the corresponding results are shown in Figs. 16-17. Figure 16 shows the output voltages for sudden

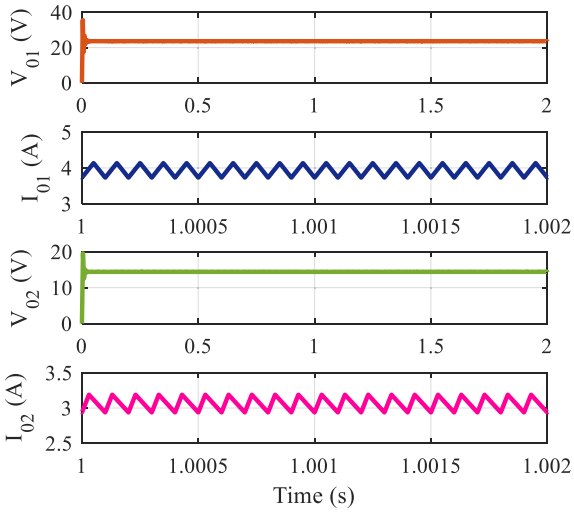

FIGURE 13. Output voltages and currents under open-loop.

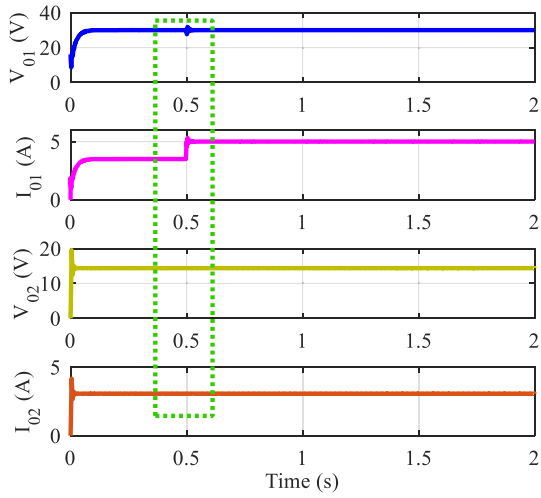

FIGURE 14. Output voltages and currents at −30% decrement of nominal value suddenly for load-1.

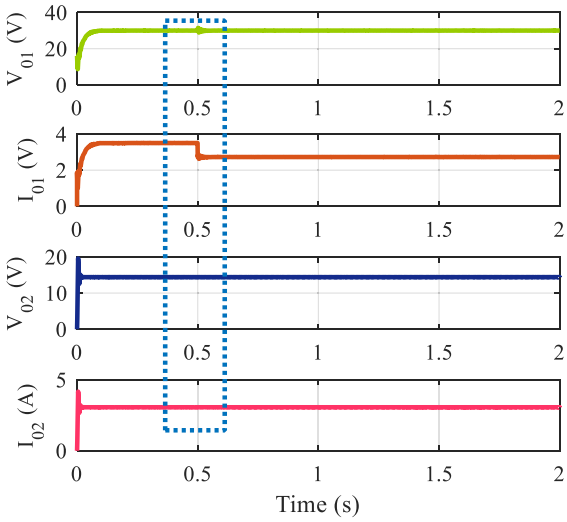

FIGURE 15. Output voltages and currents at +30% increment of nominal value suddenly for load-1.

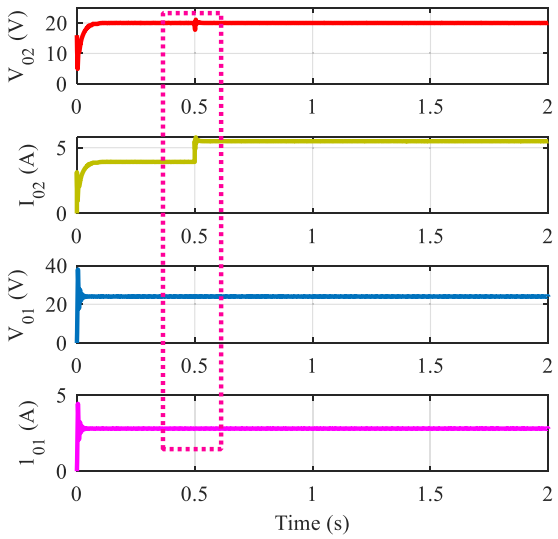

FIGURE 16. Output voltages and currents at −30% decrement of nominal value suddenly for load-2.

decrement of load-2, and Figure17 shows the output voltages due to sudden increment of load-2 at t = 0.5 sec.

The simulation results show that the closed-loop control tracks the desired reference voltages, and its performance is superior even for sudden variations of the loads. Further, it is observed that load-1(load-2) variation is not affecting the load-2 (load-1), and they are entirely decoupled during the control of loads; hence cross-regulation issues are avoided in the proposed SIDO converter.

B. EXPERIMENTAL VERIFICATION

A 100W laboratory prototype was developed to validate the proposed circuit configuration. Various components used in the experimentation are listed in Table. 1. The experimental prototype photograph is shown in Figure 18.

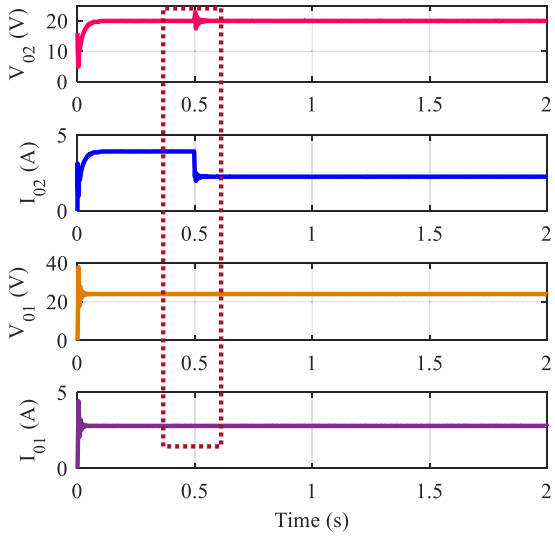

FIGURE 17. Output voltages and currents at +30% increment of nominal value suddenly for load-2.

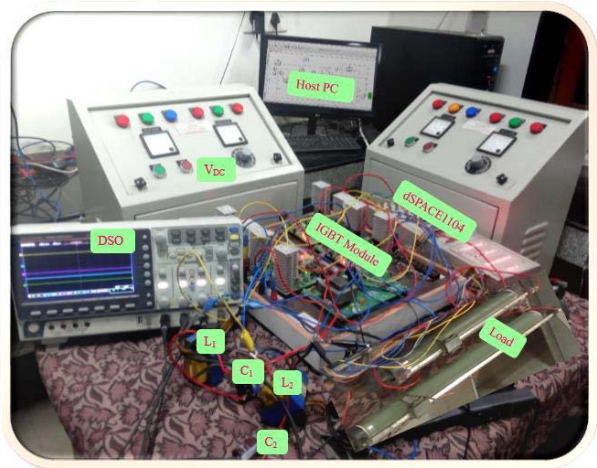

FIGURE 18. Experimental photograph of the experimental prototype setup.

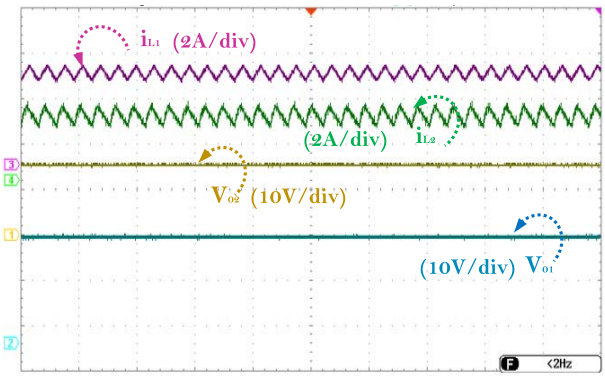

FIGURE 19. Output voltages and currents under open-loop.

dSPACE1104 controller generates control signals to IGBTs (STGW30NC120HD). The proposed converter performance is verified at $D_1 = 50\%$ and $D_2 = 30\%$. The corresponding output voltages are V_{01} at load-1 (R_1) is 24 volts, and V_{02} at load-2 (R_2) is 14.4 volts, as the converter is operating in buck mode at a supply voltage of 48 volts. The output voltages

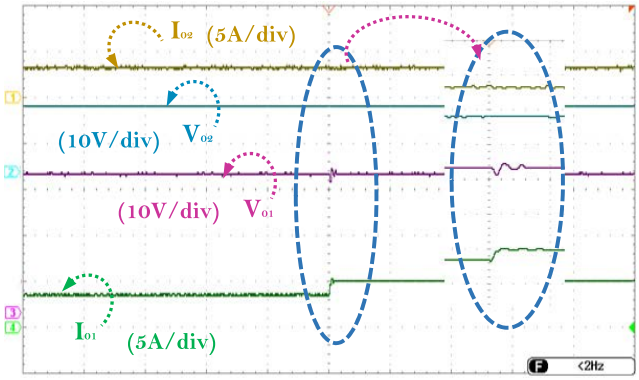

FIGURE 20. Output voltages and currents at −30% decrement of nominal value suddenly for load-1.

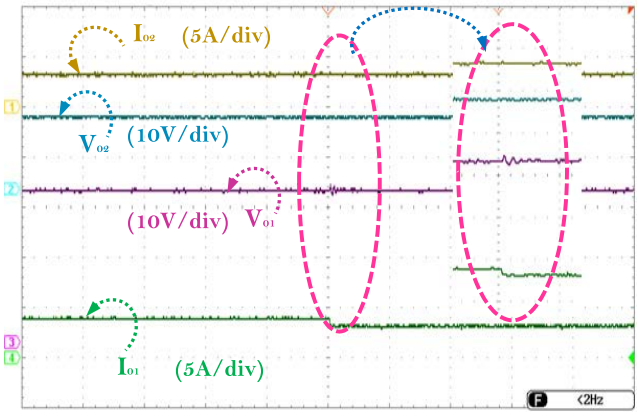

FIGURE 21. Output voltages and currents at +30% increment of nominal value suddenly for load-1.

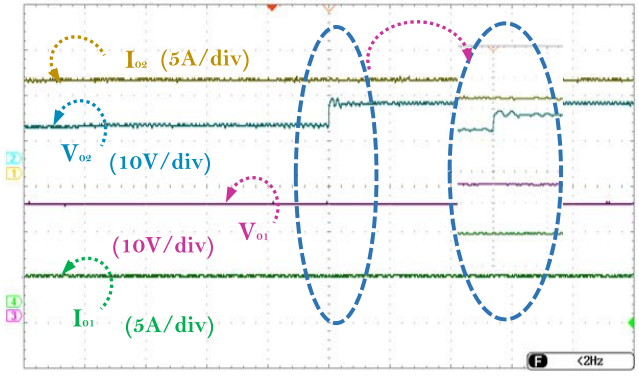

FIGURE 22. Output voltages and currents at −30% decrement of nominal value suddenly for load-2.

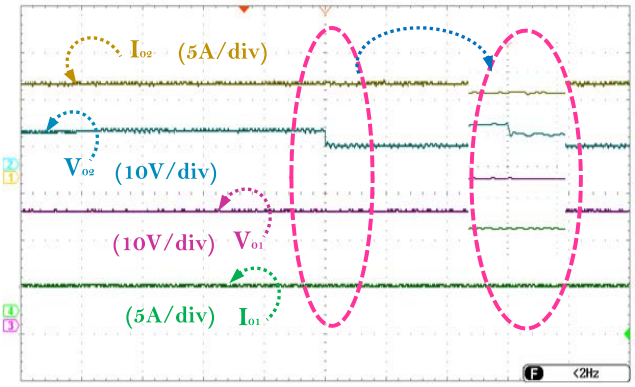

FIGURE 23. Output voltages and currents at +30% increment of nominal value suddenly for load-2.

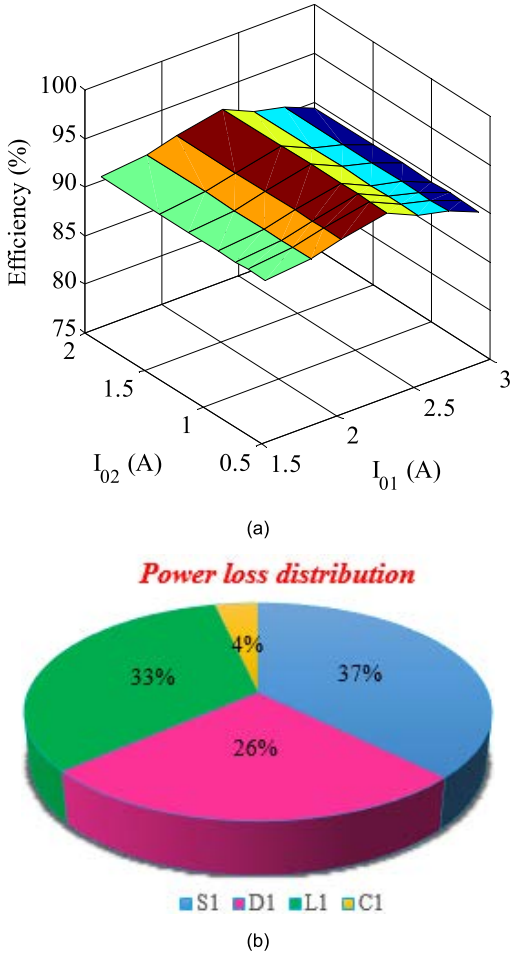

FIGURE 24. (a) Proposed converter efficiency, (b) power loss distribution of switches.

and inductor currents (i_{L1}, i_{L2}) are illustrated in Figure 19. A closed-loop controller is designed for the converter, and the efficacy of closed-loop control is also demonstrated for sudden load variations at ±30% of the nominal value. Now, load-2 (load-1) is varied suddenly while controlling load1 (load-2). Figure 20 shows the converter performance at −30% decrement of nominal value suddenly for load-1 while controlling load-1 voltage in a closed loop.

Moreover, Figure 21 shows the closed-loop control of V_{01} at +30% increment of nominal value suddenly for load-1 while controlling load-1 voltage in a closed loop. Similarly, the effectiveness of closed-loop control for rapid change in load-2 while controlling the output voltage across load-2 (V_{02}) is demonstrated in Figs. 22 and 23, respectively for

−30% decrement and +30% increment of nominal load value. The experiments show that the loads can be controlled individually, and the influence of load variation on other output voltages is negligible in the converter. Hence, the cross-regulation issue is eliminated in the proposed converter. The efficiency of the proposed converter with different load currents and power loss distribution of the components used in the designed circuit is illustrated in Figure 24(a-b).

VI. CONCLUSION

In this paper, a new schematic of the SIDO DC-DC converter topology is proposed, analyzed, and implemented for EVs' auxiliary power module. In addition, the extended version of the proposed converter topology is also proposed to get N-output voltages. The proposed converter in CCM and DCM are comprehensively explained. The proposed converter's small-signal modeling for estimating the transfer function, which is essential in the feedback control loop implementation, and the performance of the closed-control loop response of the proposed converter was verified with the bode plot analysis. The proposed SIDO converter topology is simple without any assumptions on the operational duty cycle and inductor currents during the control. It can produce the two independent output voltages at different duty ratios by avoiding the issues of cross-regulation. The controller was designed for good voltage regulation at load variations, and the converter has been validated with the simulation and experimental results. The simulation and experimental analysis of the proposed extended N-output converter will be carried out in the future. In addition, the proposed converter can also be tested for bi-polar DC microgrid applications.

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