IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 7 June 2022, accepted 11 July 2022, date of publication 20 July 2022, date of current version 3 August 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3192656

RESEARCH ARTICLE

Magnetically Coupled Single-Phase AC-AC Converter With Reduced Number of Passive Components

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ABSTRACT An AC-AC direct single-phase converter based on an impedance network is presented in this manuscript. It possesses all privileges of similar impedance source AC-AC converters such as buck-boost ability, maintaining or reversing the phase angle and sharing the same ground between input and output voltage. Furthermore, a magnetic coupling is exploited to provide high voltage gain by adjusting its turns ratio along with the duty cycle. A safe commutation strategy is implemented to avoid current and voltage spikes across switches needless to utilize snubber circuits. The presented converter offers continuous input current, and ac to ac conversion is done directly without using dc storage, making it appropriate for dynamic voltage restorer to compensate voltage sags and voltage swells. In addition, LC input and output filters are eliminated thanks to impedance network structure. In this regard, the presented topology offers good features in size and cost by reducing passive components compared to similar structures. Also, the comparative investigation shows that the proposed converter benefits from superior operational ranges among similar well-known topologies for the same conditions. Finally, theoretical analyses and operation modes of the proposed converter are discussed and testified by both simulation and experimental results.

INDEX TERMS AC-AC converter, impedance network, magnetic coupling, safe commutation.

I. INTRODUCTION

Over the recent years, single-phase dynamic voltage restorer (DVR) has been used widely to deal with power quality issues for sensitive loads. Single-phase AC-AC converters are exploited as effective series compensators in the DVR systems to compensate voltage sags and swells. The most used AC-AC converters applicable in voltage conditioners are indirect AC-AC converters, direct and indirect matrix converters, and direct PWM AC-AC converters. However, all these converters suffer from some drawbacks. Indirect AC-AC converters require costly battery banks and huge super-capacitors to supply dc sources [1]. Matrix converters utilize a high number of semiconductors devices with complex commutation and provide bounded voltage gain with a maximum of 0.86 [2], [3]. Direct PWM AC-AC converters provide slight current distortion, simple control, simple structure, small parameters, high efficiency, and improved power factor [4], [5]. However, most of them are not able to operate in buck-boost mode simultaneously and suffer from discontinuous input current.

To overcome the aforementioned drawbacks, traditional single-phase Z-source AC-AC converters were proposed in [6], [7]. Although they can both boost and buck input voltage, they suffer from discrete input current, unshared ground between input and output. Quasi Z-source AC-AC converter

The associate editor coordinating the review of this manuscript and approving it for publication was Chandan Kumar.

is introduced in [8] to solve unshared ground, discontinuous input current issues. Also, voltage stress across capacitors decreased dramatically compared to traditional single-phase Z-source AC-AC converters. In [9], a safe commutation strategy has been applied to a family of quasi Z-source AC-AC converters to remove voltage overshoots across switches without requiring snubber circuits, which causes conduction losses reduction along with efficiency improvement. To reduce the number of passive components, a modified quasi Z-source AC-AC converter is proposed in [10]. It provides high-quality output voltage without utilizing output LC filters.

Recently, magnetically coupled inductors have been used in various types of impedance source topologies. In dc-dc impedance source converters, coupled inductors are applied into impedance networks to provide high voltage boost ability with the small duty cycle of converters [11]. Meanwhile, coupled inductors based impedance source inverters appeal to researchers more and more because of their high voltage boost ability with high modulation ratio and low stress across the semiconductors devices [12]–[19]. Single-phase Z-source AC-AC converters based on coupled inductors have been introduced to control ac voltage by adjusting their turn ratio besides the duty cycle of converters. In other words, coupled inductors give more options to impedance source AC-AC converters to regulate the ac output voltage. For instance, a transformer type of quasi Z-source AC-AC converter is presented in [20] to enhance voltage gain by increasing the turn ratio of the transformer along with the duty cycle changing. In order to reduce the size of the converter, an AC-AC impedance source converter based on Γ structure is proposed to attain high voltage gain by reducing the turn ratio of coupled inductors [21]. However, it suffers from discontinuous input current with non-sinusoidal waveform and high THD. Therefore, input filter implementation is necessary to reduce harmonics of input current. Recently, a modified converter in [22] has been proposed to solve the discontinuous input current problem of the topology in [21]. An inductor-less filter has been implemented in an improved single-phase trans-Z-source AC-AC converter in [23], which offers unique features such as improved power density, restrained low-frequency oscillation, and less phase shift between the input and output voltage. Nonetheless, it must employ two more IGBT switches than other single-phase impedance source AC-AC counterparts. A class of transformer-based single-phase Z-source AC-AC converters have been presented in [24] with the combination of two coupled inductors which provide wide range of voltage gain by either increasing or decreasing the turns ratio of coupled inductors. Although, employing two transformers raises the cost and size of the converter. A family of high-frequency transformer isolated (HFTI) based Z-source AC-AC converters have been proposed in [25], [26] to be utilized as DVR without using bulk, expensive and heavy line frequency transformers. These converters employ extra passive components and additional bidirectional switches, which increase their losses, size, and cost. A modified single-phase Γ-source AC-AC converter has been presented in [27], which employs fewer number of components with a reduced number of transformer's turn ratio. However, high distortion is produced for high output voltage when the transformer's turn ratio approaches 1.

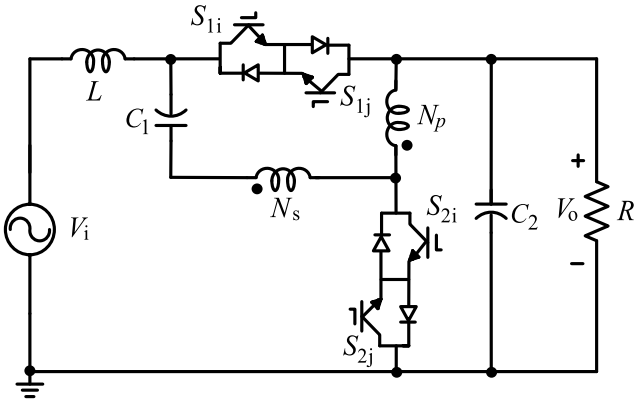

FIGURE 1. Proposed magnetically coupled AC-AC converter.

In this paper, a single-phase AC-AC converter based on coupled inductors is presented. The proposed converter has a lower number of passive components compared to similar counterparts. Its impedance source network structure produces high voltage gain with high-quality waveforms without input and output LC filter. Also, coupled inductors help the converter to attain desired voltage gain with small conducting pulses in a safe commutation strategy. Consequently, the proposed converter offers the turn ratio of coupled inductors as an extra control variable along with the converter's duty cycle. Also, output voltage shares the same ground with input which can reverse and maintain phase angle well. Circuit analysis and operation theory are detailed in the rest of the paper, and experimental tests are performed on a laboratory prototype to verify the theoretical results. In addition, a dynamic voltage restorer based on the proposed converter is presented to compensate voltage sag and voltage swell. Simulation results are provided to show the ability of the proposed converter in voltage sag and swell compensation. Furthermore, the power loss analysis of the proposed converter is then presented and finally, the conclusion of the paper is included.

II. PROPOSED MAGNETIC COUPLED SINGLE-PHASE AC-AC CONVERTER

A. CIRCUIT DESCRIPTION

The overview of the proposed AC-AC converter is shown in Fig. 1. The presented structure consists of ac input voltage, impedance network, and resistive load. Two bidirectional switches have been embedded in the impedance network. Impedance network includes input inductor (L), two capacitors (C_1 and C_2), two bidirectional switches (S_{1i-j},S_{2i-j}), one coupled inductor with two windings (N_p, N_s) where $N=N_s/N_P$ represents its turns ratio. It must be noted that each bidirectional switches consist of two back to back separated switches. It is clear that the proposed topology

utilizes passive components of impedance network instead of input and output filters to reduce switching ripple and harmonic components found in input and output sides. Hence, it saves two inductors and two capacitors in input and output, resulting in lower cost and smaller size of the converter. Furthermore, utilized coupled inductor provides high voltage gain by adjusting turns ratio of the high-frequency transformer. Input inductor connects in series to the input ac source makes the current continuous that brings advantages such as reduced in-rush current, low harmonic, better power factor, and improved efficiency. Also, input and output sides share the same ground, so the converter can operate in both boost in-phase mode and buck-boost out of phase mode, and output can reverse or maintain phase angle with input well.

B. OPERATION PRINCIPLE

Due to dead time and overlap of switches and their speed limitation practically, inductors currents and capacitors voltages might be changed instantly and produce voltage and current spikes across the power switches, which can destroy them. As a result, a snubber circuit must be implemented to provide voltage and current laws of Kirchhoff and to prevent these destructive spikes. However, snubber circuits increase the cost and complexity of the converter and decrease its efficiency. Hence, a safe commutation strategy has been applied to the proposed converter to prevent voltage and current spikes.

Fig. 2 demonstrates the switching pattern of safe commutation strategy for the proposed converter in "boost/buck" "in phase/out of phase" modes. Accordingly, by considering the dead time situation in ideal switches, the switching pattern is formed by input voltage's polarity:

- V_i is positive, and converter operates in "in-phase" mode, S_{1i} is fully turned on to provide the current path, and S_{2j} is turned on for dead time issue.
- V_i is positive, and the converter performs in "in-phase" mode, S_{2i} and S_{2j} are turned on to provide the current path, and S_{1i} is fully turned on to prevent the commutation problem throughout the dead time duration.
- V_i is negative, and converter operates in "in-phase" mode, S_{1j} is conducting as the current path, and S_{2i} is turned on because of dead time condition.
- V_i is negative, and converter performs in "in-phase" mode, S_{2i} and S_{2j} is turned on to provide the current path and S_{1j} is fully turned on for dead time situation.
- V_i is positive, and converter operates in "out-of-phase" mode, S_{1i} and S_{1j} are switched on to provide the current path and S_{2i} is turned on to prevent the commutation problem throughout the dead time.
- V_i is positive, and converter performs in "out-of-phase" mode. S_{2i} and S_{2j} are switched on as the current path and S_{1j} is turned on to prevent the commutation problem throughout the dead time.
- V_i is negative, and converter operates in "out-of-phase" mode, S_{1i} S_{1j} are conducting as the current path and S_{2j} is switched on due to the dead time condition.

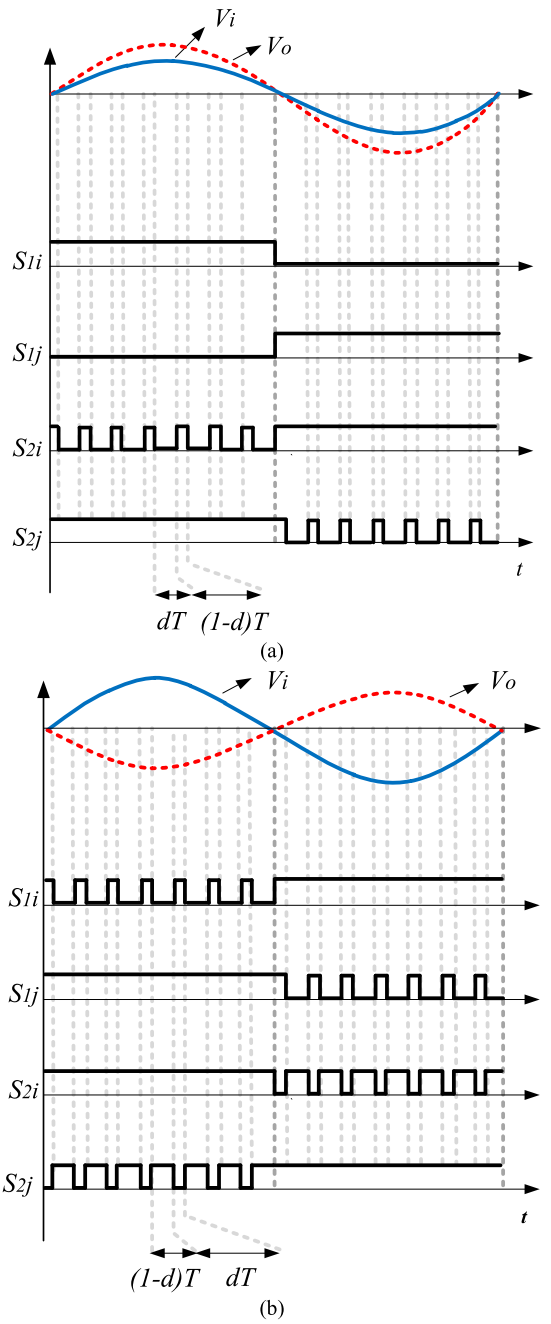

FIGURE 2. Switching pattern of safe commutation strategy for boost/buck (a) in-phase mode, and (b) out-of-phase mode.

- V_i is negative, and converter operates in "out-of-phase" mode, S_{2i} and S_{2j} are switched on as the current path and S_{1i} is switched on to prevent commutation problem.

Fig. 3 illustrates the switching signals and key waveforms of the presented converter when it operates in "in-phase" mode when input voltage is positive. It can be seen that S_{1i} and S_{2j} are fully turned on, and S_{2i} is switching at high frequency. Various current paths of the proposed converter in the boost in-phase mode have been illustrated in Fig. 4 and Fig. 5. Fig. 4 shows operation states of the proposed converter when the input voltage is positive, including state I,

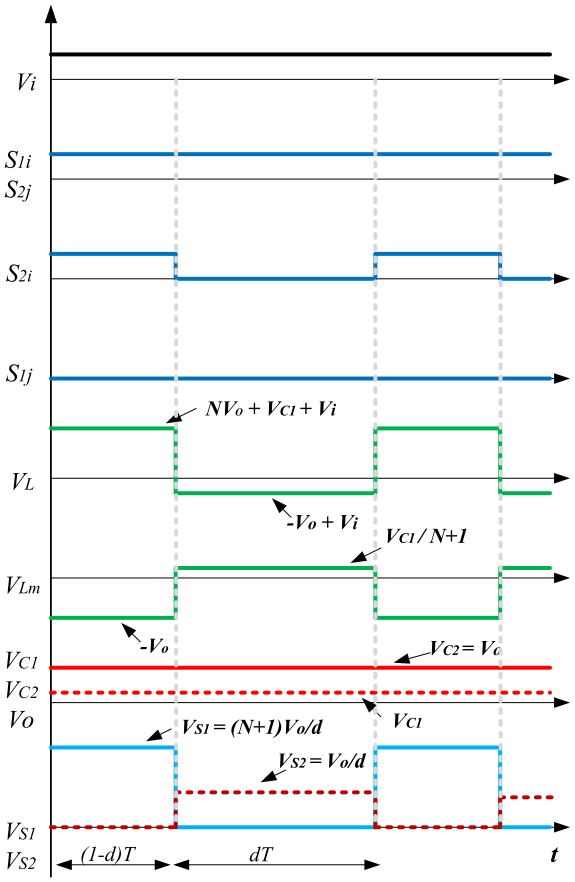

FIGURE 3. Key waveforms of the proposed converter's components in boost in-phase mode when Vi > 0.

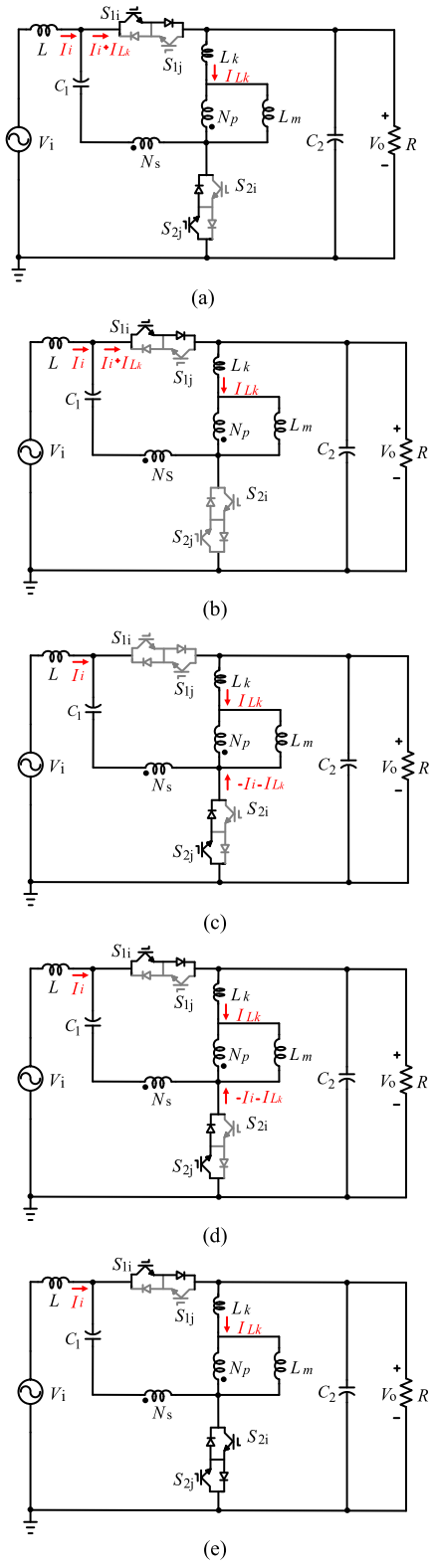

FIGURE 4. Operation intervals of the proposed converter in boost in-phase mode when Vi > 0, (a): state I, (b): commutation mode when $I_i+I_{Lk} > 0$, (c): commutation mode when $I_i+I_{Lk} < 0$ and $I_{Lk} = I_{Lm}$, (d): commutation mode when $I_i+I_{Lk} < 0$ and $I_{Lk}-I_{Lm} < 0$, (e): state II.

dead times intervals, and state II. Fig. 4 (a) depicts state I that switch S_{1i} is switched on to provide positive current from ac source to load, and S2j is switched on to eliminate commutation problem in a dead time interval, and S_{2i} is remained switched off. It must be noted that S1j can be either switched on or switched off. In similar kinds of literature, S1j- S2i (when Vi>0) and S1i- S2j (when Vi<0) are considered complementary switches, while in this paper, similar to [21], switch S1j is entirely turned off when Vi > 0 and switch S_{1i} is completely switched off when Vi < 0 due to two reasons: (1). Every switching on and off of the S1i and S1j consist of switching losses. Hence this strategy increases the lifetime of switches. (2). According to Fig. 2 in boost in-phase mode, voltage boost ability depends on the pulse width of S_{2i} and S_{2j} that is defined as (1-d) T where d and T are defined as duty cycle and switching period of the converter, respectively. As a result, employed coupled inductor helps the proposed converter to obtain high voltage boost ability by decreasing the conducting pulse width of switches. So, in this case, lower (1-d) and higher d are desired. At the same time, this opportunity cannot be attained by complementary modes since decreasing conducting pulse width of S_{2i} leads to an increment in conducting pulse width of S_{2i}. The same situation will happen for S1i and S2j. To provide state II, three various situations can occur before turning on the S_{2i} and during dead time. From Fig. 4 (b) if $I_i + I_{Lk} > 0$, S_{1i} will

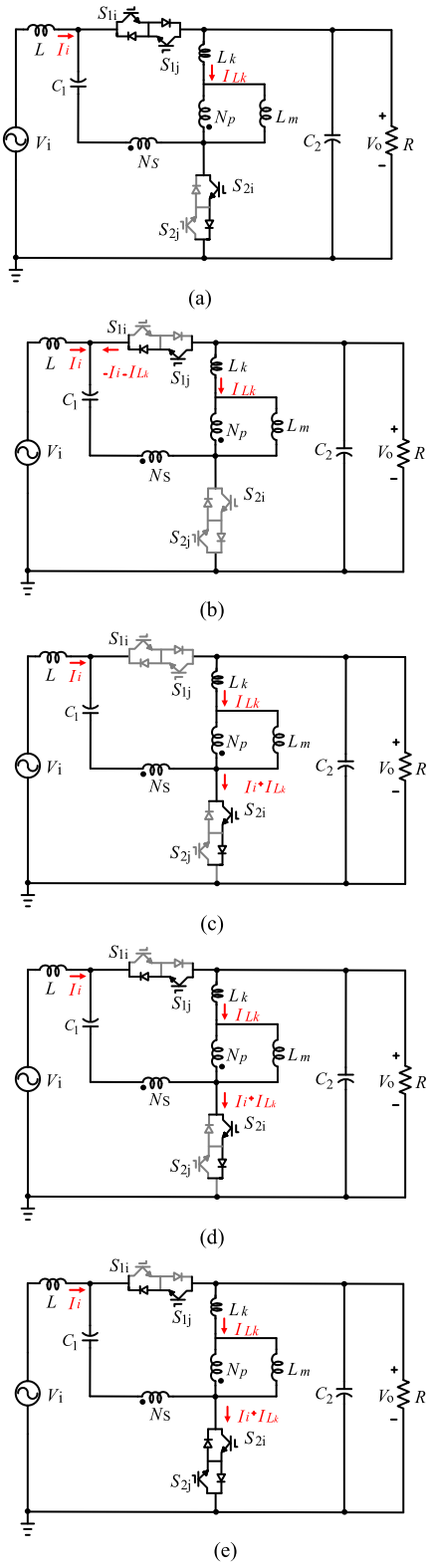

FIGURE 5. Operation intervals of the proposed converter in buck out-of-phase mode when Vi > 0, (a): state I, (b): commutation mode when I_i+I_{Lk} <0, (c): commutation mode when I_i+I_{Lk} > 0 and $I_{Lk} = I_{Lm}$, (d): commutation mode when I_i+I_{Lk} > 0 and $I_{Lk} - I_{Lm} > 0$, (e): state II.

conduct the current flow. If $I_i + I_{Lk} < 0$, two situations may happen; for $I_{Lk} = I_{Lm}$, S_{2j} conducts current flow as shown in Fig. 4 (c), but for $I_{Lk} < I_{Lm}$, current must flow through S_{1i} to energy stored in Lm decrease. As shown in Fig. 4 (d), this situation will continue until the stored energy of L_m and L_k becomes balanced where L_k and L_m represent leakage inductance and magnetizing inductance, respectively. Finally, state II will occur by switching on S_{2i} -S_{2j}, and S_{1i} is turned on to prevent commutation problems, which is demonstrated in Fig. 4 (e).

Fig. 5 illustrates operating intervals of the proposed converter in buck out-of-phase mode when the input voltage and the output voltage are positive and negative, respectively. Fig. 5 (a) depicts state I when switch S_{1j} is turned on to provide the current path and S_{2i} is turned on due to solving the commutation problems. In order to prepare state II, three different situations may occur before turning on the S_{2j} during dead time. From Fig. 5 (b), if $I_i + I_{Lk} < 0$, S_{1j} will flow the current. If $I_i + I_{Lk} > 0$, two conditions could occur according to the stored energy of L_k and L_m. If $I_{Lk} = I_{Lm}$, the current will be conducted through S_{2i}, which can be seen in Fig. 5 (c). But there is a situation when stored energy in Lk is lower than that in Lm. In this case, S1j must be switched on until the stored energy of Lm and Lk become equal. This condition can be observed in Fig. 5 (d). Lastly, state II will happen by turning on S_{2i}-S_{2j}, and S_{1j} is turned on to avoid commutation problem, which is illustrated in Fig. 5 (e).

C. CIRCUIT ANALYSIS

Following assumptions have been considered for the proposed circuit analysis: (1) It operates in continuous conduction mode (CCM). (2) The parasitic resistance of input inductor (r_L), coupled inductors (r_{Lm}) and switches (r_S) are considered. (3) The equivalent series resistance (ESR) of capacitors (r_C) are equal. (4) Frequency of the input and output voltages are lower than the switching frequency. (5) The coupling sufficient (K) is defined as $\frac{L_m}{L_m+L_K}$ and the turn ratio of coupled inductors (N) equals $\frac{v_{N_S}}{v_{N_P}} = \frac{I_{N_P}}{I_{N_S}}$. (6) The dead time effects of switches are ignored. Hence, the proposed converter operates in two states in each switching period, which are visualized in Fig. 6. Fig. 6 (a) illustrates the equivalent circuit of state I with the time interval of dT that S_1 is conducting and S_2 is turned off. In this state, the input and coupled-inductors are charged by C_2 and C_1. By applying KVL and KCL, equation (1), as shown at the bottom of the next page, can be derived.

Also, Fig. 6 (b) shows the equivalent circuit of state II with the time interval of (1-d)T. In this mode, S_2 is conducting while S_1 turns off. The stored energy in the input and coupled-inductors are released to the capacitors as in equation (2), as shown at the bottom of the next page.

According to (1) and (2), the average equations in one switching period are obtained as:

In the steady-state, the average value of the voltage/current across the inductor and coupled inductors/capacitors is zero,

so by considering zero for equations (3), as shown at the bottom of the next page, the peak of I_i, the peak of I_{Lm}, the peak of v_{C_1} and the peak value of v_O can be derived. In the ideal case resistance of inductors, capacitors, and power switches are negligible. Hence, to avoid complex equations, it is assumed that $r_{Lm} = r_L = r_C = r_S = 0$. Thus, it yields:

$$\begin{cases} I_i = \dfrac{d}{N(d-1)+2d-1}\dfrac{v_o}{R} \\ I_{L_m} = \dfrac{N(d-1)+d-1}{N(d-1)+2d-1}\dfrac{v_o}{R} \\ v_{C1} = \dfrac{NK(1-d)+1-d}{NK(d-1)+2d-1}v_i \\ v_o = \dfrac{d}{NK(d-1)+2d-1}v_i \end{cases} \tag{4}$$

Considering K=1, the voltage gain can be obtained as:

$$G_v = \frac{v_o}{v_i} = \frac{d}{N(d-1)+2d-1} \tag{5}$$

The L_m current gain can be defined as:

$$G_I = \frac{I_{L_m}}{I_i} = \frac{N(d-1)+d-1}{d} \tag{6}$$

Fig. 7 illustrates output voltage gain versus duty cycle with the various turn ratios of coupled inductors. Clearly, the proposed converter follows a different characteristic curve compared to previous single-phase AC-AC impedance source converters. It can be seen that in boost in-phase mode, the proposed converter provides higher voltage gain with lower conducting pulse width by increasing transformer's turn ratio. Furthermore, there are two operation regions based on the duty cycle range. For $d > \frac{N+1}{N+2}$, the proposed converter operates in boost in-phase mode, and when $d < \frac{N+1}{N+2}$, the proposed converter operates in buck/boost out-of-phase mode.

III. CIRCUIT DESIGN OF THE PROPOSED CONVERTER

Initially, the magnetic components of the proposed converter should be designed. Accordingly, the inductors parameters of the proposed converter are determined according to their maximum voltage and current ripple in dT interval. Regarding Fig. 5 (a), in the state I, the maximum voltage of L and

$$\begin{cases} L\dfrac{dIi(t)}{dt} = -(r_L+r_S)Ii(t) + \dfrac{r_S}{N+1}I_{L_m}(t) - v_o(t) + v_i(t) \\ Lm\dfrac{dI_{L_m}(t)}{dt} = \dfrac{Kr_S}{1+NK}Ii(t) + \left(\dfrac{-K(r_{S+}r_C)}{(1+NK)(N+1)} - r_{Lm}\right)I_{L_m}(t) + \dfrac{K}{1+NK}v_{C_1}(t) \\ C_2\dfrac{dv_o(t)}{dt} = Ii(t) - \dfrac{v_o(t)}{R} \\ C_1\dfrac{dv_{C_1}(t)}{dt} = \dfrac{-1}{N+1}I_{L_m}(t) \end{cases} \tag{1}$$

$$\begin{cases} L\dfrac{dIi(t)}{dt} = -\left(r_L + r_S + r_C + Nr_S + NKr_S + N^2Kr_S\right)Ii(t) + (r_S + NKr_S)I_{L_m}(t) + (NK)v_o(t) + v_{C_1}(t) + v_i(t) \\ Lm\dfrac{dI_{L_m}(t)}{dt} = (Kr_S + NKr_S)Ii(t) - (r_S + r_{Lm}K)I_{L_m}(t) - Kv_o(t) \\ C_2\dfrac{dv_o(t)}{dt} = -NIi(t) + I_{L_m}(t) - \dfrac{v_o(t)}{R} \\ C_1\dfrac{dv_{C_1}(t)}{dt} = -Ii(t) \end{cases} \tag{2}$$

$$\begin{cases} L\dfrac{dIi(t)}{dt} = d\left[-(r_L+r_S)Ii(t) + \dfrac{r_S}{N+1}I_{L_m}(t) - v_o(t) + v_i(t)\right] \\ +(1-d)\left[-\left(r_L + r_S + r_C + Nr_S + NKr_S + N^2Kr_S\right)Ii(t) + (r_S + NKr_S)I_{L_m}(t) + (NK)v_o(t) + v_{C_1}(t) + v_i(t)\right] \\ Lm\dfrac{dI_{L_m}(t)}{dt} = d\left[\frac{Kr_S}{1+NK}Ii(t) + \left(\frac{-K(r_S+r_C)}{(1+NK)(N+1)} - r_{Lm}\right)I_{L_m}(t) + \frac{K}{1+NK}v_{C_1}(t)\right] \\ +(1-d)\left[(Kr_S + NKr_S)Ii(t) + -(r_S + r_{Lm}K)I_{L_m}(t) - Kv_o(t)\right] \\ C_2\dfrac{dv_o(t)}{dt} = d\left[Ii(t) - \dfrac{v_o(t)}{R}\right] + (1-d)\left[-NIi(t) + I_{L_m}(t) - \frac{v_o(t)}{R}\right] \\ C_1\dfrac{dv_{C_1}(t)}{dt} = d\left[\dfrac{-1}{N+1}I_{L_m}(t)\right] + (1-d)\left[-Ii(t)\right] \end{cases} \tag{3}$$

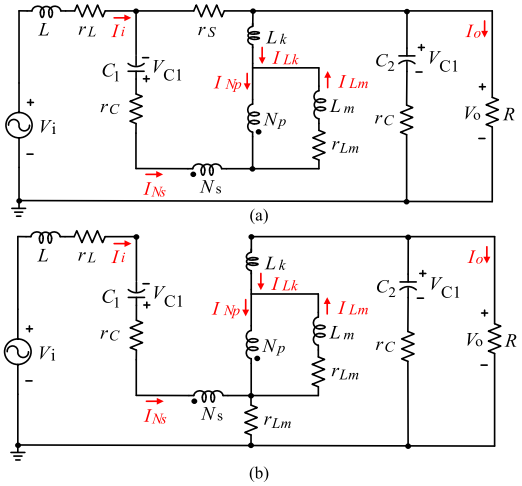

FIGURE 6. Equivalent circuits of the proposed converter in one switching period, (a). dT interval (state I), (b). (1-d) T interval (state II).

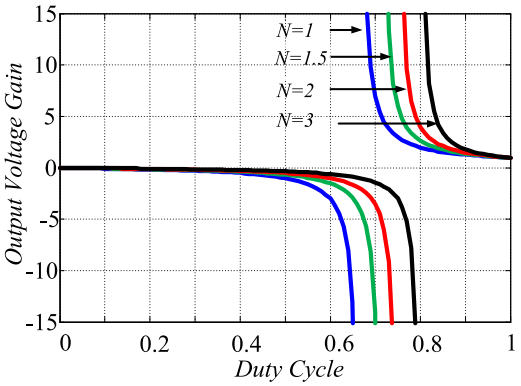

FIGURE 7. Relationship between voltage gain and duty cycle of the introduced converter with various N.

L_m are $V_i - V_{C2}$ and $\frac{V_{C1}}{N+1}$, respectively. So we can get:

$$\begin{cases} L = \dfrac{|V_{imax} - V_{C2max}|\,dT}{\Delta I_i} \\ Lm = \dfrac{\left|\frac{V_{C1max}}{N+1}\right| dT}{\Delta I_{L_m}} \end{cases} \tag{7}$$

If ΔI_i and ΔI_{L_m} are determined as $\Delta I_i \le x\% i_i$ and $\Delta I_{L_m} \le x\% i_{L_m}$, respectively, equation (8), as shown at the bottom of the page, can be obtained.

Where i_i and i_{L_m} represent RMS values of L and Lm current, respectively. In addition, the capacitors' parameters of the proposed converter are determined based on their maximum current and voltage ripple in dT interval. From Fig. 5 (a) in the state I, the maximum current of C_1 and C_2 are $(\frac{-1}{N+1} I_{L_m})$ and (Ii-Io), respectively. So (9) can be R

$$\begin{cases} C_1 = \dfrac{\left|\frac{1}{N+1} I_{L_m}\right| dT}{\Delta v_{C1}} \\ C_2 = \dfrac{|\mathrm{Ii} - \mathrm{Io}|\,dT}{\Delta v_{C2}} \end{cases} \tag{9}$$

If Δv_{C1} and Δv_{C2} are determined as $\Delta v_{C1} \le y\% V_{C1}$ and $\Delta v_{C2} \le y\% V_{C2}$, respectively, we can obtain, equation (10), as shown at the bottom of the page.

Where, V_{C1} and V_{C2} represent RMS values of C_1 and C_2 voltage, respectively. Noteworthy, the maximum value of voltage stress of bidirectional switches can be obtained from (4) and (5) as follows:

$$\begin{cases} V_{S1,max} = \dfrac{\sqrt{2}(N+1)}{N\,(d-1) + 2d - 1} v_i \\ V_{S2,max} = \dfrac{\sqrt{2}}{N\,(d-1) + 2d - 1} v_i \end{cases} \tag{11}$$

$$\begin{cases} L \ge \dfrac{|V_{imax} - V_{C2max}|\,dT}{x\% i_i} = \dfrac{\sqrt{2}\,Vi^2[N\,(d-1) + d - 1]dT}{x\% P_O[N\,(d-1) + 2d - 1]} \\ Lm \ge \dfrac{\left|\frac{V_{C1max}}{N+1}\right| dT}{x\% i_{L_m}} = \dfrac{\sqrt{2}\,Vi^2 d^2 T}{x\% P_O\,[N\,(1-d) + 1 - 2d]\,(N+1)} \end{cases} \tag{8}$$

$$\begin{cases} \mathrm{C1} \ge \dfrac{\left|\frac{1}{N+1} I_{L_m}\right| dT}{y\% V_{C1}} = \dfrac{\sqrt{2}\,P_O[N\,(d-1) + 2d - 1]T}{y\% Vi^2 (N+1)} \\ \mathrm{C2} \ge \dfrac{|\mathrm{Ii} - \mathrm{Io}|\,dT}{y\% V_{C2}} = \dfrac{\sqrt{2}\,P_O[N\,(1-d) + 1 - d][N\,(d-1) + 2d - 1]T}{y\% Vi^2 d} \end{cases} \tag{10}$$

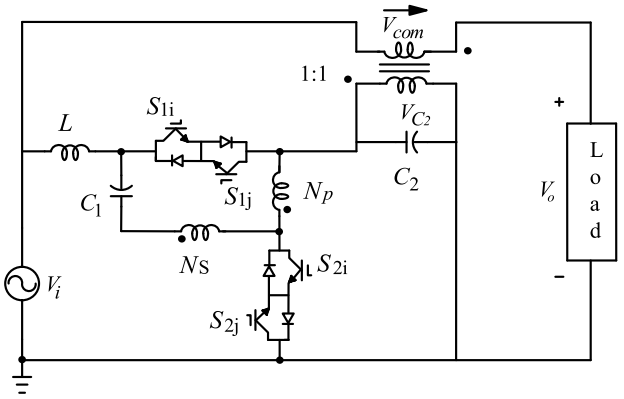

FIGURE 8. Proposed dynamic voltage restorer.

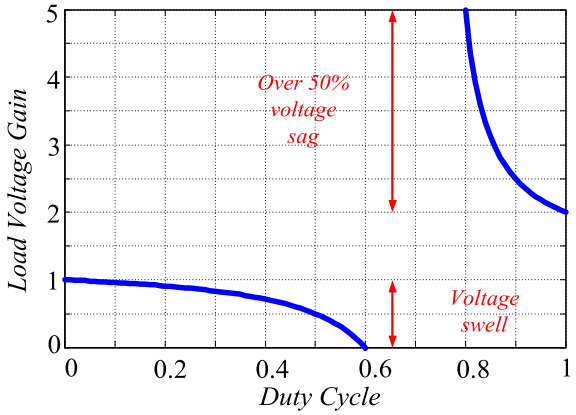

FIGURE 9. Load voltage gain versus duty cycle in voltage sag and swell condition.

The peak and RMS current stress of the bidirectional switches can be obtained as (12) and (13), respectively.

$$\begin{cases} I_{S1,max} = \dfrac{\sqrt{2}\,P_O}{dv_i} \\ I_{S2,max} = \dfrac{\sqrt{2}(N+1)P_O}{dv_i} \end{cases} \tag{12}$$

$$\begin{cases} I_{S1,rms} = \dfrac{\left(\sqrt{1-d}\right)P_O}{dv_i} \\ I_{S2,rms} = \dfrac{\sqrt{d}(N+1)P_O}{dv_i} \end{cases} \tag{13}$$

IV. APPLICATION OF THE PROPOSED CONVERTER AS DYNAMIC VOLTAGE RESTORER

Fig. 8 depicts a dynamic voltage restorer based on the proposed single-phase ac-ac converter. The line voltage *Vi* is linked to the input of the proposed converter in shunt. Also, the output of the converter is connected in series with the line voltage and load by an injection transformer. Since the injection transformer ratio is 1:1, the compensation voltage *Vcom* is equal to the converter output voltage V_{C2}. In the other words, the proposed DVR adjusts the load voltage *Vo* by injecting in-phase/out-of-phase boost/buck voltage in series with the line voltage in three operation states as follows:

A. BYPASS MODE

In this mode, the line voltage has the normal amount without voltage sag/swell faults. In this state, the proposed converter operates with the duty cycle of 1 and the output voltage of 0, when the bidirectional switch S_1 is entirely switched off, while the bidirectional switch S_2 conducts fully.

B. BOOST IN-PHASE MODE

This state starts when the voltage sag happens and the line voltage is lower than the determined amount. In this mode the proposed topology performs in boost in-phase state. From (5) and Fig. 8, by applying KVL we can get

$$v_o = v_i + v_{com} = v_i + \left(\frac{d}{N\,(d-1)+2d-1}\right)v_i \tag{14}$$

C. BUCK OUT-OF-PHASE MODE

This mode starts when the voltage swell occurs and the line voltage is higher than the determined value. In this state the proposed converter operates in buck out—of-phase mode. Again from (5) and Fig. 8, by applying KVL we can obtain

$$v_o = v_i - v_{com} = v_i - \left(\frac{d}{N\,(1-d)-2d+1}\right)v_i \tag{15}$$

By assuming N=2, the load voltage can be obtained as:

$$v_o = \left(\frac{5d-3}{4d-3}\right)v_i \tag{16}$$

From (16), the load voltage gain versus the switching duty ratio is shown in Fig. 9. According to Fig. 9, the presented DVR can compensate up to over 50% voltage sag for D = (0.75, 1). Additionally, the proposed DVR can compensate voltage swell when D = [0, 0.6).

V. COMPARATIVE STUDY

Since the voltage characteristic of the proposed converter is different from other topologies, its voltage gain is compared to that in modified quasi Z-source single-phase AC-AC converters, which offer the same voltage characteristic curve. Fig. 10 shows that the proposed converter provides higher voltage gain with a lower conducting pulse width (higher d and lower 1-d) than the modified single-phase quasi Z-source AC-AC converter in the boost mode. Compared to the asymmetrical Γ-source AC-AC converter, the proposed topology provides a wider range for the transformer turns ratio to increase voltage gain for the boost in-phase mode.

The proposed converter exploited a different structure of the windings compared with the converter in [27]. This

TABLE 1. Operational parameter design considerations of the proposed topology versus similar single-phase AC-AC converters.

Parameter	[6]	[8]	[10]	[20]	[21]	[23]	[27]	Proposed
$\frac{Vo}{Vi}$	$\frac{1-d}{1-2d}$	$\frac{1-d}{1-2d}$	$\frac{1-d}{1-2d}$	$\frac{1-d}{1-(N+2)d}$	$\frac{1-d}{1-(1+\frac{1}{N+1})d}$	$\frac{1}{1-(N+2)d}$	$\frac{1-d}{1-(1+\frac{N}{N+1})d}$	$\frac{d}{N(d-1)+2d-1}$
Ii	$\frac{Po}{Vi\sqrt{1-d}}$	$\frac{Po}{Vi}$	$\frac{Po}{Vi}$	$\frac{Po}{Vi}$	$\frac{dPo}{Vi(1-d)}$	$\frac{Po}{Vi}$	$\frac{Po}{Vi}$	$\frac{Po}{Vi}$
$\frac{V_{C1}}{Vi}$	$\frac{1-d}{1-2d}$	$\frac{1-d}{1-2d}$	$\frac{1-d}{1-2d}$	$\frac{(N+1)d}{1-(N+2)d}$	$\frac{1-d}{1-(1+\frac{1}{N+1})d}$	$\frac{(N+1)d}{1-(N+2)d}$	$\frac{Nd}{d(2N-1)-N-1}$	$\frac{N(1-d)+1-d}{N(d-1)+2d-1}$
$\frac{V_{C2}}{Vi}$	$\frac{1-d}{1-2d}$	$\frac{1-d}{1-2d}$	$\frac{1-d}{1-2d}$	$\frac{1-d}{1-(N+2)d}$	-	$\frac{1-d}{1-(N+2)d}$	-	$\frac{d}{N(d-1)+2d-1}$
I_{L1}	$\frac{Po}{Vi}$	$\frac{Po}{Vi}$	$\frac{Po}{Vi}$	$\frac{Po}{Vi}$	-	$\frac{Po}{Vi}$	$\frac{Po}{Vi}$	$\frac{Po}{Vi}$
I_{L2}	$\frac{Po}{Vi}$	$\frac{Po}{Vi}$	$\frac{(1-d)Po}{dVi}$	-	-	-	-	-
I_{Lm}	-	-	-	$\frac{(N+1)Po}{Vi}$	$\frac{Po}{Vi}$	$\frac{(N+1)Po}{Vi}$	$\frac{(N+1)dPo}{Vi}$	$\frac{(N+1)(d-1)Po}{dVi}$
N_C	3	3	2	3	2	3	2	2
N_I	3	3	2	2	1	1	1	1
N_{CI}	-	-	-	1	1	1	1	1
N_{SW}	2	4	4	4	4	6	4	4
N_{total}	8	10	8	10	8	11	8	8

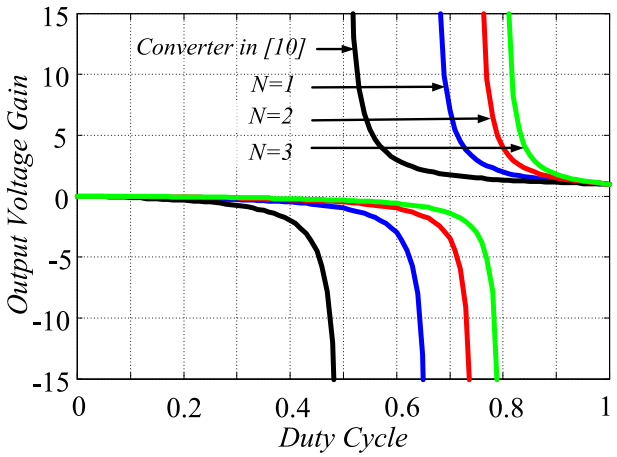

FIGURE 10. Relationship between voltage gain and duty cycle of the modified single-phase qZS AC-AC converter and introduced converter with various N.

diversity brings some advantages to the proposed converter. In [27], the voltage gain can be increased by lowering the transformer's turn ratio. However, it can be a plus, especially in terms of the size; the converter suffers from the narrow range of the turn ratio. In other words, the practical range of the turn ratio for the high voltage requirement is 1.5 to 1.3, which can be a limitation for the design issue. Because by lowering the turn number in practice, distortion in output waveforms will occur. To solve this problem, the proposed converter attains high voltage boost/buck ability by increasing the turns from 1 to more than 6 in the design process according to the required voltage compensating in voltage sag/swell problems. Unlike conventional z-source and Γ-source AC-AC converters, the presented structure offers a continuous sinusoidal input current with lower THD.

In addition, the proposed converter exploits a reduced number of passive components compared to topologies in [20]–[24]. Likewise, the proposed converter utilizes a lower number of active components in comparison to the modified trans-Z-source AC-AC converter [23]. In this regard, a detailed comparison between the proposed topology and similar single-phase direct AC-AC converters is provided in Table 1 to 4. This investigation encompasses the operational, structural, and performance considerations of the proposed single-phase direct AC-AC converter as well as other similar ones. Accordingly, the number of active and passive components including inductors(N_I), coupled inductors (N_{CI}), power switches (N_{SW}), the total number of circuit components (N_{total}) are considered. Furthermore, voltage gain, voltage/current equations of capacitors/inductors, input current, voltage and current stress of the semiconductors are taken into account. Finally, a brief comparison of the pros and cons of each circuit design is presented in Table 4.

VI. EVALUATION AND RESULTS

To further investigate the correctness of the proposed topology, the circuit configuration was simulated in MATLAB environment. Then, the simulation results were compared to experimental ones obtained from a laboratory prototype presented in Fig.11. The setup specification is brought in table 5. Particularly, the safe-commutation strategy is performed by utilizing the digital signal processor (DSP-TMS320F28335). Two bidirectional switches have been used to implement the safe commutation strategy. Notably, each bidirectional switch consists of two back to back Power MOSFETs. High frequency coupled inductors have been designed with the

TABLE 2. Structural parameter designs of the proposed topology and similar single-phase AC-AC converters.

Ref.	$C_{1,min}$	$C_{2,min}$	$L_{1,min}$	$L_{2,min}$	$L_{m,min}$
[6]	$\frac{\sqrt{2}Po(1-d)(2d-1)T}{y\%Vi^2d}$	$\frac{\sqrt{2}Po(1-d)(2d-1)T}{y\%Vi^2d}$	$\frac{\sqrt{2}Vi^2(1-d)d^2T}{x\%Po(1-2d)^2}$	$\frac{\sqrt{2}Vi^2(1-d)d^2T}{x\%Po(1-2d)^2}$	-
[8]	$\frac{\sqrt{2}Po(1-d)(2d-1)T}{y\%Vi^2d}$	$\frac{\sqrt{2}Po(2d-1)T}{y\%Vi^2}$	$\frac{\sqrt{2}Vi^2(1-d)dT}{x\%Po(1-2d)}$	$\frac{\sqrt{2}Vi^2(1-d)dT}{x\%Po(1-2d)}$	-
[10]	$\frac{\sqrt{2}Po(1-d)(2d-1)T}{y\%Vi^2d}$	$\frac{\sqrt{2}Po(2d-1)T}{y\%Vi^2}$	$\frac{\sqrt{2}Vi^2(1-d)dT}{x\%Po(1-2d)}$	$\frac{\sqrt{2}Vi^2d^2T}{x\%Po(1-2d)}$	-
[20]	$\frac{(1-d)TI_{Lf}}{y\%Vi(N+1)}$	$\frac{dT(N+1)I_{Lf}}{y\%Vi}$	$\frac{\sqrt{2}Vi^2(1-(3+2N)d)dT}{x\%Po(1-(N+2)d)}$	-	$\frac{\sqrt{2}Vi^2(1-d)dT}{x\%Po(N+1)(1-(N+2)d)}$
[21]	$\frac{\sqrt{2}PoNdT}{y\%ViVo(N-1)}$	-	-	-	$\frac{\sqrt{2}ViVoNdT}{x\%Po(N-1)(N-1)I_{Lm}}$
[23]	$\frac{\sqrt{2}Po(1-(N+2)d)dT}{y\%Vi^2(N+1)}$	$\frac{\sqrt{2}Po(N+1)(1-(N+2)d)d^2T}{y\%Vi^2}$	$\frac{\sqrt{2}Vi^2(1-d)T}{x\%Po(1-(N+2)d)}$	-	$\frac{\sqrt{2}Vi^2(1-d)T}{x\%Po(N+1)(1-(N+2)d)}$
[27]	$\frac{\sqrt{2}Po(N-1-d(2N-1))T}{y\%Vi^2N}$	$\frac{\sqrt{2}Po(N-1-d(2N-1))NdT}{y\%Vi^2(N-1)^2(1-d)}$	$\frac{\sqrt{2}Vi^2(1-d)(N-1)dT}{x\%Po(N-1-d(2N-1))}$	-	$\frac{\sqrt{2}Vi^2N^2(1-d)^2dT}{x\%Po(N-1-d(2N-1))(1+(N-1)d))}$
P	$\frac{\sqrt{2}Po((N+1)(d-1)+d)T}{y\%Vi^2(N+1)}$	$\frac{\sqrt{2}Po(N+1)(1-d)((N+1)(d-1)+d)T}{y\%Vi^2d}$	$\frac{\sqrt{2}Vi^2(N(d-1)+d-1)dT}{x\%Po(N(d-1)+2d-1)}$	-	$\frac{\sqrt{2}Vi^2d^2T}{x\%Po(N(1-d)+1-2d)(N+1))}$

TABLE 3. Performance criteria of the proposed topology and similar single-phase AC-AC converters.

Ref.	$I_{S1,max}$	$I_{S2,max}$	$I_{S3,max}$	$V_{S1,max}$	$V_{S2,max}$	$V_{S3,max}$
[6,8,10]	$\frac{\sqrt{2}Po}{Vi(1-d)}$	$\frac{\sqrt{2}Po}{Vi(1-d)}$	-	$\frac{\sqrt{2}Vi}{(1-2d)}$	$\frac{\sqrt{2}Vi}{(1-2d)}$	-
[20]	$\frac{\sqrt{2}Po}{Vi(1-d)}$	$\frac{\sqrt{2}Po(N+1)}{Vi(1-d)}$	-	$\frac{\sqrt{2}Vi(N+1)}{1-(N+2)d}$	$\frac{\sqrt{2}Vi}{1-(N+2)d}$	-
[21]	$\frac{\sqrt{2}Po}{Vi(1-d)}$	$\frac{\sqrt{2}Po(2N(1-d)-1)}{Vi(1-d)(N-1)}$	-	$\frac{\sqrt{2}Vi}{N(d-1)+1}$	$\frac{\sqrt{2}Vi}{N(d-1)+1}$	-
[23]	$\frac{\sqrt{2}dPo}{Vi}$	$\frac{\sqrt{2}dPo(-N-d)}{Vi(1-d)}$	$\frac{\sqrt{2}dPo}{Vi(1-d)}$	$\frac{\sqrt{2}Vi}{1-(N+2)d}$	$\frac{\sqrt{2}Vi}{1-(N+2)d}$	$\frac{\sqrt{2}Vi(N+1)d}{1-(N+2)d}$
[27]	$\frac{\sqrt{2}Po}{Vi(1-d)}$	$\frac{\sqrt{2}NPo}{Vi((N-1)(1-d)}$	-	$\frac{\sqrt{2}NVi}{(N-1)-d(2N-1)}$	$\frac{\sqrt{2}(N-1)Vi}{(N-1)-d(2N-1)}$	-
P	$\frac{\sqrt{2}dPo}{dVi}$	$\frac{\sqrt{2}(N+1)Po}{dVi}$	-	$\frac{\sqrt{2}Vi}{(N(d-1)+2d-1)}$	$\frac{\sqrt{2}(N+1)Vi}{(N(d-1)+2d-1)}$	-

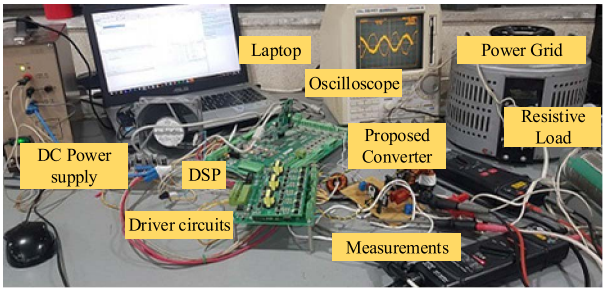

FIGURE 11. Picture of the implemented setup.

turns number of ten and twenty for the primary and secondary sides, respectively. Also, each circuit component is chosen for the circuit design and its mathematical analyses described in previous sections. In addition, both of the simulations and experimentations were conducted in the same conditions. Accordingly, the experimental results of the proposed converter supplying a resistive load (80Ω) in boost in-phase operating mode are presented in Fig.12.

In this state, the duty cycle is assumed 0.9. The input voltage waveform is depicted in Fig.12.a. According to Table 5 and the obtained mathematical equations, the peak value of the output voltage, input current, and output current are approximately 150 V, 2.8 A, and 1.8 A, respectively verified by experimental waveforms in Fig. 12.a-c. This case (boost factor of 1.5) can be a suitable range for the 50% voltage sag compensation, applicable in dynamic voltage restorer. To achieve this boost factor by the modified single-phase AC-AC quasi Z-source converter, the duty cycle must be considered as d = 0.75. In other words, the pulse width of the S_{2i} and S_{2j} is 25% of the switching period. While with the same condition, the switches pulse width is 10% of the switching period in the proposed converter. Hence, the introduced topology can attain the equal voltage boost factor by the slighter conducting losses that increase the efficiency. Furthermore, the overview of the boost mode operation of the proposed converter can be seen in Fig.12.c describing the output voltage maintains the phase angle with the input voltage well. Additionally, the current and voltage waveforms

TABLE 4. Overall Investigation of the proposed topology compared to similar single-phase AC-AC converters.

Ref.	*Advantage*	*Disadvantage*
[6]	- buck-boost ability - low number of switches - direct AC-AC conversion	- discontinuous input current with high THD - switching spikes problem - unshared ground and phase maintenance problem - high stress on the capacitor
[8]	- buck-boost ability with safe commutation strategy - continuous input current - low input current THD - shared ground	- high switching losses - requiring output filter
[10]	- buck-boost ability with safe commutation strategy - continuous input current with low THD and filter-less structure - shared ground - reduced number of passive components	- high switching losses - requiring output filter
[20]	- buck-boost ability with safe commutation strategy - continuous input current with low THD - regulating the output voltage by controlling the turns ratio of the transformer along with the duty cycle - shared ground	- requiring output filter - increasing transformer's turns ratio for high voltage compensating
[21]	- buck-boost ability with safe commutation strategy - increasing the output voltage by lowering the transformer's turns ratio along with duty cycle controlling - shared ground	- discontinuous input current - high input current THD - high voltage distortion when transformer's turns ratio limits to 1
[23]	- buck-boost ability with safe commutation strategy - continuous input current with low THD - regulating the output voltage by controlling the transformer's turns ratio along with duty cycle - shared ground - inductor-less output filter, high efficiency	- higher number of switches
[27]	- buck-boost ability with safe commutation strategy - continuous input current with low THD - increasing the output voltage by lowering the turns ratio of the transformer along with duty cycle controlling - shared ground - filter-less structure, high efficiency with low conducting loss	- high voltage distortion when transformer's turns ratio limits to 1
P	- buck-boost ability with safe commutation strategy - continuous input current with low THD - regulating the output voltage by controlling the transformer's turns ratio along with duty cycle - shared ground - filter-less structure, high efficiency with low conducting loss	- increasing transformer's turns ratio for high voltage compensating

TABLE 5. Topology properties.

Specification	Details
Vi	100 V
L_m	800 µH
f_s	20 k Hz
C_1	15 µF
C_2	47 µF
Turn ratio ($\frac{N_S}{N_P}$)	$\frac{2}{1}$
Duty cycle (d)	0.9 for boost mode 0.2 for buck mode
Input voltage frequency	50 Hz
Coupling coefficient	1
Switches	IRFP460 Power MOSFET

of the switches in such operating conditions are added to Fig.12.d and e. From these figures, it can be seen that the voltage and current spikes across the switches have been eliminated thanks to the safe commutation strategy.

On the other hand, the operation of the proposed converter supplying a purely resistive load (10Ω) in buck out-of-phase operating mode is investigated and the results are presented in Fig.13. In this state, the duty cycle is considered as d=0.2. The noticeable point for these waveforms is their phase differences. Unlike input and output voltage phase alignment in boost mode, there is 180 degrees phase deviation in buck operating mode. From theoretical equations, the peak value of the output voltage, input current, and output current are about 9 V, 0.1 A, and 1 A, respectively, which are verified by experimental results in Fig. 13.a to c. This case (boost factor of 0.09) can be appropriate for the range of the 10% voltage swell compensation. In addition, low peak value of the output voltage shows the high voltage buck ability of the proposed converter. From the experimental results, it is obvious that the input current is continuous and sinusoidal, completely in both boost and buck operating modes.

The output voltage and input current THD of the proposed converter in boost and buck operation modes are presented in Table 6. It is clear that in buck operation mode, the output voltage and input current THDs are about 2.67% and 45.85%. Also, in boost operation mode, the output voltage and input current THDs are about 2.37% and 3.20%. As a result, the proposed converter offers high-quality voltage and current

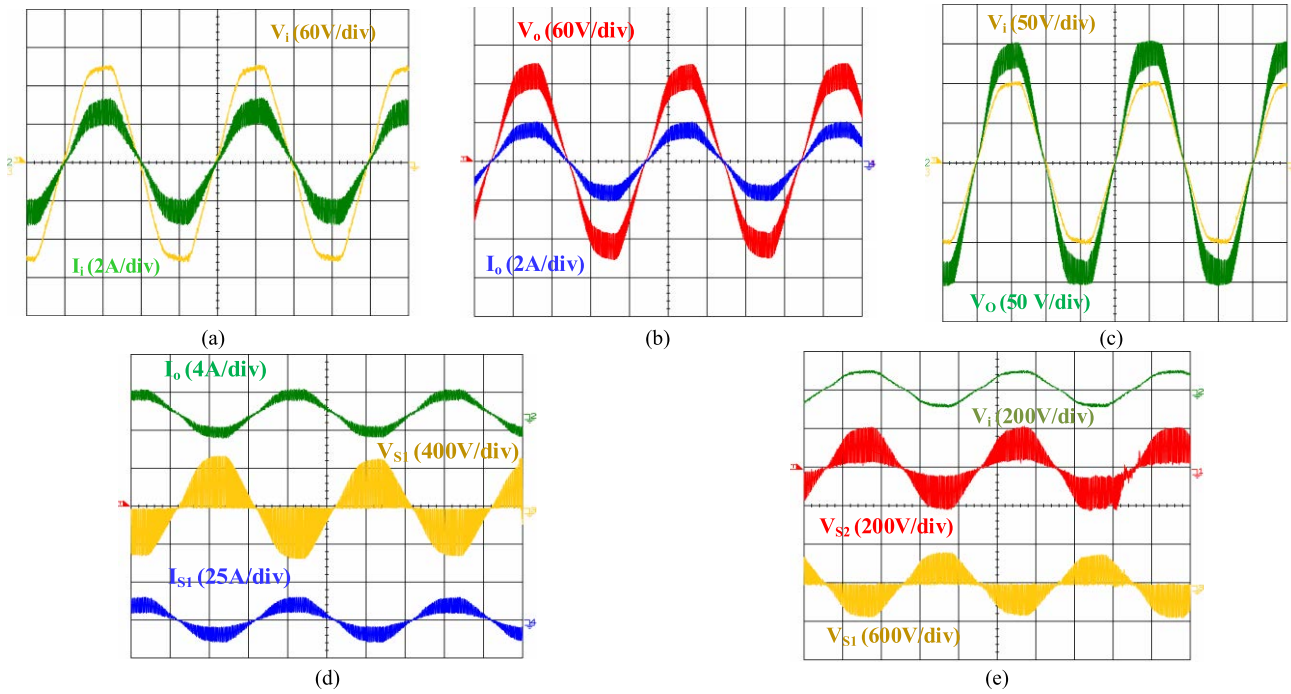

FIGURE 12. Boost operating mode behavior of the proposed converter includes: (a) input waveforms, (b) output waveforms, (c) input vs output, (d) S_1, and (e) S_2.

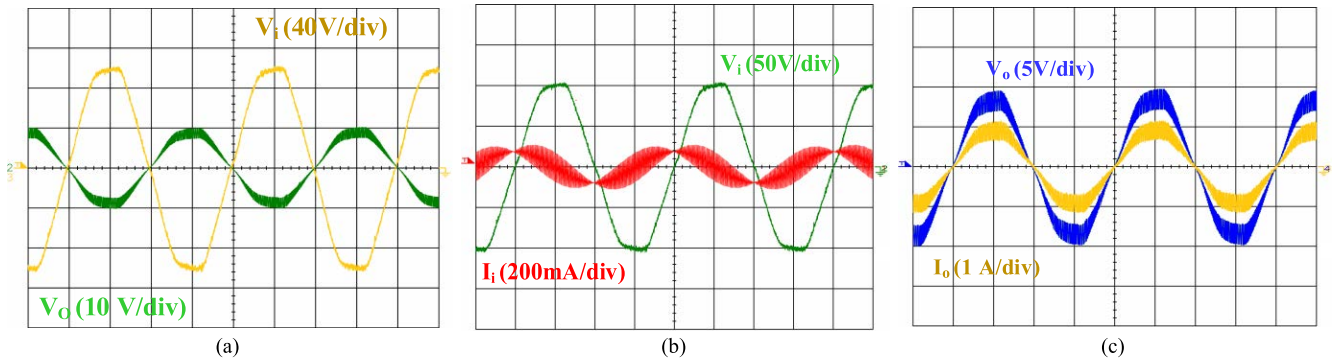

FIGURE 13. Buck mode results of the proposed converter include: (a) input and output voltage waveform, (b) input waveforms, and (c) output waveforms.

TABLE 6. Harmonic contents of the proposed converter.

THD	Output voltage	Input current
d = 0.2	2.67%	45.85%
d = 0.9	2.37%	3.20%

TABLE 7. Input current THD of the proposed converter versus similar ones.

THD	[6]	[8]	[10]	[21]	[23]	Proposed converter
Boost mode	39.75%	3.384%	3.459%	51.92%	6.011%	3.20%
Buck mode	180.5%	35.07%	36.35%	126.4%	9.362%	45.85%

waveforms without utilizing input and output filters. In addition, Table 7 compares the input current THD of the proposed topology versus the similar converters. From this table, it can be found that in the boost mode, the presented topology has a lower input current THD than the other converters, while providing it in the reasonable value in the buck mode.

Fig. 14 shows the simulation waveforms of the proposed converter with non-linear load for input frequency of 60 Hz, RMS input voltage of 73 V, duty cycle of 0.9, and transformer turn ratio of 2. A single-phase diode bridge rectifier with output capacitor of 470 μF has been determined for a non-linear load [28], [29]. Fig. 14(a) and Fig. 14(b) show the input and output voltage waveforms, respectively. It can be seen that the proposed converter provides a sinusoidal output

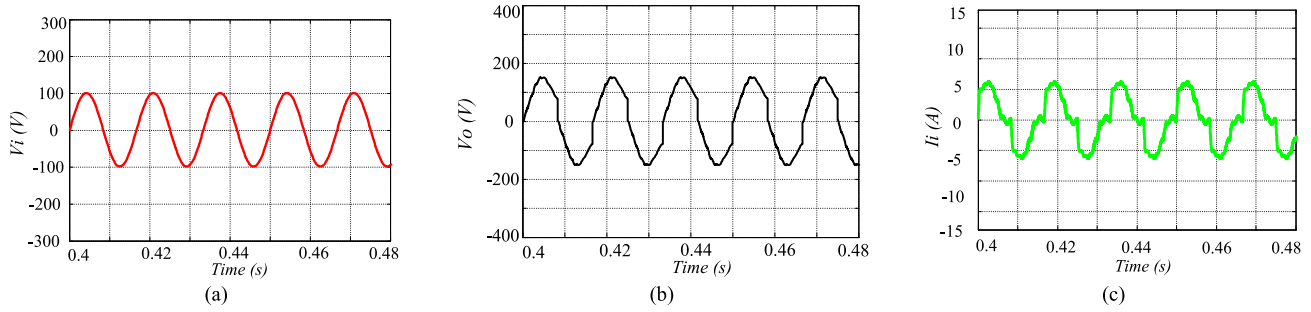

FIGURE 14. Simulation waveforms of the proposed converter with non-linear load: (a) input and (b) output voltages, (c) input current.

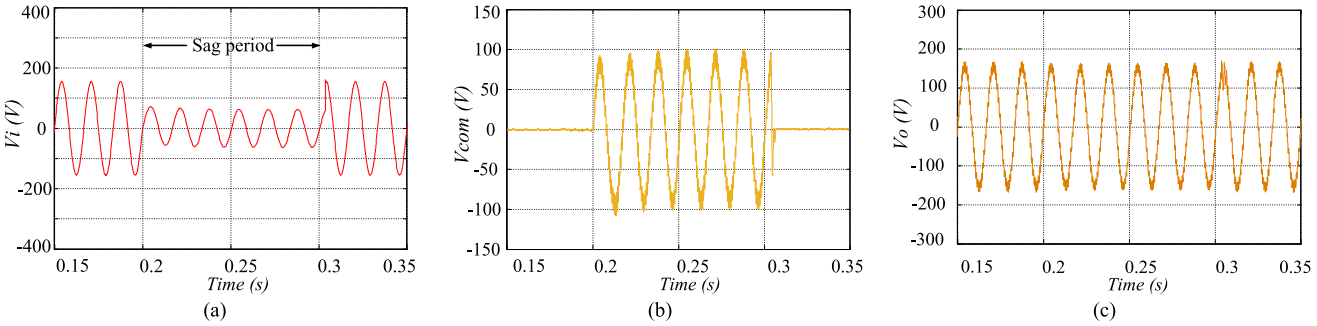

FIGURE 15. Simulation waveforms of the proposed DVR at 60% voltage sag compensation: (a) line voltage, (b) compensation voltage, (c) load voltage.

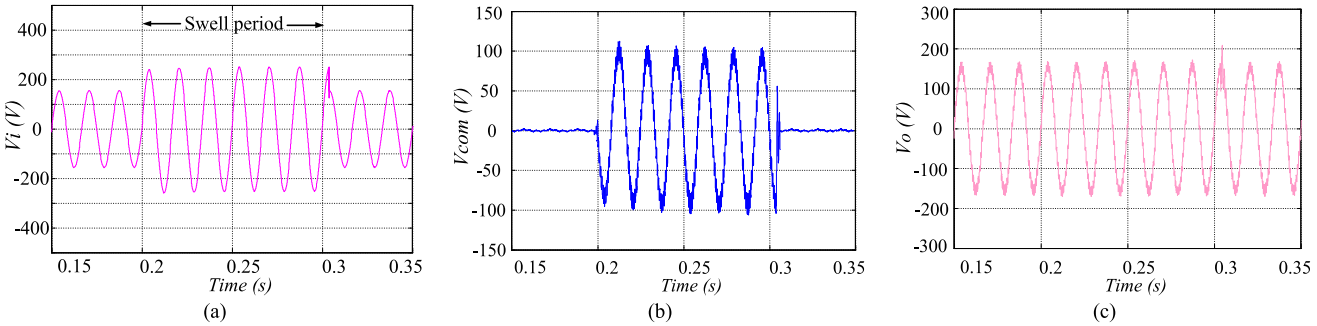

FIGURE 16. Simulation waveforms of the proposed DVR at 60% voltage swell compensation: (a) line voltage, (b) compensation voltage, (c) load voltage.

voltage under non-linear load. Furthermore, it is shown that the output voltage maintains the phase angle with the input voltage well. Fig. 14(c) shows the input current waveform. The THD of the input current and output voltage is about 27% and 12%, respectively.

Fig. 15 and Fig. 16 show the simulation results of the voltage sag and voltage swell compensation by utilizing the DVR based on the proposed converter. A proportional integral (PI) controller has been used to control the load voltage. According to Fig. 15, when 60% voltage sag occurs in line voltage at interval time of 0.2-0.3 sec, the load voltage is well compensated to a demanded value of 110 V_{rms}. From Fig. 16, when 60% voltage sag happens in the line voltage at interval time of 0.2-0.3 sec, the load voltage is adjusted by the proposed DVR with a demanded value of 110 V_{rms}.

VII. POWER LOSS ANALYSIS

The main power losses of the proposed converter come from the magnetic losses, semiconductors losses, and ESR of the capacitors. The magnetic losses include copper and core losses. Based on [30], the copper losses of the inductor and coupled inductors can be calculated from (17) and (18), respectively.

$$P_{cu-L} = \frac{\rho\,(MLT)\,I_i^2}{W_A K_u} \tag{17}$$

$$P_{cu-CI} = \frac{\rho\,(MLT)\,n_1^2 (I_{Np} + NI_{Ns})^2}{W_A K_u} \tag{18}$$

where $\rho, MLT, n_1, I_i, I_{Np-S}, W_A, K_u$ present the wire effective resistivity, mean length per turns, primary winding turns, RMS current of inductor, RMS current of winding, core window area, and winding fill factor, respectively. Also, the

core loss is obtained from (19). Notably, K_{fe}, B_{max}, β, A_C, l_m represent core loss coefficient, peak ac flux density, core loss exponent, core cross-sectional area, and mean magnetic path length, respectively.

$$P_{fe} = K_{fe} B_{max}^{\beta} A_c l_m \tag{19}$$

Hence, the total magnetic loss can be obtained from (20).

$$P_{M-tot} = P_{cu-L} + P_{cu-CI} + P_{fe} \tag{20}$$

Moreover, semiconductor loss itself comprises switching and conduction loss, whereas the former is originated from the time delay in turning ON or OFF of the device and the latter is caused due to the parasitic resistance of the device [31]. Also, switching loss is caused by an inherent behavior of all switching devices that can be calculated by:

$$P_{s,on} = \frac{1}{6} f_s V_{off-state} I_{on-state} t_{on} \tag{21}$$

$$P_{s,off} = \frac{1}{6} f_s V_{off-state} I_{on-state} t_{off} \tag{22}$$

where, $V_{off-state}$ and $I_{on-state}$ are off-state voltage and switch current when the switch becomes fully turned on, respectively [32]. Also, f_S is the switching frequency and t_{on}/ t_{off} is the length of the time delay that takes for the switch to turn completely on/ off. Thus, the overall switching loss of the circuit (P_{SW}) is calculated by (23).

$$P_{sw} = \sum_{j=1}^{N_{switch}} \left(P_{sj,on} + P_{sj,off} \right) \tag{23}$$

In case of conduction loss, each switching device is modeled by a parasitic resistance and parasitic voltage source (acting against the current flow), then:

$$\begin{cases} P_{con-SW} = V_{on}^{sw}.i_{av-SW} + R_{on}^{sw}.i_{rms-SW}^2 \\ P_{con-D} = V_{on}^{D}.i_{av-D} + R_{on}^{D}.i_{rms-D}^2 \end{cases} \tag{24}$$

where,V_{on}^{sw}, V_{on}^{D} are the on state voltage of switch and the on state voltage of diode, respectively. Also, R_{on}^{sw} is the on-state resistance of switches and R_{on}^{D} is the on-state resistance of diode [32], [33]. i_{rms} and i_{avg} are the RMS and average current of semiconductors. Then, the total conduction loss of the circuit is obtained by:

$$P_{con}^{total} = \sum (P_{con-SW} + P_{con-D}) \tag{25}$$

Fig. 17 compares the efficiency of the proposed topology in various output power with similar AC-AC converters. For fair comparison, the same conditions are assumed for the converters. The parasitic resistance of the input inductor, coupled inductors, and equivalent series resistance of capacitors equal to 1 Ω. Also, the ON resistances of switches are equal to 0.27 Ω, and the leakage inductance of coupled inductors is 2 μH. It can be seen that from Fig. 17, the proposed converter offers higher efficiency in comparison with similar topologies. The main reasons for this reduction are a safe commutation strategy with smaller conducting duration, and

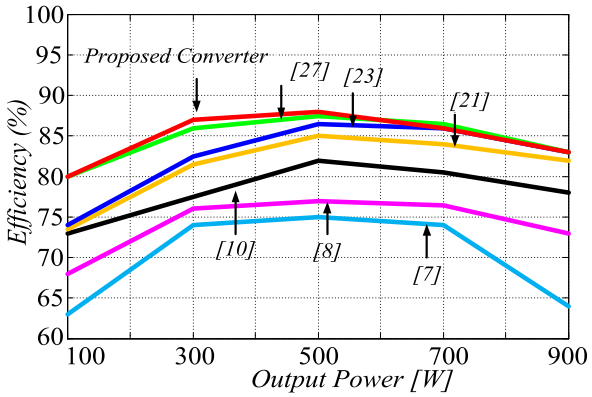

FIGURE 17. Efficiency comparison.

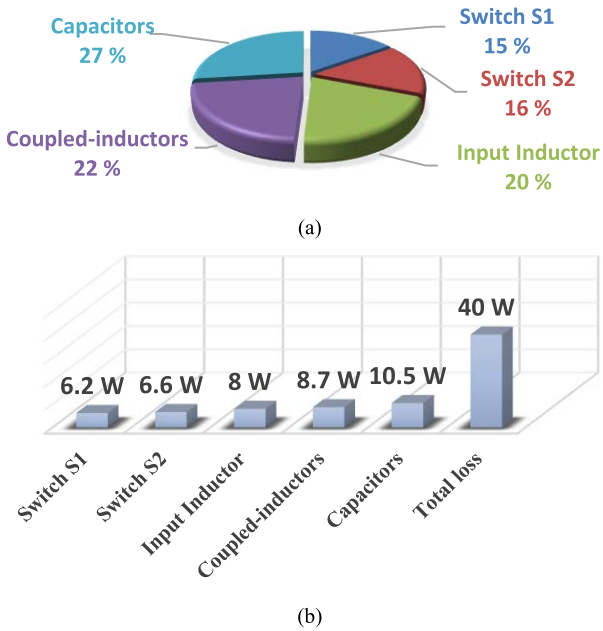

FIGURE 18. Loss charts in the proposed topology at an output power of 300 W: (a) distribution and (b) circuit components losses.

input and output filter elimination which can reduce the power losses.

Fig. 18 (a) and (b) show the power loss distribution of the proposed converter at an output power of 300W. It can be found that the bidirectional switches have lower power losses than other components, which proves the low conducting and switching losses of the converter. While, in the previous AC-AC converters, the significant power loss comes from semiconductors.

VIII. CONCLUSION

A novel single-phase direct AC-AC converter has been presented in this paper. The proposed converter inherits all the advantages of the conventional single-phase impedance source AC-AC converters as follows: (1). It can operate in boost in-phase mode or buck-boost out of phase mode.

(2). Output voltage shares the same ground with the input voltage; hence it can maintain or reverse-phase angle well with the input voltage. (3). It can be utilized as a dynamic voltage restorer to compensate voltage sags or voltage swells without using any dc storage such as battery or capacitor banks. A unique impedance network has been applied to the proposed converter to connect the ac source to the load directly. Thanks to the proposed impedance structure, it does not require passive components as input and output filters which leads to reducing in the size and cost of the converter. Magnetically coupled inductors have been employed in the proposed converter to provide high voltage boost ability with a small conducting duration of the switches by adjusting its turn ratio. As a result, the proposed converter offers high efficiency, low conducting losses and a high lifetime of semiconductors devices. A safe commutation strategy has been applied for the proposed converter to remove voltage or current spikes across the switches without needing any snubber circuits. Furthermore, the input current of the proposed converter is continuous, so it does not suffer from non-sinusoidal waveforms, high THD, high peak, and inrush current. Finally, the performance of the proposed converter has been testified within experimental results.

REFERENCES

[1] P. Alemi, Y.-C. Jeung, and D.-C. Lee, "DC-link capacitance minimization in T-type three-level AC/DC/AC PWM converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1382–1391, Mar. 2015.

[2] M. Vijayagopal, P. Zanchetta, L. Empringham, L. de Lillo, L. Tarisciotti, and P. Wheeler, "Control of a direct matrix converter with modulated model-predictive control," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2342–2349, Jun. 2017.

[3] S. S. Sebtahmadi, H. B. Azad, S. H. A. Kaboli, M. D. Islam, and S. Mekhilef, "A PSO-DQ current control scheme for performance enhancement of Z-source matrix converter to drive IM fed by abnormal voltage," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1666–1681, Feb. 2018.

[4] U. A. Khan, A. A. Khan, H. Cha, H.-G. Kim, J. Kim, and J.-W. Baek, "Dual-buck AC–AC converter with inverting and non-inverting operations," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9432–9443, Nov. 2018.

[5] A. A. Khan, H. Cha, and H. F. Ahmed, "An improved single-phase direct PWM inverting buck–boost AC–AC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5384–5393, Sep. 2016.

[6] X. P. Fang, Z. M. Qian, and F. Z. Peng, "Single-phase Z-source PWM AC–AC converters," *IEEE Power Electron Lett.*, vol. 3, no. 4, pp. 121–124, Dec. 2005.

[7] Y. Tang, S. Xie, and C. Zhang, "Z-source AC–AC converters solving commutation problem," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2146–2154, Nov. 2007.

[8] M.-K. Nguyen, Y.-G. Jung, and Y.-C. Lim, "Single-phase AC–AC converter based on quasi-Z-source topology," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2200–2210, Aug. 2010.

[9] L. He, S. Duan, and F. Peng, "Safe-commutation strategy for the novel family of quasi-Z-source AC–AC converter," *IEEE Trans. Ind. Informat.*, vol. 9, no. 3, pp. 1538–1547, Aug. 2013.

[10] M.-K. Nguyen, Y.-C. Lim, and Y.-J. Kim, "A modified single-phase quasi-Z-source AC–AC converter," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 201–210, Jan. 2012.

[11] A. Mostaan, J. Yuan, Y. P. Siwakoti, S. Esmaeili, and F. Blaabjerg, "A trans-inverse coupled-inductor semi-SEPIC DC/DC converter with full control range," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10398–10402, Nov. 2019.

[12] X. Kong, C.-K. Wong, and C.-S. Lam, "Effects of parasitic resistances on magnetically coupled impedance-source networks," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9171–9183, Sep. 2020.

[13] J. Ma, H. Liu, J. Chen, Y. Li, and P. C. Loh, "A family of coupled dual-winding impedance-source inverters with continuous input currents and no DC-link voltage spikes," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Oct. 28, 2020, doi: 10.1109/JESTPE.2020.3034394.

[14] W. Mo, P. C. Loh, and F. Blaabjerg, "Asymmetrical Γ-source inverters," *IEEE Trans. Ind. Electron*, vol. 61, no. 2, pp. 637–647, Feb. 2014.

[15] S. Esmaeili, A. Mahmoudi, S. Kahourzadeh, and A. Mostaan, "Dual winding magnetically coupled impedance-source inverters with DC-rail voltage clamping circuits," in *Proc. IEEE 12th Energy Convers. Congr. Expo. Asia (ECCE-Asia)*, May 2021, pp. 2286–2291.

[16] Z. Aleem and M. Hanif, "Operational analysis of improved Γ-Z-source inverter with clamping diode and its comparative evaluation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 12, pp. 9191–9200, Dec. 2017.

[17] H. Liu, Z. Zhou, K. Liu, P. C. Loh, W. Wang, D. Xu, and F. Blaabjerg, "A family of high step-up coupled-inductor impedance-source inverters with reduced switching spikes," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9116–9121, Nov. 2018.

[18] H. Liu, Z. Zhou, K. Liu, P. C. Loh, W. Wang, D. Xu, and F. Blaabjerg, "High step-up Y-source inverter with reduced DC-link voltage spikes," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5487–5499, Jun. 2019.

[19] Z. Aleem, H.-K. Yang, H. F. Ahmed, and J.-W. Park, "Quasi-clamped ZSI with two transformers," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9455–9466, Oct. 2021.

[20] M. R. Banaei, R. R. Ahrabi, and M. Elmi, "Single-phase safe commutation trans-Z-source AC–AC converter," *IET Power Electron.*, vol. 8, no. 2, pp. 190–201, Feb. 2015.

[21] M. R. Banaei, R. Alizadeh, N. Jahanyari, and E. Seifi Najmi, "An AC Z-source converter based on gamma structure with safe-commutation strategy," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1255–1262, Feb. 2016.

[22] S. Esmaeili, A. Mahmoudi, and S. Kahourzade, "Sinusoidal input current single-phase AC–AC converter based on coupled transformer with reduced turns ratio," in *Proc. IEEE 12th Energy Convers. Congr. Expo. Asia (ECCE-Asia)*, May 2021, pp. 426–431.

[23] L. He, J. Nai, and J. Zhang, "Single-phase safe-commutation trans-Z-source AC–AC converter with continuous input current," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5135–5145, Jun. 2018.

[24] Z. Aleem, H.-K. Yang, H. F. Ahmed, S. L. Winberg, and J.-W. Park, "A class of single-phase Z-source AC–AC converters with magnetic coupling and safe-commutation strategy," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 8104–8115, Aug. 2020.

[25] H. F. Ahmed, H. Cha, A. A. Khan, and H.-G. Kim, "A family of high-frequency isolated single-phase Z-source AC–AC converters with safe-commutation strategy," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7522–7533, Nov. 2016.

[26] H. F. Ahmed and H. Cha, "A new class of single-phase high-frequency isolated Z-source AC–AC converters with reduced passive components," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1410–1419, Feb. 2018.

[27] S. M. J. Mousavi, E. Babaei, D. Alizadeh, and H. Komurcugil, "Single-phase AC–AC Z-source converter based on asymmetrical gamma structure with continuous input current and safe commutation strategy," *IET Power Electron.*, vol. 14, no. 3, pp. 680–689, Feb. 2021.

[28] C. Kumar and M. Mishra, "An improved hybrid DSATCOM topology to compensate reactive and nonlinear loads," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6517–6527, Dec. 2014.

[29] C. Kumar and M. K. Mishra, "Predictive voltage control of transformerless dynamic voltage restorer," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2693–2697, May 2015.

[30] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA: Kluwer, 2001.

[31] A. Khodaparast, M. J. Hassani, E. Azimi, M. E. Adabi, J. Adabi, and E. Pouresmaeil, "Circuit configuration and modulation of a seven-level switched-capacitor inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 7087–7096, Jun. 2021.

[32] E. Azimi, A. Tavasoli, H. Hafezi, and A. Nateghi, "A dumbbell type (D-type) multilevel inverter based on switched capacitor concept," *Int. J. Electron.*, vol. 109, no. 1, pp. 152–168, Jan. 2022.

[33] A. Khodaparast, E. Azimi, A. Azimi, M. E. Adabi, J. Adabi, and E. Pouresmaeil, "A new modular multilevel inverter based on step-up switched-capacitor modules," *Energies*, vol. 12, no. 3, p. 524, Feb. 2019.

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