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RESEARCH ARTICLE

Design and Analysis of a Novel HVDC Circuit Breaker Test Bench Based on an H-Bridge Cell MMCC

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ABSTRACT This paper proposes a novel circuit configuration for a high-voltage direct-current circuit breaker (HVDCCB) test bench that differs significantly from conventional test benches. The proposed test bench consists of a modular multilevel cascaded converter (MMCC) that is based on H-bridge cells, an output inductor, and an auxiliary capacitor bank. The proposed test bench is capable of generating controllable output currents up to several kiloamperes and output voltages up to several hundred kilovolts because each MMCC cell is operated by phase-shifted pulse-width-modulated (PSPWM) signals. Consequently, the proposed test bench can simulate a wide range of fault conditions within hardware limitations to test different HVDCCB types with various current and voltage ratings. The flexibility of the proposed test bench is complemented by a longer service lifetime with inherent circuit protection in the case of operational failure of the HVDCCB. The concept of the proposed test bench is verified experimentally on a downscaled test bench that consists of nine H-bridge cells and operates at an equivalent switching frequency of 92.5 kHz.

INDEX TERMS DC circuit breaker, HVDC, MMCC, test bench, test circuit.

I. INTRODUCTION

The change in public opinion on the usage of fossil fuels for power generation is creating a void that can be filled by renewable power sources [1]. However, these new power sources require the development of new power transmission infrastructure. Although the cost of terminal equipment is higher, high-voltage direct current (HVDC) technology exhibits good potential because of its lower losses [2]–[4] compared with high-voltage alternating current (HVAC) technology. There is a general consensus that multi-terminal (MT) HVDC grids [5] are ideal for the connection of renewable power sources [6]; however, special consideration must be given to fault protection. Fault-blocking converters can be used to clear faults in MT HVDC grids [7], but the entire grid must be shut down, which is an inefficient procedure. Instead, the faulty part should be isolated using HVDC circuit breakers (HVDCCBs) so that the remainder of the grid can function normally. The HVDCCB is significantly more complex than its HVAC counterpart because it must be able to provide an artificial current zero-crossing and absorb any energy that remains in the faulty transmission line [8].

Every HVDCCB must be tested and verified before use. At present, there are no international HVDCCB testing standards, but preliminary guidelines have been provided [9], [10]. An ideal HVDCCB test bench should satisfy the following requirements [10]:

1) provide nominal initial operating conditions for the HVDCCB;
2) generate a test current that can increase to the rated load condition;
3) generate and sustain the HVDCCB transient interrupt voltage (TIV);

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4) provide enough energy based on agreed upon-requirements;
5) provide the required dielectric stress after HVDCCB operation;
6) provide circuit protection in the case of operational failure of the HVDCCB;
7) be technically feasible, practical, and economical.

Conventional HVDCCB test benches are based on charged capacitors [11], [12] or charged inductors [13], followed by low-frequency AC short-circuit generators [14], [15]. Power-converter-based HVDCCB test benches [16], [17] are a recent addition. Charged capacitor-based and charged inductor-based test benches are simple, economical, and ideal for current-breaking tests. The low-frequency AC short-circuit generator-based test bench is also comparatively economical and can provide sufficient energy for both the current-breaking and the maximum TIV withstand tests. However, these conventional test benches have the significant disadvantage of being unable to control the output waveforms, which means that the accuracy of the HVDCCB test data will be lower, the HVDCCB cannot be tested under different fault conditions, and different circuits will be required to fully test the HVDCCB. On the other hand, with complete control of the output waveforms, power-converter-based test benches appear to be the ideal solution because the HVDCCB can be fully tested under different fault conditions with high accuracy. However, the power-converter-based solution is not economical. An HVDCCB test requires a tremendous amount of energy from large capacitors, inductors, or power converters with an appropriately high rating. This problem is further complicated by HVDCCBs with auto-reclosing capability because their energy absorption rating is multiple times higher.

This paper proposes a novel circuit configuration for an HVDCCB test bench that combines a modular multilevel cascaded converter (MMCC) with an auxiliary capacitor bank to overcome some of the limitations of conventional test benches. The MMCC is used to control the output current and voltage during the current-breaking, maximum TIV withstand, and dielectric withstand tests to simulate a wide range of fault conditions. The proposed test bench combines and extends the functionality of multiple conventional test benches into a single circuit, which can also provide test continuity. The feasibility problem of a high-power MMCC is solved by using an auxiliary capacitor bank to offset the HVDCCB voltage during the maximum TIV and dielectric withstand tests. In addition, the external and internal fault-handling capabilities of the MMCC can be repurposed to serve as a protective measure in the case of operational failure of the HVDCCB [18], [19], which will reduce the overall complexity of any external protection circuits. The concept of the proposed test bench was verified on a downscaled test bench that consists of nine cells and operates at an equivalent switching frequency of 92.5 kHz.

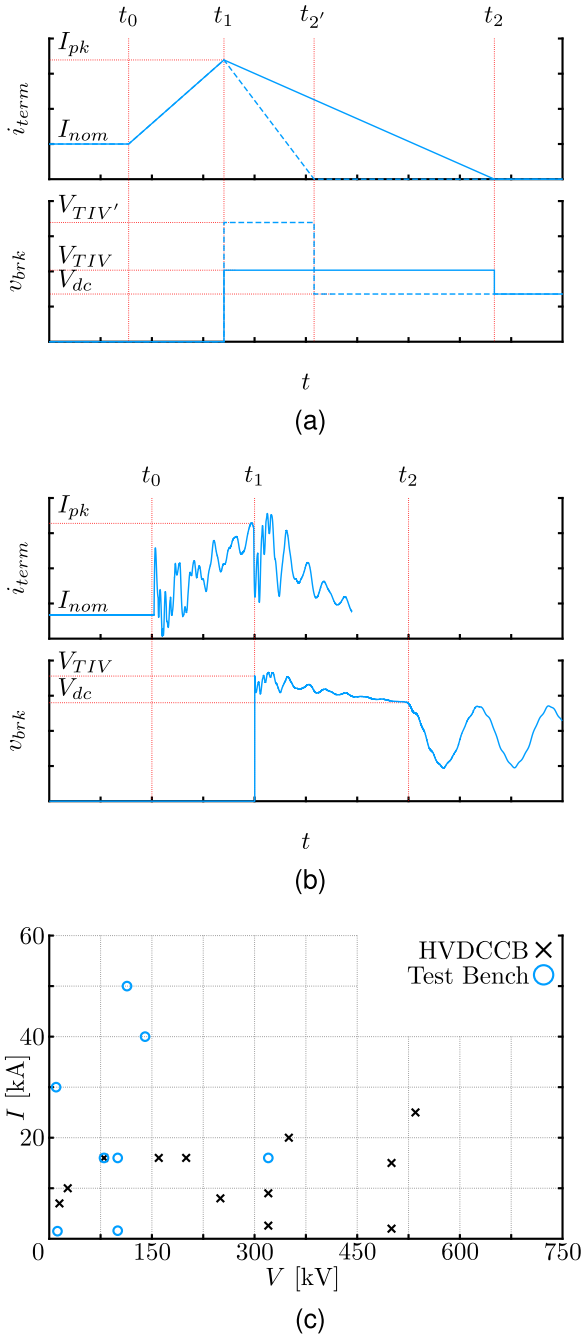


FIGURE 1. HVDC fault waveforms and current and voltage ratings of test benches and various HVDCCB designs: a) Idealized line-to-ground fault near the terminals of the HVDCCB, b) Line-to-ground fault along the HVDC transmission line with traveling wave effects, c) Current and voltage ratings.

II. REVIEW OF HVDCCB TESTING

Without clearly defined testing standards, the best approach to HVDCCB testing is to recreate the HVDC fault conditions in a controlled laboratory environment. When a fault occurs, the HVDCCB can be exposed to a wide range of current and voltage conditions that depend on the location of the fault point. For example, Fig. 1 shows the idealized waveforms of

a line-to-ground fault that occurs near the terminals of the HVDCCB. i_{term} represents the output current of the HVDC grid terminal and v_{brk} represents the voltage across the terminals of the HVDCCB. HVDCCB operation can be divided into four distinct periods:

1) Period of normal operation ($t < t_0$);
2) Fault period with current commutation ($t_0 \leq t < t_1$);
3) Fault period with current limiting ($t_1 \leq t < t_2$);
4) Period after fault clearance ($t_2 \leq t$).

The period of normal operation sets the initial operating conditions for the HVDCCB. The fault period with current commutation is characterized by a linear increase in i_{term}. The duration is affected by the detection threshold and the HVDCCB type. The fault period with current limiting is characterized by an opened HVDCCB, a v_{brk} that is clamped by the arrester array, and an i_{term} that decreases linearly toward zero because the remaining energy is absorbed by the arrester array. The voltage across the arrester array is known as the TIV V_{TIV}, and is designed to be between 150 % and 250 % of the nominal grid voltage V_{dc} [10]. During the period after fault clearance, i_{term} is zero and v_{brk} is reduced to V_{dc}. Detailed information on the operation of various HVDCCB designs can be found in other research papers [6], [14], [20], [21]. In a laboratory, the fault period with current commutation, the fault period with current limiting, and the period after fault clearance are synonymous with the *current-breaking*, the *maximum TIV withstand*, and the *dielectric withstand* tests, respectively.

Another example of HVDC fault waveforms is shown in Fig. 1b. The fault is assumed to have occurred somewhere along the transmission line, which means that the behavior of the current and voltage waveforms will be affected by traveling waves [22]–[25] that can expose the HVDCCB to more severe conditions than those shown in Fig. 1a. For example, the expected peak current and voltage ratings can be exceeded or even reversed across the terminals of the HVDCCB, which can lead to an overload. To optimize the performance, the HVDCCB should also be subjected to these complex conditions.

The process of HVDCCB testing is further complicated by the relationship between the current and voltage ratings of the various test benches and HVDCCB designs, as shown in Fig. 1c [10], [13], [16], [26]–[36]. With multiple units connected in parallel, test benches can output currents up to 50 kA, but the output voltage is usually below 150 kV. In contrast, HVDCCB ratings can exceed 20 kA and 500 kV. In such cases, the HVDCCB can be subjected to modular testing or testing with reduced ratings [10].

A. CHARGED CAPACITOR-BASED TEST BENCH

The charged capacitor-based test bench (CCTB) is one of the simplest circuits used for HVDCCB verification [11], [12]. The generic circuit configuration is shown in Fig. 2. It consists of a capacitor C that stores the energy for the test, an inductor L that is used to set the gradient of the output current, a switch S that is used to trigger the test, and the CB to be tested.

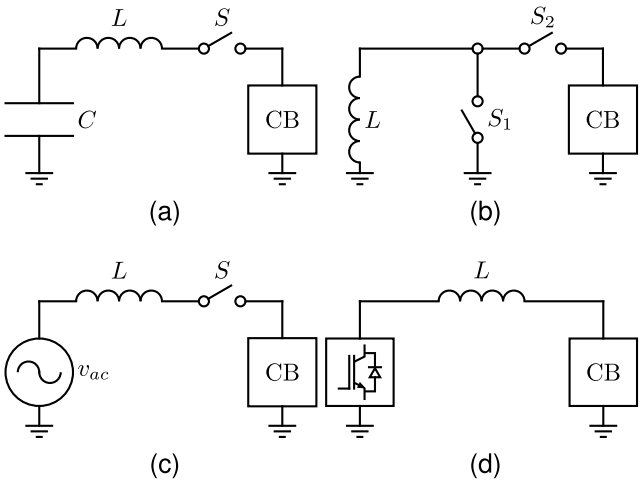


FIGURE 2. Simplified circuit configurations of various HVDCCB test benches: a) Charged capacitor-based test bench, b) Charged inductor-based test bench, c) Low-frequency AC short-circuit generator-based test bench, d) Power-converter-based test bench.

The main advantages of the CCTB are its simplicity and ability to produce high current gradients, which make it ideal for the current-breaking test. However, the maximum TIV and dielectric withstand tests require large capacitors, which makes the CCTB bulky and impractical. Without any control over the output waveforms, initial conditions for the CB cannot be provided, and it is impossible to generate the waveforms shown in Fig. 1a and 1b. The simplicity of the CCTB requires additional protective equipment in the case of operational failure of the CB. Improvements can be introduced [26], but the usability of the CCTB remains limited.

B. CHARGED INDUCTOR-BASED TEST BENCH

The charged inductor-based test bench (CITB) is another simple circuit that is used for HVDCCB verification [13]. The generic circuit configuration is shown in Fig. 2b. It consists of an inductor L that stores the energy for the test, switches S_1 and S_2 that are used to control the power flow, and the CB to be tested.

The main advantages of the CITB are its simplicity, large output current rating, and lack of additional protective equipment because the output current equals the rated current of the HVDCCB. However, a large output current and a long-duration maximum TIV withstand test require one or more large and high-quality L. The output waveform is not a perfect DC current, and it cannot be controlled, which means that the initial conditions for the CB cannot be provided, and that the waveforms shown in Fig. 1a and 1b cannot be generated. The dielectric withstand test requires a separate circuit, and the timings of S_1 and S_2 must be highly accurate to ensure proper operation. In short,

just like the CCTB, the CITB is limited in terms of its usability.

C. LOW-FREQUENCY AC SHORT-CIRCUIT GENERATOR-BASED TEST BENCH

The low-frequency AC short-circuit generator-based test bench (ACTB) is a more advanced circuit used for HVDCCB verification [14], [15]. The generic circuit configuration is shown in Fig. 2c. It consists of a low-frequency AC short-circuit generator v_{ac} that provides the power for the test, an inductor L that is used to control the output current and as energy storage, a switch S that is used to trigger the test, and the CB to be tested.

The ACTB is superior to both the CCTB and the CITB, and is suitable for both the current-breaking and the maximum TIV withstand tests. Because S can be used to control the application of v_{ac} to L, the output current can be controlled. The initial investment in the ACTB can be reduced by retrofitting existing generators. However, although an AC voltage can be applied to the HVDCCB during the dielectric withstand test, the application of a DC voltage requires a separate circuit. The AC waveform cannot be used to provide the initial conditions for the CB. The difference between V_{TIV} and v_{ac} can exceed the insulation rating of the generators. The waveforms shown in Fig. 1a and 1b cannot be generated. Finally, additional protective equipment is required in the case of operational failure of the CB.

D. POWER-CONVERTER-BASED TEST BENCH

The power-converter-based test bench (PCTB) is a comparatively new concept that is considered for HVDCCB verification with only a few full-sized prototypes [16], [37]. The generic circuit configuration is shown in Fig. 2d. It consists of a power converter that provides power for and controls the execution of the test, an inductor L that is necessary for output current control, and the CB to be tested. The generic circuit configuration of the PCTB shown in Fig. 2d may not necessarily reflect actual test benches because it depends on the power converter.

The most important advantage of the PCTB is its ability to completely control the output waveforms. Consequently, the complex waveforms shown in Fig. 1a and 1b can be generated to test different CB types of various ratings under a wide range of fault conditions. Furthermore, the current-breaking, maximum TIV withstand, and dielectric withstand tests can be performed using only one circuit. However, there are some disadvantages that need to be considered. For example, in [16], the output of the test bench is unipolar, limiting its flexibility, and the output voltage rating is low, which means that the maximum TIV and dielectric withstand tests cannot be performed. In [37], the required current and voltage can be generated; however, the output waveforms are unipolar, and additional protective equipment is required in the case of operational failure of the CB. Similar problems have been observed in [34]. The design of a PCTB my be infeasible depending on the required power rating.

TABLE 1. Advantages and disadvantages of various test benches based on the conditions listed in the introduction.

	CCTB	CITB	ACTB	PCTB
Requirement 1	NO	NO	NO	YES
Requirement 2	YES	YES	YES	YES[1]
Requirement 3	NO[2]	NO[2]	YES	YES
Requirement 4	NO[2]	NO[2]	YES	YES
Requirement 5	NO[2]	NO	NO	YES
Requirement 6	NO	NO	NO	YES
Requirement 7	YES	YES	YES	NO[3]

[1] Full control of the output current enables generation of a wide range of fault conditions
[2] Requires very large energy storage that may be impractical
[3] Heavily dependent on the required power rating.

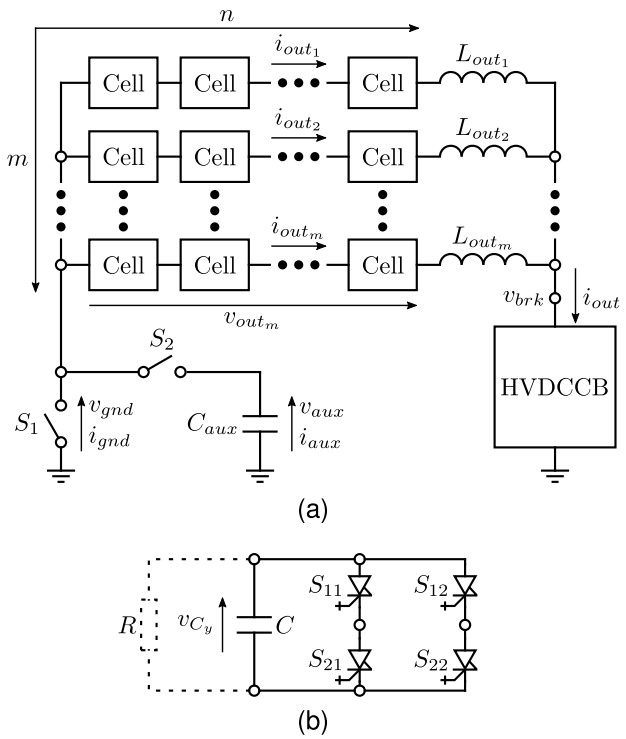


FIGURE 3. The circuit configuration of the proposed HVDC circuit breaker test bench: a) Overall circuit configuration, b) Internal cell circuit configuration.

Table 1 summarizes the advantages and disadvantages of the test benches shown in Fig. 2a, 2b, 2c, and 2d. This summary was made in accordance with the requirements listed in the introduction, and footnotes are provided to emphasize exceptions.

III. PROPOSED HVDCCB TEST BENCH

The main functions of the proposed HVDCCB test bench are to output a controlled current to simulate different fault conditions and to obtain accurate data pertaining to the HVDCCB behavior. The circuit configuration of the proposed test bench is illustrated in Fig. 3a. It consists of an H-bridge cell-based MMCC with associated output inductors L_{out_x}, an auxiliary capacitor bank C_{aux}, switches S_1 and S_2, and the HVDCCB to be tested.

The main component is the MMCC, which consists of m converter strings that increase the maximum output current i_{out}. Each string consists of n cells to increase the output voltage v_{out_x}. The cells are driven by phase-shifted pulse-width-modulated (PSPWM) signals that are phase shifted by $180°/n$ with respect to the preceding cell within the string. This arrangement increases the equivalent switching frequency f_{sw_x} of the string. Furthermore, every string is phase shifted by $180°/(mn)$ with respect to the preceding string. Thus, the equivalent switching frequency f_{sw} of the entire MMCC is increased significantly. Consequently, the sampling time T_s of the controller is reduced, which makes it possible to generate even complex transient waveforms. The PSPWM operation reduces the harmonic content in the output waveform, which implies that lower values of L_{out_x} can be used.

L_{out_x} operate in conjunction with the associated MMCC string to control the output current i_{out_x}. All i_{out_x} are balanced and combined to form the total output current i_{out}. Because of the operating principle, L_{out_x} should be lower than L shown in Fig. 2a, 2b, and 2c to achieve the necessary fault current gradients.

S_1 and S_2 are used for current flow control. Note that the switches are shown as mechanical to highlight the capability of bidirectional operation. However, in a full-scale test bench, S_1 and S_2 should be solid-state switches for performance reasons. S_1 provides a path for i_{out} up to time t_1 shown in Fig. 1a. Therefore, the relationship $i_{out} = i_{gnd}$ holds as long as S_1 is on. On the other hand, S_2 connects and disconnects C_{aux} from the circuit. S_1 and S_2 must be in opposite states during operation.

C_{aux} is used to increase the maximum output voltage rating of the proposed test bench. During the normal operating period and the fault period with current commutation, the relationship $v_{brk} = 0$ holds because the HVDCCB is closed. If the circuit is successfully disconnected, during the fault period with current limiting, the relationship $v_{brk} = 0$ no longer holds, S_1 is turned off, S_2 is turned on, and the relationship $i_{out} = i_{gnd}$ becomes $i_{out} = i_{aux}$. The step-like change in v_{brk} at time t_1 shown in Fig. 1a is compensated by $v_{gnd} = v_{aux}$. Because v_{aux} can be higher or lower than v_{brk}, v_{out_x} is used for fine tuning.

The last component is the HVDCCB, which can be of different types and ratings [20], [21]. The proposed test bench should be sufficiently flexible to enable testing of a wide range of devices under various conditions. Fig. 1a represents only one of many possible fault conditions, but even waveforms similar to those shown in Fig. 1b could be generated. The property of the proposed test bench to generate different conditions is achieved by controlling i_{out} and compensating v_{brk} with v_{out_x} and v_{aux}.

The operation of the proposed test bench shown in Fig. 3a can be summarized by the following equation:

$$v_{out_x} = R_{esr_x} i_{out_x} + L_{out_x} \frac{d}{dt} i_{out_x} - v_{brk} + v_{gnd}, \qquad (1)$$

where R_{esr_x} and x are the equivalent series resistance and subscript that describe the output circuit of each MMCC string, respectively. R_{esr_x} includes different physical resistances, such as the on-state resistance of the power devices, the parasitic resistance of the wires, and resistance of the inductors, as well as virtual resistive effects that stem from switching, dead-time, and harmonic content in the output waveforms. In short, R_{esr_x} is the equivalent series resistance that the MMCC "sees" at its output terminals, and is a dynamic value. However, in this paper, the variance of R_{esr_x} is considered negligible, which means that R_{esr_x} is considered constant. The value of R_{esr_x} that is presented in this paper was obtained experimentally. Note that the range of the subscript is $x \in \{1, 2, \ldots, m\}$.

The MMCC is based on the cascaded connections of many identical H-bridge cells. The structure of the cells is shown in Fig. 3b. The H-bridge cell was selected because

1) The equivalent switching frequency of each cell is twice the frequency f_c of the carrier wave.
2) Bidirectional output current and voltage capability are required for HVDCCB testing [10].

Each cell consists of four semiconductor switches S_{11}, S_{12}, S_{21}, and S_{22}, a capacitor C, and an optional resistor R.

The four switches control the application of the cell voltage v_{C_y} to the inductor L_{out_x}, where $y \in \{1, 2, \ldots, n\}$. Although metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs) are desirable to provide a high equivalent switching frequency f_{sw_x}, thyristors are required to achieve a large output current. For the proposed test bench, reverse-conducting integrated gate-commutated thyristors (RC-IGCTs) or bidirectional thyristors can be used [38]–[40].

A. OPERATING PRINCIPLE

The operating principle of the proposed HVDCCB test bench is explained using the waveforms shown in Fig. 1a. The entire process is divided into individual steps.

1) CHARGING

Before an HVDCCB test can be initiated, the auxiliary capacitor bank C_{aux} shown in Fig. 3a and cell capacitor C shown in Fig. 3b must be charged to their respective designed initial voltages V_{aux} and V_C. The charging circuit itself is not discussed because it is outside the scope of this research.

2) NORMAL OPERATING PERIOD - $t < t_0$

When the command to begin the HVDCCB test is given, the switch S_1 shown in Fig. 1a is turned on to connect the MMCC to ground and allow the output current i_{out} to flow. The proposed test bench generates the nominal grid current I_{nom} shown in Fig. 1a. This means that the relationship $i_{gnd} = i_{out} = I_{nom}$ is satisfied. Theoretically, the duration of this operating period can be unlimited because, ideally, the leakage of the cell capacitor C shown in Fig. 3b and other parasitic components that could dissipate energy is be zero.

3) FAULT PERIOD WITH CURRENT COMMUTATION - $t_0 \leq t < t_1$

During the fault period with current commutation (current-breaking test), switch S_1 shown in Fig. 1a is kept on to allow the output current i_{out} to flow. The proposed test bench can begin increasing i_{out} linearly from I_{nom} with a gradient $\dot{I}_{ramp}$ that is defined by the test requirements, and the duration depends on the HVDCCB characteristics. In the case of operational failure of the HVDCCB, the expected peak current I_{pk} can be exceeded, which triggers a shutdown of the proposed test bench. This safety feature is also used by any MMCC when a fault occurs in an HVDC grid.

4) FAULT PERIOD WITH CURRENT LIMITING - $t_1 \leq t < t_2$

The fault period with current limiting (maximum TIV withstand test) begins at time t_1 when current commutation is completed. The output current i_{out} reaches its peak value I_{pk}, and the HVDCCB disconnects the circuit. i_{out} is forced to flow through the arrester array of the HVDCCB, which causes a step-like change in the HVDCCB voltage v_{brk}. At this moment, switches S_1 and S_2 shown in Fig. 3a must be turned off/on simultaneously. When S_2 is turned on, the auxiliary capacitor bank C_{aux} is connected to the circuit, which means that v_{brk} is compensated by v_{aux}. The output voltage v_{out_x} of the MMCC balances the difference between v_{aux} and v_{brk}. In short, the relationships $i_{aux} = i_{out}$ and $v_{brk} = v_{aux} + v_{out_x}$ are satisfied.

5) PERIOD AFTER FAULT CLEARANCE - $t_2 \leq t$

The period after fault clearance (dielectric withstand test) begins at time t_2. At this time, although the output current i_{out} is equal to zero, the states of switches S_1 and S_2 shown in Fig. 3a must not be changed. This allows the proposed test bench to output the nominal grid voltage V_{dc} to the HVDCCB. Thus, the relationship $v_{brk} = V_{dc} = v_{aux} + v_{out_x}$ is satisfied.

6) TEST TERMINATION

After the HVDCCB test is completed, switch S_2 shown in Fig. 3a can be turned off to disconnect the auxiliary capacitor bank C_{aux} from the circuit (S_1 was already turned off at time t_1). At this point, the proposed test bench can be returned to step one, or it can be allowed to slowly discharge.

B. CONTROL SYSTEM

The control system of the proposed HVDCCB test bench is based on a modified version of the well-known proportional-integral (PI) controller. The PI controller was chosen because of its ease of implementation and very low computational requirements, which means that more processing power can be devoted to increasing the total equivalent switching frequency f_{sw}. Note that the present version of the controller assumes operation only during an HVDCCB test because other functionalities that depends on the scale and implementation of the proposed test bench influence the final implementation of the controller.

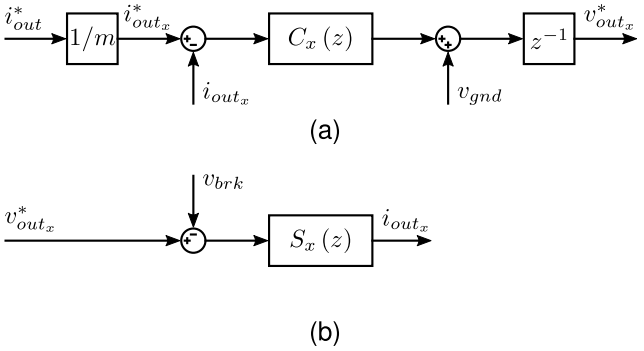


FIGURE 4. Partial block diagram of Fig. 3: a) Digital current control system, b) Plant model used in MATLAB simulations.

The block diagram of the proposed test bench is shown in Fig. 4. The proposed test bench is divided between the PI controller $C_x(z)$ shown in Fig. 4a, and the model $S_x(z)$ of the output circuit shown in Fig. 4b. Because of the digital nature of the PI controller, the transfer function is given in the $\mathcal{Z}$ domain as follows:

$$C_x(z) = K_{P_x} + \frac{K_{I_x} T_s}{z-1}, \tag{2}$$

where K_{P_x} and K_{I_x} are the proportional and integral gains, respectively, and T_s is the controller sampling time. Because it is desirable to have a separate implementation of the controller for each MMCC string, the subscript x is included to identify the individual strings. For this reason, the total input reference current i^*_{out} is divided by the number m of MMCC strings. The output of $C_x(z)$ is offset by the feedforward control branch that adds the voltage v_{gnd} to compensate for the behavior of the HVDCCB voltage v_{brk}, and to improve the transient response. The voltage reference $v^*_{out_x}$ control variable is generated after a time delay of one T_s. The delay T_s is represented by the z^{-1} block. Unfortunately, this delay is inherent in all digital control systems and cannot be eliminated.

In contrast to the controller, the output circuit is a continuous system that can be described in the $\mathcal{L}$ domain as follows:

$$S_x(s) = \frac{1}{L_{out_x} s + R_{esr_x}}, \tag{3}$$

where L_{out_x} is the inductor at the output of an MMCC string and R_{esr_x} is the equivalent series resistance that the MMCC string "sees" at its output terminals. As mentioned, R_{esr_x} is a dynamic value that includes the physical resistance of various components as well as virtual resistive effects that stem from circuit operation. The model $S_x(s)$ considers a constant R_{esr_x}. For consistency and ease of use, (3) is transcribed into the $\mathcal{Z}$ domain using the *Forward Euler Approximation*, which yields

$$S_x(z) = \frac{T_s}{(z-1) L_{out_x} + R_{esr_x} T_s}. \tag{4}$$

The input of $S_x\,(s)$ is the reference voltage $v^*_{out_x}$ generated by the PI controller.

The control system shown in Fig. 4 was analyzed thoroughly to derive equations for optimal controller parameters, implement steady-state output error compensation, etc. However, this information will not be discussed in detail because it is lengthy and out of the scope of the paper.

C. HARDWARE DESIGN CONSIDERATIONS

The hardware design of the proposed HVDCCB test bench is an optimization challenge. The parameters that need to be defined are the number m of MMCC strings, the number n of H-bridge cells per string, the capacitance C of each cell, the initial voltage V_C of the cells, the capacitance C_{aux} of the auxiliary capacitor bank, the initial voltage V_{aux} of the auxiliary capacitor bank C_{aux}, and the output inductance L_{out_x}. These parameters depend largely on the expected maximum values of the nominal grid voltage V_{dc}, the TIV V_{TIV}, the peak output current I_{pk}, the gradient $\dot{I}_{ramp}$ of the output current, and the duration of the fault period with current limiting.

To define C_{aux}, the standard capacitor current equation can be used:

$$i_{aux}\,(t) = C_{aux}\frac{d}{dt}v_{aux}\,(t)\,. \tag{5}$$

Because i_{aux} flows only during the fault period with current limiting (maximum TIV withstand test), assuming a linear change in i_{aux} from I_{pk} to zero, C_{aux} can be calculated from (5) as follows:

$$C_{aux} = 0.5\,I_{pk}\frac{\Delta t}{v_{aux}\,(t_1) - v_{aux}\,(t_2)}, \tag{6}$$

where Δt, $v_{aux}\,(t_1)$, and $v_{aux}\,(t_2)$ are the duration of the fault period with current limiting, the initial voltage V_{aux} of C_{aux}, and the charge remaining in C_{aux} at time t_2, respectively. A set of convenient values can be expressed as

$$v_{aux}\,(t_1) = V_{aux} = V_{TIV}, \tag{7}$$

$$v_{aux}\,(t_2) = V_{dc}. \tag{8}$$

Although V_{TIV} and V_{dc} may be ideal values, they may be technically unattainable depending on the remainder of the parameters. However, (7) and (8) simplify the analysis.

The preferred type of switch for the MMCC cells is the RC-IGCT because of its high current-carrying and bidirectional current conduction capabilities. Based on the maximum thyristor current I_T and I_{pk}, m can be calculated as follows:

$$m = \left\lceil \frac{I_{pk}}{I_T} \right\rceil. \tag{9}$$

On the other hand, n must consider several limits that depend on voltage constraints, which can vary significantly. For example, n must be sufficiently high to allow the MMCC to output the voltage difference between v_{brk} and v_{aux} at any time during operation, and to achieve the required equivalent switching frequency f_{sw}. Therefore n must satisfy:

$$n \geq \max\,(\alpha, \beta, \gamma)$$

$$\alpha = \left\lceil \frac{|v_{aux}\,(t_1) - V_{TIV}|}{m\,(1-\varepsilon_1)\,V_C} \right\rceil$$

$$\beta = \left\lceil \frac{|v_{aux}\,(t_2) - V_{dc}|}{m\,(1-\varepsilon_2)\,V_C} \right\rceil$$

$$\gamma = \left\lceil \frac{f_{sw}}{2mf_c} \right\rceil \tag{10}$$

where ε and f_c are the capacitor C discharge factor and carrier signal frequency of the cells, respectively. The discharge factor is a design variable that can be selected within the range $0 < \varepsilon < 1$. However, ε must be balanced appropriately because if it approaches zero, n will achieve its minimal value, whereas C will tend to infinity. Likewise, if ε approaches one, n tends to infinity and it will not be possible to control the output voltage during the dielectric withstand test.

The capacitance C depends on the amount of energy that needs to be stored for the MMCC to maintain the balance between v_{aux} and v_{brk}. The value of C can be calculated as

$$C \geq \frac{L_{out_x} I^2_{pk}}{nm^2 V^2_C \left[1 - (1-\varepsilon_2)^2\right]}. \tag{11}$$

Equation (11) requires L_{out_x}, which is bounded by both minimum and maximum values:

$$\frac{m^2 V_C}{2f_{sw}\Delta I_{out}} \leq L_{out_x} \leq \frac{nm\,(1-\varepsilon_2)\,V_C}{\dot{I}_{ramp}}. \tag{12}$$

In (12), the lower bound is defined by the maximum allowable ripple current ΔI_{out} of the output current i_{out}. The upper bound is defined by the maximum output current gradient $\dot{I}_{ramp}$ that the proposed test bench should be able to generate.

IV. EXPERIMENTAL RESULTS

The experimental results presented in this section were obtained using a downscaled test bench. The downscaled test bench consists of nine cells and operates at an equivalent switching frequency of 92.5 kHz.

A. THE DOWNSCALED TEST BENCH

Fig. 5 shows the circuit configuration of the downscaled test bench. Compared with Fig. 3, it can be seen that there are some differences, which were introduced because of convenience, scale, and component availability. However, the operating principle and general behavior were not affected.

The first difference is in the presence of the charging circuits shown in Fig. 5. The charging circuit for C_{aux} is shown in Fig. 5a and consists of a variable voltage source v_{chg} that is protected from overvoltage conditions by the body diode of S_4. The charging current i_{chg} is limited to a maximum of 250 mA to avoid skewing the results of the circuit breaker test. The charging circuit for the MMCC is shown in Fig. 5b, and consists of a variable three-phase auto-transformer (Auto TF), an isolation transformer (Y-Δ TF), and full-bridge rectifiers. The variable auto-transformer is used to easily vary the initial cell voltage V_C. The isolation transformer is used to provide galvanic isolation between the power grid and the downscaled test bench, as well as

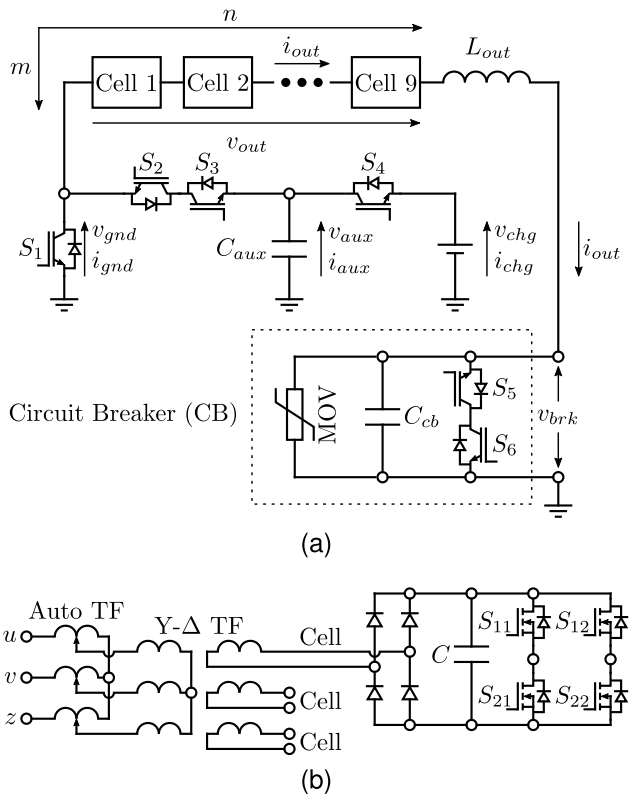


FIGURE 5. Downscaled circuit breaker test bench circuit configuration: a) Overall circuit configuration, b) Internal cell circuit configuration.

between the cells of the MMCC. The secondary side of the isolation transformer was separated into three individual phases that are routed to three cells. The full-bridge rectifiers attached to each H-bridge cell convert the AC voltage into DC. The remaining cells are powered up in the same manner by connecting two more isolation transformers to the auto-transformer.

Switches S_1 and S_2 shown in Fig. 3a are implemented using IGBT switches because of convenience and speed of operation, as shown in Fig. 5a. Similarly, the switches in the cells shown in Fig. 3b were replaced with MOSFET switches, as shown in Fig. 5b. This change was necessary to allow a high f_{sw} to be achieved with a lower number of cells.

A simple solid-state circuit breaker was constructed to verify the operation of the downscaled test bench. The circuit configuration of the circuit breaker is shown in Fig. 5a. It consists of two IGBT switches S_5 and S_6, which are connected in anti-series to provide a bidirectional path for the output current i_{out}, a capacitor C_{cb} to smooth out voltage transients, and a metal-oxide varistor (MOV) to absorb the remaining energy.

The parameters of the downscaled test bench are listed in Table 2. The MMCC is composed of a single string $m = 1$, which consists of a total of $n = 9$ cells. Each cell is operated with a carrier signal frequency of $f_c = 5.14\,\text{kHz}$, which means that an equivalent switching frequency of $f_{sw} = 92.52\,\text{kHz}$ can be achieved. A high f_{sw} ensures that the output waveforms are controllable and smooth when using

TABLE 2. Downscaled test bench parameters.

Parameter	Description	Value	
m	MMCC string count	1	
n	H-bridge cell count	9	
f_c	Cell carrier frequency	5.14	kHz
f_{sw}	Equivalent switching frequency	92.52	kHz
L_{out}	Inductance for current control	280	µH
R_{esr}	Equivalent series resistance	0.539	Ω
C	Capacitance of each cell	14.1	mF
C_{aux}	Auxiliary capacitor bank capacitance	3300	µF
C_{cb}	Circuit breaker capacitance	1	µF

smaller output inductors $L_{out_x} = 280\,\mu\text{H}$. However, f_c may appear to be excessively high for a single cell, and could potentially cause significant switching losses under heavy loads. This is a unique situation in the downscaled test bench. In a theoretical full-scale test bench, the output inductance and number n of cells will be higher, which means that the required f_{sw} can be achieved with an f_c value that is as low as a few hundred hertz. The equivalent series resistance $R_{esr} = 0.539\,\Omega$ of the output circuit was obtained experimentally. The large capacitance $C = 14.1\,\text{mF}$ of the cells is necessary to sustain the cell voltage v_{C_y} at a reasonable level because the initial cell voltage V_C is low. The auxiliary capacitor bank capacitance, $C_{aux} = 3300\,\mu\text{F}$, was calculated from (6) and manually adjusted during testing. The circuit breaker capacitance, $C_{cb} = 1\,\mu\text{F}$, was chosen arbitrarily.

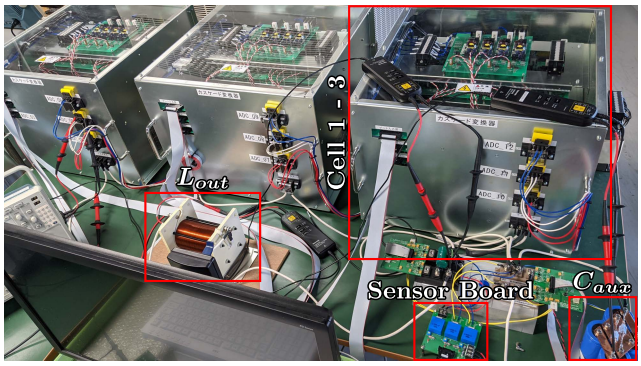
1) THE ASSEMBLED DOWNSCALED TEST BENCH

The downscaled test bench shown in Fig. 5 was assembled in the laboratory from available components, and the result is shown in Fig. 6. The MMCC cells are housed in metal enclosures with three cells per enclosure. The cells were designed and fabricated by a third party. The front panel in Fig. 6a exposes the input connectors for the PWM signals and cell capacitors C and the output connectors for the current and voltage sensors and cells, respectively. Small yellow polystyrene capacitors (not shown in Fig. 5b), full-bridge rectifiers, inductor L_{out}, and auxiliary capacitor bank C_{aux} can also be seen.

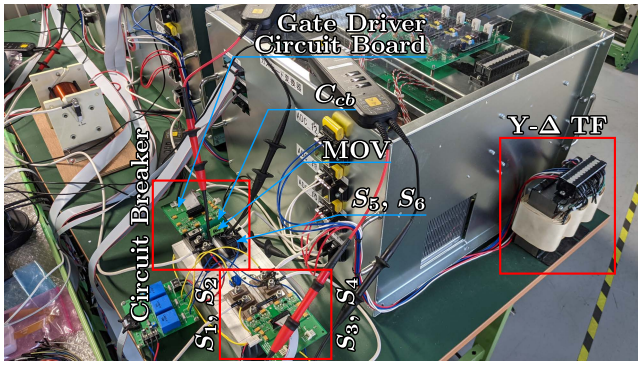
The simple solid-state circuit breaker and external switches S_1, S_2, S_3, and S_4 are mounted on an aluminum heatsink, which can be seen more clearly in Fig. 6b. The main switch of the circuit breaker (S_5 and S_6) is composed of IGBT modules that are controlled using a gate driver board that is soldered directly onto the gate terminals. The circuit breaker capacitor C_{cb} is a physically large green ceramic capacitor. The MOV can be seen next to C_{cb}. S_1, S_2, S_3, and S_4 are also half-bridge IGBT modules because of the availability of the components. The green printed circuit board (PCB) with three blue voltage sensors, which can be seen at the bottom of Fig. 6a, is used to monitor v_{brk}, v_{gnd}, and v_{aux}.

B. MEASUREMENTS AND DATA GRAPHS

The experiments that were performed on the downscaled test bench were based on the waveforms shown in Fig. 1a under the conditions listed in Table 3. Experiments with the



(a)



(b)

FIGURE 6. Photo of the downscaled test bench that was assembled in the laboratory.

TABLE 3. Experimental test conditions.

Parameter	Description	Value	
V_C	Initial cell capacitor voltage	13	V
V_{dc}	Specified DC supply voltage	120	V
V_{TIV}	Circuit breaker clamping voltage	150	V
V_{aux}	Initial voltage of level of C_{aux}	130	V
I_{nom}	Nominal current	20	A
I_{pk}	Peak current	50	A
I_{th}	Circuit breaker threshold current	35	A
$\dot{I}_{ramp}$	Fault current gradient	150	A/ms

waveforms shown in Fig. 1b are not yet possible considering the complexity of implementation. This functionality will be addressed in future research.

The initial cell voltage was set to $V_C = 13\,\text{V}$, which means that the maximum output voltage of the MMCC was $v_{out} \approx \pm 110\,\text{V}$. The nominal DC grid voltage and TIV were set to $V_{dc} = 120\,\text{V}$ and $V_{TIV} = 150\,\text{V}$, respectively, which extended the test duration to approximately 7 ms. The initial voltage of the auxiliary capacitor bank was set to $V_{aux} = 130\,\text{V}$. V_{aux} is higher than the expected V_{dc}, and is approximately 15 % lower than the expected V_{TIV}. The nominal current was set to $I_{nom} = 20\,\text{A}$, which is equal to 40 % of the maximum allowable peak current $I_{pk} = 50\,\text{A}$. The fault detection threshold was set to $I_{th} = 35\,\text{A}$. The fault current gradient was set to $\dot{I}_{ramp} = 150\,\text{A ms}^{-1}$, with an additional

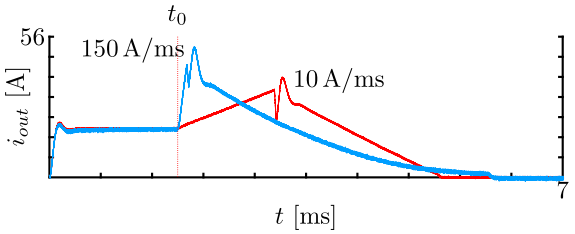


FIGURE 7. Output current i_{out} from two tests with $\dot{I}_{ramp} = 10\,\text{A ms}^{-1}$ and $\dot{I}_{ramp} = 150\,\text{A ms}^{-1}$.

experiment performed at $10\,\text{A ms}^{-1}$. It was established that values of $\dot{I}_{ramp}$ equal to or higher than $200\,\text{A ms}^{-1}$ cannot be controlled by the downscaled test bench in its present state. Note that the downscaled test bench was operated near its maximum current and voltage ratings, which the switches S_{11}, S_{12}, S_{21}, and S_{22} in the cells can handle without voltage ringing.

The data shown below were collected using the following equipment:

- Tektronix MSO5204B oscilloscope
- Tektronix MDO4104C oscilloscope
- Tektronix TPP0500B passive voltage probe
- Tektronix TMDP0200 differential voltage probes
- Tektronix TCP305A current probe

1) OPERATION WITH DIFFERENT GRADIENTS

The first experiment was performed with different values of the fault current gradient $\dot{I}_{ramp}$ to verify the ability of the downscaled test bench to control the output current i_{out}. Fig. 7 shows the results obtained from the $10\,\text{A ms}^{-1}$ and the nominal $150\,\text{A ms}^{-1}$ experiments. It can be seen that in both cases, regardless of the preset $\dot{I}_{ramp}$, i_{out} is smooth and the test can be completed in a straightforward manner. These experiments confirmed that the downscaled test bench has the ability to control i_{out}. Furthermore, with a steady-state output error of only 2.5 % up to time t_0, these results highlight the importance of determining the equivalent series resistance R_{esr}. Operating the downscaled test bench with an integral gain $K_I = 0$ resulted in 10 % steady-state output error. Note that the $10\,\text{A ms}^{-1}$ experiment was manually controlled to match the duration of the $\dot{I}_{ramp} = 150\,\text{A ms}^{-1}$ experiment.

2) COMPLETE TEST DATA

Fig. 8 shows the complete set of results that were obtained from the downscaled test bench. In this experiment, the proportional gain K_P was set to 40 % above the optimal value to increase the speed of the step response.

At time $t = 0$, the period of normal operation is started, and the downscaled test bench is instructed to output the nominal current I_{nom}. The MMCC generates an output voltage $v_{out} \approx 70\,\text{V}$, which quickly tends toward zero as i_{out} approaches I_{nom}. Once the steady-state condition is established, v_{out} begins to oscillate around $v_{brk} = 3\,\text{V}$. Theoretically, the steady-state condition can be maintained

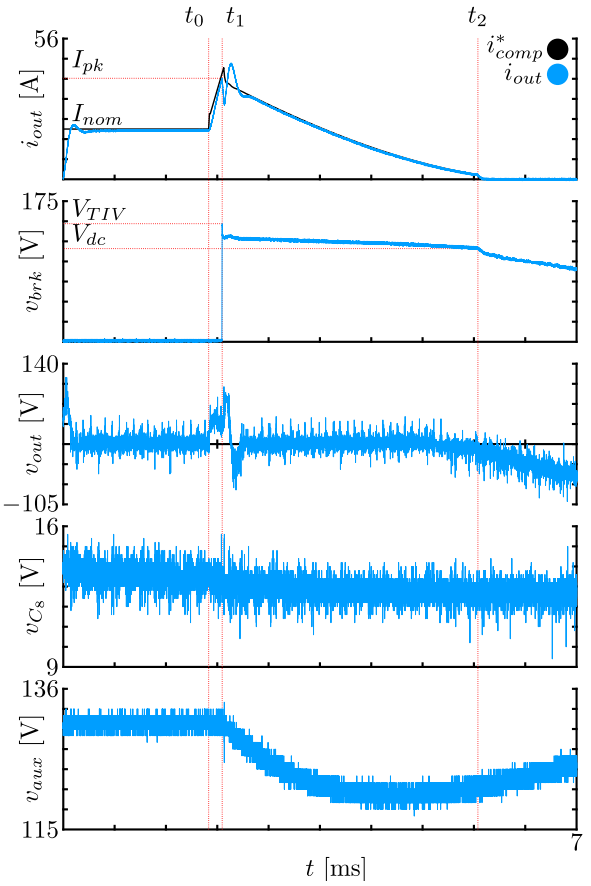


FIGURE 8. Result of the 150 A ms^{-1} circuit breaker test performed with the downscaled test bench.

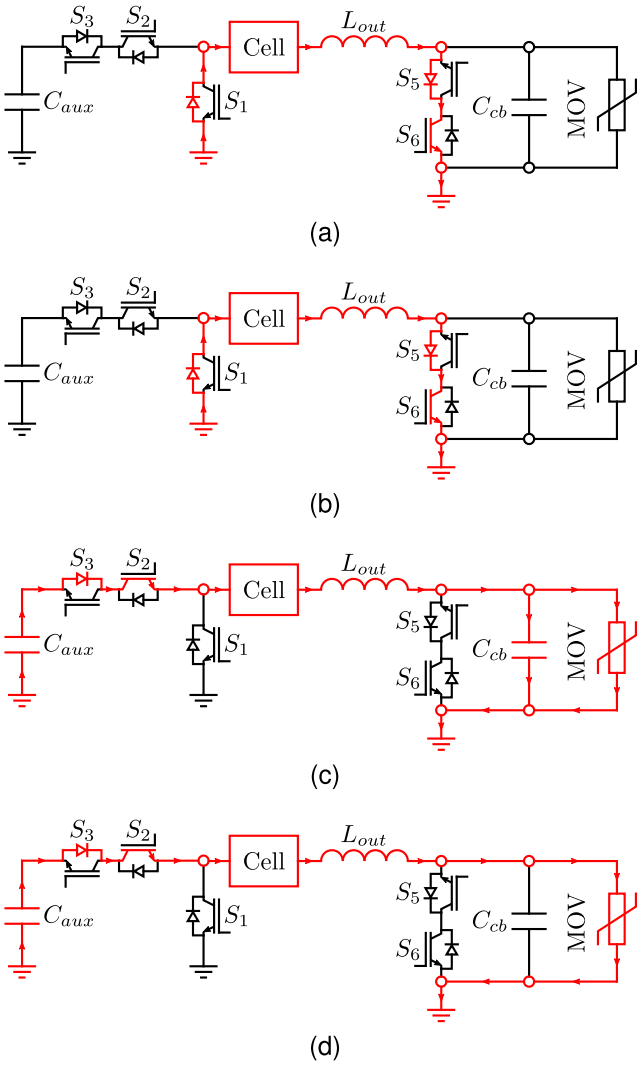


FIGURE 9. The operating principle of the simple solid-state circuit breaker: a) Period of normal operation ($t < t_0$), b) Fault period with current commutation ($t_0 \leq t < t_1$), c) Fault period with current limiting ($t_1 \leq t < t_2$), d) Period after fault clearance ($t_2 \leq t$).

indefinitely, but the parasitic resistance of the circuit dissipates energy, which decreases the cell voltage v_{C_8} over time. Because of the high capacitance C of each cell, the voltage drop is less than $\varepsilon_1 \leq 0.025$ after 2 ms. During this period, the relationship $i_{out} = i_{gnd}$ is maintained.

At time t_0, the downscaled test bench enters the fault period with current commutation (current-breaking test). A step offset is applied to i^*_{comp} one T_s before t_0, as shown in the graph of i_{out}. With this offset, i_{out} immediately begins to increase linearly from time t_0. However, it can be seen that the gradient of i_{out} is slightly higher, which is related to the increased proportional gain K_P and the steady-state output error compensation method. As i_{out} increases, there is a significant transfer of energy from C to L_{out}, which causes v_{C_8} to drop further by approximately 1 V in 162 µs. Because the circuit breaker is still closed, v_{brk} remains near zero, and the relationship $i_{out} = i_{gnd}$ is still satisfied.

After i_{out} exceeds the circuit breaker fault current detection threshold $I_{th} = 35$ A, the circuit breaker begins its operation to disconnect the circuit. However, i_{out} continues to increase up to 45 A because of the delay in the circuit breaker operation, which is approximately 67 µs under the present conditions. Because this delay is variable and completely dependent on the characteristics of the circuit breaker, it is impossible to determine time t_1 in advance.

At time t_1, after successful operation, the circuit breaker disconnects the circuit. This marks the beginning of the fault period with current limiting (maximum TIV withstand test). Because i_{out} cannot flow through S_5 and S_6, it is redirected to the MOV, which results in a step-like increase in the circuit breaker voltage v_{brk}. The MOV clamping voltage is $V_{TIV} \approx 150$ V. This change disturbs the controller. Because v_{brk} is higher than v_{out}, the voltage across L_{out} is reversed, and i_{out} drops sharply immediately after t_1. This drop in i_{out} cannot be avoided because it is caused by the transfer of energy from L_{out} to the MOV, which can be detected by the controller only after one T_s. Based on this information, it can be concluded that it is possible to mitigate this effect by reducing T_s and/or increasing L_{out}. Both options significantly impact the design of the proposed test bench.

After the change in v_{brk} is detected, S_2 is turned on to connect C_{aux} to the circuit. Because of the structure of the switches, the state of S_1 is changed automatically. Therefore, the relationships $v_{gnd} \approx v_{aux}$ and $i_{out} = i_{aux}$ are satisfied. Connecting C_{aux} to the circuit causes another disturbance for the controller because v_{aux} is slightly delayed compared with v_{brk}. Although the difference is small, an overshot of i_{out} appears immediately after the initial drop. The feedforward branch of the controller mitigates this effect; however, the inherent T_s delay of the controller prevents it from being completely eliminated. After the transients subside, i_{out} begins to decrease naturally as energy is dissipated across the MOV. Most of this energy is provided by C_{aux}, which can be seen in the decrease in v_{aux}. The MMCC will also expend some energy to control i_{out} based on the test parameters and the detected parameters of the circuit breaker. The decrease of the cell voltage is $\varepsilon_2 \leq 0.13$.

At time t_2, the energy remaining in the circuit is almost completely dissipated, as indicated by the near-zero i_{out}. Theoretically, zero will never be reached because of the exponential decrease of i_{out}. Therefore, to enter the period after fault clearance (dielectric withstand test), the relationship $i^*_{comp} = 0$ is asserted by the downscaled test bench. However, during the dielectric withstand test, the controller cannot properly control the output voltage of the MMCC; therefore, v_{brk} begins to deviate from the expected value of the grid voltage V_{dc}. Note that v_{aux} begins to increase during this period because C_{aux} is still connected to the charging circuit with a limited output current.

Although the downscaled test bench has revealed some interesting phenomena, the results shown in Fig. 8 prove that the concept of the proposed HVDCCB test bench is valid and that it can be used for HVDCCB verification.

V. CONCLUSION

This paper presents a test bench for high-voltage direct-current circuit breakers (HVDCCB) that is based on an H-bridge cell modular multilevel cascaded converter (MMCC) with small-sized inductors and an auxiliary capacitor bank. The proposed test bench is capable of providing initial operating conditions for the HVDCCB and performing controlled current-breaking, maximum transient interrupt voltage (TIV) withstand, and dielectric withstand tests. The MMCC is used to control the output current during the current-breaking and maximum TIV withstand tests and to tune the output voltage for the dielectric withstand test. This means that the proposed test bench is capable of simulating a wide range of fault conditions for various types of HVDCCB designs with different current and voltage ratings. Smooth control of the output waveforms is achieved using phase-shifted pulse-width-modulated (PSPWM) signals that drive the MMCC cells. The auxiliary capacitor bank is used to compensate for the TIV of the HVDCCB and to allow the proposed test bench to output the nominal grid voltage for the dielectric withstand test. The proposed test bench has an unprecedented level of flexibility, which cannot be achieved by conventional test benches. The quality of the output waveforms and the accuracy of the HVDCCB test results is further improved by mitigating steady-state output errors. The validity of the proposed test bench circuit configuration was experimentally verified on a downscaled test bench that consists of nine H-bridge cells and operates at an equivalent switching frequency of 92.5 kHz.

APPENDIX A
OBTAINING R_{esr_x}

It is difficult to obtain R_{esr_x} theoretically because it is a dynamic value that consists of physical resistance and virtual resistive effects. However, R_{esr_x} can be calculated using measured experimental data. The equation can be derived from the closed loop transfer function of the proposed test bench when the K_{I_x} gain is set to zero, which yields

$$\frac{i_{out_x}(z)}{i^*_{out_x}(z)} = \frac{K_{P_x} T_s}{z^2 L_{out_x} + z\left(R_{esr_x} T_s - L_{out_x}\right) + K_{P_x} T_s}. \quad (13)$$

Let $i^*_{out_x}(z)$ be given as a step input expressed as

$$i^*_{out_x}(z) = \frac{z}{z-1} I_{step}, \quad (14)$$

where I_{step} is a constant reference in amperes. Substituting (14) into (13) and applying the final value theorem yields

$$\begin{aligned} i_{out_x}(\infty) &= \lim_{z=1} \frac{(z-1) K_{P_x} T_s \frac{z}{z-1} I_{step}}{z^2 L_{out_x} + z\left(R_{esr_x} T_s - L_{out_x}\right) + K_{P_x} T_s} \\ &= \frac{K_{P_x}}{R_{esr_x} + K_{P_x}} I_{step}. \end{aligned} \quad (15)$$

In (15), the values of K_{P_x} gain and I_{step} are known, which means that R_{esr_x} can be obtained by measuring the value of the output current $i_{out_x}(\infty)$ in the steady-state.

The process can be divided into individual steps:

1) Set K_{I_x} to zero;
2) Set K_{P_x} to its optimal value;
   - Ensure a critically damped response;
3) Operate the test bench with a step input;
4) Measure the final value of i_{out_x};
5) Calculate R_{esr_x} using (15).

APPENDIX B
SIMPLE SOLID STATE CIRCUIT BREAKER

This section is provided as supplementary data. The operating principle of the simple solid-state circuit breaker is easily described using Fig. 9, which shows the various currents that flow during operation. During the period of normal operation, the current generated by the MMCC flows from ground, through the body diode of S_1, to the main switch of the circuit breaker, which is composed of S_5 and S_6. This situation is illustrated in Fig. 9a. The path of the current does not change during the fault period with current commutation (current-breaking test) because the circuit breaker has either not detected the fault or is still in the process of disconnecting the circuit. This situation is illustrated in Fig. 9b.

The situation changes during the fault period with current limiting (maximum TIV withstand test). Because S_5 and S_6 are off, the current is forced to flow through C_{cb} and the MOV. Because of the low capacitance, C_{cb} will be charged quickly after time t_1 and will become an open circuit. To compensate for the increase of the circuit breaker voltage, S_2 and S_3 are turned on, which forcefully turns off the body diode of S_1 and redirects the current through C_{aux}. This situation is illustrated in Fig. 9c. Finally, during the period after fault clearance (dielectric withstand test), only a residual current flows from C_{aux}, through the MMCC, to the MOV. This situation is illustrated in Fig. 9d.

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