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RESEARCH ARTICLE

A New Reduced Switch Seven-Level Triple Boost Switched Capacitor Based Inverter

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ABSTRACT This paper proposes a new reduced switch count seven-level triple boost inverter based on switched capacitor technique. The proposed topology has fewer number of components and has the ability of balancing the voltage across the capacitors. The structure of the proposed topology is very simple and can be easily extended to higher number of voltage levels. The generalized structure for higher number of levels is presented. The level shifted pulse width modulation approach is used to evaluate the proposed topology. In addition, design of switched capacitors and power loss calculation of semiconductor switches are provided. This proposed inverter topology is compared with the state-of-art topologies to demonstrate its superior performance. Further, thermal modelling of the topology is done in PLECS to calculate the power losses and efficiency. Finally, this proposed 7-level topology is simulated using MATLAB/Simulink and tested on experimental prototype for the performance verification and the results are included.

INDEX TERMS Switched capacitor, multilevel inverter, DC-AC conversion, triple boost, high gain, self-voltage balancing.

I. INTRODUCTION

Multilevel inverters (MLI) have been gaining popularity in renewable energy conversion systems and industrial applications due to its high-quality output waveform over the two-level inverters. The attractive features of multilevel inverters are near sinusoidal output waveform, low dv/dt stress, reduced power loss and low total harmonic distortion (THD). The traditional multilevel inverters are majorly divided into 3 categories such as neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) multilevel inverters [1]. However, these classical MLI have their limitations such as capacitor voltage balancing in NPC and FC. The CHB MLI stands out among these inverters but it needs a greater number of isolated DC sources. These classical MLI require a greater number of switches to get higher voltage levels.

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Considering all the above issues of classical MLI, several efforts have been made by the researchers and developed many numbers of reduced device count MLI. These topologies use fewer switches and diodes to get the same number of levels compared with the basic MLI topologies [2], [3]. The classical and reduced device count MLI do not have the ability of voltage boosting. This boosting of voltage will be essential in renewable energy conversion systems because of the low voltage generated by the PV panels and fuel cells. Therefore, switched capacitor technique was developed by the researchers to get the greater number of voltage levels and high gain with only one DC source. In this technique, the capacitors are charged by connecting them in parallel to the DC source and discharged to the load in series with the DC source to get higher voltage levels [4], [5].

In [6], three H-bridges are interconnected using two switches having bidirectional voltage blocking capability. Among the three H-bridges, only one H-bridge is supplied with DC source, other two H-bridges are equipped with switched capacitors. The charging of these capacitors is

enabled using the interconnected switches. The authors in [7] proposed a topology which has lower number of switching devices compared to existing single phase seven level inverters. In [8], authors proposed a seven level triple gain topology using single DC source with maximum blocking voltage of switches is $2V_{dc}$ and this topology has inherent negative voltage level generation capability without the need of H-bridge. In [9], the voltage boosting is achieved by the interconnection of non-isolated interleaved buck-boost converter and an inverter through two capacitors. The interleaved front-end boost stage may provide voltage gain of three while reducing peak current load on the switching devices. A new topology was proposed in [10] with less number of components and low voltage stress on the switches to get a voltage of 3. A (2N+1) level multilevel inverter is developed in [11], which consists of three parts. The front-end boost stage is followed by active SC cell(s) in the center and an H-bridge inverter in the last. In [12], authors developed a triple gain diamond shaped topology with low total standing voltage (TSV). In [13], a novel five level inverter with a gain of 2 is developed and is extended to generalized inverter. A quasi-soft charging cell is added in this architecture to decrease current stress and keep the charging current of the capacitors within acceptable limits. The authors in [14] developed a topology which has low number of components. The authors claim that their architecture has power regeneration capacity, which implies that if the capacitors become overcharged, they will automatically discharge to the source. In [15], a topology was developed using a full bridge inverter and two 3-level T-type structures to gat 7 level voltage but the switch count is very high.

All the articles discussed above can generate seven level output voltage with a gain of three. There are many topologies in the literature with seven level output voltage but with a boosting ratio of 1:1.5 only. In [16], authors developed a topology without H-bridge so that the TSV of the topology is greatly reduced. Moreover, the voltage stress of the switches is limited to input voltage only. A new T-type switched capacitor inverter is proposed in [17] which maximizes the utilization of two capacitors. In [18], a novel active neutral point clamped (ANPC) inverter is proposed which is capable of giving unity or boosted voltage gain. A novel topology with 10 switches and one capacitor is proposed in [19] to get seven level output voltage. The structure of this topology is similar to conventional ANPC. In [20], a seven level topology with low voltage stresses is proposed, however, it uses 3 capacitors. In [21], a new 8 switch boost ANPC is introduced for seven level inverter. It has a very high TSV of 7.3. In [22], the packed U-cell (PUC) is improved to have less number of switches to get 7 levels in the output voltage. A reduced switch seven level inverter is developed by adding a half bridge and switched capacitor circuit in [23]. In [24], a seven level inverter is formed by adding DC-link converter, bidirectional switch network and output converter. In [25], a new dual T-type ANPC is proposed to have the maximum output voltage level of 1.5 V_{dc}, however, the maximum voltage stress on the switch is $2V_{dc}$. In [26], a topology was proposed by the combination of T-type network and an extra floating capacitor and it has very high TSV of 10.66. In [27], a 13 level output voltage is generated with 13 switches and 3 capacitors using a switched capacitor technique.

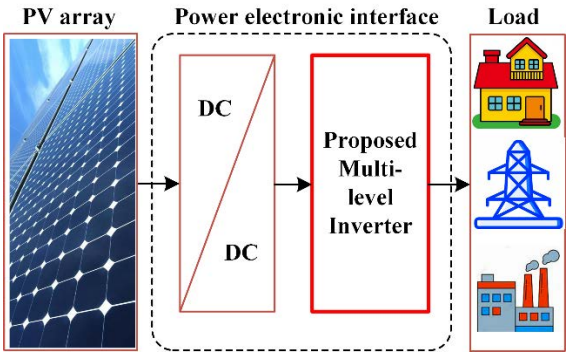

FIGURE 1. Multilevel power conversion system with solar PV.

Some of the generalized structures based on switched capacitor technique are proposed in [28]–[34]. In [28], a topology is proposed by the addition of two circuits. In the frontend, a quasi-resonant switched capacitor circuit (QRSCC) is used, while in the backend, an H-bridge circuit is used. In [29], a generalized structure is formed by using a repeating unit of 5 switches and one capacitor. In [30], a topology is proposed using the interconnection of T module, cross module and T' module. It can be extendable to higher levels by adding the extra cross modules. In [31], a generalized structure is formed by cascade connection of several H-bridges, where the isolated DC source is replaced by switched capacitors. In [32], a generalized topology is proposed by the combination of one T-type unit and number of crisscross capacitor units. In [33], an SC unit is proposed with four switches and one capacitor. This SC unit can be repeated to form a generalized structure to get a greater number of levels. In [34], a generalized multilevel inverter is formed by connecting more number of SC circuits consisting of 2 switches, one diode and one capacitor.

All the topologies based on switched capacitor technique does not require any sensor circuit for balancing of voltage across the capacitors, they have self-balancing ability of the voltage across the capacitors. All the topologies discussed above have a greater number of components. In this paper, authors put an effort to develop a topology with low number of switches, diodes and capacitors. The proposed topology can be used for low and medium voltage applications. In distribution generation systems like grid integration with small scale solar PV, the voltage ratings will be in medium ranges, for which the proposed topology with H-bridge is best suitable for these applications. The proposed topology can be implemented using the photovoltaic system as shown in Figure 1. The proposed topology has the following features.

- It has only 8 switches and one diode for seven-level inverter.

- It has a gain of 3 with single DC source.
- It is suitable for all types of loads.
- It has self-voltage balancing of capacitors.
- Four switches operate at fundamental frequency, which decreases the switching losses and enhances the efficiency.
- Only 2 out of 8 switches are involved in capacitor charging path, which reduces the conduction losses.

The remaining paper is structured as follows. The proposed seven level triple boost inverter with its operating modes and the voltage stress on the switches is discussed in section 2. Section 3 discusses the level shifted PWM scheme used to get the pulses to the switches in the inverter. Design of capacitor and loss calculations are done in section 4. The generalized topology for the proposed inverter is presented in section 5. In section 6, the proposed topology is compared with the literature. To know the performance of the proposed topology, simulation and hardware prototype results are presented in section 7.

II. PROPOSED 7-LEVEL INVERTER

The proposed 7-level triple boost multilevel inverter is shown in Figure 2. This topology has a total of 8 switches, two capacitors, and one diode. The switches S_1 and S_4 should have the reverse voltage blocking capability. The two capacitors are charged separately to V_{dc} by connecting them in parallel with the DC source and these are discharged in series with the DC source to the load to get higher voltage levels. This topology can generate the voltage levels of 0, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$. Therefore, the gain of this topology is 3. There are two sets of complementary switches (S_5, S_6) and (S_7, S_8) to avoid the short circuit of the DC source. The switches in H-bridge (S_5-S_8) have the MBV of $3V_{dc}$, the switches S_1 and S_4 have the MBV of V_{dc}, and the switches S_2, S_3 and diode have the MBV of $2V_{dc}$. Therefore, the per unit TSV of this topology is 6.66. The voltages across the capacitors are well balanced at V_{dc} by charging and discharging alternatively in each cycle of output voltage. The four switches in the H-bridge (S_5-S_8) changes its state (on or off) only once in each cycle, i.e., these switches operate at fundamental frequency which enhances the efficiency. The gate signals for the switches of the proposed topology are given according to Table 1. In this table, turn-on and turn-off states of the switches are shown as 1 & 0 respectively. The charging, discharging, and floating conditions (without charging or discharging) of the capacitor are represented as '↑', '↓' and '-' respectively.

A. OPERATING MODES

The operating modes of the proposed topology is shown in Figure 3. In this figure, red color indicates the generation of voltage level at the load and green color indicates the charging path. During the operation with inductive load, the load current reverses. The path of the current in the circuit during inductive load is shown with blue color.

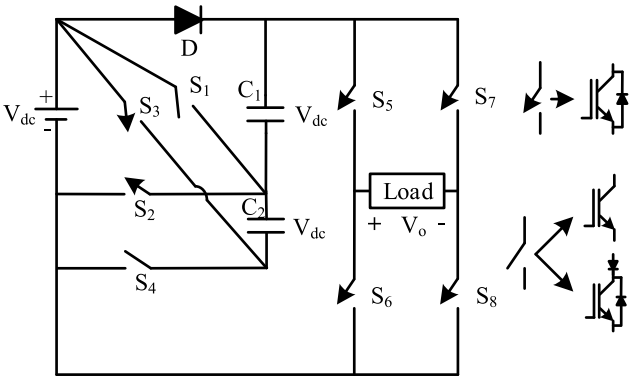

FIGURE 2. Proposed 7-level inverter.

TABLE 1. Switching pattern and their effect on switched capacitors for 7-level topology.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	C_1	C_2	V_o
0	0	1	0	1	0	0	1	↓	↓	$+3V_{dc}$
1	0	0	1	1	0	0	1	↓	↑	$+2V_{dc}$
0	1	0	0	1	0	0	1	↑	-	$+V_{dc}$
0	1	0	0	1	0	1	0	↑	-	0
0	1	0	0	0	1	0	1	↑	-	0
0	1	0	0	0	1	1	0	↑	-	$-V_{dc}$
1	0	0	1	0	1	1	0	↓	↑	$-2V_{dc}$
0	0	1	0	0	1	1	0	↓	↓	$-3V_{dc}$

Voltage level (0V): Zero voltage level can be obtained by two switching redundancies, either by turning on the switches S_5, S_7 or by S_6, S_8 as shown in Figure 4(a)&(b). The capacitor C_1 can be charged in this level by turning on the switch S_2. The capacitor C_2 is in floating mode in this state.

Voltage level ($+V_{dc}$) : The switches S_5 and S_8 are turned on to get $+V_{dc}$ voltage level as shown in Figure 4(c). The capacitor C_1 can be charged by turning on the switch S_2. The capacitor C_2 is in floating mode.

Voltage level($+2V_{dc}$) : The switches S_1, S_5 and S_8 are turned on to get the voltage level of $+2V_{dc}$ as shown in Figure 4(d). The capacitor C_1 is discharged along with the source to the load to get this level. The capacitor C_2 can be charged to V_{dc} by turning on the switch S_4. The diode gets reverse biased by the voltage across the capacitor C_1.

Voltage level ($+3V_{dc}$) : The voltage level of $+3V_{dc}$ can be obtained by turning on the switches S_3, S_5 and S_8 as shown in Figure 4(e). The two capacitors C_1 and C_2 are discharged to the load to get this voltage level. The diode gets reverse biased by the total voltage across both capacitors C_1 and C_2.

Voltage level($-V_{dc}$): The negative V_{dc} level ($-V_{dc}$) can be obtained by turning on the switches S_6 and S_7 as shown in Figure 4(f). The capacitor C_1 is in charging condition as S_2 is turned on and the capacitor C_2 is in floating condition.

Voltage level($-2V_{dc}$): This level can be generated by using the voltage across the capacitor C_1 and supply voltage and turning on the switches S_1, S_6 and S_7 as shown in Figure 4(g). The switch S_4 is turned on to charge the capacitor C_2. The diode is in reverse biased mode with a voltage stress of V_{dc}.

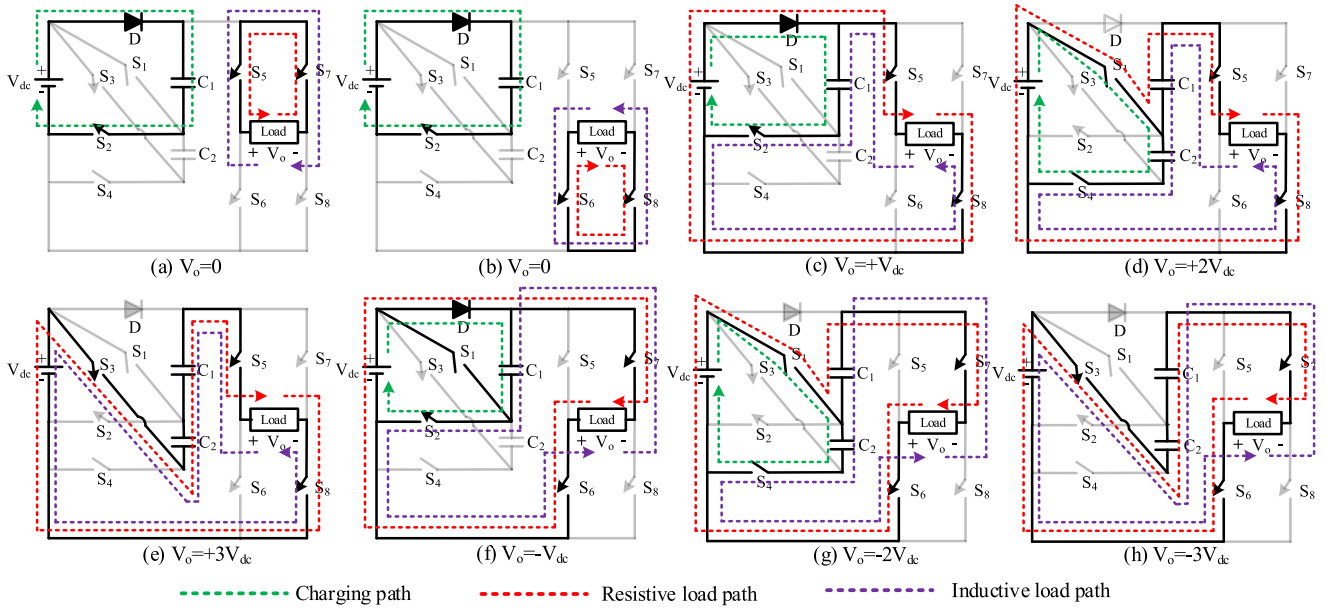

FIGURE 3. Operating modes of a proposed 7-level topology.

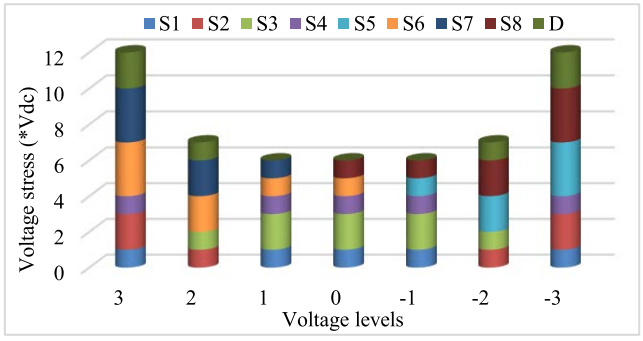

FIGURE 4. Voltage stress on different switches at different voltage levels.

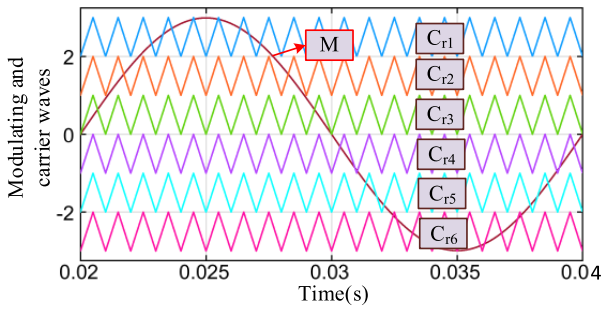

FIGURE 5. Level shifted PWM scheme.

Voltage level ($-3V_{dc}$): Both the capacitors C_1 and C_2 should be in discharge condition in series with source to get this voltage level as shown in Figure 4(h). The voltage stress across the diode will be $2V_{dc}$ in this condition.

B. VOLTAGE STRESS ON THE SWITCHES

In the proposed topology, the four switches forming the H-bridge (S_5-S_8) have the blocking voltage of $3V_{dc}$, the two

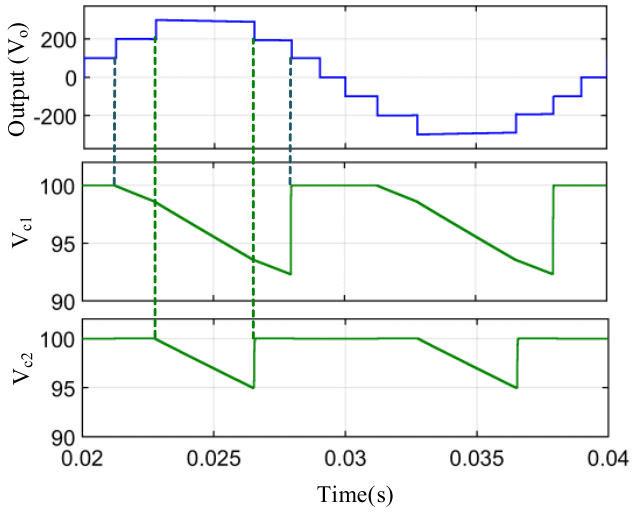

FIGURE 6. Capacitor voltages in relation to output voltage.

switches (S_1, S_4) have the blocking voltage of V_{dc} and the other two switches (S_2, S_3) have the blocking capacity of $2V_{dc}$. The diode has a blocking voltage of $2V_{dc}$. The voltage stress on different switches at different voltage levels is shown in Figure 4. The total standing voltage ($TSV_{p.u}$) is calculated using the formula (1)

$$TSV_{p.u} = \frac{\sum V_{sw\_off} + \sum V_{D\_off}}{V_{o\,max}} \tag{1}$$

The above formula is applicable only for the topologies having one voltage source. Here, V_{sw_off} is the blocking voltage of each switch, V_{D_off} is the diode reverse blocking voltage, and V_{omax} is the maximum output voltage. $TSV_{p.u}$ of the proposed seven level triple boost multilevel inverter is 6.66.

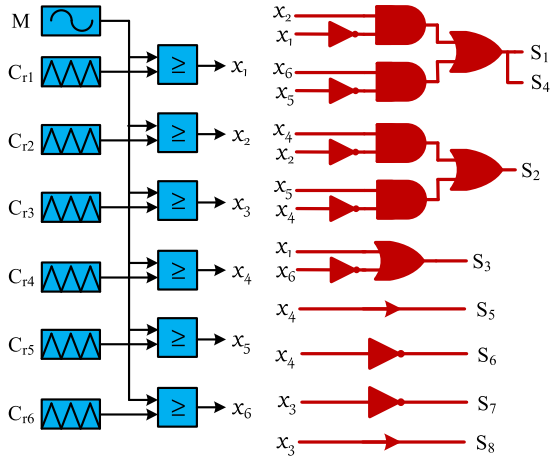

FIGURE 7. Switching logic.

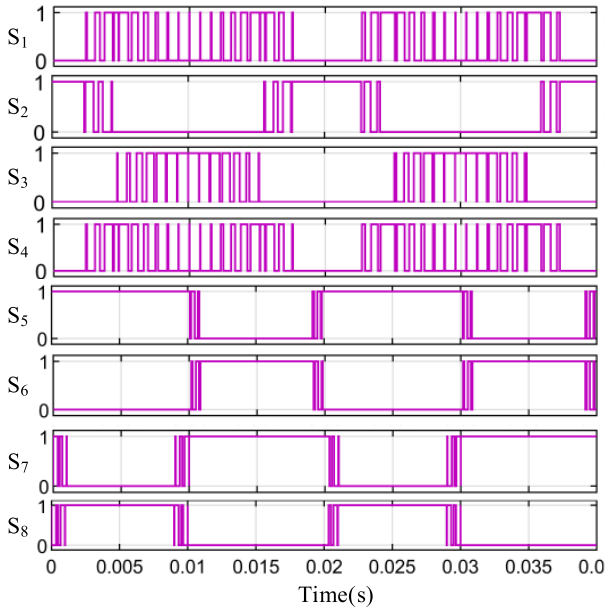

FIGURE 8. Pulses to the switches in proposed topology.

III. MODULATION SCHEME

The level shifted pulse width modulation technique is used to generate pulses to the switches in the topology as shown in Figure 5. As it is a seven-level topology, six carrier triangular waves (C_{r1}-C_{r6}) are required. All these carriers are arranged one over the other and in phase with each other. By comparing these carrier signals with the modulating sine wave, six signals (x_1-x_6) are generated as shown in Figure 7. These signals (x_1-x_6) are given to the logic pattern shown in Figure 7 to get gate signals to the switches. The pulses for the switches S_1-S_8 are generated as shown in Figure 8.

IV. CAPACITANCE AND EFFICIENCY CALCULATIONS

A. DESIGN OF CAPACITOR

The value of capacitors employed in any circuit is specified by the capacitors' longest discharge duration. In the proposed seven-level structure, the capacitor C_1 discharges at $\pm 2V_{dc}$ and $\pm 3V_{dc}$ voltage levels, whereas the capacitor C_2 discharges at $\pm 3V_{dc}$ voltage level as shown in Figure 6. Integrating the current through the capacitors throughout the longest discharge duration under maximum loading circumstances yields the highest amount of discharge in each half cycle (equation (2)).

$$Q_{Ci} = \int_{t_a}^{t_b} I_{load} \sin(2\pi f_m t)\, dt \tag{2}$$

where Q_{Ci} is the maximum discharge amount of the capacitor. The start and end timings of the discharge period are denoted by t_a and t_b. The quantity of charge that a capacitor can store should be more than Q/k in order to design a capacitor with k (p.u) ripple. i^{th} capacitor's value is

$$C_i > \frac{Q_{Ci}}{k.V_{dc}} \tag{3}$$

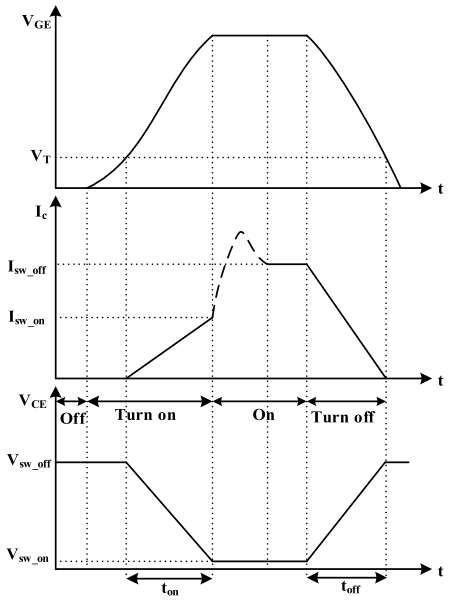

FIGURE 9. Turn-on and turn-off characteristics of the semiconductor switches.

B. LOSS AND EFFICIENCY CALCULATIONS

In semiconductor devices, there are two types of losses: switching losses and conduction losses. Switching losses occurred as a result of delays in the turn-on and turn-off processes. Conduction losses are caused by semiconductor on-state resistance [29].

1) SWITCHING LOSSES

Non-instantaneous turn-on and turn-off operations cause switching losses. When the switch is turned on, the collector current (I_C) begins to rise after the gate-emitter voltage (V_{GE}) exceeds the threshold value (V_T). When the V_{GE} exceeds the V_T, the collector-emitter voltage (V_{CE}) begins to fall. V_{CE} takes a long time to reach V_{sw_on}, while I_C takes a long time to reach I_{sw_on}. Both V_{CE} and I_C have finite nonzero values, resulting in on-time switching losses, as indicated in

equation (4). Similarly, during the turn-off operation, both I_C and V_{CE} have finite values for t_{off} time, as illustrated in Figure 9, resulting in turn-off switching losses, as indicated in equation (5).

$$\begin{aligned} P_{SL,i(ON)} &= f_{cr}\int_0^{t_{on}} V_{sw\_off,i}(t) * i(t)\,dt \\ &= f_{cr}\int_0^{t_{on}} \left(-\frac{V_{sw\_off,i}}{t_{on}}(t-t_{on})\right)\left(\frac{I_{sw\_on1,i}}{t_{on}}t\right)dt \\ &= \frac{1}{6}f_{cr} * V_{sw\_off,i} * I_{sw\_on,i} * t_{on} \end{aligned} \tag{4}$$

$$\begin{aligned} P_{SL,i(OFF)} &= f_{cr}\int_0^{t_{off}} V_{sw\_off,i}(t) * i(t)\,dt \\ &= f_{cr}\int_0^{t_{off}} \left(\frac{V_{sw\_off,i}}{t_{off}}t\right)\left(-\frac{I_{sw\_off2,i}}{t_{off}}(t-t_{off})\right)dt \\ &= \frac{1}{6}f_{cr} * V_{sw\_off,i} * I_{sw\_on2,i} * t_{off} \end{aligned} \tag{5}$$

where $P_{SL,i(ON)}$ is the turn-on switching loss of the i^{th} switch, and $P_{SL,i(OFF)}$ is the turn-off switching loss of the ith switch. The number of turn-on and turn-off of each switch and diode are calculated from the equation (6). Where, N_{s_on} & N_{s_off} are the number of turn-on and turn-off in one cycle respectively. f_m is modulating frequency and f_{cr} is carrier frequency.

$$N_{S\_on} = N_{S\_off} = \frac{f_{cr}}{f_m} \tag{6}$$

By summing the entire turn-on and turn-off losses of all switches, the total switching losses of all switches are computed using the equation (7).

$$P_{SL(Total)} = \sum_{i=1}^{N_{sw}} \left(\sum_{j=1}^{N_{on(i)}} P_{SL\_on(ij)} + \sum_{j=1}^{N_{off(i)}} P_{SL\_off(ij)} \right) \tag{7}$$

where $P_{SL(TOTAL)}$is the total switching losses and N_{SW} is the total number of switches in the MLI topology.

2) CONDUCTION LOSSES

Conduction losses in semiconductor switches occur when the switches are turned on. Losses occur during the on-state owing to the switch's on-state resistance and voltage drop across the switch. Equations (8) and (9) may be used to compute the conduction losses of switches and diodes, respectively:

$$P_{con\_sw} = V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms} \tag{8}$$

$$P_{con\_D} = V_{D\_on} * i_{D\_avg} + R_{D\_on} * i^2_{D\_rms} \tag{9}$$

where, P_{con_sw} is conduction loss of semiconductor switch, P_{con_D} is conduction loss of diode, V_{sw_on} is on-state voltage across switch (V_{DS}), V_{D_on} is on-state voltage across diode, R_{sw_on} and $R_{D_on}$are on state resistance of switch and diode respectively. i_{sw_avg}, i_{sw_rms}, i_{D_avg}, i_{D_rms} are average & RMS currents of switch and diode respectively. For the proposed 7-level inverter, the conduction losses become

$$\begin{aligned} P_{con(V_o=+1V_{dc})} &= 2\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) \\ &\quad + 1\left(V_{D\_on} * i_{D\_avg} + R_{D\_on} * i^2_{D\_rms}\right) \\ P_{con(V_o=+2V_{dc})} &= 3\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) \\ P_{con(V_o=+3V_{dc})} &= 3\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) \\ P_{con(V_o=-1V_{dc})} &= 2\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) \\ &\quad + 1\left(V_{D\_on} * i_{D\_avg} + R_{D\_on} * i^2_{D\_rms}\right) \\ P_{con(V_o=-2V_{dc})} &= 3\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) \\ P_{con(V_o=-3V_{dc})} &= 3\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) \end{aligned} \tag{10}$$

Because the number of switches and diodes in conduction varies with output voltage level, conduction losses are estimated independently for each voltage level. Three switches are in conduction at $+3V_{dc}$ and $+2V_{dc}$ levels. At $+1V_{dc}$, two switches and one diode are in conduction. As illustrated in equation (10), the process is repeated for the negative cycle of the output voltage. The total conduction losses are obtained by adding the conduction losses at each level as shown in equation (11).

$$\begin{aligned} P_{con(Total)} &= P_{con(V_o=+1V_{dc})} + P_{con(V_o=+2V_{dc})} \\ &\quad + P_{con(V_o=+3V_{dc})} + P_{con(V_o=-1V_{dc})} \\ &\quad + P_{con(V_o=-2V_{dc})} + P_{con(V_o=-3V_{dc})} \end{aligned} \tag{11}$$

The overall efficiency of the multilevel inverter is given from equations (12) and (13)

$$\text{Efficiency } \eta = \left(\frac{P_{input} - P_{losses}}{P_{input}}\right) * 100 \tag{12}$$

$$\eta = \left(\frac{V_{dc} * I_{dc} - P_{con(Total)} - P_{SL(Total)}}{V_{dc} * I_{dc}}\right) * 100 \tag{13}$$

where, η is efficiency of the topology, V_{dc} & I_{dc} are input DC voltage and current respectively, $P_{con(total)}$ and $P_{SL(total)}$ are total conduction and switching losses respectively of all switches.

V. PROPOSED GENERALIZED TOPOLOGY

In the grid integration of renewable energy applications, it is required to have a high gain inverter to match the grid voltage since the voltage generated by the renewable sources is of low value. Therefore, the above proposed 7-level topology can be extended to any number of levels by connecting the red colored 3 components (two switches and one capacitor) additionally as shown in Figure 10. For a (2N+1) level topology (where N is the gain),

$$\text{Number of switches} = 2N + 2 \tag{14}$$

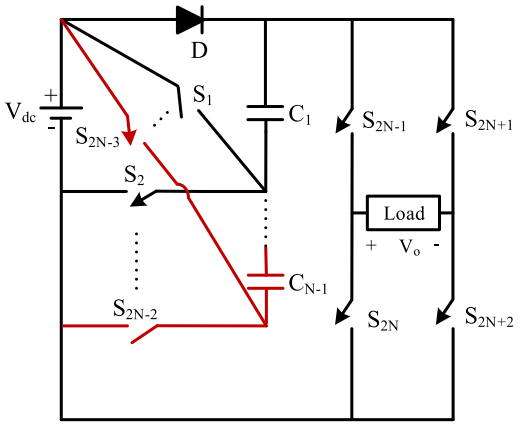

FIGURE 10. Proposed generalized topology.

$$\text{Number of capacitors} = \text{N-1} \quad (15)$$

$$\text{Maximum voltage stress on H-bridge} = NV_{dc} \quad (16)$$

$$\text{Maximum voltage stress on the diode} = (\text{N-1})V_{dc} \quad (17)$$

There is a need of only one separate diode and two series diodes for the topology having any number of levels. Among the switches from S_1 to S_{2N-2}, two switches have the MBV of V_{dc}, two switches have the MBV of $2V_{dc}$, two switches have the MBV of $3V_{dc}$ and so on.

$$TSV = (N^2 + 4N - 1) * V_{dc} \quad (18)$$

All the capacitors can be well balanced at V_{dc} by properly selecting the charging and discharging paths in each cycle of output voltage.

VI. COMPARISON WITH OTHER TOPOLOGIES

The proposed seven-level triple boost switched capacitor inverter is compared with other seven-level topologies in the literature, as shown in table 2, in terms of number of switches, number of series/separate diodes, number of capacitors, number of sources, number of driver circuits, number of switches in charging circuit, gain, $TSV_{p.u}$, MBV, and cost factor (CF). The formula used in finding the cost factor is given in equation (14).

$$CF = N_{sw} + N_{sd} + N_c + N_s + N_{dr} + \alpha TSV_{p.u.} \quad (19)$$

where α is the weight factor and its value depends on the weightage given to switching components and $TSV_{p.u.}$ If $\alpha > 1$, more weightage is given to $TSV_{p.u}$, if $\alpha < 1$, more weightage is given to the switching components. Equal weightage is given to both switching components and $TSV_{p.u}$ in the proposed topology, therefore, α is taken as 1.

The topology in [23] has a smaller number of switches, and driver circuits than the proposed topology, however, it has a gain of 1.5 only. The topology in [22] has one capacitor less than the proposed topology, but it has a gain of only 1.5. The switches in the charging circuit have more losses than other switches, therefore, number of switches in the charging circuit is one of the parameters to be considered for comparison analysis. It is worth mentioning that the number

TABLE 2. Comparison of the proposed topology with other 7-level topologies.

T	N_{sw}	N_{dr}	N_d	N_c	N_{ch}	G	$TSV_{(p.u)}$	CF
[6]	16	16	0	2	8	3	5.3	40.3
[7]	9	9	1	2	5	3	6	28
[8]	12	12	0	2	8	3	5.3	32.3
[9]	12	12	2	3	6	3	7.67	37.6
[10]	10	10	4	2	4	3	6	33
[11]	11	11	1	4	5	3	7	35
[12]	12	11	0	2	8	3	5.3	31.3
[13]	11	10	0	3	9	3	6	31
[14]	9	9	4	2	5	3	5.66	30.6
[16]	10	8	0	2	4	1.5	5.3	26.3
[17]	10	8	0	2	4	1.5	6	27
[20]	10	8	0	3	4	1.5	5.3	27.3
[22]	9	9	0	1	4	1.5	4.66	26
[23]	7	7	2	2	5	1.5	5	24
[24]	10	8	0	4	4	1.5	6	29
[P]	8	8	1	2	3	3	6.66	26.6

T=Topology, N_{sw}= number of switches, N_d = number of diodes, N_c = number of capacitors, N_{dr} = number of gate driver circuits, G=gain, N_{ch} = number of switches in charging circuit.

TABLE 3. Comparison of proposed generalized MLI topology with other 2N+1 level topologies.

T	N_{sw}	N_d	N_c	N_{dr}	G	N_{total}
[28]	2N+2	N	N	2N+2	N	4N+2
[29]	5N-1	0	N-1	5N-1	N	6N-2
[30]	3N+5	0	N	2.5N+4	N	4N+5
[31]	4N+2	N+1	N	4N+2	N	6N+3
[32]	3N+9	0	0.5N-1	3N+8	N/2	4N+7
[33]	4N	0	N-1	4N	N	5N-1
[34]	2N+2	N-1	N-1	2N+2	N	4N
[P]	2N+2	1	N-1	2N+2	N	3N+2

$N_{total} = N_{sw} + N_d + N_c$.

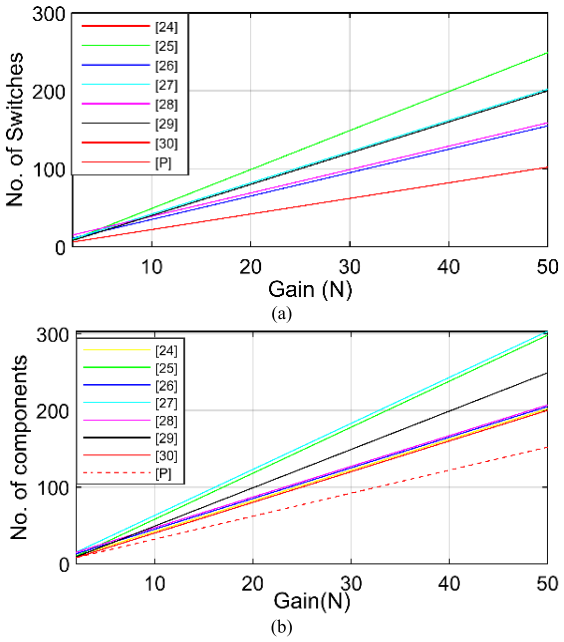

FIGURE 11. Comparison plots with other generalized topologies (a) No. of switches (b) No. of components.

of switches in the proposed topology has least number of switches in charging circuit compared to all other topologies. The TSVp.u of the proposed topology is nearer to the average

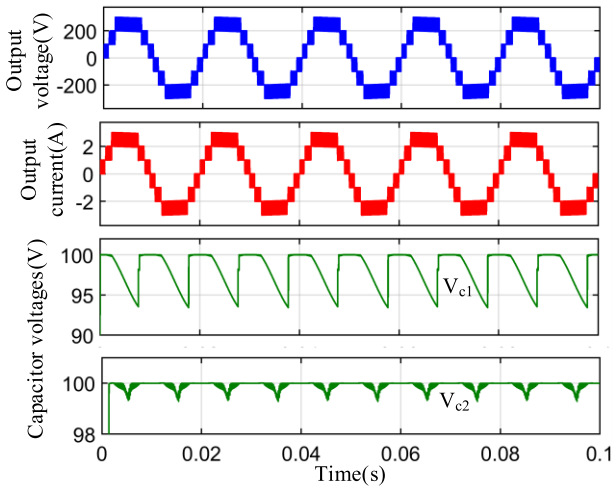

FIGURE 12. Output voltage, current and capacitor voltages for R load.

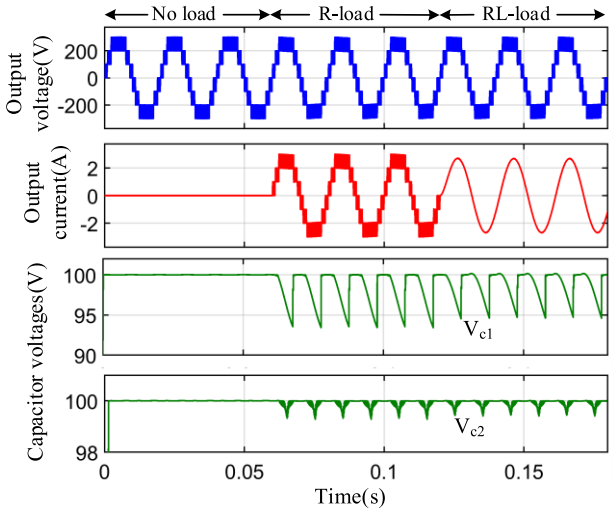

FIGURE 13. Output voltage, current and capacitor voltage at different load conditions.

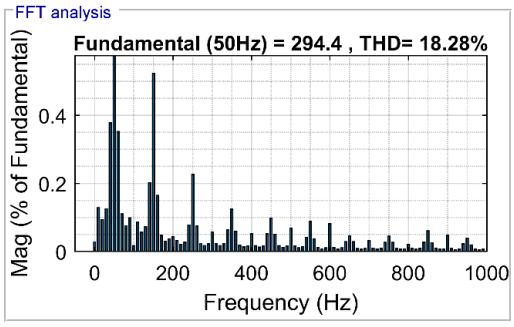

FIGURE 14. THD of output voltage at $m_a = 1$ with RL load.

TSV of all the topologies. It can be observed that the CF of the proposed topology is much lower compared to all the topologies having gain of 3. The topologies [16], [18], [22], [23] in the table have less CF than the proposed topology, however. These have a boosting ratio of 1:1.5 only.

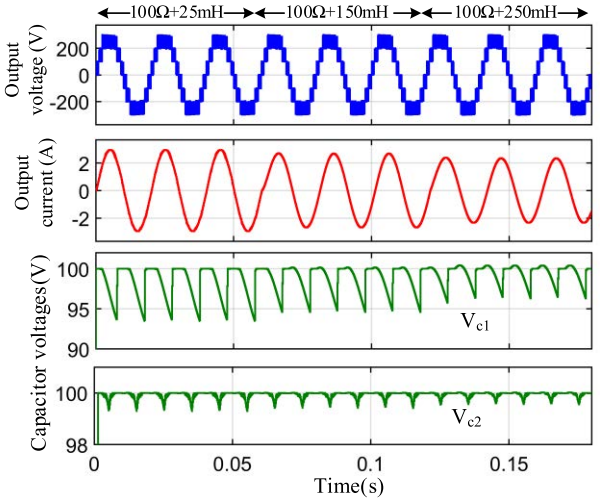

FIGURE 15. Output voltage and current at different RL loads.

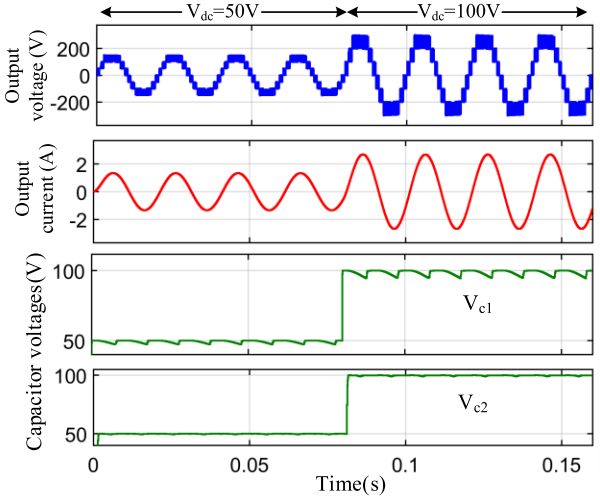

FIGURE 16. Output voltage, current and capacitor voltage with change in supply voltage.

The proposed generalized N gain, 2N+1 level topology is compared with other 2N+1 level topologies in the literature, as shown in table 3. It can be observed that the proposed topology has least number of switches, as in [28], [34] than the other topologies, however, the total number of components in these topologies is more than the proposed topology. The proposed topology uses only one diode for any number of levels. The comparison of the proposed topology with other generalized topologies in terms of number of switches and components is shown in Figure 11.

VII. RESULTS AND DISCUSSION

A. SIMULATION RESULTS

The proposed 7-level triple boost switched capacitor inverter is simulated using the MATLAB/Simulink with different parameter variations. The values of the DC supply and load are taken as $V_{dc} = 100V$, $R = 100\Omega$ and $L = 150mH$. Figure 12 shows the output voltage, current, and capacitor

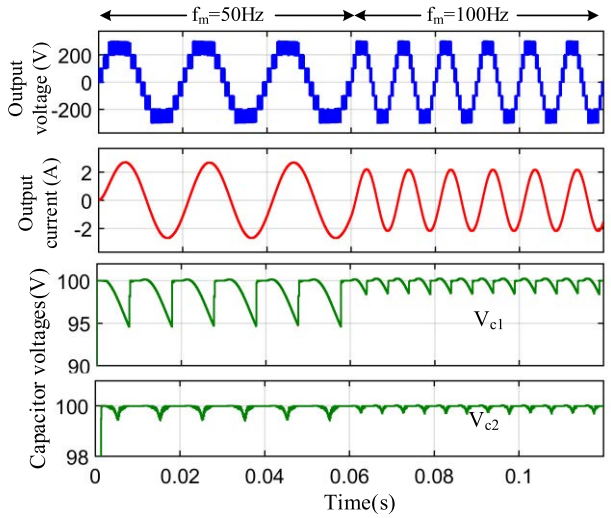

FIGURE 17. Output voltage, current with change in modulating frequency.

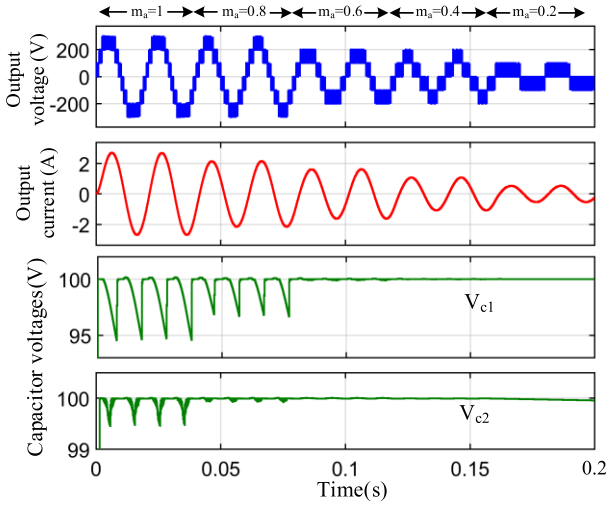

FIGURE 18. Output voltage, current with change in modulation index.

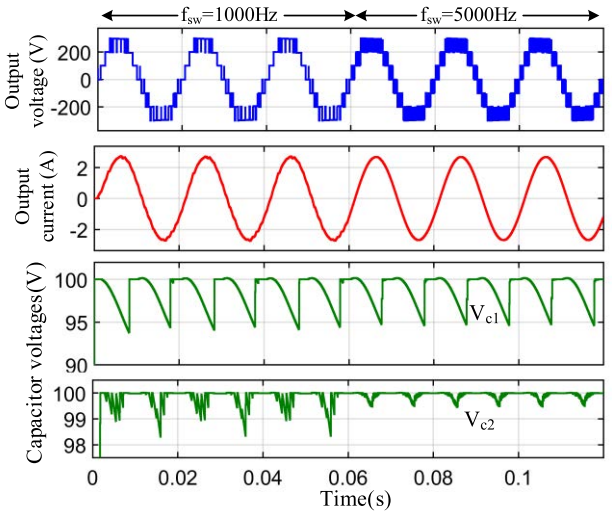

FIGURE 19. Output voltage, current with change in switching frequency.

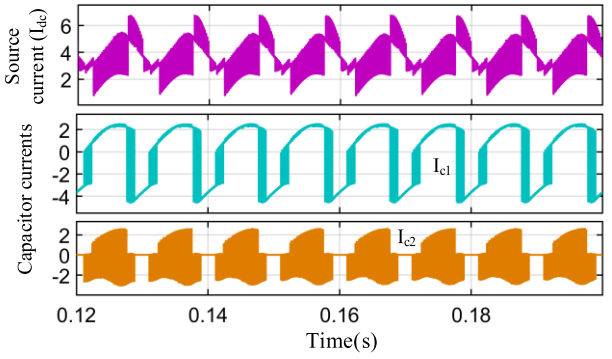

FIGURE 20. Source and capacitor currents.

TABLE 4. THD analysis with change in modulation index.

m_a	Peak of fundamental(V)	THD (%)
1	294.4	18.28
0.8	236.4	24.36
0.6	178.7	33.27
0.4	119.8	44.32
0.2	59.98	105.96

voltages for resistive load. The ripple in V_{c1} is more than the ripple in V_{c2} since the capacitor C_1 discharges in both $2V_{dc}$ and $3V_{dc}$ levels, but capacitor C_2 discharges only in $3V_{dc}$ level. The output voltage, output current and capacitors voltage waveforms at different load conditions is shown in Figure 13. It can be observed that the voltage across the capacitors is well balanced at 100V with all load variations and the ripple in capacitor voltages with RL load is less than the R load. The value of THD for the output voltage waveform is 18.28% with RL load at a modulation index of $m_a = 1$, as shown in Figure 14. The peak of the fundamental is observed to be 294.4V. Figure 15 shows the output voltage, current and capacitor voltage waveforms with the variation of load inductance. It is seen that the value of output current decreases with increase in load inductance value. It is also observed that the ripple voltage decreases with increase in inductive load. The output voltage, current and capacitor voltage waveforms with the variation of supply voltage from 50V to 100V is shown in Figure 16. The sudden jump in capacitor voltage from 50V to 100V can be seen in the same figure. Figure 17 shows the change in output voltage, current and voltages across the capacitors with the variation of modulating frequency from 50Hz to 100Hz. It can be observed that the load current decreases as the modulating frequency increases, which increases the value of inductance in the load. As the modulating frequency increases, the pulse width decreases, therefore, the discharging period decreases which gives the less ripple voltage in capacitors. The variation of output voltage, current and capacitor voltage waveforms with change in modulation index is shown in Figure 18. As the modulation index decreases from 1 to 0.8, the width of the $2V_{dc}$ level decreases and the width of the V_{dc} level increases.

The change of modulation index from 0.8 to 0.6 generates only a 5-level waveform since the modulating wave is

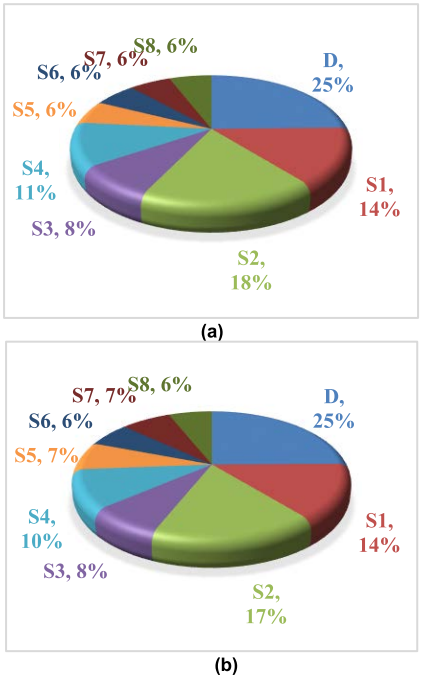

FIGURE 21. Total losses in switches at (a)100Ω, (b)100Ω+150mH.

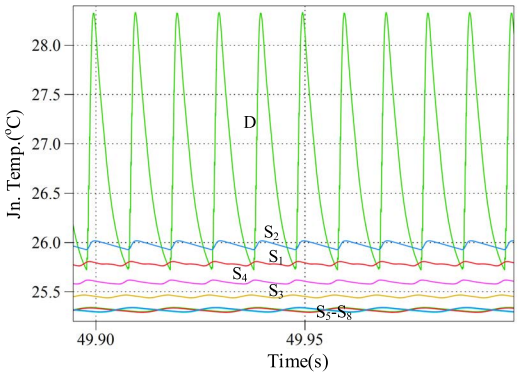

FIGURE 22. Junction temperatures of all the switches at R=100Ω load.

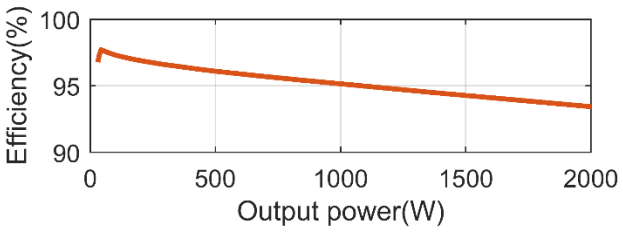

FIGURE 23. Efficiency curve vs output power.

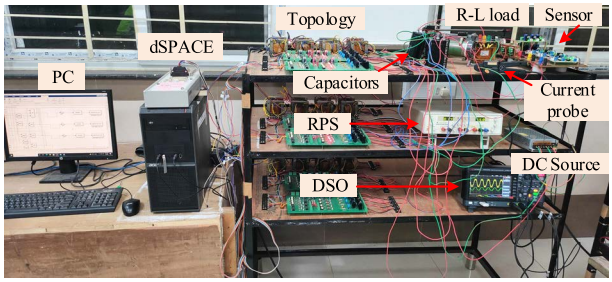

FIGURE 24. Hardware prototype in the laboratory.

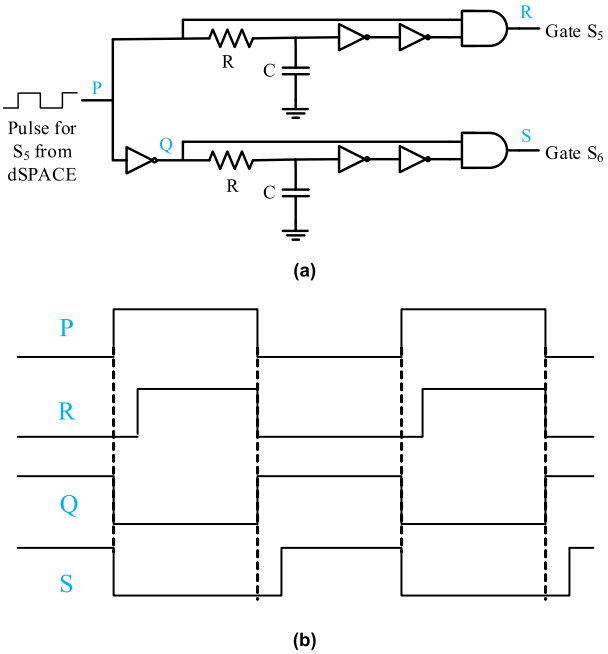

FIGURE 25. (a) Dead band circuit (b) Signals at nodes P,Q,R and S.

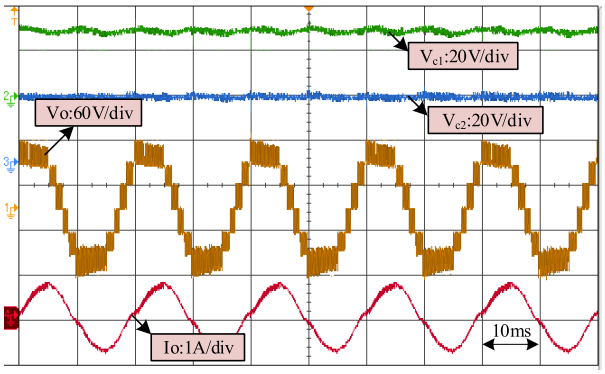

FIGURE 26. Output voltage and current for RL load.

compared with the 4 triangular carriers, and the change of modulation index from 0.4 to 0.2 generates only a 3-level waveform since the modulating wave is compared with the 2 triangular carriers. As the modulation index decreases, the peak of the fundamental waveform also decreases and the value of THD increases, as shown in table 4. In electric drive applications, the voltage output of the converter is to be reduced to decrease the speed of the motor. When the output voltage has 5 levels, only capacitor C_1 discharges and C_2 will not discharge. Similarly, when the topology is generating only 3 levels, both C_1 and C_2 will not discharge, therefore, no ripples can be seen. The variation of switching frequency from 1000Hz to 5000Hz can be seen in Figure 19. It can be observed that the current waveform is smooth with high switching frequency. The ripple voltage is seen to be less with high switching frequency as is charges and discharges so

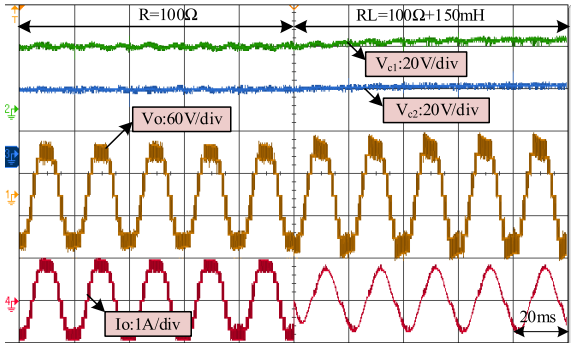

FIGURE 27. Output voltage and current from R to RL load.

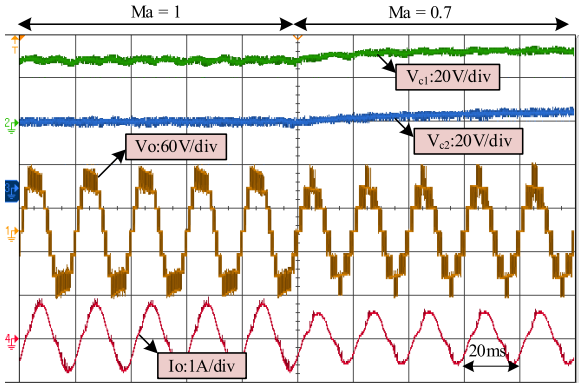

FIGURE 28. Output voltage and current with change in modulation index from $m_a = 1$ to $m_a = 0.7$.

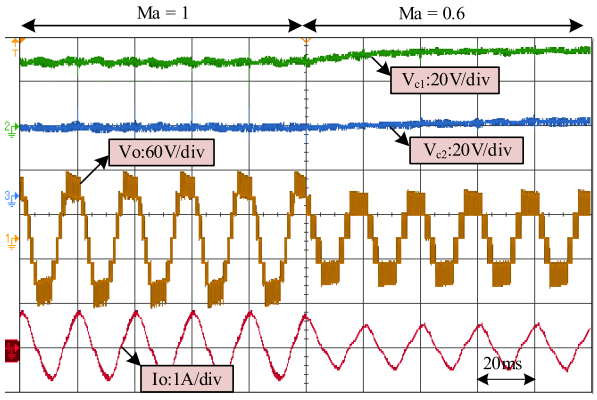

FIGURE 29. Output voltage and current with change in modulation index from $m_a = 1$ to $m_a = 0.6$.

frequently. Figure 20 shows the waveforms of source current and capacitor currents.

B. THERMAL MODELLING

The thermal modelling of the switches in the topology is done in PLECS software. The percentage of total losses switches and diode at a load of 100Ω and 100Ω+150mH is shown in Figure 21(a) and (b) respectively. It can be seen that the losses in diode and switch S_2 are more compared to other switches as these are associated with charging circuit. The junction temperatures of all the switches at R load are observed and

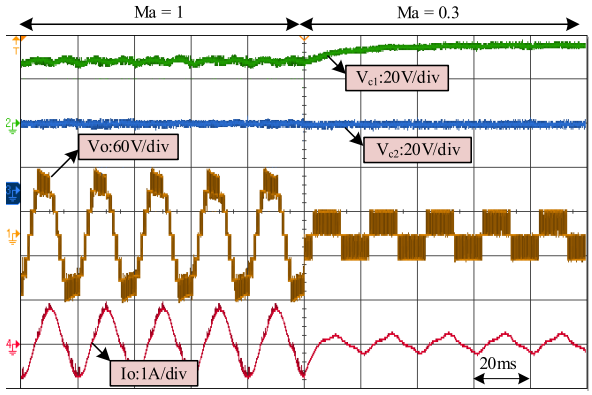

FIGURE 30. Output voltage and current with change in modulation index from $m_a = 1$ to $m_a = 0.3$.

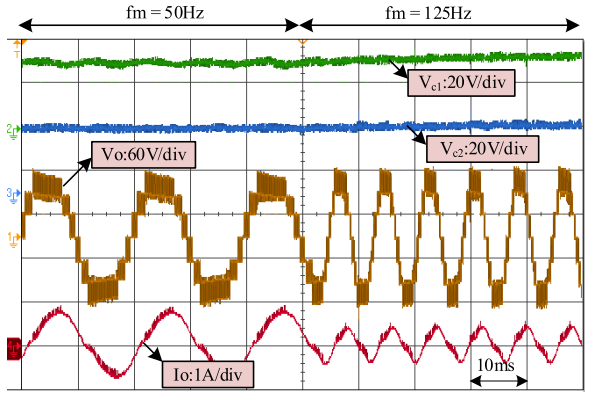

FIGURE 31. Output voltage and current with change in modulating frequency from $f_m = 50$Hz to 125Hz.

found to be around 26°C, plotted in Figure 22. The efficiency is calculated by considering only R loads and is plotted against the output power (0-2KW). It has an efficiency in range of 97.63% to 93.2% as shown in Fig. 23. As the load increases, the efficiency decreases. This is because with the increase in load, the conduction losses increase, which intern increase the temperatures, so, the decrease in efficiency is observed.

C. HARDWARE RESULTS

The proposed seven-level inverter is verified by an experimental prototype as shown in Figure 24. The pulses to the switches in the inverter are generated using dSPACE1104. The values of the components used in the hardware are: DC source = 30V, Capacitor = 2200μF, Switches=IRFP460, Power diode=MUR860, R-load=100Ω and L-load = 150mH. Further, a small value of inductor (10μH) is connected in the charging path to suppress the current spike in the capacitors. The dead band is created for the gate signals of the two switches in the H-bridge. The circuit used for the creation of dead band is shown in Figure 25(a). The signals at different points in the circuit are shown in Figure 25(b). It is clearly seen that the signals R and S have dead band between them to avoid the short circuit of the DC source. The

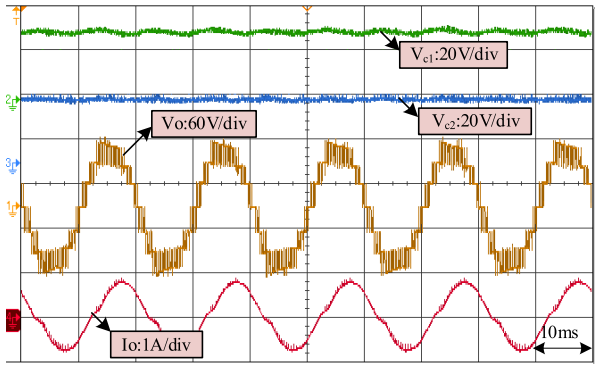

FIGURE 32. Output voltage and current with switching frequency of 2.5kHz.

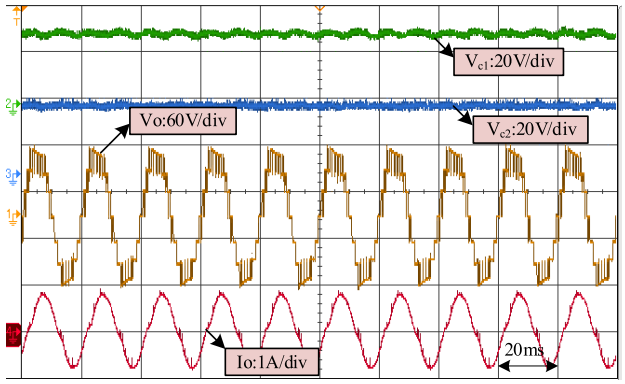

FIGURE 33. Output voltage and current with switching frequency of 1kHz.

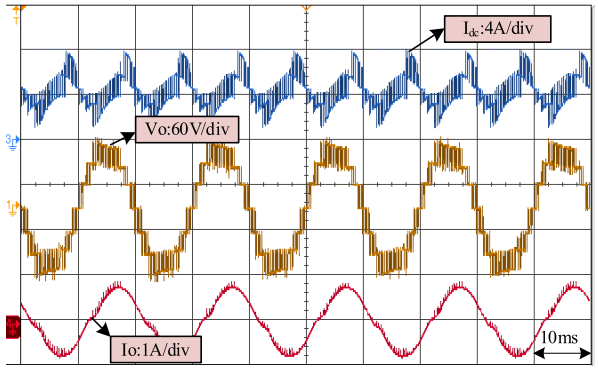

FIGURE 34. Source current, output voltage and current.

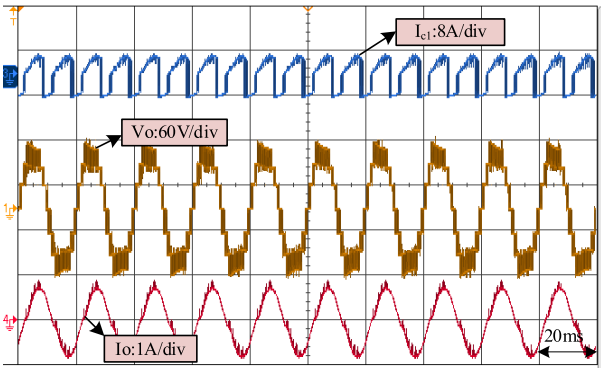

FIGURE 35. Current in capacitor C_1, output voltage and current.

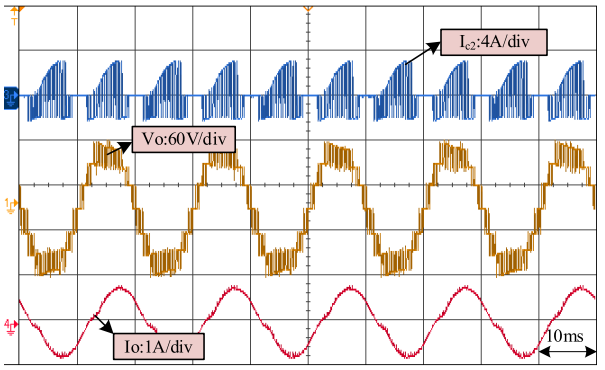

FIGURE 36. Current in capacitor C_2, output voltage and current.

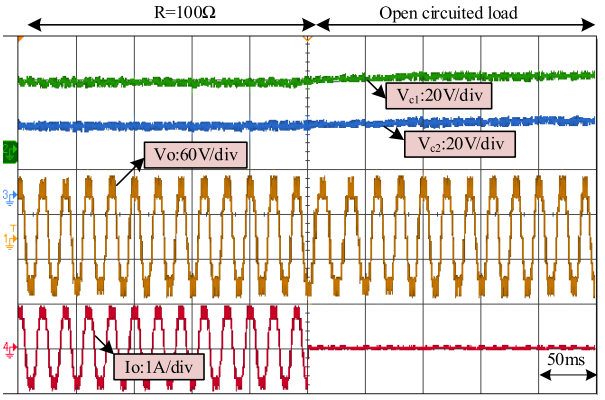

FIGURE 37. Capacitor voltages, output voltage and current under fault condition.

output voltage, current and capacitors voltage waveforms for RL load are shown in Figure 26. It can be observed that the current waveform is lagging to the voltage waveform. The change of transition in current waveform from R to RL load can be seen in Figure 27. The capacitor voltages seen to be raised due to the addition of inductance in the load. The effect of change in modulation index on output voltage and current can be observed in Figures 28, 29 and 30. In Figure 31, the modulating frequency is changed from 50Hz to 125Hz. Therefore, this proposed topology can work effectively with higher frequencies. Figure 32 and 33 show the output voltage and current waveforms with a switching frequency of 2.5kHz and 1kHz respectively. The current drawn from the DC source and the currents flowing through the capacitors C_1 and C_2 are shown in Figures 34, 35 and 36 respectively, which resembles the waveforms obtained in simulation. When the load is suddenly opened, the current becomes zero, however, the voltage remains same which is shown in Figure 37. When the open circuit fault occurs at load, the capacitors don't have path to discharge, therefore, the voltage across the capacitors will rise to the source voltage.

VIII. CONCLUSION

A new seven-level triple boost inverter based on switched capacitor technique is proposed in this paper. This topology

has an ability of self-balancing of voltage across the capacitors. This topology is simulated in MATLAB/Simulink with the variations in load parameters, supply voltage, modulation index, modulating frequency and switching frequency. It can be inferred that the proposed topology can work with all types of loads. This proposed topology is compared with existing seven-level topologies in the literature to know its better features. It can be concluded that the proposed topology has least number of switches and components with a reasonable TSVp.u. Further, it is also extended to 2N+1 level topology. The efficiency of this topology is also calculated by calculating the conduction and switching losses of the switches using the PLECS software. The maximum efficiency of 97.63% is observed. Finally, the effectiveness of the proposed topology is tested on hardware prototype and the results are presented.

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