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RESEARCH ARTICLE

Three Phase Four Switch Inverter Based DVR for Power Quality Improvement With Optimized CSA Approach

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ABSTRACT Industries driven by electric power require controlled and improved power quality for the optimal exploitation of resources. However, certain crucial issues greatly influence power quality, causing monetary losses to both the utility and customers. Numerous custom power devices are available to compensate for power quality issues; however, these devices alter the parameters of the transmission and distribution systems. Hence, a dynamic voltage restorer (DVR) is adopted in this study, which mitigates voltage disorders by establishing the desired quality and voltage level demanded by any sensitive load. The DVR adopts a 3ϕ four-switch voltage-source inverter (VSI) that acts as a cost-effective solution with a reduced number of switches. The cuckoo search algorithm (CSA) was utilized in this study as it solves multiple optimization issues with ease of implementation. Because it is robust to variations in the system, it significantly aids in enhancing the efficiency of the DVR by compensating for the variations in voltage and minimizing the total harmonic distortion (THD). The entire work was verified in MATLAB/Simulink to demonstrate the effectiveness of the introduced technique in smoothing the distorted voltage. The proposed approach achieved an efficiency of 92.6% witha simulation THD of 2.8% and hardware THD of 2.95%.

INDEX TERMS DVR, CSA, power quality, voltage swell, injection transformer, voltage sag.

I. INTRODUCTION

In distribution systems, the necessity for power quality enhancement has shown an increase in improving the economic and technical growth of power sectors with high efficiency. A continuous power supply is essential for improving the cumulative performance of the power system, as it contributes a crucial part in distributing power to utilities and domestic consumers. Hence, the power supply must be constantly provided without interruptions to meet customer demands. However, in distribution systems, the occurrence of various disturbances diminishes power supply quality; therefore, it is essential to eliminate these disturbances. The use of converter-based equipment and non-linear loads has initiated the occurrence of disturbances in power quality (PQ), such as voltage sags and swells, transients, interruptions, voltage fluctuations, and harmonics, which have severe impacts on the power distribution system. Because these issues affect the power supply over a wider range, the mitigation of these issues is crucial [1]. Moreover, the service continuity of the power system is perturbed by these issues, resulting in equipment breakdown and economic loss. In power systems, PQ issues have caused several disadvantageous impacts such as low efficiency, reduced life span of equipment, high maintenance costs, interruption in production, and high energy losses [2]–[5]. Thus, it is mandatory to accurately identify the nature of the PQ problem to resolve these issues using eminent solutions. However, it is very difficult to eliminate PQ problems in complicated power systems [6]. Hence, various devices are used to eliminate PQ problems with high robustness.

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In electric power distribution networks, voltage imbalance is regarded as a frequently encountered power quality issue [7]–[10]. To eliminate this issue, several processes like phase rearrangement and balancing among particular medium voltage feeders, the configuration of distribution line and radial arrangement based power distribution energy converter banks are suggested, which assist in rectifying the voltage variation. Despite their advantageous impacts, these approaches have delivered less effective outcomes in eliminating voltage fluctuations. In addition, these processes concentrate on medium-voltage distribution systems and fail to satisfy the requirements of high-power systems. Hence, regulated or manual feeder switching control is employed with numerous problem-solving algorithms to obtain optimal results. However, it is insufficient for completely solving the voltage imbalance because it fails to balance the system load [11]–[13].

The use of fixed and switch capacitors/reactors has gained considerable attention in certain periods of time to mitigate PQ issues. Despite their numerous beneficial effects, these devices have disadvantages such as additional losses, large size, slow response time, and inadequate bandwidth [14]–[19]. Hence, two-level converters were implemented to compensate for the reduced power distribution systems. This is because the high-frequency functioning of two-level converters causes switching loss and restricted power rating [20], other devices [21]–[23], shunt [24]–[26], and hybrid active power filters [27]–[29] are implemented. The shunt active power filters (APFs) are linked in parallel to the non-linear loads, whereas the series APF are located within the load and utility grid to compensate for the load reactive power, harmonic currents, and load imbalances [30]. Although the current harmonics are mitigated by these filters, voltage fluctuations remain unresolved. Then, the PI controller is employed to control these filters to improve the transient response, but it fails to compensate for unbalanced voltage sags. [31]. Thus, adaptive self-tuned PI controllers are used to compensate for voltage sags. However, the load voltage outputs of these controllers exhibit slow transient responses [32], [33].

In consideration of the aforementioned issues, FACTS devices such as static volt-amps reactive (VAR) compensators (SVC) and static synchronous compensators (STATCOM) are utilized to mitigate PQ issues. Among various FACTS devices, the DVR plays a crucial role in addressing issues such as voltage swells, sags, harmonics, interruptions, and flickers, as it safeguards the loads from tripping losses [34]–[39]. As the DVR has no storage elements, energy is either attained directly from the major source or from storage elements such as external storage devices, self-storage capacitors, and super magnetic energy storage [40], [41]. The DVR performs the injection of a specific voltage and phase angle in series with a distribution line to generate a load voltage [42]. In addition, the DVR can operate in several compensation modes, such as in-phase mode [43], pre-sag mode [44], energy optimized mode [45], and self-supported mode [46]. A superconducting magnetic storage energy-based DVR using d-q transform control performs well in the mitigation of voltage quality disturbances as it compensates for the transient voltage waveform. However, this approach faces a short-time overvoltage disturbance, which is regarded as a major drawback [47]. Then, an approach is designed for improving low-voltage distribution systems, in which the DVR is utilized as a continuous voltage compensator to prevent voltage and overvoltage issues. This approach requires high investment in the energy-storage setup, which results in an increase in the overall system cost [48]. A multilevel DVR was implemented to compensate for the power quality of the sensitive loads. It generates increased voltage levels for each converter leg using an appropriate pulse-width modulation (PWM) strategy. However, this approach requires current controllers and sensors to compensate for common-mode current [49]–[54]. Hence, a feedback-control-based DVR was implemented to rectify the voltage disturbances. Although it aids in minimizing the occurrence of voltage quality issues, it is not applicable to high-power transmission systems [55]. Another approach based on the smart branch controller was adopted to compensate for various disturbances in the power quality. The elimination of harmonics is performed without any filter, but the smart branch controller generates nonlinearity in the circuit [56]–[60]. Fuzzy logic-based compensation is also adopted to improve the power quality; however, the validation requires extensive testing with a hardware setup [61]. Artificial neural networks (ANN) are also deployed to reduce power quality issues but demand processors with parallel processing power [62]. Thus, a CSA based DVR was implemented in the present study to rectify all the specified issues. When considering the convergence speed, CSA outperformed other algorithms and was found to be computationally efficient [63]. It also has the ability to reduce real power losses by maintaining the voltage fluctuations within an acceptable level. Hence, CSA is adopted in this approach to solve optimization issues.

A novel methodology using a CSA-based DVR was introduced to augment the power quality of the distribution system. The DVR circuit effectively mitigates power quality issues by compensating for the voltage swell and sag. Because the DVR is a device for energy compensation, it controls the flow of active energy in the distribution system to generate an improved power factor. The CSA is adopted to tune the parameters of the PI controller, which in turn generates optimized outputs. These outputs are fed to the PWM generator, which generates corresponding pulses to be applied to a cost effective3ϕ 4-switch VSI with reduced switching losses.

The entire setup is less complicated and generates a stable output with an improved power quality.

Section II of this paper includes the modeling of the DVR, its operating modes, and the modeling of the control algorithm. Section III presents the hardware and simulation outcomes obtained using this approach. Finally, Section IV

summarizes the paper, with proper validation. The proposed approach reduced the transient overshoot and tracking errors of the system.

II. PROPOSED CONTROL FOR DVR SYSTEM

The hybrid power distribution system is shown in Fig. 1. As PQ issues have severe impacts on the distribution system, numerous approaches have been utilized to rectify these issues. In the mitigation of PQ problems, DVR plays a significant role, as it effectively eliminates these issues. The ultimate goal of DVR in a distribution system is to efficiently compensate for voltage swells and sags. In addition, it assists in events such as fault-current restriction, transient-voltage reduction, and compensation of line-voltage harmonics. In the proposed approach, DVR is utilized with CSA to improve the power quality of the system. The proposed approach generated improved results under both transient and steady-state conditions. A block illustration of the proposed methodology is shown in Figure 1.

The DVR continuously generates reactive power, which is injected into the transmission line. The injected voltage was supplied by an injection transformer to the distribution system. The inverter functioning of the DVR is controlled by a PI controller, which is the simplest and most well-known control approach. The tuning of the controller parameters is performed by the CSA, which aids in generating optimized results. The control signals generated by the PI controller are converted to pulses by a PWM generator for the operation of a 3ϕ 4-switch VSI. Finally, a stable output was generated and fed to the load.

A. DYNAMIC VOLTAGE RESTORER

Fig. 2 shows the equivalent circuit of the DVR. It comprises a control unit and a power circuit. An injection transformer was used to connect the DVR with the distribution system. If the control circuit detects any voltage sag, then the injected voltage obtained by the VSI is coupled with the supply voltage. The voltage supplied by the filtered VSI was increased to the desired level by the injection transformer. The injection transformer also offers isolation between the distribution system and the DVR. The storage element is used in this system to supply DC voltage to the VSI, and the inverter converts this voltage into a sinusoidal voltage with an appropriate phase angle, frequency, and magnitude. The real power required by the DVR during sag compensation is provided by the energy storage device and DC link. The DC voltage required was obtained from the topology with energy storage to compensate for the load voltage under sag conditions.

The DC energy-storage element supplies the DC voltage, which is converted into a sinusoidal voltage of the required frequency, phase angle, and magnitude by the VSI. The harmonic filter in the VSI was utilized to mitigate harmonics. A harmonic filter is utilized for damping the switching harmonics, which aids in maintaining the harmonic content within an acceptable level. The VSI is controlled by the PWM

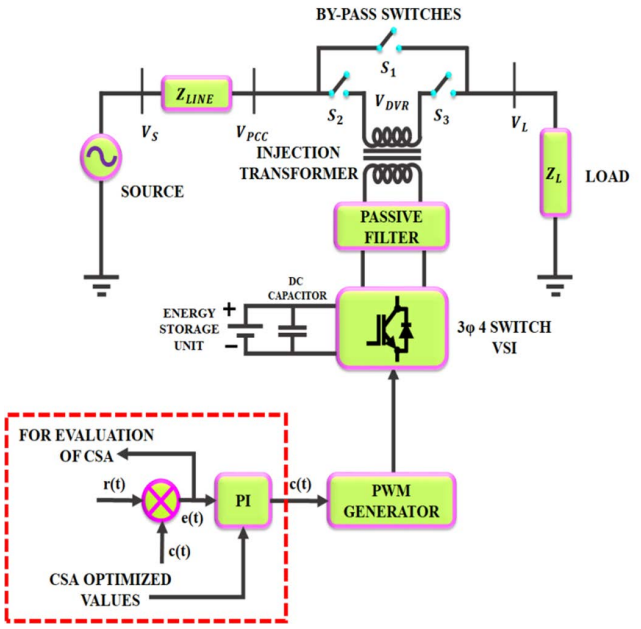


FIGURE 1. Block representation of the methodology proposed.

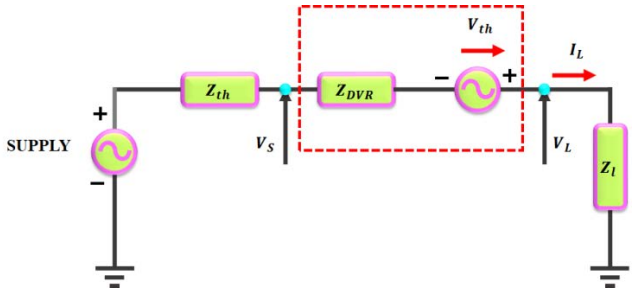


FIGURE 2. Equivalent Circuit of DVR.

technique; normally, the switching harmonics are centered at the switching frequency and its multiples if the value of the modulation index is less than 1. Harmonic filters are inserted in the low or high-voltage side of the injection transformer, and bypass switches are used to provide an alternate path to ensure the flow of load current, which prevents the system from overload, maintenance, and fault conditions. These switches assist the DVR in preventing interference with the existing protection equipment and protecting the device during the short circuit.

The corresponding equivalent equation is given as,

$$V_D = V_l + Z_{th}I_l - V_{th} \tag{1}$$

where V_l indicates the voltage of the load, Z_{th} is the impedance of the system, I_l is the current through the load, and V_{th} is the voltage across the system.

The current through the load I_l is expressed as,

$$I_l = \frac{P_l + jQ_l}{V_l} \tag{2}$$

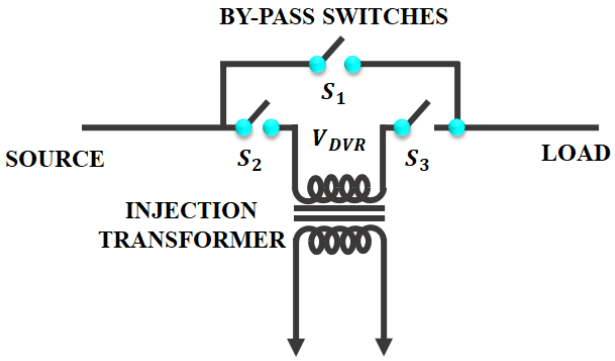


FIGURE 3. Operating mode of DVR.

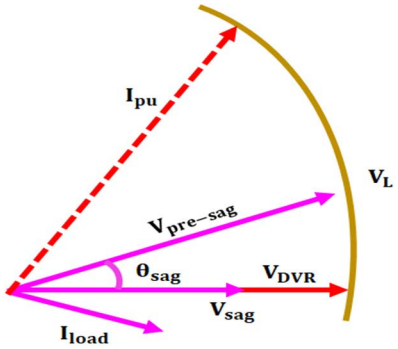


FIGURE 4. In-phase compensation.

The reference equation is given as,

$$V_D\angle\propto = V_l\angle 0 + Z_{th}I_l\angle(\beta-\theta) + V_{th}\angle\delta \tag{3}$$

Here, the angle of V_{th} is specified as δ whereas the angle of Z_{th} is specified as β.

The load power angle is expressed as,

$$\theta = tan^{-1}\frac{Q_l}{P_l} \tag{4}$$

where, Q_l indicates the load reactive power, P_l indicates the load active power.

1) OPERATING MODES

The operating modes of the DVR are explained in the equivalent circuit diagram shown in Fig. 3.

a: PROTECTION MODE

During the short-circuit condition of the load, a high load current and inrush current occur in the DVR. Hence, the DVR is isolated from the distribution system during fault conditions by utilizing bypass switches denoted by S_2, S_3, which are open. It generates an alternate load current path using the closed condition of switch S_1.

b: MODE STANDBY MODE ($V_D = 0$)

In this mode, the DVR performs a short-circuit operation or injects less voltage to minimize the losses or voltage drop across the transformer reactance. Usually, this standby mode of operation of a DVR is widely preferred. The injected voltage of the DVR is represented as V_D.

c: INJECTION MODE ($V_D > 0$)

The DVR operates in injection mode when voltage sag is detected. To perform compensation, an AC voltage of the desired wave shape, phase, and magnitude was injected in series with the distribution system. where V_D is the injected voltage of the DVR.

2) VOLTAGE COMPENSATION APPROACHES

The utilized approaches of the voltage compensation using DVR are explained as follows.

a: IN-PHASE COMPENSATION APPROACH

In this approach, the in-phase voltage is injected into the supply voltage with the assistance of the DVR. During the application of linear loads, this in-phase compensation is utilized because it only requires the voltage magnitude for compensation. As the injected voltage was low, the DC link voltage rating was minimal. Hence, real power is required for voltage compensation. In addition, the phase angle jump was not restored. The corresponding equations are as follows:

$$V_D = V_{injec}. \tag{5}$$

$$|V_{injec}| = |V_{pre}| - |V_{sag}| \tag{6}$$

$$\angle V_{injec} = \theta_{injec} = \theta_s \tag{7}$$

The working of this approach is highlighted in Fig. 4.

Where, V_D represents the voltage of DVR, V_{injec} denotes the injected voltage, V_{pre} represents the magnitude of voltage before sag, V_{sag} represents the magnitude of voltage after sag and $\angle V_{injec} = \theta_{injec}$ represents the angle of injected DVR voltage.

b: PRE-SAG COMPENSATION APPROACH.

This approach continuously tracks the supply voltage to detect voltage disturbances with the generation and injection of different voltages. In this approach, the load phasor voltage is maintained without variation, and the sensitive voltage is restored to the same magnitude and phase angle. It is used for nonlinear loads and is influenced by changes in the phase angle. The operation of this approach is illustrated in Fig. 5.

The corresponding equations are given by,

$$V_{pre} = V_l, V_{sag} = V_s, V_D = V_{injec} \tag{8}$$

$$|V_{injec}| = |V_{pre}| - |V_{sag}| \tag{9}$$

$$\theta_{injec} = tan^{-1}\left\{\frac{V_{pre}sin(\theta_{pre})}{V_{pre}cos(\theta_{pre}) - V_{sag}cos(\theta_{sag})}\right\} \tag{10}$$

where θ_{pre} represents the angle before sag and θ_{sag} represents the angle during sag.

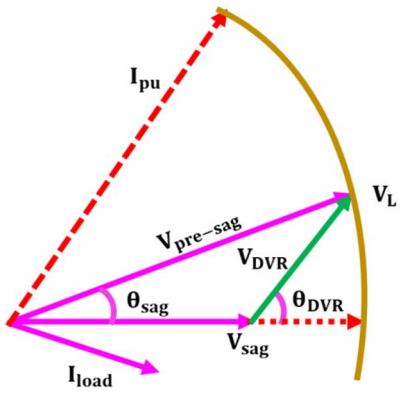


FIGURE 5. Pre-sag compensation.

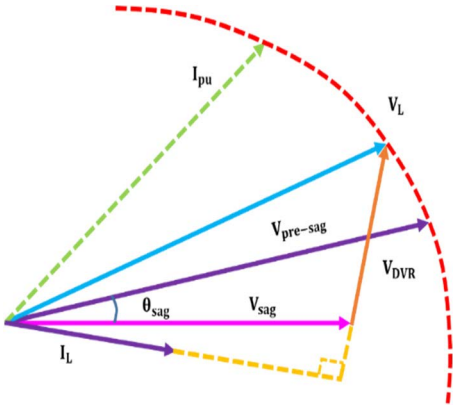


FIGURE 6. In-phase advanced compensation approach.

The phase-angle variation and voltage sag were restored. In addition, the transient current or circulating current at the load side was avoided. This approach requires real power for the compensation.

c: ADVANCED IN THE PHASE COMPENSATION APPROACH

As shown in Fig. 6, the injected voltage maximizes the voltage of the DVR. Hence, the line current and injected voltage phasor are perpendicular. The general objective of this approach is to provide a real zero-injected power component.

The voltage and load current were stationary. Hence, the phase of the sag voltage is altered. A higher rating of the VSI is required, as this approach only uses reactive power during compensation.

B. 3ϕ 4-SWITCH VSI

Considering a conventional 3ϕ inverter topology, six power electronic switches are required for the overall operation. Considering a power circuit, a cost-effective solution is to replace the six switches with four switches. This 3ϕ inverter topology with a small number of switches, as shown in Fig. 7, reduces the inverter cost. It also exhibits less

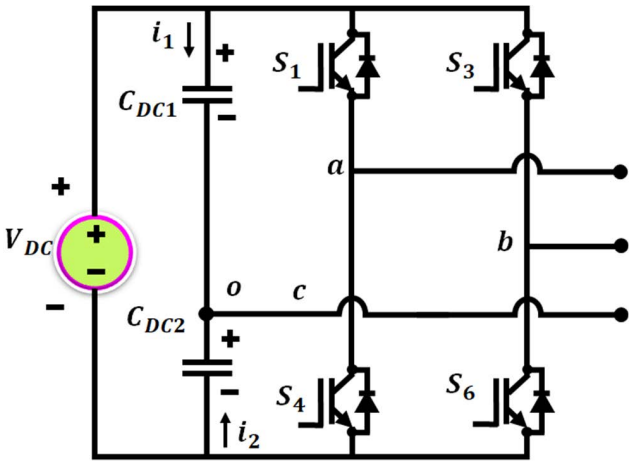


FIGURE 7. 3ϕ 4-switch VSI.

complex gate driving circuitry and a reduction in conduction losses.

Here, S_1, S_3, S_4 and S_6 indicate the four switches and C_{DC1}, C_{DC2} indicate the two split capacitors. The voltage V_{DC} indicates the DC source voltage obtained from the energy storage. The phase c is connected between the split capacitors while the phases a, b are connected to the two inverter legs. The upper switch states are complementary to the states of the lower switches such that $S_4 = 1 - S_1$ and $S_6 = 1 - S_3$. V_{a1}, V_{b1}, V_{c1} Indicate the terminal voltages of the inverter and are expressed as given by,

$$V_{a1} = \frac{V_c}{3}(4S_3 - 2S_1 - 1) \tag{11}$$

$$V_{b1} = \frac{V_c}{3}(-2S_3 + 4S_1 - 1) \tag{12}$$

$$V_{c1} = \frac{V_c}{3}(-2S_3 - 2S_1 + 2) \tag{13}$$

The voltage across the split capacitors is denoted by V_c. S_1, S_3 indicate the switching functions related to each leg phase. Where V_{a1}, V_{b1}, V_{c1} represent the inverter output voltages. The pulses required for the operation of the VSI switches are obtained from the PWM generator. The inverter includes an LC filter with the following design equation:

$$L = \frac{Z_0}{4\pi f_c} \tag{14}$$

$$C = \frac{1}{4Z_0\pi f_c} \tag{15}$$

A CSA tuned PI controller was adopted to generate control signals for the PWM generator, and the corresponding control approach is explained as follows.

C. PI CONTROLLER FOR DVR

The controller is regarded as an essential component of the DVR. Closed-loop control in a rotating dq reference frame was utilized to control the DVR system. The PI controller injected appropriate pulses through the PWM generator

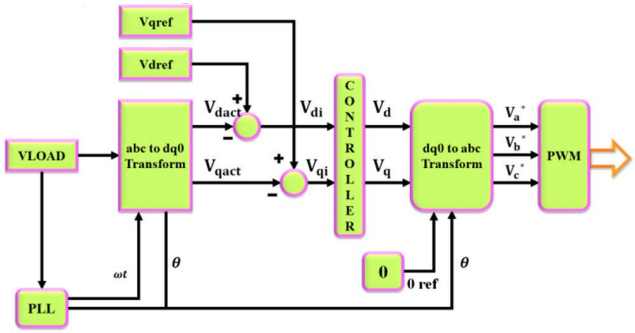


FIGURE 8. Circuit diagram of PI controller.

during the disturbances. Fig.8 shows the PI controller circuit of the DVR.

Using (11), (12), and (13), the $abc3\Phi$ coordinate structure is transformed into $dq0$ coordinate structure, which is given as

$$V_d = \frac{2}{3}\left[V_a sin\omega t + V_b \sin\left(\omega t - \frac{2\pi}{3}\right) + V_c \sin\left(\omega t + \frac{2\pi}{3}\right)\right] \tag{16}$$

$$V_q = \frac{2}{3}\left[V_a cos\omega t + V_b \cos\left(\omega t - \frac{2\pi}{3}\right) + V_c \cos\left(\omega t + \frac{2\pi}{3}\right)\right] \tag{17}$$

$$V_0 = \frac{1}{3}\left[V_a + V_b + V_c\right] \tag{18}$$

The dq values were compared with the reference values to calculate the disturbance that occurred in the dq coordinates. In addition, a phase-locked loop (PLL) is utilized to measure the frequency of the system.

$$error_d\,(t) = V_{dref} - V_{dact} \tag{19}$$

$$error_q\,(t) = V_{qref} - V_{qact} \tag{20}$$

The abovementioned error signals that occur between the reference and actual values of dq voltage are utilized as inputs for the PI controller, and the corresponding control circuit is shown in Fig.9.

VLoad indicates the load voltage, which is measured and converted to the $dq0$ coordinates. The PI controller input was the error between the actual and reference dq voltages. The outputs are converted into *abc* coordinates and applied to the PWM circuit to generate suitable plses of the VSI.

The performance of the PI controller was enhanced by tuning its parameters. Although various traditional methods are utilized for tuning the PI parameters, these methods exhibit certain nonlinearities and disadvantages. Hence, meta-heuristic optimization approaches were adopted to tune the PI parameters in an efficient manner.

D. TUNING OF PI CONTROLLER BY CUCKOO SEARCH ALGORITHM

In this approach, a cuckoo search algorithm (CSA) is adopted to tune the PI parameters, as it can solve optimization issues with a quick response and compensate for the requirements

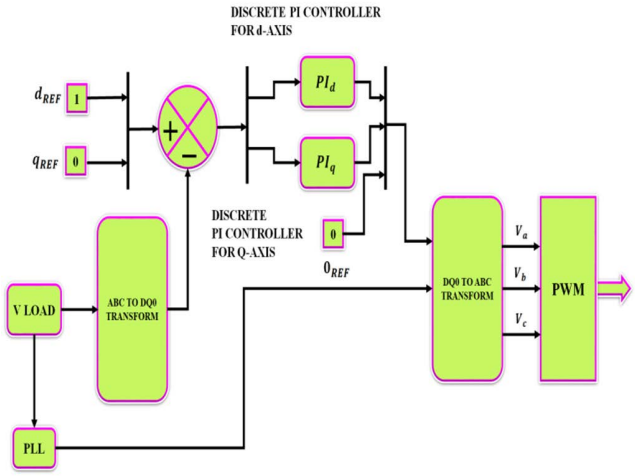


FIGURE 9. PI control circuit.

of global convergence with easy implementation. This is regarded as a meta-heuristic approach inspired by the breeding behavior of cuckoos. Owing to their pleasing sound and forceful reproduction strategy, cuckoos are regarded as entrancing birds. These birds exhibit the characteristics of laying eggs in shared nests and getting rid of the eggs of others. This was done to improve the likelihood of their eggs. The host birds accept the foreign eggs by becoming fooled, but the eggs are dumped outside or the nest is completely destroyed if the eggs are discovered. The search for the best nest plays a major role in the reproduction method of the cuckoo. This process is similar to that of searching for food, and based on Levy's flight mathematical function model, the walk and directions are selected and modeled.

In this algorithm, several nests are considered, where every egg indicates a solution and the egg of a cuckoo indicates a new solution, whereas the worst solution in the nest is replaced by a new solution. By considering CSA, the inputs are power loss (P_l), change in error voltage (ΔeV(k)), and error voltage (eV(k)). A flowchart of the CSA utilized is shown in Fig. 10.

The steps in the CSA are mentioned as given below.

Step 1: Define the objective function, which is considered an optimization issue, and is given by

$$O_f = \min(P_l) \tag{21}$$

The values of $eV(k)$ and $\Delta eV(k)$ were varied to minimize optimization. Thus, regulation of the DC link voltage is performed, which improves the DVR compensation.

Step 2: Randomly initialize the host nests by considering the array size of the nest as n.

$$P_k = \{p_1, p_2, \ldots\ldots, p_n\} \tag{22}$$

$$Q_k = \{q_1, q_2, \ldots\ldots, q_n\} \tag{23}$$

In the above equations, P_k and Q_k are represented as the error voltage $(eV(k))$ and change in error voltage $(\Delta eV(k))$ respectively. Every nest p_n indicates a solution vector for the

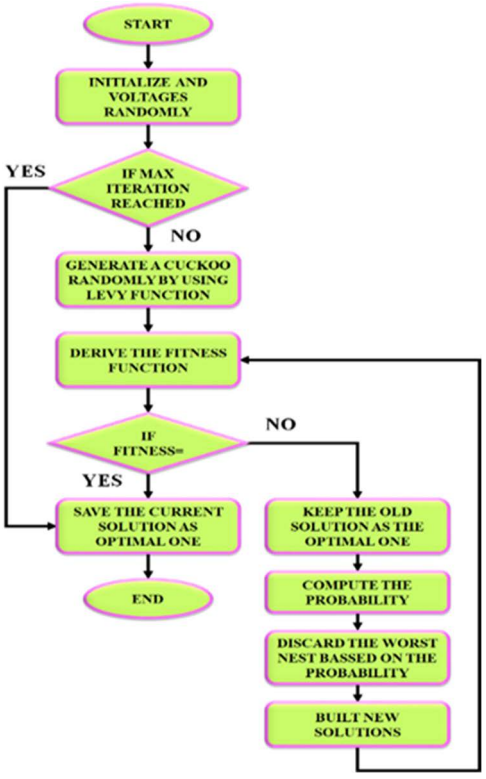


FIGURE 10. Flowchart for CSA.

optimization issues. The objective function was reduced by adopting an optimized n number of variables.

Step 3: Create the new cuckoo generation.

Using the Levy function, the cuckoo generates a new solution randomly and estimates the quality of the solutions. The cuckoo was evaluated using the objective function. The corresponding Levy function is given as

$$P_K^{t+1} = P_k^t + \alpha \oplus (q\lambda) \tag{24}$$

Step 4: Determine the fitness value for all inputs.

For all inputs, the fitness function (F) is given as,

$$fitnessfunction\,(F) = \min\,(P_l) \tag{25}$$

Here, the power loss (P_l) depends on the variations in the voltage, which is determined as

$$P_l = 2V_{dc} - (eV\,(k) + \Delta eV(K)) \tag{26}$$

Thus, the quality of the obtained solutions was estimated. The current solution is considered to be optimized only if the fitness function is reduced. If not, then Step 5 is performed.

Step 5: Eliminate the worst nest based on the probability values and determine the best solutions based on quality.

Step 6: The process is repeated until the iteration terminates. The corresponding outputs were noted.

TABLE 1. Parameters of CSA.

S.NO	Parameters	Values
1	Population size	25
2	Maximum iterations	100
3	Number of runs	10
4	Probability(Pa)	0.25
5	scale parameter(α1)	7.63
6	scale parameter(α2)	24.52

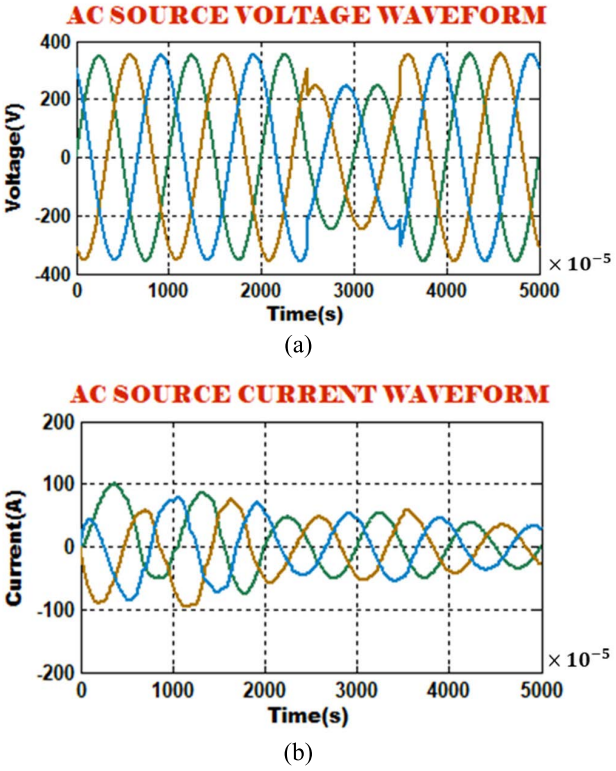


FIGURE 11. AC source waveforms (a) Voltage=350V (b) Current.

E. DESIGN VALUES

The Inverter is acquired using the developed harmonic minimization function. The objective function is minimized by applying Cuckoo Search Optimization algorithm. The parameters for the population size, maximum iterations and number of runs are taken as 25, 100 and 10. The angles are found to be same, i.e. $\alpha 1 = 7.63$ and $\alpha 2 = 24.52$ in every run.

The computational time taken by the algorithm to determine results, i.e. the switching angles is 0.7∼0.9s only for 100 iterations in one run are listed in Table 1.The obtained outputs are considered the best solutions, which are used for tuning the PI controller parameters of the DVR.

The proposed optimization algorithm reduces the error between the actual and reference voltages of the PI controller and controls the DVR to enhance system performance. The DC-link voltage is regulated through the obtained outputs, and the optimized minimal power loss is evaluated for the voltage compensation of the DVR.

TABLE 2. Cuckoo search algorithm implementation parameters.

S.NO	Parameters	Values
1	Number of nest	5x10
2	Solution space in lower bound	100
3	Solution space in upper bound	100
4	Tolerance	1.0e-5;
5	Number of iteration	100
6	Discovery rate of solution	0.25

TABLE 3. System parameters.

Parameters	Values
Source voltage	415 V
Frequency	50 Hz
Resistance	1000 Ω
Inductance	9.24 mH
Load	16.8 MW
V_{DC}	800 V
L_f, C_f	$5mH, 7000\ \mu F$
Switching frequency	10 KHz

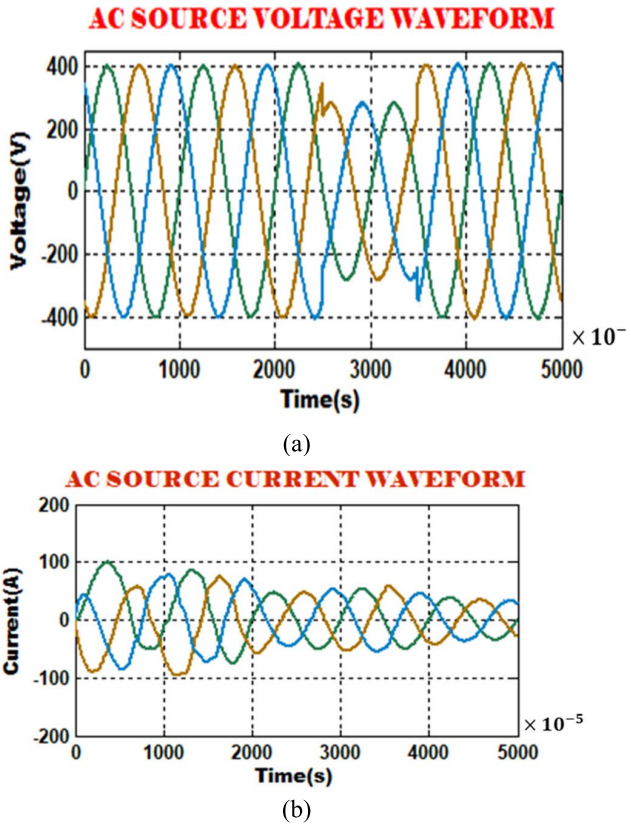


FIGURE 12. AC source waveforms (a) Voltage=400V (b) Current.

F. IMPLEMENTATION PARAMETERS OF CSA CONTROLLER BASED DVR

The MATLAB implementation parameters used for developing the proposed CSA controller is presented in in Table 2.

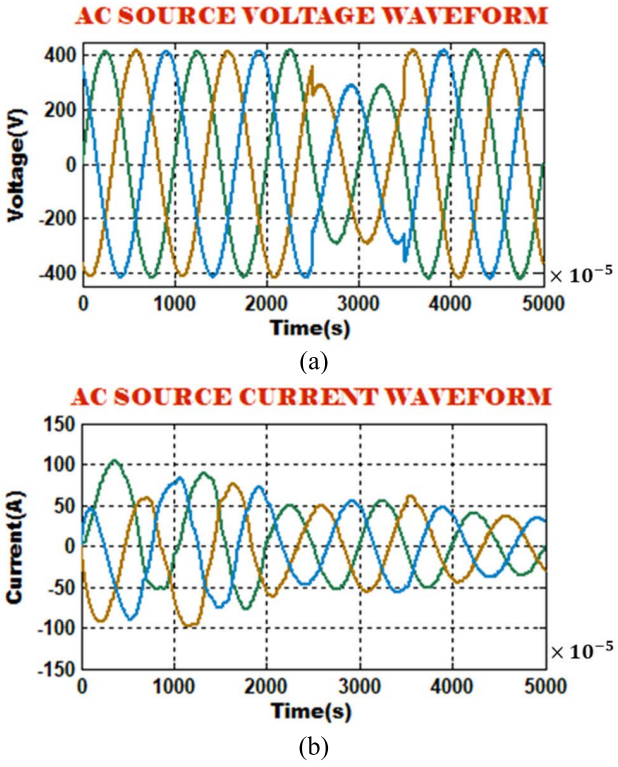


FIGURE 13. AC source waveforms (a) Voltage=410V (b) Current.

III. RESULTS AND DISCUSSION

The proposed DVR effectively rectifies the fluctuations, distortions, unbalanced voltage swells, and sags. A CSA-tuned PI controller is employed in this system to regulate the inverter of the DVR and to attain reactive power compensation. Hence, it delivers optimal results for mitigating power-quality issues. The simulation was performed in MATLAB-Simulink, and the parameter specifications of the system are listed in Table 3.

A. SIMULATION RESULTS

Different AC source inputs were applied to the proposed system with voltages of 350 V, 400 V, 410 V, 420 V and 500 V. The AC source current waveforms for different voltage inputs are shown in the subsequent figures.

Fig.11 shows the voltage and current waveforms of the AC source. The AC source voltage was by 350V in which a sag in voltage occurred from 0.025s to 0.035s. The corresponding current waveform is shown in Fig. 11 (b), which indicates that an output current of 30A was retained as a constant.

The waveforms of the AC current and voltage for the input of **400V** are significantly highlighted in Fig. 12, which validates that the output current is constantly maintained as **30A**. Even though a voltage sag occurs from **0.025s** to **0.035s**, the obtained current is maintained constant with the optimized control approach of the DVR.

A voltage of 410V was given as the input, and an output current of 30A was constantly retained, as shown in Fig.13.

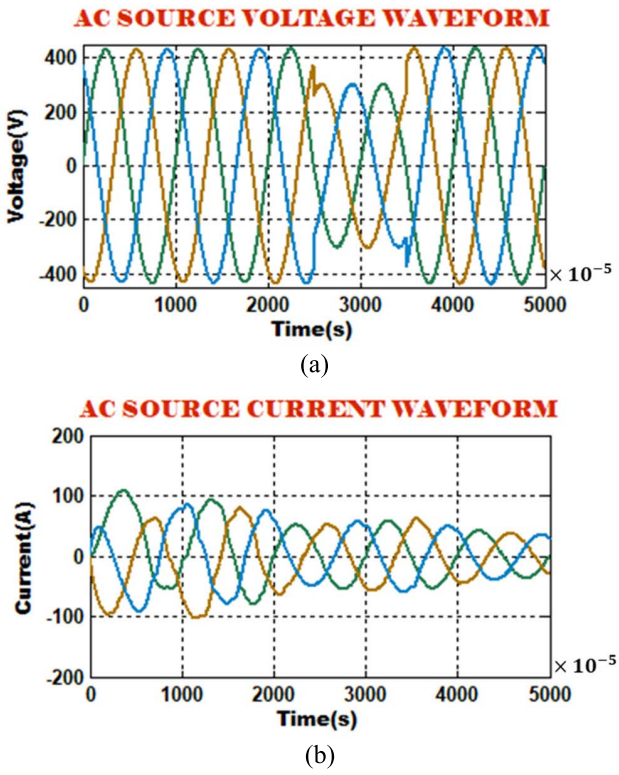


FIGURE 14. AC source waveforms (a) Voltage=420V (b) Current.

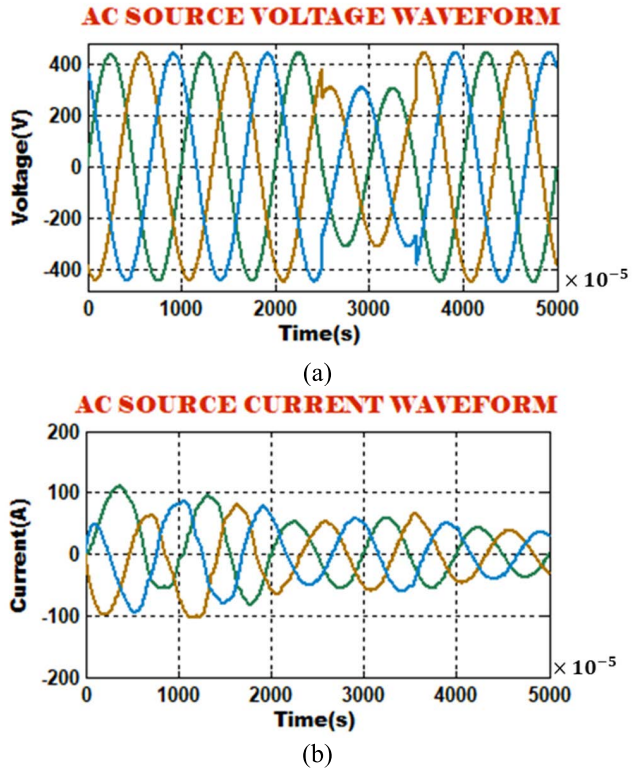


FIGURE 15. AC source waveforms (a) Voltage=430V (b) Current.

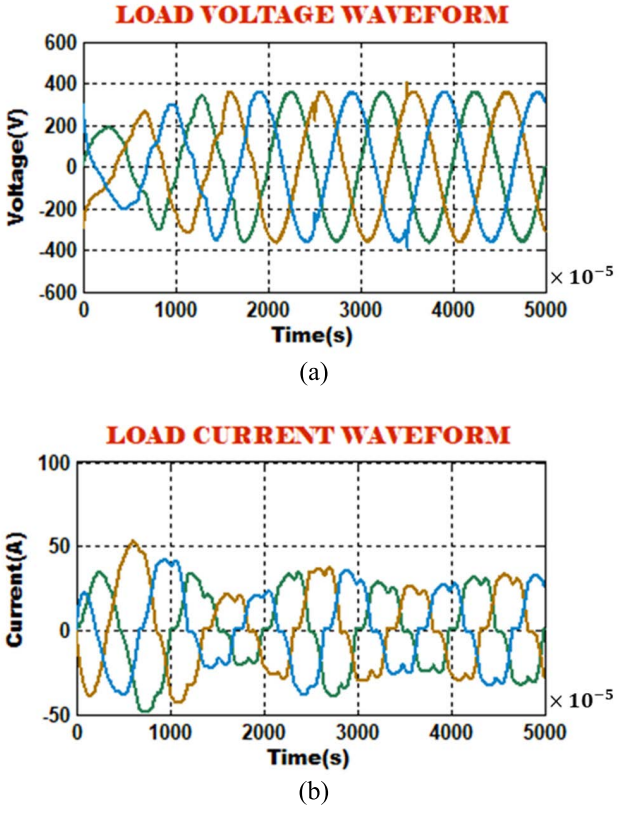


FIGURE 16. Load waveforms (a) Voltage (b) Current.

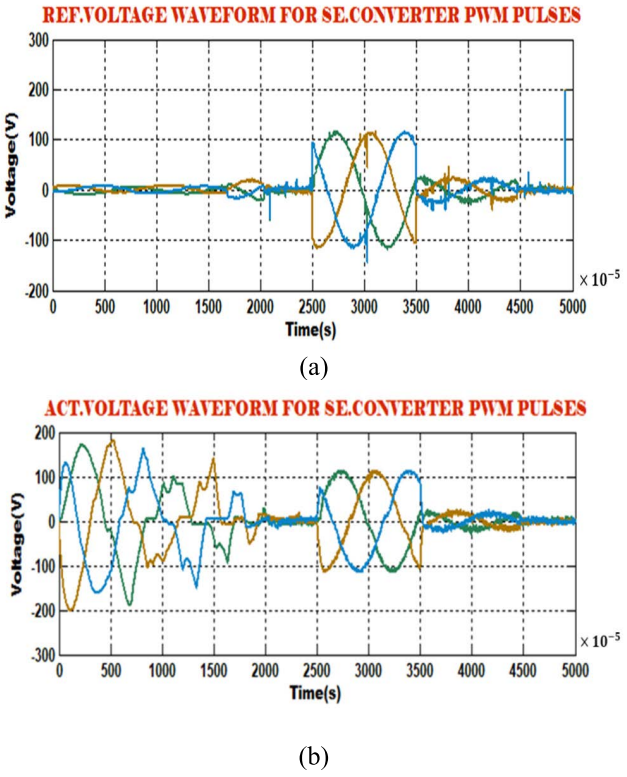


FIGURE 17. Waveforms for (a) reference voltage (b) actual voltage.

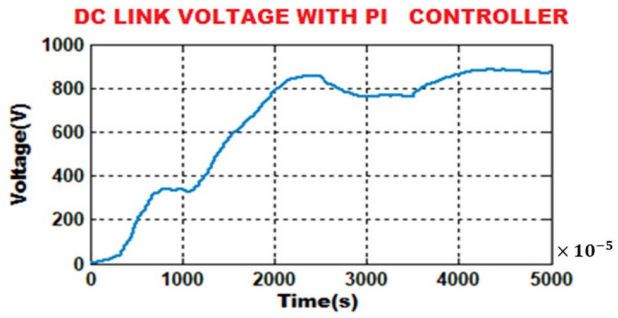


FIGURE 18. Waveforms for DC link voltage.

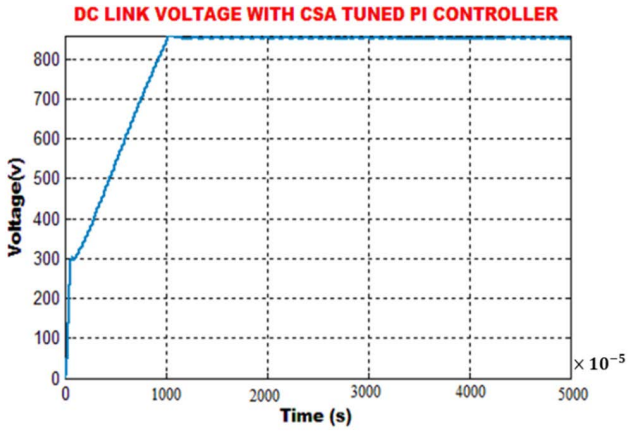


FIGURE 19. Waveforms for DC link voltage with CSA tuned PI controller.

The AC source voltage exhibited a voltage sag from **0.025*s*** to **0.035*s*** which influences the power quality. However, in the proposed approach, the effects of the voltage sag are mitigated by actual and reference voltage generation.

The Fig. 14, the input voltage is set to **420*V*** but has a sag in voltage from **0.025*s*** to **0.035*s***. However, the current waveform indicates that a constant current value of 30A is attained with the optimized control approach.

Fig.15 depicts the current and voltage waveforms of AC source, which portrays that the input voltage is set as **430*V***. The voltage sag present in the AC source voltage from **0.025*s*** to **0.035*s*** do not affect the current which is given in Fig. 15 (b).

Fig. 16 shows the load waveforms for the voltage and current. Irrespective of the fluctuating input voltages owing to voltage sag issues, the obtained values of the load voltage and load current remain constant. This is because of the proposed DVR with an optimized control approach.

Fig. 17 shows the waveforms of the reference and actual voltages. The reference and actual values were compared to generate the change in error voltage and error voltage values. At the time period of 0.025*s* to 0.035*s*, the actual and reference voltages were generated, which in turn tackled the voltage sag issues of the source voltage. These values are further optimized by CSA to attain the best fitness values.

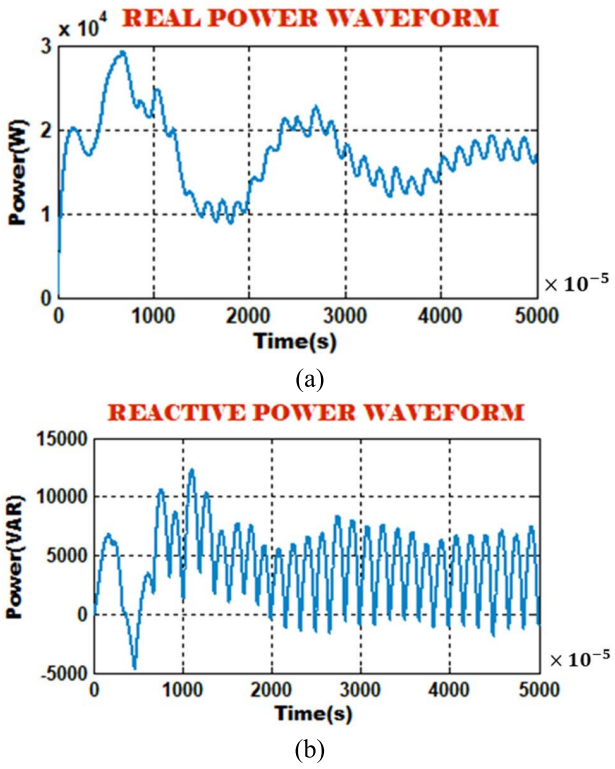


FIGURE 20. Waveforms for (a) real power (b) reactive power.

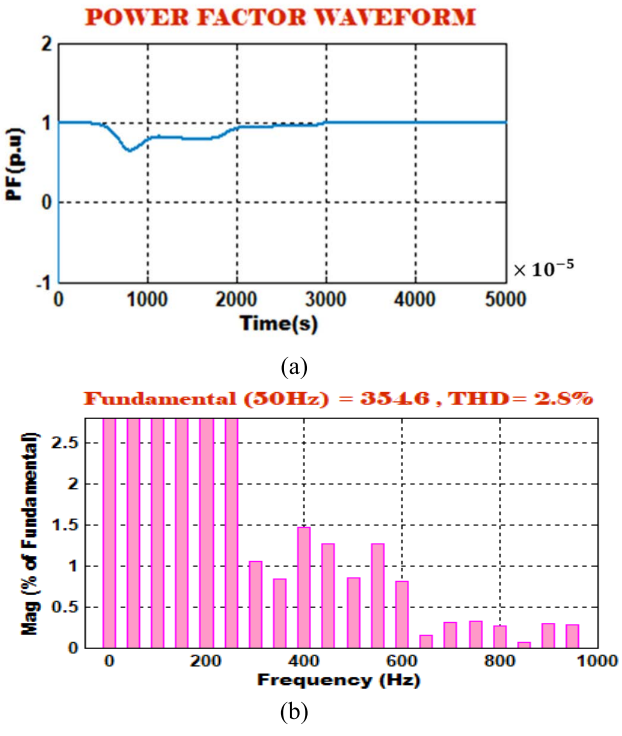


FIGURE 21. (a) Waveforms for power factor (b) THD obtained.

Fig. 18 shows the waveform of the DC-link voltage, which was controlled by the PI controller. The output indicated a varying DC-link voltage without stability.

FIGURE 22. Hardware setup.

Fig.19 shows the DC-link voltage obtained with the CSA-tuned PI controller. The adopted CSA effectively tunes the parameters of the PI controller to generate optimized outputs, which are further converted to pulses by a PWM generator. These pulses control the 3ϕ 4-switch VSI operation; hence, a constant DC link voltage is maintained. An efficiently regulated DC link voltage without fluctuations is generated and the settling time obtained is found to be $0.02s$.The regulated DC link voltage delivers enhanced voltage compensation with reduced power quality issues.

Fig.20 shows the values of the real power and reactive power.

Fig.21 (a) shows that a unity power factor is obtained, which indicates that improved compensation is attained through the mitigation of power quality issues. Fig.21 (b) shows that the obtained THD value is 2.8%. These improved power quality and THD values indicate the effectiveness of the proposed approach in mitigating power quality issues.

Table 4 shows a comparison of the load voltage with and without CSA assisting the DVR. The proposed approach generates efficient results in the alleviation of voltage swells, sags, and source voltage harmonics.

TABLE 4. Comparison of load voltage.

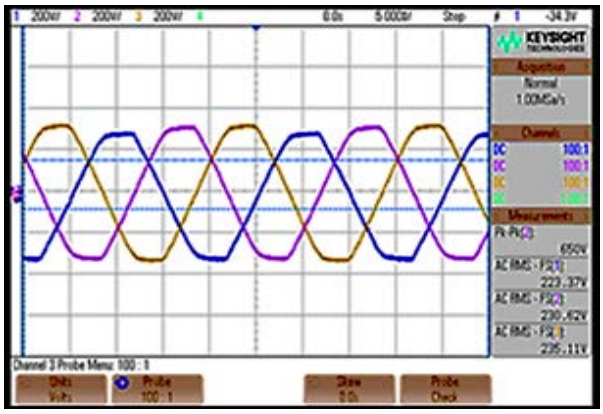
Issues of power quality	Load voltage in the absence of DVR	Load voltage with CSA utilized DVR
Voltage swell	1.2	2.5
Voltage sag	2.58	2.4
Source voltage ($2^{nd}, 3^{rd}$) harmonics	10.2	2.3
Source voltage ($3^{rd}, 4^{th}$) harmonics	10.2	2.6
Source voltage ($5^{th}, 7^{th}$) harmonics	10.2	2.0

B. HARDWARE RESULTS

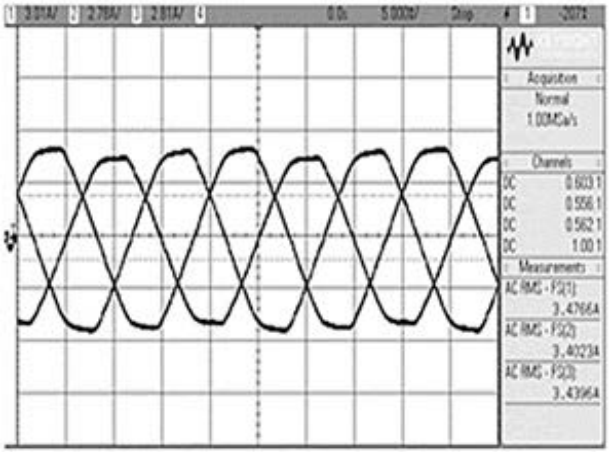
The main purpose of the DVR is to rectify voltage swells and sags in the distribution system. The CSA-assisted DVR was utilized to solve PQ issues effectively. The proposed approach generated improved results under both transient and steady-state conditions. Hardware implementation of the system was performed to investigate the operational efficacy of the proposed approach. Through the hardware outcomes, it is understood that the DVR with CSA effectively improves the operation of the system by rectifying PQ issues. The hardware setup of the proposed control approach is shown in Fig.22. It comprises an FPGA controller that manages the interfacing functions of input and output. A TLP250 driver circuit is adopted, which acts as an isolated IGBT driver IC. It comprises a Zener diode and transistors to amplify the PWM pulses to be fed to the IGBT switch.

Fig. 23 displays the AC source voltage and current waveforms. Fig. 24 (a) indicates the DC link voltage waveform. The link voltage is maintained at a reference value with the help of the utilized PI controller.

The power changes in the distribution system are analyzed using the CSA-adopted PI controller, which feeds the output to the pulse width modulator (PWM). The generated PWM



(a)



(b)

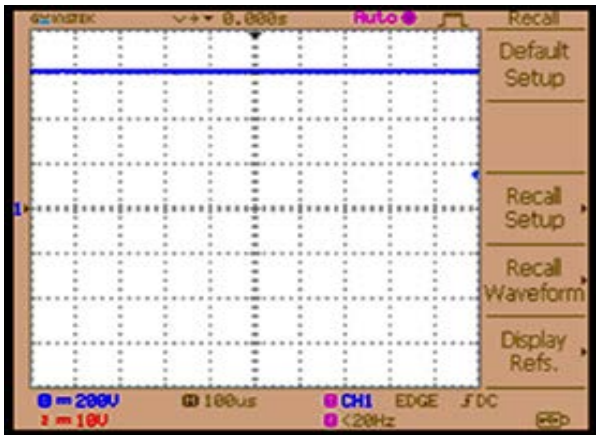
FIGURE 23. Input (a) AC voltage waveform (b) current waveform.

TABLE 5. Comparison of THD.

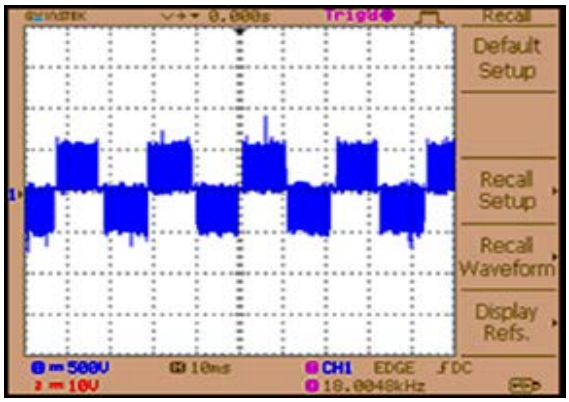
Controllers	Simulation THD(%)	Hardware THD(%)
PI	9.5	9.86
Fuzzy-PI	4.1	4.7
GWO-PI	3.8	4.35
PSO-PI	3.43	3.2
CSA-PI	2.8	2.95

pulses are applied to the inverter to enhance its operation. Fig. 24 (b) depicts the generated output of 3ϕ VSI.

Finally, the output of the VSI is filtered and provided to the load. Fig. 25 shows the waveforms of the load voltage and load current. Thus, the proposed DVR system aids in supplying a stable harmonic free current to the load under both transient and steady-state conditions. Fig. 26 shows the THD obtained for the hardware implementation with a value of 2.95%.



(a)



(b)

FIGURE 24. (a) DC link voltage waveform (b) Output voltage of VSI.

Analysis of power loss

The switch conduction losses are given by,

$$P_{SW,con} = \frac{1}{T}\int_0^T I_{SW}^2 R_{SW,0n} dt = 1300mW \tag{27}$$

The diode conduction losses are given by,

$$P_{D,con} = \frac{1}{T}\int_0^T I_D V_{DF} dt = 2150mW \tag{28}$$

The switch switching losses are given by,

$$P_{SW,switch} = \frac{1}{8T}\int_0^T I_{SW} V_{SW,off} dt = 12mW \tag{29}$$

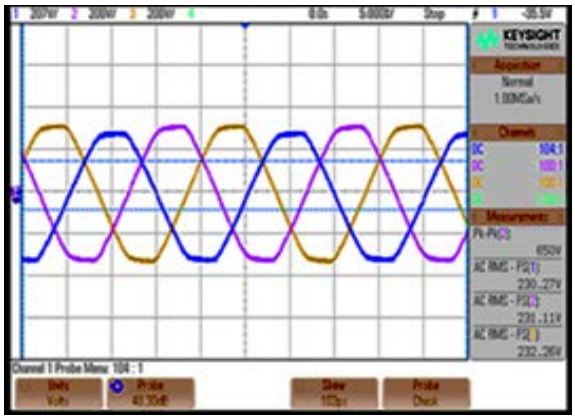
The diode switching losses are given by,

$$P_{D,switch} = \frac{1}{4T}\int_0^T Q_{RR} V_{D,off} dt = 70.5mW \tag{30}$$

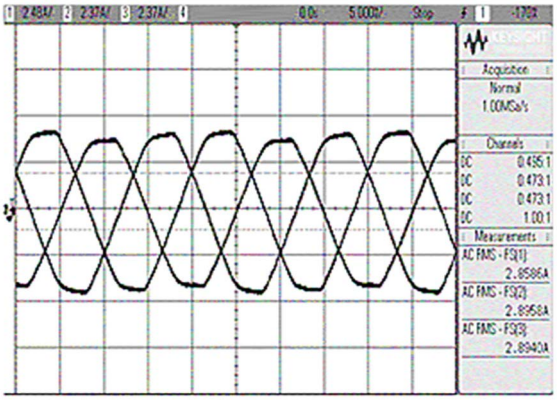
The gate losses are given by,

$$P_G = \left(Q_{g-H} + Q_{g-L}\right) \times V_{gs} \times \frac{1}{T} = 20mW \tag{31}$$

Here, I_{SW} represents the switch conduction current, $R_{SW,0n}$ represents the switch ON resistance, I_D denotes the free-wheeling diode forward current, V_{DF} denotes the diode



(a)



(b)

FIGURE 25. (a) Load voltage waveform (b) Load current waveform.

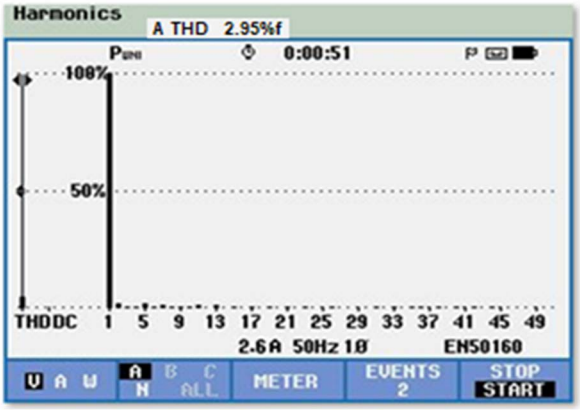
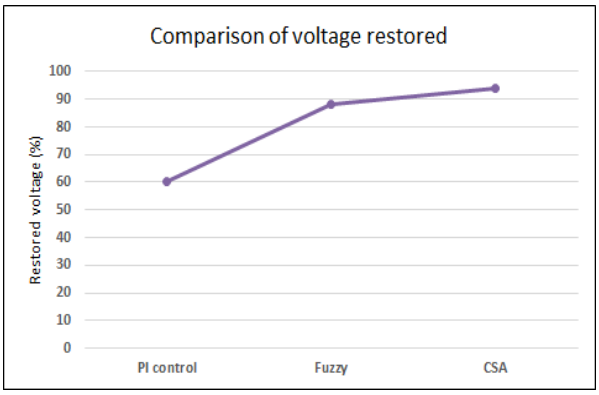
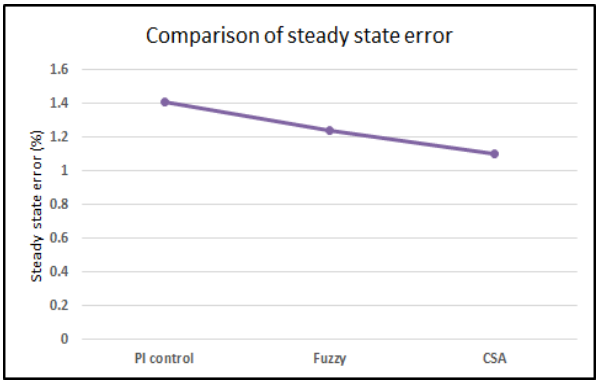


FIGURE 26. THD obtained.

forward voltage, $V_{SW,off}$ denotes the switch blocking voltage, Q_{RR} indicates the diode reverse recovery charge, $V_{D,off}$ represents the diode blocking voltage, Q_{g-H} indicates the high side switch gate electric charge, Q_{g-L} denotes the low side switch gate electric charge, V_{gs} is the gate drive voltage, T denotes the time period.



(a)



(b)

FIGURE 27. Comparison of (a) Voltage restored (b) Steady state error.

The efficiency is calculated by,

$$\%\eta = \frac{P_{out}}{P_{out}+P_{loss}} \tag{32}$$

The losses and efficiency are evaluated at a switching frequency of $10KHz$.

Fig. 27 represents the comparison of restored voltage and steady state error of the proposed approach. The performance of CSA is analogized with fuzzy control and PI control methods. When the voltage sag is **40**%, the proposed control restores **94**% of the voltage but other approaches like PI control and fuzzy restore **60**% and **88**% respectively. The proposed approach generates a steady state error of **1.1**% while PI control and fuzzy generated **1.41**% and **1.24**% respectively.

Fig. 28 denotes the comparison of efficiency of the proposed approach with fuzzy control and PI control methods. The efficiency of the proposed approach is 92.68% while traditional PI control and fuzzy-PI generate the efficiency of 89.2% and 90.7% respectively.

Table 5 compares the THD values obtained from the simulation and the hardware results. The THD values of the proposed approach were **2.8**% for the simulation and **2.95**% for the hardware results. Compared with other control

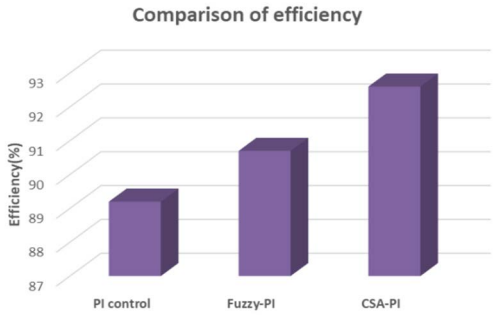


FIGURE 28. Comparison of efficiency.

TABLE 6. Comparison of power factor with existing works.

Methods	Power factor
Santhana et al. [55]	0.96
Nagarajan et al. [56]	0.995
Proposed	0.997

TABLE 7. Comparison of THD with existing works.

Methods	THD (%)
Rakeshwri et al. [57]	7.85
Nagarajan et al. [56]	5.67
Dung et al. [58]	4.01
Naeem et al. [59]	4
Proposed approach	2.8

approaches, the proposed approach generates improved THD values.

Tables 3 and 4 compare the power factor and THD of the proposed work with those of existing works. The obtained values indicate that the proposed approach generates an enhanced power factor of **0.997** with a reduced THD of **2.8**% which in turn indicates an improved power quality and efficiency.

IV. CONCLUSION

The utilization of DVR for the mitigation of power quality issues such as harmonics, voltage swells, and sags is expounded in this study. The DVR is a self-contained solution for rectifying PQ issues. The proposed control technique based on DVR is highly effective in compensating for the distorted load voltage. In addition, it assists in maintaining a smoother and more stable voltage level with less harmonic content. Owing to the adaptive characteristics, the CSA is implemented in this study, which delivers improved compensation with an acceptable value of THD in linear and nonlinear loads. It also provides efficient voltage control with an improved transient response and delivers a settling time of 0.02s.Hence, it is validated that the proposed methodology delivers better performance with an efficiency of 92.6%,a simulation THD value of 2.8% and a hardware THD value of 2.95%.

REFERENCES

[1] A. A. P. Biscaro, R. A. F. Pereira, M. Kezunovic, and J. R. S. Mantovani, "Integrated fault location and power-quality analysis in electric power distribution systems," *IEEE Trans. Power Del.*, vol. 31, no. 2, pp. 428–436, Apr. 2016.

[2] G. S. Chawda, A. G. Shaik, M. Shaik, S. Padmanaban, J. B. Holm-Nielsen, O. P. Mahela, and P. Kaliannan, "Comprehensive review on detection and classification of power quality disturbances in utility grid with renewable energy penetration," *IEEE Access*, vol. 8, pp. 146807–146830, 2020.

[3] G. S. Chawda, A. G. Shaik, O. P. Mahela, S. Padmanaban, and J. B. Holm-Nielsen, "Comprehensive review of distributed FACTS control algorithms for power quality enhancement in utility grid with renewable energy penetration," *IEEE Access*, vol. 8, pp. 107614–107634, 2020.

[4] A. Moghassemi, P. Sanjeevikumar, V. K. Ramachandaramurthy, M. Mitolo, and M. Benbouzid, "A novel solar photovoltaic fed TransZSI-DVR for power quality improvement of grid-connected PV systems," *IEEE Access*, vol. 9, pp. 7263–7279, 2021.

[5] P. Singh, "Delta-bar-delta neural-network-based control approach for power quality improvement of solar-PV-interfaced distribution system," *IEEE Trans. Ind. Informat.*, vol. 16, no. 2, pp. 790–801, Feb. 2020.

[6] Y. Lu, "Detection and classification of power quality disturbances in distribution networks based on VMD and DFA," *CSEE J. Power Energy Syst.*, vol. 6, no. 1, pp. 122–130, 2020.

[7] X. J. Zeng, H. F. Zhai, M. X. Wang, M. Yang, and M. Q. Wang, "A system optimization method for mitigating three-phase imbalance in distribution network," *Int. J. Electr. Power Energy Syst.*, vol. 113, pp. 618–633, Dec. 2019.

[8] H. Nian, T. Wang, and Z. Q. Zhu, "Voltage imbalance compensation for doubly fed induction generator using direct resonant feedback regulator," *IEEE Trans. Energy Convers.*, vol. 31, no. 2, pp. 614–626, Feb. 2016.

[9] T. Routtenberg, R. Concepcion, and L. Tong, "PMU-based detection of voltage imbalances with tolerance constraints," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 484–494, Feb. 2016.

[10] M. Lu, J. Hu, R. Zeng, W. Li, and L. Lin, "Imbalance mechanism and balanced control of capacitor voltage for a hybrid modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5686–5696, Jul. 2017.

[11] A. Anzalchi, A. Sundararajan, A. Moghadasi, and A. Sarwat, "High-penetration grid-tied photovoltaics: Analysis of power quality and feeder voltage profile," *IEEE Ind. Appl. Mag.*, vol. 25, no. 5, pp. 83–94, Jul. 2019.

[12] M. Sedighizadeh, R. V. Doyran, and A. Rezazadeh, "Optimal simultaneous allocation of passive filters and distributed generations as well as feeder reconfiguration to improve power quality and reliability in microgrids," *J. Cleaner Prod.*, vol. 265, Aug. 2020, Art. no. 121629.

[13] P. T. Ogunboyo, R. Tiako, and I. E. Davidson, "Effectiveness of dynamic voltage restorer for unbalance voltage mitigation and voltage profile improvement in secondary distribution system," *Can. J. Electr. Comput. Eng.*, vol. 41, no. 2, pp. 105–115, 2018.

[14] K. Meng, Z. Y. Dong, P. K. C. Wong, and T. Ting, "Unbalance mitigation via phase-switching device and static VAR compensator in low voltage distribution network," *IEEE Trans. Power Syst.*, vol. 35, no. 6, pp. 4856–4869, May 2020.

[15] Y.-W. Liu, S.-H. Rau, C.-J. Wu, and W.-J. Lee, "Improvement of power quality by using advanced reactive power compensation," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 18–24, Aug. 2017.

[16] D. Subhra and S. Debnath, "Optimal switching strategy of an SVC to improve the power quality in a distribution network," *IET Sci., Meas. Technol.*, vol. 13, no. 5, pp. 640–649, Jul. 2019.

[17] K. Nikum, A. Wagh, R. Saxena, and B. Mishra, "New economical design of SVC and passive filters to improve power quality at railway substation: A case study," *J. Inst. Eng.*, vol. 100, no. 5, pp. 529–540, Oct. 2019.

[18] F. H. Gandoman, A. Ahmadi, A. M. Sharaf, P. Siano, J. Pou, B. Hredzak, and V. G. Agelidis, "Review of FACTS technologies and applications for power quality in smart grids with renewable energy systems," *Renew. Sustain. Energy Rev.*, vol. 82, pp. 502–514, Feb. 2018.

[19] T. Ahmed, A. Waqar, R. M. Elavarasan, J. Imtiaz, M. Premkumar, and U. Subramaniam, "Analysis of fractional order sliding mode control in a D-STATCOM integrated power distribution system," *IEEE Access*, vol. 9, pp. 70337–70352, 2021.

[20] J. Pereda and T. C. Green, "Direct modular multilevel converter with six branches for flexible distribution networks," *IEEE Trans. Power Del.*, vol. 31, no. 4, pp. 1728–1737, Aug. 2016.

[21] D. Li, K. Yang, Z. Q. Zhu, and Y. Qin, "A novel series power quality controller with reduced passive power filter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 773–784, Jan. 2016.

[22] T. Toufik, A. Allali, A. Meftouhi, O. Abdelkhalek, A. Benabdelkader, and M. Denai, "Robust control of series active power filters for power quality enhancement in distribution grids: Simulation and experimental validation," *ISA Trans.*, vol. 107, pp. 350–359, Dec. 2020.

[23] H. Ouadi, A. Aitchihab, and F. Giri, "Adaptive nonlinear control of three-phase series active power filters with magnetic saturation," *J. Control, Autom. Electr. Syst.*, vol. 31, no. 3, pp. 726–742, Jun. 2020.

[24] P. K. Ray, "Power quality improvement using VLLMS based adaptive shunt active filter," *CPSS Trans. Power Electron. Appl.*, vol. 3, no. 2, pp. 154–162, 2018.

[25] A. Benzahia, R. Boualaga, A. Moussi, L. Zellouma, M. Meriem, and B. Chaima, "A PV powered shunt active power filter for power quality improvement," *Global Energy Interconnection*, vol. 2, no. 2, pp. 143–149, 2019.

[26] E. L. L. Fabricio, S. C. S. Júnior, C. B. Jacobina, and M. B. de Rossiter Correa, "Analysis of main topologies of shunt active power filters applied to four-wire systems," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2100–2112, Mar. 2017.

[27] S. R. Das, P. K. Ray, and A. Mohanty, "Improvement in power quality using hybrid power filters based on RLS algorithm," *Energy Proc.*, vol. 138, pp. 723–728, Oct. 2017.

[28] N. Babu P, B. K. Choudhury, B. Kar, B. Halder, and N. Meghalaya, "Modelling of a hybrid active power filter for power quality improvement using synchronous reference frame theory," *Int. J. Eng. Res.*, vol. 6, no. 3, pp. 369–374, Mar. 2017.

[29] L. Wang, C. S. Lam, and M. C. Wong, "Selective compensation of distortion, unbalanced and reactive power of a thyristor-controlled LC-coupling hybrid active power filter (TCLC-HAPF)," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9065–9077, Dec. 2017.

[30] R. A. Modesto, S. A. O. da Silva, A. A. de Oliveira, and V. D. Bacon, "A versatile unified power quality conditioner applied to three-phase four-wire distribution systems using a dual control strategy," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5503–5514, Aug. 2016.

[31] R. A. J. Amalorpavaraj, P. Kaliannan, S. Padmanaban, U. Subramaniam, and V. K. Ramachandaramurthy, "Improved fault ride through capability in DFIG based wind turbines using dynamic voltage restorer with combined feed-forward and feed-back control," *IEEE Access*, vol. 5, pp. 20494–20503, 2017.

[32] N. Mallick and V. Mukherjee, "Self-tuned fuzzy-proportional-integral compensated zero/minimum active power algorithm based dynamic voltage restorer," *IET Gener., Transmiss. Distrib.*, vol. 12, no. 11, pp. 2778–2787, 2018.

[33] A. Parreño-Torres, P. Roncero-Sánchez, J. V. del Real, and F. J. López-Alcolea, "A discrete-time control method for fast transient voltage-sag compensation in DVR, *IEEE Access*, vol. 7, pp. 170564–170577, 2019.

[34] A. Karthikeyan, D. G. A. Krishna, S. Kumar, B. V. Perumal, and S. Mishra, "Dual role CDSC-based dual vector control for effective operation of DVR with harmonic mitigation," *IEEE Trans. Power Electron.*, vol. 66, no. 1, pp. 4–13, Jan. 2019.

[35] C. K. Sundarabalan and K. Selvi, "Compensation of voltage disturbances using PEMFC supported dynamic voltage restorer," *Int. J. Electr. Power Energy Syst.*, vol. 71, pp. 77–92, Oct. 2015.

[36] K. K. Prabhakaran and A. Karthikeyan, "Electromagnetic torque-based model reference adaptive system speed estimator for sensorless surface Mount permanent magnet synchronous motor drive," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5936–5947, Jul. 2020.

[37] S. Agalar and Y. A. Kaplan, "Power quality improvement using STS and DVR in wind energy system," *Renew. Energy*, vol. 118, pp. 1031–1040, Apr. 2018.

[38] G. Chen, M. Zhu, and X. Cai, "Medium-voltage level dynamic voltage restorer compensation strategy by positive and negative sequence extractions in multiple reference frames," *IET Power Electron.*, vol. 7, no. 7, pp. 1747–1758, 2014.

[39] Z. Zheng, X. Xiao, X. Chen, C. Huang, L. Zhao, and C. Li, "Performance evaluation of a MW-class SMES-BES DVR system for mitigation of voltage," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3090–3099, Jul. 2018.

[40] S. B. Supported, A. M. Gee, F. Robinson, and W. Yuan, "A superconducting magnetic energy storage-emulator/battery supported dynamic voltage restorer," *IEEE Trans. Energy Convers.*, vol. 32, no. 1, pp. 55–64, Sep. 2017.

[41] E. M. Molla and C.-C. Kuo, "Voltage sag enhancement of grid connected hybrid PV-wind power system using battery and SMES based dynamic voltage restorer," *IEEE Access*, vol. 8, pp. 130003–130013, 2020.

[42] P. Jayaprakash, B. Singh, D. P. Kothari, and A. Chandra, "Control of reduced-rating dynamic voltage restorer with a battery energy storage system," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1295–1303, Apr. 2014.

[43] J. Ye and H. B. Gooi, "Phase angle control based three-phase DVR with power factor correction at point of common coupling," *J. Modern Power Syst. Clean Energy*, vol. 8, no. 1, pp. 179–186, 2019.

[44] A. Moghassemi and S. Padmanaban, "Dynamic voltage restorer (DVR): A comprehensive review of topologies, power converters, control methods, and modified configurations," *Energies*, vol. 13, no. 16, p. 4152, 2020.

[45] C. Tu, Q. Guo, F. Jiang, C. Chen, X. Li, F. Xiao, and J. Gao, "Dynamic voltage restorer with an improved strategy to voltage sag compensation and energy self-recovery," *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 3, pp. 219–229, 2019.

[46] T. A. Naidu, S. R. Arya, R. Maurya, and V. Rajgopal, "Compensation of voltage-based power quality problems using sliding mode observer with optimised PI controller gains," *IET Gener., Transmiss. Distrib.*, vol. 14, no. 14, pp. 2656–2665, 2020.

[47] Z. Zheng, X. Xiao, X. Y. Chen, C. Huang, and J. Xu, "Performance evaluation of a MW-class SMES-based DVR system for enhancing transient voltage quality by using $d-q$ transform control," *IEEE Trans. Appl. Supercond.*, vol. 28, no. 4, Jun. 2018, Art. no. 5700805.

[48] H. Ghosh, "A new approach to improve PV power injection in LV electrical systems using DVR," *IEEE Syst. J.*, vol. 12, no. 4, pp. 3324–3333, Dec. 2018.

[49] G. A. de Almeida Carlos, C. B. Jacobina, and J. P. R. A. Méllo, "Cascaded open-end winding transformer based DVR," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1490–1501, Nov. 2018.

[50] D. G. A. Krishna, K. Anbalagan, K. K. Prabhakaran, and S. Kumar, "An efficient pseudo-derivative-feedback-based voltage controller for DVR under distorted grid conditions," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 2, no. 1, pp. 71–81, Jan. 2021.

[51] P. Ray and S. R. Salkuti, "Smart branch and droop controller based power quality improvement in microgrids," *Int. J. Emerg. Electr. Power Syst.*, vol. 21, no. 6, pp. 228–238, 2020.

[52] S. R. Das, D. P. Mishra, P. K. Ray, S. R. Salkuti, and A. K. Sahoo, "Power quality improvement using fuzzy logic-based compensation in a hybrid power system," *Int. J. Power Electron. Drive Syst.*, vol. 12, no. 1, p. 576, Mar. 2021.

[53] D. P. Mishra, A. S. Nayak, T. Tripathy, S. R. Salkuti, and S. Mishra, "A novel artificial neural network for power quality improvement in AC microgrid," *Int. J. Power Electron. Drive Syst.*, vol. 12, no. 4, pp. 2151–2159, Dec. 2021.

[54] C. S. Lakshmi and C. Nagarajan, "Neural controlled multi-level inverter based DVR for power quality improvement," in *Proc. Conf. Emerg. Devices Smart Syst. (ICEDSS)*, 2018, pp. 42–47.

[55] L. Nagarajan and M. Senthilkumar, "Power quality improvement in distribution system based on dynamic voltage restorer using rational energy transformative optimization algorithm," *J. Electr. Eng. Technol.*, vol. 17, no. 1, pp. 121–137, Jan. 2022.

[56] R. Pal and S. Gupta, "Topologies and control strategies implicated in dynamic voltage restorer (DVR) for power quality improvement," *Iranian J. Sci. Technol., Trans. Electr. Eng.*, vol. 44, no. 2, pp. 581–603, Jun. 2020.

[57] D. Vo Tien, R. Gono, and Z. Leonowicz, "A multifunctional dynamic voltage restorer for power quality improvement," *Energies*, vol. 11, no. 6, p. 1351, 2018.

[58] A. Naeem, S. Dilshad, A. Khalid, M. S. Saleem, and N. Khan, "Power quality improvement using dynamic voltage restorer," *IEEE Access*, vol. 8, pp. 164325–164339, 2020.

[59] V. Babu, S. S. Basha, Y. M. Shuaib, M. Manikandan, and S. S. Enayathali, "A novel integration of solar fed dynamic voltage restorer for compensating sag and swell voltage in distribution system using enhanced space vector pulse width modulation (ESVPWM)," *Universal J. Electr. Electron. Eng.*, vol. 6, no. 5, pp. 329–350, Dec. 2019, doi: 10.13189/UJEEE.2019.060504.

[60] V. Babu and M. Manikandan, "Power quality enhancement using dynamic voltage restorer (DVR) based predictive space vector transformation (PSVT) with proportional resonant (PR)-controller," *IEEE Access*, vol. 9, pp. 155380–155392, 2021, doi: 10.1109/ACCESS.2021.3129096.
[61] M. Manikandan and V. Babu, "A novel intrinsic SPACE vector transformation based solar fed dynamic voltage restorer for power quality improvement in distribution system," *J. Ambient Intell. Humanized Comput.*, vol. 10, no. 9, pp. 7102–7114, Jan. 2021, doi: 10.1007/S12652-020-02831-0.
[62] M. Manikandan and A. M. Basha, "ODFF: Optimized dual fuzzy flow controller based voltage sag compensation for SMES-based DVR in power quality applications," *Circuits Syst., Sci. Res. Publication*, vol. 7, no. 10, pp. 2959–2974, 2016, doi: 10.4236/CS.2016.710254.
[63] S. R. Salkuti, "Optimal reactive power scheduling using cuckoo search algorithm," *Int. J. Electr. Comput. Eng.*, vol. 7, no. 5, p. 2349, Oct. 2017.

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