

Received 7 June 2022, accepted 26 June 2022, date of publication 29 June 2022, date of current version 8 July 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3187087

RESEARCH ARTICLE

Compact Load Network Having a Controlled Electrical Length for Doherty Power Amplifier

KUHYEON KWON[®]¹, WOOJIN CHOI[®]^{1,2}, JAEKYUNG SHIN[®]^{1,2}, YIFEI CHEN¹, YOUNG CHAN CHOI[®]¹, SOONCHEOL BAE¹, HYEONGJIN JEON^{1,2}, JIWON HWANG[®]¹, SEUNGMIN WOO¹, YOUNG YUN WOO³, KANG-YOON LEE[®]¹, (Senior Member, IEEE), KEUM CHEOL HWANG[®]¹, (Senior Member, IEEE), AND YOUNGOO YANG[®]^{1,2}, (Senior Member, IEEE)

¹Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, South Korea

Corresponding author: Youngoo Yang (yang09@skku.edu)

This work was supported by the National Research Foundation of Korea (NRF) Grant by the Korean Government through the MSIT under Grant 2018R1A2B3005479.

ABSTRACT The load network of the carrier amplifier for the conventional Doherty power amplifier (DPA) consists of an impedance matching circuit, an offset line, and a $\lambda/4$ transmission line (TL), so that the overall electrical length of the network can easily exceed the minimum value of 90°. Then for appropriate impedance modulation, it should be 270° with an additional 180°. This excessive electrical length of the load matching network limits the bandwidth at either the low-power or peak-power level. In this paper, a compact quasilumped $\lambda/4$ impedance transformer (ITF) having simultaneous multiple functions of impedance matching and load impedance modulation with a controlled electrical length of 90° is presented. The proposed load network includes the internal components of the transistor, the simplest high-pass network using a shunt inductor, and a low-pass L-C network. Using the optimized value of the shunt inductor, the electrical length of the load match the optimum load impedance. To verify the proposed load network, a DPA was designed and implemented using 10 W GaN-HEMTs for both carrier and peaking amplifiers. Using a 5G New Radio (NR) signal with signal bandwidth of 100 MHz and peak-to-average power ratio (PAPR) of 7.8 dB, a drain efficiency (DE) of 47 - 54.2%, and adjacent channel leakage power ratio (ACLR) of -27.9 - -23 dBc were achieved at an average output power level of 35.8 - 36.3 dBm for the frequency band of 3.4 - 3.8 GHz.

INDEX TERMS Doherty power amplifier, compact load network, controlled electrical length, 5G New Radio, GaN-HEMT.

I. INTRODUCTION

Power amplifiers for the recent wireless communication systems are required to have high efficiency at large output power back-off (OBO) due to the high PAPR of the modulated signals. DPAs have been used in the base transceiver systems, because of the simple structure and high efficiency in the large OBO condition [1]–[25].

Two power states, such as low-power and peak-power levels, should be simultaneously considered for the band-

The associate editor coordinating the review of this manuscript and approving it for publication was S. M. Rezaul Hasan^(D).

width of the DPAs. The bandwidths for the two power states are generally in strong trade-off with each other. For the carrier amplifier of the conventional DPAs, the load network generally has an electrical length of 270° or more, since an impedance matching network, an offset line, and a $\lambda/4$ TL for a load modulation should be included. A large electrical length of the load network makes this trade-off worse and limits the overall bandwidth of the DPAs.

Transformer-less load modulation (TLLM) techniques have been reported to extend the bandwidth of the DPAs, and to reduce the size of the load network [11]–[13]. Akbarpour *et al.* [11] proposed a DPA that can be designed

²para-PA Inc., Suwon 16419, South Korea

³Samsung Electronics Company Ltd., Suwon 16677, South Korea



FIGURE 1. Simplified load network of the proposed DPA.

using a two-point impedance matching technique, without a $\lambda/4$ TL and an offset line at the load network. However, the design method is very complex, and the synthesized circuit was composed of multiple sections, using many lumped components for both the carrier and peaking amplifiers. Watanabe *et al.* [12] implemented a DPA using an output combining balun to remove an additional $\lambda/4$ TL and an offset line. The impedance matching network was still needed, since the output combining balun could not match the optimum impedance. Shao *et al.* [13] reported a DPA that was designed without an additional $\lambda/4$ TL and a post-matching network. However, the impedance matching network was complex and an additional offset line for electrical length control was still required.

In this paper, a quasi-lumped $\lambda/4$ ITF having simultaneous multiple functions of impedance matching and load impedance modulation with a controlled electrical length of only 90° is proposed for the load network of the DPAs. The proposed load network of the carrier amplifier has a quasilumped $\lambda/4$ ITF including the internal components of the transistor, the simplest high-pass network using only a shunt inductor, and a low-pass L-C network. The value of the shunt inductor can be adjusted to have an electrical length of the load network of 90°, while the L-section low-pass network should be accordingly tuned to match the optimum load impedance. Since the overall load network even including the internal components of the transistor has an electrical length of only 90°, the bandwidth for the load impedance modulation can be extended in the trade-off between the low-power and peak-power bandwidth. The proposed DPA was designed and implemented using GaN-HEMTs for the frequency band of 3.4 - 3.8 GHz. Experimental results using a CW signal and a 5G NR signal are presented.

II. DESIGN OF THE LOAD NETWORK

A. PROPOSED LOAD NETWORK

The electrical length of the load network affects the size of the load network and the load modulation bandwidth of the DPA. Fig. 1 shows a simplified schematic of the proposed load network of the DPA. Since the electrical length of the load network should be $90^{\circ}+n\times180^{\circ}$ for a desired load

 TABLE 1. Component values and the electrical lengths of the proposed load network for three cases.

	L_1	L_2	C_1	Electrical length
Case I	0.37 nH	0.22 nH	2.37 pF	40°
Case II	1.13 nH	0.76 nH	1.74 pF	90°
Case III	∞	0.83 nH	2.66 pF	125°

modulation, where n is an integer, including the internal components such as the output capacitance (C_{OUT}) , bondwire inductance (L_B) , and packaging capacitance (C_P) of the transistor, the internal components should be extracted first [14]. When the proposed quasi-lumped $\lambda/4$ ITF has a characteristic impedance of $\sqrt{2R_{OPT} \cdot R_L}$ and an electrical length of 90°, the load impedance at the low power level of the carrier amplifier at the current source plane, Z_C , becomes $2R_{OPT}$. Then, Z_C , at the peak power level, is converted to R_{OPT} . The load impedance toward the combining node, Z'_C , is converted from R_L at the low power level, to $2R_L$ at the peak power level. For the peaking amplifier, the load impedance at the current source plane, Z_P , becomes R_{OPT} at the peak power level. The load impedance toward the combining node, Z'_p , is converted from infinity at the low power level, to $2R_L$ at the peak power level.

The proposed load network of the carrier amplifier is composed of a high-pass network using a shunt inductor and a L-section low-pass network. This network is one of the π -type transformers which have been used for impedance matching [15]. In general, when only a L-section low-pass network is used for the impedance matching, the electrical length of the matching network cannot be controlled. However, a shunt inductor before the L-section low-pass network is deployed, which allows the electrical length to be controlled while having an optimum load impedance matching condition by adjusting the other components, L_2 and C_1 .

B. QUASI-LUMPED $\lambda/4$ ITF USING AN OPTIMIZED SHUNT INDUCTOR

For the low power level, the load impedance of the carrier amplifier, Z_C , should be $2R_{OPT}$. From this condition, the component values of L_2 and C_1 of the matching network can be derived as a function of L_1 as given in (1) and (2), as shown at the bottom of the next page, where, ω_0 is the center frequency. The electrical length of the load network of the carrier amplifier can be calculated according to the value of L_1 using the corresponding component values of L_2 and C_1 . Fig. 2 presents the calculated electrical length. For L_1 of 1.13 nH, the electrical length becomes 90° at ω_0 .

Table 1 shows the values of L_2 , C_1 , and the electrical length of the load network of the carrier amplifier for three values of L_1 . For case II using an optimum L_1 of 1.13 nH, the electrical length of the load network can be adjusted exactly to 90°. For case I using an L_1 of 0.37 nH, an additional



FIGURE 2. Calculated electrical length of the proposed load network for the various values of the shunt inductor, L_1 .



FIGURE 3. Load impedance trajectories of the proposed load network for the low power level.

offset line with an electrical length of 50° is needed to have the overall electrical length of 90°. For case III using no shunt inductor (conventional case), an additional offset line to make the overall electrical length of 270° is still needed since the electrical length of the network is already more than 90°. Fig. 3 shows the load impedance trajectories at the low power level for the three cases. For all three cases, the load impedance can be transformed from R_L of 25 Ω to $2R_{OPT}$ of 50 Ω through different trajectories using different component values.

Fig. 4 shows the simulated load impedances of the carrier amplifier on an ideal 1 dB power contour for the



FIGURE 4. Simulated load impedances on an ideal 1 dB power contour for three cases at the frequency band of 2.5 - 4.5 GHz: (a) Z_C for the low power level, and (b) Z_C for the peak power level.

three cases at the frequency band of 2.5 - 4.5 GHz. For cases I and II, a little difference in the load modulation bandwidths (600 vs. 720 MHz for the intersection between the low-power and peak-power bandwidths) can be found. However, these cases have a considerably extended load modulation bandwidth, compared to case III (320 MHz) with a total electrical length of 270° including an additional offset line. Case II has a more compact load network compared to case I, because of the absence of an additional offset line.

$$C_{1} = \frac{1}{\omega_{0}R_{L}} \sqrt{\frac{R_{L} - \operatorname{Re}\{(2R_{OPT} \parallel \frac{1}{j\omega_{0}C_{OUT}} + j\omega_{0}L_{B}) \parallel (\frac{1}{j\omega_{0}C_{P}} \parallel j\omega_{0}L_{1})\}}{\operatorname{Re}\{(2R_{OPT} \parallel \frac{1}{j\omega_{0}C_{OUT}} + j\omega_{0}L_{B}) \parallel (\frac{1}{j\omega_{0}C_{P}} \parallel j\omega_{0}L_{1})\}}},$$
(1)

$$L_{2} = \frac{\omega_{0}C_{1}R_{L}^{2} - (1 + \omega_{0}^{2}C_{1}^{2}R_{L}^{2})\operatorname{Im}\{(2R_{OPT} \parallel \frac{1}{j\omega_{0}C_{OUT}} + j\omega_{0}L_{B}) \parallel (\frac{1}{j\omega_{0}C_{P}} \parallel j\omega_{0}L_{1})\}}{\omega_{0}(1 + \omega_{0}^{2}C_{1}^{2}R_{L}^{2})},$$
(2)



FIGURE 5. Schematic of the designed DPA.



FIGURE 6. Photograph of the implemented DPA.

III. IMPLEMENTATION AND MEASUREMENT RESULTS

Fig. 5 shows a schematic of the designed DPA using the proposed load network. The shunt inductor was realized using a short-circuited stub with an electrical length of 25°. The series inductor, L_2 , was also replaced with a transmission line whose electrical length is 20.2°. The shunt capacitor, C_1 , was replaced with an open-circuited stub with an electrical length of 60.9°. The same load network was used for the peaking amplifier with an additional offset line to have the overall electrical length of 180° at ω_0 . Both the carrier and peaking amplifiers were designed using 10 W GaN-HEMT, Cree's CG2H40010F. Fig. 6 shows a photograph of the implemented DPA on a PCB using Rogers' RO4350B with a dielectric constant of 3.66. The overall circuit size is 6.6 cm \times 7.8 cm.

Fig. 7 shows the measured results of the implemented DPA using a continuous wave (CW) signal. Fig. 7(a) & (b) show



FIGURE 7. Measured performances using a CW signal: (a) Gain, and (b) DE.

the power gain and DE of the DPA, respectively. For the frequency band of 3.4 - 3.8 GHz, the implemented DPA exhibited the DE of 62 - 70% at the peak output power level of 43.6 - 44.4 dBm and the DE of 46 - 60% at the 6 dB OBO levels.

Fig. 8 shows the measured results of the implemented DPA using a 5G NR signal with signal bandwidth of 100 MHz and

TABLE 2. Performance comparison to the previous works.

Ref.	Frequency (GHz)	P _{sat} (dBm)	Pavg (dBm)	$\begin{array}{c} DE_{avg} \\ (\%) \end{array}$	ACLR** (dBc)	PAPR (dB)	Signal BW (MHz)	Signal	Device
[11]	1.96-2.46	39.8-41.7	34.4	40*	-34/NA [†]	7.3	20	WiMAX	CGH40010F
[12]	1.63-1.98	31-34	25-28 [‡]	20-49*	-25/NA [†]	9	5	WCDMA	NA
[13]	0.8-1.2	40.2-42.9	34.2-36.9 [‡]	30.3-40.1*	NA	NA	NA	NA	CGH40010F
[16]	3.4-3.6	43	35	43*	-24/-50†	LTE	20	7.2	GaN MMIC
[17]	3.3-3.55	47.5	39	50.6^{*}	-26/-46.7†	7.5	20	LTE	CGH40025 CGH40035
[18]	3.45-3.75	41.8-43.5	34.6-36.8	38.5-50.2	-24.6/NA	7.8	100	5G NR	CGH40006P CG2H40010F
[19]	3.3-4.3	43.2-44.5	37.2	48	-27/-48.9†	7.2	20	LTE	CGH60015D
[20]	2.8-3.55	43-45	38.4	56.7	-32.3/-53.7†	6.5	40	OFDM	CGH40010F
[21]	3.3-3.75	48-48.8	40.7	53	-30/NA	8	40	LTE	CGHV27030S
This work	3.4-3.8	43.6-44.4	35.8-36.6	47-54.2	-23/-42	7.8	100	5G NR	CG2H40010F

80 3.4 GH; 3 6 GH DE (%) 40 20 0-32 36 24 28 ۵'n Average output power (dBm) (a) -10 — 3.4 GHz 3.5 GH 3.6 GH ACLR (dBc) -30 3 8 GF 22 24 26 28 30 32 34 36 Average output power (dBm) (b)

FIGURE 8. Measured performances using a 5G NR signal: (a) DE, and (b) ACLR.

PAPR of 7.8 dB. Fig. 8(a) & (b) show the DE and ACLR, respectively. The implemented DPA exhibited the DE of 47 - 54.2% at an average output power level of 35.8 - 36.3 dBm with ACLR of -27.9 - 23 dBc. Fig. 9 shows the measured power spectral densities(PSDs) using a 5G NR signal before and after linearization using a digital predistortion (DPD) at an average power. Table 2 summarizes the measurement results. Compared to the previous works,

70444



*: Power-added efficiency (PAE), **: Before DPD / After DPD,

[†]: Adjacent channel power ratio (ACPR), [‡]: 6 dB OBO, NA: Not available

FIGURE 9. Measured PSDs using a 5G NR signal before and after DPD at the frequency of 3.6 GHz.

the proposed DPA using a very compact load network shows high efficiency at relatively broad bandwidth.

IV. CONCLUSION

In this paper, a compact quasi-lumped $\lambda/4$ ITF for both impedance matching and load impedance modulation with a controlled electrical length of only 90° is proposed for the load network of the DPAs. The proposed load network includes the simplest high-pass network using only a shunt inductor and a L-section low-pass network. The optimum value of the shunt inductor was selected to have an electrical length of the load network of 90° while the L-section lowpass network was accordingly matched to the optimum load impedance. The proposed DPA was designed and implemented using 10 W GaN-HEMTs for both the carrier and peaking amplifiers. Using a 5G NR signal with signal bandwidth of 100 MHz and PAPR of 7.8 dB, DE of 47 - 54.2% and ACLR of -27.9 - 23 dBc were achieved at an average output power level of 35.8 - 36.3 dBm for the broad frequency band of 3.4 - 3.8 GHz. Compared to the previous

works, this work exhibited high efficiency at relatively broad bandwidth.

REFERENCES

- B. Kim, J. Kim, I. Kim, and J. Cha, "The Doherty power amplifier," *IEEE Microw. Mag.*, vol. 7, no. 5, pp. 42–50, Oct. 2006.
- [2] Y. Yang, J. Cha, B. Shin, and B. Kim, "A fully matched N-way Doherty amplifier with optimized linearity," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 3, pp. 986–993, Mar. 2003.
- [3] Y. Yang, J. Yi, Y. Y. Woo, and B. Kim, "Optimum design for linearity and efficiency of a microwave Doherty amplifier using a new load matching technique," *Microw. J.*, vol. 44, no. 12, pp. 20–36, Dec. 2001.
- [4] H. Kang, W. Lee, S. Oh, H. Oh, W. Choi, H. Lee, K. C. Hwang, K.-Y. Lee, and Y. Yang, "Optimized broadband load network for Doherty power amplifier based on bandwidth balancing," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 3, pp. 280–283, Mar. 2021.
- [5] H. Lee, W. Lim, J. Bae, W. Lee, H. Kang, K. C. Hwang, K.-Y. Lee, C.-S. Park, and Y. Yang, "Highly efficient fully integrated GaN-HEMT Doherty power amplifier based on compact load network," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 12, pp. 5203–5211, Dec. 2017.
- [6] G. Lv, W. Chen, X. Liu, F. M. Ghannouchi, and Z. Feng, "A fully integrated C-band GaN MMIC Doherty power amplifier with high efficiency and compact size for 5G application," *IEEE Access*, vol. 7, pp. 71665–71674, 2019.
- [7] W. Choi, H. Kang, H. Oh, K. C. Hwang, K.-Y. Lee, and Y. Yang, "Doherty power amplifier based on asymmetric cells with complex combining load," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 4, pp. 2336–2344, Apr. 2021.
- [8] J. Nan, H. Wang, M. Cong, and W. Yang, "A broadband Doherty power amplifier with a new load modulation network," *IEEE Access*, vol. 9, pp. 58025–58033, 2021.
- [9] H.-Y. Liu, X.-H. Fang, and K.-K.-M. Cheng, "Bandwidth enhancement of frequency dispersive Doherty power amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 2, pp. 185–188, Feb. 2020.
- [10] J. J. M. Rubio, V. Camarchia, M. Pirola, and R. Quaglia, "Design of an 87% fractional bandwidth Doherty power amplifier supported by a simplified bandwidth estimation method," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 3, pp. 1319–1327, Mar. 2018.
- [11] M. Akbarpour, M. Helaoui, and F. M. Ghannouchi, "A transformerless load-modulated (TLLM) architecture for efficient wideband power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 9, pp. 2863–2874, Sep. 2012.
- [12] S. Watanabe, Y. Takayama, R. Ishikawa, and K. Honjo, "A miniature broadband Doherty power amplifier with a series-connected load," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 572–579, Feb. 2015.
- [13] J. Shao, R. Zhou, H. Ren, B. Arigong, M. Zhou, H. S. Kim, and H. Zhang, "Design of GaN Doherty power amplifiers for broadband applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 4, pp. 248–250, Apr. 2014.
- [14] H. Kang, H. Lee, W. Lee, H. Oh, W. Lim, H. Koo, C.-S. Park, K. C. Hwang, K.-Y. Lee, and Y. Yang, "Octave bandwidth Doherty power amplifier using multiple resonance circuit for the peaking amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 2, pp. 583–593, Feb. 2019.
- [15] A. Grebennikov, *RF and Microwave Power Amplifier Design*. New York, NY, USA: McGraw-Hill, 2004.
- [16] S. Maroldt and M. Ercoli, "3.5-GHz ultra-compact GaN class-E integrated Doherty MMIC PA for 5G massive-MIMO base station applications," in *Proc. 12th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Oct. 2017, pp. 196–199.
- [17] J. Zhou, W. Chen, L. Chen, and Z. Feng, "3.5–0Hz high-efficiency broadband asymmetric Doherty power amplifier for 5G applications," in *Proc. Int. Conf. Microw. Millim. Wave Technol. (ICMMT)*, May 2018, pp. 1–3.
- [18] Y. C. Choi, W. Choi, H. Oh, Y. Chen, J. Shin, H. Jeon, K. C. Hwang, K.-Y. Lee, and Y. Yang, "Doherty power amplifier with extended highefficiency range based on the utilization of multiple output power backoff parameters," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 4, pp. 2258–2270, Apr. 2022.
- [19] C. Shen, S. He, X. Zhu, J. Peng, and T. Cao, "A 3.3–4.3-GHz highefficiency broadband Doherty power amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 11, pp. 1081–1084, Nov. 2020.

- [20] M. Li, J. Pang, Y. Li, and A. Zhu, "Bandwidth enhancement of Doherty power amplifier using modified load modulation network," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 6, pp. 1824–1834, Jun. 2020.
- [21] C. Huang, S. He, and F. You, "Design of broadband modified class-J Doherty power amplifier with specific second harmonic terminations," *IEEE Access*, vol. 6, pp. 2531–2540, 2018.
- [22] A. Grebennikov, "Multiband Doherty amplifiers for wireless applications," *High Freq. Electron.*, vol. 13, pp. 30–46, May 2014.
- [23] Z. Yang, Y. Yao, M. Li, Y. Jin, T. Li, Z. Dai, F. Tang, and Z. Li, "Bandwidth extension of Doherty power amplifier using complex combining load with noninfinity peaking impedance," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 2, pp. 765–777, Feb. 2019.
- [24] X. Y. Zhou, W. S. Chan, W. Feng, X. Fang, T. Sharma, and S. Chen, "Broadband Doherty power amplifier based on coupled phase compensation network," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 1, pp. 210–221, Jan. 2022.
- [25] Y. Xu, J. Pang, X. Wang, and A. Zhu, "Enhancing bandwidth and backoff range of Doherty power amplifier with modified load modulation network," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 4, pp. 2291–2303, Apr. 2021.



KUHYEON KWON was born in Boryeong, South Korea, in 1996. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, in 2021. He is currently pursuing the M.S. degree with the Department of Electrical and Computer Engineering, Sungkyunkwan University. His current research interests include design of RF power amplifiers for base stations, broadband techniques, and MMICs.



WOOJIN CHOI was born in Siheung, South Korea, in 1993. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, in 2018. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Sungkyunkwan University. His current research interests include design of RF power amplifiers for base stations, broadband techniques, and MMICs.



JAEKYUNG SHIN was born in Seoul, South Korea, in 1993. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Korea Aerospace University, Goyang, South Korea, in 2018. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, South Korea. His current research interests include design of RF/mm-wave power amplifiers, efficiency enhancement techniques,

broadband techniques, and microwave power transmission.



YIFEI CHEN was born in Hebei, China, in 1994. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Korea University, Seoul, South Korea, in 2018. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, South Korea. His current research interests include design of RF/mm-wave power amplifiers, broadband techniques, and mm-wave integration circuits.



YOUNG CHAN CHOI was born in Seoul, South Korea, in 1996. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, in 2020. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Sungkyunkwan University. His research interests include design of RF/mm-wave power amplifiers, efficiency enhancement techniques, linearization techniques,

broadband techniques, and mm-wave integrated circuits and systems.



SOONCHEOL BAE was born in Daegu, South Korea, in 1995. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, in 2019. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Sungkyunkwan University. His current research interests include design of RF/mm-wave power amplifiers, RF and analog integrated circuits, and wireless power transfer.



HYEONGJIN JEON was born in Mokpo, South Korea, in 1994. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, in 2020. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Sungkyunkwan University. His research interests include design of RF/mm-wave power amplifiers, efficiency enhancement techniques, linearization techniques,

broadband techniques, and mm-wave integrated circuits and systems.



JIWON HWANG was born in Seongnam, South Korea, in 1995. She received the B.S. degree from the Department of Information and Communication Engineering, Namseoul University, South Korea, in 2019. She is currently pursuing the M.S. degree with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, South Korea. Her current research interests include design of RF/mm-wave power amplifiers, broadband techniques, and mm-wave integration circuits.



SEUNGMIN WOO was born in Daegu, South Korea, in 1996. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, in 2021. He is currently pursuing the M.S. degree with the Department of Electrical and Computer Engineering, Sungkyunkwan University. His current research interests include design of RF power amplifiers for base stations, broadband techniques, and MMICs.



YOUNG YUN WOO received the Ph.D. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2007. In 2007, he joined Samsung Electronics and has been working on the H/W Research and Development Group. His current research interests include 5G RF PA design, DPD linearization techniques, and 5G RF advanced techniques.



KANG-YOON LEE (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Seoul National University, Seoul, Korea, in 1996, 1998, and 2003, respectively. From 2003 to 2005, he was with GCT Semiconductor Inc., San Jose, CA, USA, where he was the Manager of the Analog Division and worked on the design of CMOS frequency synthesizer for CDMA/PCS/PDC and single-chip CMOS RF chip sets for W-CDMA,

WLAN, and PHS. From 2005 to 2011, he was with the Department of Electronics Engineering, Konkuk University, as an Associate Professor. Since 2012, he has been with the Department of Electrical and Computer Engineering, Sungkyunkwan University, South Korea, where he is currently an Associate Professor. His research interests include implementation of power integrated circuits, CMOS RF transceiver, analog integrated circuits, and analog/digital mixed-mode VLSI system design.



KEUM CHEOL HWANG (Senior Member, IEEE) received the B.S. degree in electronics engineering from Pusan National University, Busan, South Korea, in 2001, and the M.S. and Ph.D. degrees in electrical and electronic engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2003 and 2006, respectively. From 2006 to 2008, he was a Senior Research Engineer at the Samsung Thales, Yongin, South Korea, where he was

involved with the development of various antennas including multiband fractal antennas for communication systems and Cassegrain reflector antenna and slotted waveguide arrays for tracking radars. He was an Associate Professor with the Division of Electronics and Electrical Engineering, Dongguk University, Seoul, South Korea, from 2008 to 2014. In 2015, he joined the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, South Korea, where he is currently an Associate Professor. His research interests include advanced electromagnetic scattering and radiation theory and applications, design of multiband/broadband antennas and radar antennas, and optimization algorithms for electromagnetic applications. He is a Life Member of KIEES and a member of IEICE.



YOUNGOO YANG (Senior Member, IEEE) was born in Hamyang, South Korea, in 1969. He received the Ph.D. degree in electrical and electronic engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2002. From 2002 to 2005, he was with Skyworks Solutions, Inc., Newbury Park, CA, USA, where he designed power amplifiers for various cellular handsets. Since 2005, he has been with the School of Information and Communication Engineering,

Sungkyunkwan University, Suwon, South Korea. His research interest includes RF power amplifiers.