IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 30 May 2022, accepted 20 June 2022, date of publication 29 June 2022, date of current version 8 July 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3187005

RESEARCH ARTICLE

Single-Input Quadruple-Boosting Switched-Capacitor Nine-Level Inverter With Self-Balanced Capacitors

KAZEM VARESI[1], FATEMEH ESMAEILI[1], SAEID DELIRI[1], AND HADI TARZAMNI[2], (Student Member, IEEE)

[1]Faculty of Electrical Engineering, Sahand University of Technology, Tabriz 51335-1996, Iran
[2]Department of Electrical Engineering and Automation, Aalto University, 02150 Espoo, Finland

Corresponding author: Hadi Tarzamni (hadi.tarzamni@aalto.fi)

This work was supported by the Finnish Electronic Library (FinElib), Finland, under the FinELib Consortium's Agreement with IEEE.

ABSTRACT This paper suggests a single-input switched-capacitor Nine-level inverter configuration advantaging from quadruple voltage-boosting ability, natural voltage balancing of capacitors, and reduced components per level. Also, the single-source character of the proposed topology makes it cheaper and more compact. The cascaded version of the suggested topology has also been introduced, by which high boosting factors, as well as large number of steps, can be obtained. The proposed topology can effectively supply the resistive-inductive or pure inductive load types. The capacitors' impulsive-charging-current issue has been solved by simple small-inductance-based inductor-diode (L-D) networks. The comparative analysis affirms the fewer device-usage in suggested configuration per equal gain or level count than existed structures, resulting in less size and cost. The usage of Nearest-Level modulation guarantees the low-frequency operation of semiconductors and reduces the switching losses. The comparative analysis and experimental outcomes affirm the competitiveness and accurate functionality of suggested configuration.

INDEX TERMS Multilevel inverter, number of levels, self-balanced capacitors, switched-capacitor, voltage gain.

I. INTRODUCTION

The Multi-Level Inverters (MLI)s are well-known for high-quality output voltage and low voltage stress on switching devices [1]. The conventional MLIs are mainly categorized as: A) Cascaded H-Bridge (CHB), B) Diode-Clamped (DC), and C) Floating-Capacitor (FC) inverters. The CHB inverters produce many voltage steps but have no voltage boosting ability and usually require numerous DC supplies and power semiconductors [2]–[4]. Also, the DC and FC inverters demand more clamping-diodes, DC-link, or floating-capacitors to acquire increased-levels. The requirement of voltage sensors and complex strategies for balancing the charge of capacitors is another shortcoming of NPC and FC inverters [5], [6].

The associate editor coordinating the review of this manuscript and approving it for publication was Zhilei Yao.

To increase the number of voltage steps in MLIs, more DC supplies, semiconductors, and driver circuits are required, which leads to a bulky, heavy, and costly converter. So, many studies have focused on presenting reduced-component structures like [7], [8]. In [9], the authors aimed to decrease the semiconductors (and gate-driver circuits). As aimed in [10], [11], reducing the number of DC supplies (as large and expensive parts) is more beneficial than other components. The utilization of Switched-Capacitor Cells (SCCs) in MLIs can provide a higher number of levels without the need to increase DC sources. This critical feature improves output voltage quality and simultaneously keeps the converter as compact/cheap as possible [12], [13]. From viewpoint of voltage boosting ability, the Switched-Capacitor Multi-Level Inverters (SCMLIs) are classified into boost (step-up), step-down or unity-gain categories. The [14], [15] present two step-down converters, where the peak voltage ($V_{o,max}$) is lower than total inputs. The topologies presented in [16]–[19] are examples of unity-gain converters with equal peak output voltage and summation of input sources. Usually, the MLIs utilizing capacitors only in DC-link(s) produce unity gain. But, the step-up or boost SCMLIs like [11], [20]–[24] have voltage boosting ability and can produce larger voltage than total inputs. The voltage boosting ability becomes very vital for grid-tied SCMLIs fed by Photovoltaics (PVs) or Fuel Cells (FCs), where the input voltage(s) is (are) much less than the grid voltage [25], [26]. The semiconductors' blocking-voltage is relatively high in step-up SCMLIs that may impact the price and efficiency of converter [27]. For the applications where significant step-up capability is not required, mild or low-gain structures with low voltage stress are preferred [28].

The SCMLIs usually realize the bipolar waveform through the conventional or developed H-bridge, two half-bridges, or inherently. The topologies presented in [29]–[31] apply an H-bridge unit, whose switches must tolerate $V_{o,max}$. The [32] employs a developed H-bridge for negative voltage level generation, where two switches tolerate the maximum output voltage. The generation of a bipolar waveform in [33] is achieved inherently, but four switches suffer from voltage stress of $V_{o,max}$. The [34], [35] use two half-bridges for a negative voltage-level generation. Accordingly, 2 and 0 switches tolerate $V_{o,max}$ respectively in [34], [35]. Similar to [29]–[31] and due to application of the H-bridge in [36], four switches withstand the $V_{o,max}$. The structures with a larger number of switches tolerating $V_{o,max}$, suffer from large Total Voltage Stress (TVS) on semiconductors. The [30], [31], [33]–[36] outputs nine voltage levels through a single DC source, while the [32] requires two input sources. The application of more sources negatively impacts the converter's overall size, cost and weight. The [37] presents a double-input two H-bridge-based switched-capacitor 27-level topology that gives a gain of 1.3. The TVS of semiconductors in [37] is relatively low, and none of them tolerate the $V_{o,max}$.

This article suggests a single-source 9-level switched-capacitor inverter that is capable of providing quadruple voltage-gain. The large boosting capability, capacitors' natural charge balancing as well as fundamental frequency operation of H-bridge switches are distinguished features of suggested inverter. In the following, the suggested basic and cascaded topologies are introduced and explained in Sections II and III. The design consideration of capacitors, suppression of capacitors' charging current, and modulation strategy are presented in Sections IV-VI. Section VII provides the comparative analysis. The loss analysis is done in Section VIII. Finally, implemented set-up results and conclusion are given in Sections IX and X, respectively.

II. PROPOSED 9-LEVEL INVERTER

The proposed switched-capacitor-based inverter (shown in Fig. 1) is composed of level generation and polarity generation units. The level generation unit is formed of a single DC source, single-diode, two capacitors, and seven switches (MOSFETs), as (1). The S_1 - S_2 are bidirectional common-source switches. The others are unidirectional switches. The end-side H-bridge plays the role of the polarity generation unit.

$$N_{Source} = 1, \quad N_{Switch} = N_{Driver} = 11, \; N_{MOSFET} = 13,$$
$$N_{Capacitor} = 2, \quad N_{Diode} = 1, \; N_{Component} = 26 \tag{1}$$

TABLE 1. Switching pattern and charge/discharge of C_1-C_2.

$S_1 S_2 S_3 S_4 S_5 S_6 S_7 H_1 H_2 H_3 H_4 D_1$	V_o	C_1	C_2
000100001011	0	▲	-
000100010101	0	▲	-
100100010011	$+V_{dc}$	▲	-
100100001101	$-V_{dc}$	▲	-
011001110010	$+2V_{dc}$	▼	▲
011001101100	$-2V_{dc}$	▼	▲
000110110011	$+3V_{dc}$	▲	▼
000110101101	$-3V_{dc}$	▲	▼
001010110010	$+4V_{dc}$	▼	▼
001010101100	$-4V_{dc}$	▼	▼

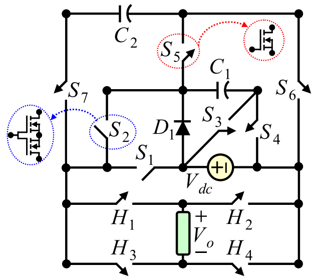


FIGURE 1. Proposed 9-level inverter.

Table 1 shows different switching states of switches, forward/reverse bias of D_1 diode, and charge/discharge mode of C_1-C_2 capacitors. The green up and red down symbols represent the charging and discharging modes, respectively. Fig. 2 displays various operational modes of the suggested circuit. As seen, the positive and negative voltage steps are generated respectively by turning on the (H_1, H_4) and (H_2, H_3) switch pairs. Also, there is only one redundant state, which leads to zero voltage level.

States **1-2 (Figs. 2(a) and 2(b)):** During zero voltage level generation ($V_o = 0$), the input-source charges the C_1 ($v_{C1} = V_{dc}$) through D_1 and S_4.

States **3-4 (Figs. 2(c) and 2(d)):** The $V_o = \pm V_{dc}$ voltage levels are produced by the input DC source. Simultaneously the C_1 capacitor keeps on being charged by the input DC source.

States **5-6 (Figs. 2(e) and 2(f)):** The $V_o = \pm 2V_{dc}$ voltage steps are generated by a series connection of input source and C_1 capacitor. At the same time, The C_2 capacitor is paralleled with the cascaded input source and C_1 capacitor. So, the C_2 capacitor is charged to $v_{C2} = V_{dc} + v_{C1} = 2V_{dc}$.

States **7-8 (Figs. 2(g) and 2(h)):** In order to synthesize the $V_o = \pm 3V_{dc}$ on the load, the input source is cascaded with C_2 capacitor. Meanwhile, the parallel connection of the input source and C_1 capacitor keeps its voltage on $v_{C1} = V_{dc}$.

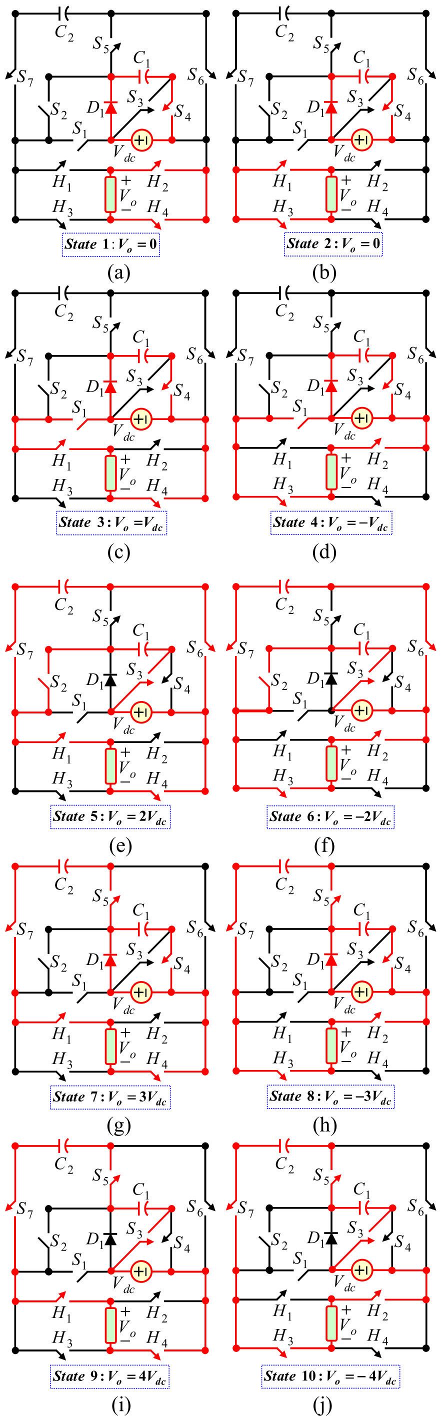


FIGURE 2. Operational-modes of suggested 9-level inverter. (a) State 1: $V_o = 0$, (b) State 2: $V_o = 0$, (c) State 3: $V_o = V_{dc}$, (d) State 4: $V_o = -V_{dc}$, (e) State 5: $V_o = 2V_{dc}$, (f) State 6: $V_o = -2V_{dc}$, (g) State 7: $V_o = 3V_{dc}$, (h) State 8: $V_o = -3V_{dc}$, (i) State 9: $V_o = 4V_{dc}$, (j) State 10: $V_o = -4V_{dc}$.

***States* 9-10 (Figs. 2(i) and 2(j)):** Finally, the $V_o = \pm 4V_{dc}$ voltage steps are provided by cascading the input DC source, C_1 and C_2 capacitors.

Table 1 and Fig. 2 show that the suggested converter can produce 9 voltage steps (including 0, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$ and $\pm 4V_{dc}$) with a maximum output voltage of $V_{o,max} = 4V_{dc}$. So, the voltage gain (G) of the suggested topology is

TABLE 2. Voltage stress on semiconductors.

Semiconductor	Voltage Stress	Semiconductor	Voltage Stress
S_1	$3V_{dc}$	S_7	$3V_{dc}$
S_2	$2V_{dc}$	H_1	$4V_{dc}$
S_3	V_{dc}	H_2	$4V_{dc}$
S_4	V_{dc}	H_3	$4V_{dc}$
S_5	$2V_{dc}$	H_4	$4V_{dc}$
S_6	$2V_{dc}$	D_1	V_{dc}

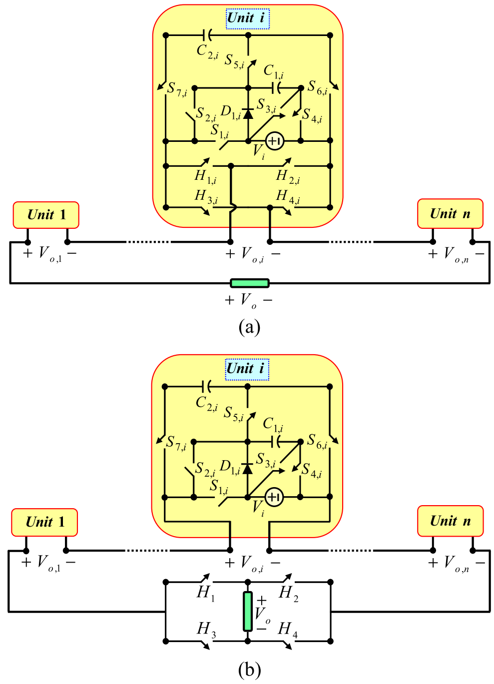


FIGURE 3. Suggested extended configurations: (a) First version (T_1), (b) Second version (T_2).

equal to 4. Also, as shown in (2), the C_1 and C_2 capacitors are charged to V_{dc} and $2V_{dc}$, respectively.

$$V_{C_1} = V_{dc}, \quad V_{C_2} = 2\,V_{dc}, \; V_{o,\max} = 4\,V_{dc}, \\ G = \left(V_{o,\max}/V_{dc}\right) = 4 \tag{2}$$

The Voltage Stress (VS) on the semiconductors has been shown in Table 2. The H-bridge switches tolerate the $V_{o,max}$, but operate at low-frequencies, leading to limited switching losses.

III. PROPOSED CASCADED STRUCTURES

According to Fig. 3, the suggested basic 9-level inverter can be extended in two forms to achieve an increased number of levels: First extended topology (T_1), which employs multiple H-bridges (Fig. 3(a)), and Second extended topology (T_2) that applies single H-bridge (Fig. 3(b)). These structures are explained in the following.

A. 1^{ST} EXTENDED TOPOLOGY (T_1)

As evident from Fig. 3(a), the number of required devices in proposed first extended topology are as (3):

$$N_{Source} = n, \quad N_{Switch} = N_{Driver} = 11n, \; N_{MOSFET} = 13n,$$

$$N_{Capacitor} = 2n, \quad N_{Diode} = n, \; N_{Component} = 26n \tag{3}$$

For level-count maximization, the DC-sources' voltage is decided as (4). The DC-sources' variety is n.

$$V_1 = V_{dc}, \quad V_i = 9^{i-1} V_{dc} \tag{4}$$

where, the $V_{o,max\,j}$ denotes the maximum output voltage of j^{th} cascaded unit. Also, the V_i represents the input source of i^{th} cascaded unit ($i = 1, 2, \cdots, n$).

The maximum output voltage of each unit, as well as the whole cascaded structure, are computed as (5).

$$V_{o,\max_i} = 4\,V_i = 4(9)^{i-1} V_{dc},$$
$$V_{o,\max} = \sum_{i=1}^{n} V_{o,\max_i} = \frac{(9^n - 1)\,V_{dc}}{2} \tag{5}$$

The voltage-levels and gain are as (6)-(7), respectively.

$$N_{Level} = 9^n \tag{6}$$
$$G = (V_{o,\max} / \sum_{i=1}^{n} V_i) = 4 \tag{7}$$

The TVS for first extended topology is calculated from (8).

$$TVS = \sum VS_{S,H,D} = \frac{30}{8}(9^n - 1)\;V_{dc} \tag{8}$$

The Average Voltage Stress (AVS) on switches/diodes of first extended topology is as (9).

$$AVS = \frac{TVS}{N_{Switch} + N_{Diode}} = \frac{30}{96n}(9^n - 1)\;V_{dc} \tag{9}$$

B. 2ND EXTENDED TOPOLOGY (T_2)

The 2nd extended structure is shown in Fig. 3(b). The number of different components has been presented in (10).

$$N_{Source} = n, \quad N_{Switch} = N_{Driver} = 7n + 4, \; N_{Diode} = n,$$
$$N_{Capacitor} = 2n, \quad N_{MOSFET} = 9n + 4, \; N_{Component} = 18n + 8 \tag{10}$$

For level-count maximization in 2nd extended structure, the size of DC-sources is decided as (11).

$$V_1 = V_{dc}, \quad V_i = 5^{i-1} V_{dc} \tag{11}$$

The peak output voltage of each unit and the total output voltage are shown in (12).

$$V_{o,\max_i} = 4\,V_i = 4(5)^{i-1} V_{dc},$$
$$V_{o,\max} = \sum_{i=1}^{n} V_{o,\max_i} = (5^n - 1)\,V_{dc} \tag{12}$$

According to (12), the level-count and gain of 2nd extended structure is computed respectively from (13) and (14).

$$N_{Level} = 2(5)^n - 1 \tag{13}$$
$$G = (V_{o,\max} / \sum_{i=1}^{n} V_i) = 4 \tag{14}$$

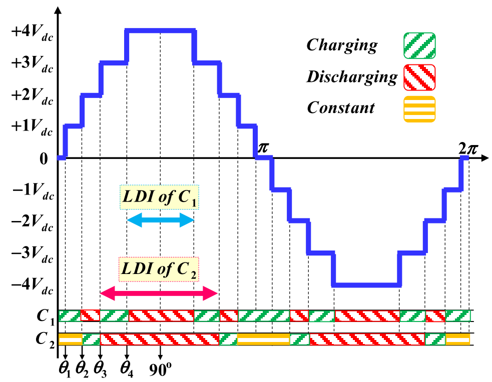


FIGURE 4. Charge/discharge intervals of C1-C2 capacitors.

The TVS and AVS of the second extended topology are obtained respectively from (15) and (16).

$$TVS = \frac{30}{4}(5^n - 1)\,V_{dc} \tag{15}$$
$$AVS = \frac{30}{4(8n + 4)}(5^n - 1)\,V_{dc} \tag{16}$$

IV. DESIGN OF CAPACITORS

The proper determination of capacitances leads to low voltage ripple and power loss in capacitors. The capacitors are designed such that their voltage ripple during Longest Discharge Interval (LDI) be limited to the desired value (ΔV_C). According to Fig. 4, the LDI of C_1 capacitor occurs during the generation of $\pm 4V_{dc}$. Also, the LDI of C_2 capacitor happens at $\pm 3V_{dc}$ and $\pm 4V_{dc}$. The beginning and ending of LDI of C_1 capacitor are θ_4 and π - θ_4, respectively. Also, the LDI of C_2 capacitor starts at θ_3 and finishes at π-θ_3. So, the duration of LDI of C_1 - C_2 capacitors are $\theta_{C1} = \pi$-$2\theta_4$ and $\theta_{C2} = \pi$ - $2\theta_3$, respectively.

From (17), the capacitances are determined to limit their voltage-ripple to ΔV_C. Note that $I_{o,max}$: maximum load current, θ_C: duration of LDI of C capacitor, $\cos\varphi$: load power-factor, f: fundamental-frequency, ΔV_C: capacitor's voltage-ripple.

$$C \geq \frac{I_{o,\max} \cos\varphi \sin(\theta_C/2)}{\pi f \,\Delta\, V_C} \tag{17}$$

V. SUPPRESSION OF CAPACITORS' CHARGING CURRENT

The capacitors' impulse charging current is one of the main challenges associated with switched-capacitor-based multi-level inverters, which subject the semiconductors to large current stress and increase the losses. In this study, the C_i's charging-current is restricted by inductor-diode (L_i - D_i') cells, as Fig. 5. The presented equivalent circuits show that the limiting inductors (L_i)s are place on the charging path of capacitors, leading to lower charging currents. But, at discharging modes, these charge-limiting inductors are bypassed by the reverse diodes (D_i)s.

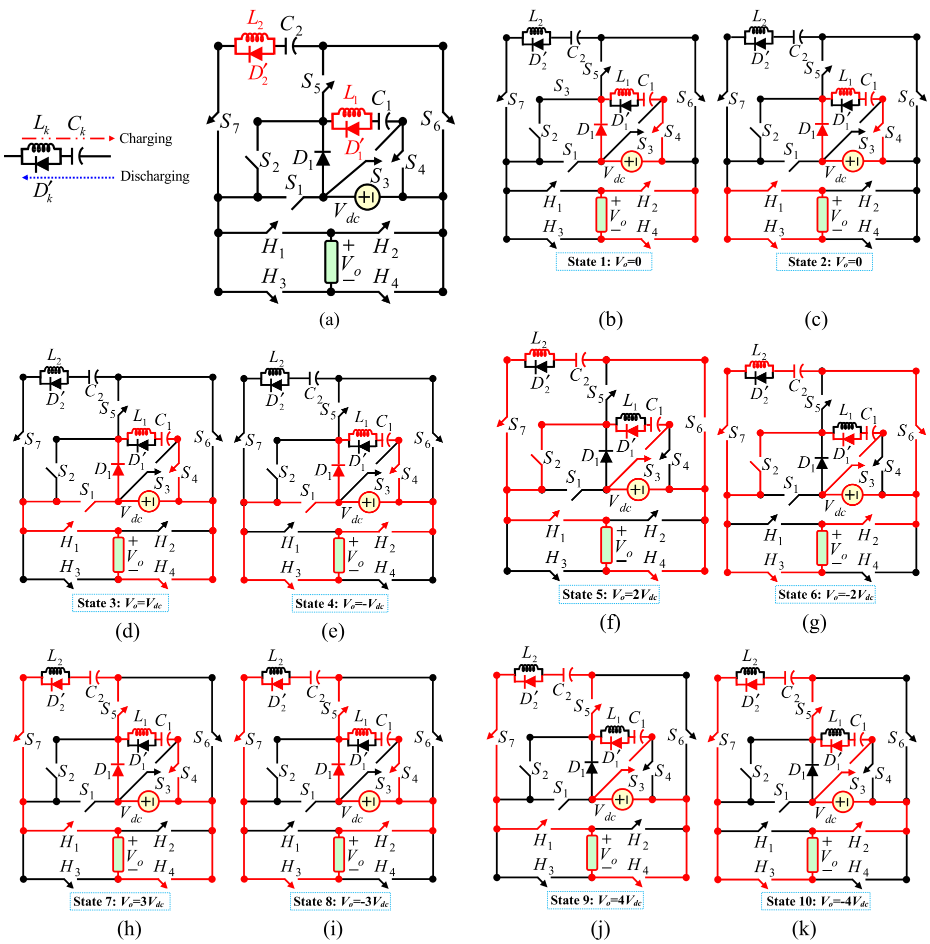


FIGURE 5. **Proposed inverter and its operational modes in presence of inrush-current limiting cells. (a) Proposed configuration. (b) State 1: $V_o = 0$, (c) State 2: $V_o = 0$, (d) State 3: $V_o = V_{dc}$, (e) State 4: $V_o = -V_{dc}$, (f) State 5: $V_o = 2V_{dc}$, (g) State 6: $V_o = -2V_{dc}$, (h) State 7: $V_o = 3V_{dc}$, (i) State 8: $V_o = -3V_{dc}$, (j) State 9: $V_o = 4V_{dc}$, (k) State 10: $V_o = -4V_{dc}$.**

VI. NEAREST LEVEL MODULATION (NLM)

In recent years many different modulation techniques have been presented for MLIs. This paper employs the "Fundamental Frequency" or "Nearest Level" modulation technique, which profits from generality, simplicity, ease of implementation, fast operation speed and low-frequency operation of semiconductors, and reduced switching losses [9]. A sinusoidal reference ($V_{ref} = A_r \sin(\omega t)$) waveform with an amplitude of A_r and frequency of $f = \omega/2\pi = 50$[Hz] is compared with producible levels (0, $\pm V_{dc}$, $\pm 2V_{dc}, \cdots, \pm N_P V_{dc}$), where $0 < A_r \leq N_P$ and the N_P denotes the maximum positive level. The control block diagram of "Nearest Leve" modulation techniques as well as resulted switching pulses have been shown in Fig. 6. It is seen that the H-bridge switches (H_1 - H_4) operate at fundamental frequency. The other remaining semiconductors also operate at low frequencies.

VII. COMPARISONS

This part compares the suggested topologies with existed SCMLIs from viewpoints of level and device count, voltage-stress on semiconductors, voltage-boosting capability and efficiency. In Table 3, the suggested basic 9-level inverter is compared with similar 9-level inverters.

As seen, the proposed basic topology requires fewer total switches and diodes than other counterparts for producing 9 levels. Among selected topologies, the [32] utilizes two DC-sources, while the others and suggested basic configuration use on a single DC source. Table 3 confirms that the proposed basic topology employs only two capacitors (the same as [32], [35]), while the others use 3 capacitors. According to Table 3, the proposed basic topology and [31], [32], [34] use minimum total devices, where the [22] utilize maximum devices. As seen from Table 3, the TVS on semiconductors of suggested basic inverter is higher than other counterparts, which is considered as its main drawback. Among selected topologies, the [22] has the least maximum voltage stress ($= 0.25V_{o,max}$) on its semiconductors than other structures. The maximum voltage gain (quadruple gain) belongs to proposed basic inverter and [22], [30], [31], [34], [35], where the [32] has the least gain (double gain).

Based on Table 3, none of semiconductors in [22], [35] tolerate $V_{o,max}$. In [32], [34] two semiconductors tolerate $V_{o,max}$, while this amount in proposed basic inverter and [30], [31]

TABLE 3. Comparison results of basic 9-level topologies.

Topology	N_{Level}	$N_{SW}+N_D$	N_{DC}	N_C	N_{TC}	TVS	TVS_{pu}	MVS	$V_{o,max}$	Gain	NMB	Efficiency	Negative level generation
[22]	9	22	1	3	45	$19V_{dc}$	4.75	$0.25V_{o,max}$	$4V_{dc}$	4	0	88.9% @74W	Inherent
[30]	9	13	1	3	27	$25V_{dc}$	6.25	$V_{o,max}$	$4V_{dc}$	4	4	91.5% @138W	H-Bridge
[31]	9	14	1	3	26	$26V_{dc}$	6.5	$V_{o,max}$	$4V_{dc}$	4	4	91.6% @60W	H-Bridge
[32]	9	12	2	2	26	$22V_{dc}$	5.5	$V_{o,max}$	$4V_{dc}$	2	2	90-94.5% @50-500W	Developed H-Bridge
[34]	9	11	1	3	26	$24V_{dc}$	6	$V_{o,max}$	$4V_{dc}$	4	2	96-97.7% @5-50W	2 Half-Bridges
[35]	9	12	1	2	27	$21V_{dc}$	5.25	$0.5V_{o,max}$	$4V_{dc}$	4	0	97.9% @160W	2 Half-Bridges
Proposed	9	12	1	2	26	$31V_{dc}$	7.75	$V_{o,max}$	$4V_{dc}$	4	4	87-95.5% @10-390W	H-Bridge

N_{Level}: Number of levels, **N_{SW}:** Number of switches, **N_D:** Number of diodes, **N_{DC}:** Number of sources, **N_C:** Number of capacitors, **N_{TC}:** Number of total components, **TVS:** Total voltage stress, **N_{Var}:** Number of DC sources variety, **$V_{o,max}$:** Maximum output voltage, **G:** voltage gain, **NMB:** Number of switches tolerating $V_{o,max}$

TABLE 4. Comparison results of extended topologies.

Type	Topology	N_{level}	N_{sw}	N_{GD}	N_C	TVS/V_{dc}	N_D	N_{DC}	$V_{o,max}$	N_{TC}	N_{Var}	G	NMB
Asymmetric	[38]	$(2n+3)^2$	$4n+8$	$4n+8$	$2n$	$20n^2+44n+16$	$2n$	2	$2n^2+6n+4$	$12n+18$	2	$n+1$	2
	[39]	$2(3^n)(3^n+2)+1$	$10n+8$	$10n+8$	4n	$\left(3^n+2\right)\left(\frac{13(3^n)-5}{2}\right)$	$2n$	2	$3^n(3^n+2)$	$26n+18$	2		0
	[36]	$2^{n+1}+1$	$3n+3$	$3n+3$	n	$7(2^n)-3$	1	1	2^n	$7n+8$	1	2^n	4
	[30]	5^n	$6n$	$6n$	n	$5(5^n-1)/2$	n	n	$(5^n-1)/2$	$15n$	n	2	0
	Proposed T_1	9^n	$11n$	$11n$	$2n$	$30(9^n-1)/8$	n	n	$(9^n-1)/2$	$26n$	n	4	0
	Proposed T_2	$2(5)^n-1$	$7n+4$	$7n+4$	$2n$	$30(5^n-1)/4$	n	n	5^n-1	$18n+8$	n	4	4
Symmetric	[33]	$8n+1$	$6n+2$	$6n+2$	$2n$	$16n+8$	n	n	$4n$	$16n+4$	1	2	2
	[10] 1SC	$4n+1$	$2n+8$	$2n+8$	1	$\frac{12n-2}{n}$	-	n	$2n$	$5n+17$	1	2	0
	[10] 2SC	$6n+1$	$2n+14$	$2n+14$	2	$\frac{18n-2}{n}$	-	n	$3n$	$5n+30$	1	3	0
	[40]	$6n+1$	$11n$	$11n$	$2n$	$16n$	0	n	$3n$	$25n$	1	3	0
	[28]	$8n+1$	$10n$	$10n$	$2n$	$11n$	0	n	$4n$	$23n$	1	2	0
	[41]	$4n+1$	$9n$	$9n$	n	$9n$	0	n	$2n$	$20n$	1	2	0
	Proposed P_1	$8n+1$	$11n$	$11n$	$2n$	$31n$	n	n	$4n$	$26n$	1	4	0

N_{Level}: Number of levels, **N_{SW}:** Number of switches, **N_D:** Number of diodes, **N_{DC}:** Number of sources, **N_C:** Number of capacitors, **N_{TC}:** Number of total components, **TVS:** Total voltage stress, **N_{Var}:** Number of DC sources variety, **$V_{o,max}$:** Maximum output voltage, **G:** voltage gain, **NMB:** Number of switches tolerating $V_{o,max}$

is four. Based on Table 3, none of semiconductors in [22], [35] tolerate $V_{o,max}$. In [32], [34] two semiconductors tolerate $V_{o,max}$, while this amount in proposed basic inverter and [30], [31] is four.

Table 3 presents and compares the efficiency of proposed converter with that of [22], [30]–[35]. As seen, the efficiency of topologies presented in [22], [30] and [31] are 88.9%, 91.5%, and 91.6%, respectively at 74[W], 138[W], and 60[W]. The efficiency of proposed converter in this range of output power is about 90.9% to 93.5%, which is higher than the reported efficiency of [22], [30], [31]. The reported efficiency range of [32] across output power range of 50[W] to 500[W] is [90%-94.5%]. During almost the same output power range, the efficiency of proposed topology is about 90.6% to 95.5%, which is slightly higher than that of [32]. Meanwhile, the reported efficiencies of topologies presented in [34], [35] are higher than the efficiency of proposed converter.

The proposed basic inverter and [30], [31] use an H-bridge, while the [32] use a developed H-bridge and [34], [35] employ two half-bridges for negative voltage generation. This feature is realized inherently in [22].

The proposed cascaded inverter and generalized counterparts presented in [10], [28], [30], [33], [36], [38]–[41] are compared in Table 4. Fig. 7 present the comparison results as plots. The topologies presented in [38], [39] utilize 2 DC sources, but the proposed topology (T_1, T_2 and P_1) and [10], [28], [30], [33], [36], [40], [41] demand only a single DC source at basic version. This further decreases the overall weight, expense and volume of the converter (Fig. 7(a)). Fig. 7(b)-7(c) show that the proposed T_1 and T_2 topologies and [30], [36] require equal or less switching devices (switches and diodes) than other counterparts, which accordingly leads to less gate-driver circuits, less complexity, low size and low losses. Based on Fig. 7(d), the proposed T_1 and T_2 topologies utilize the second least number of capacitors

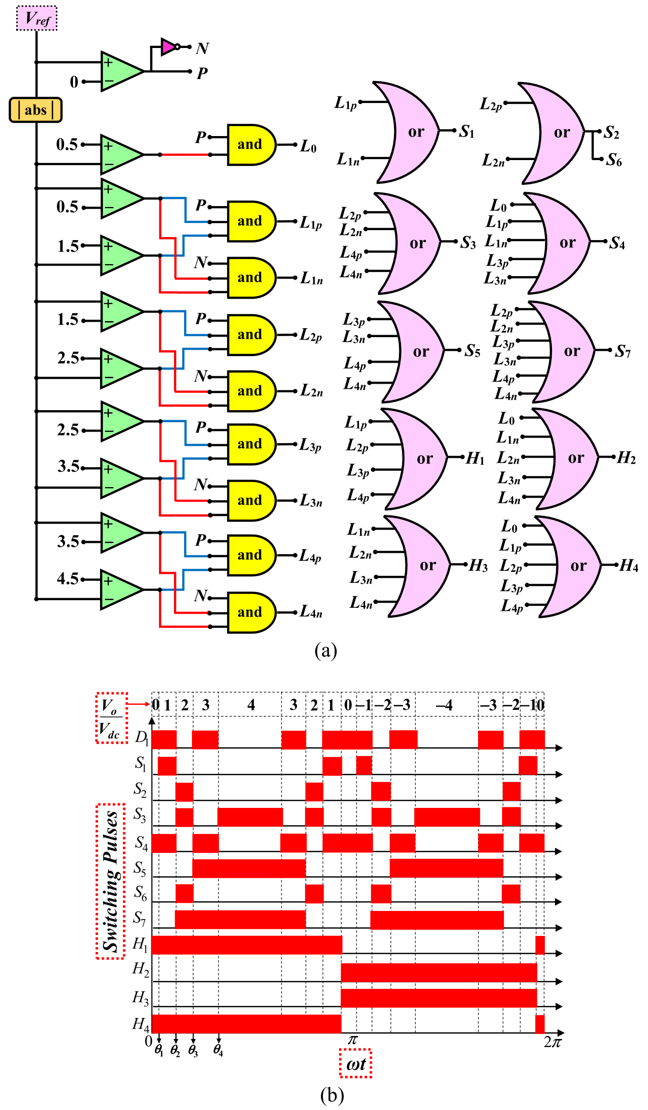


FIGURE 6. Nearest level modulation technique, (a) Control block diagram, (b) switching pulses.

to produce equal levels with similar counterparts. Also, it is seen from Fig. 7(e) that the proposed T_1 and T_2 topologies provide the third-highest (after [30], [36]) ratio of levels to total devices ($N_{TC} = N_{DC}+N_{SW}+N_{GD}+N_D+N_C$). This can result in a compact and less-complicated structure. As seen from Fig. 7(f), the gain of converters presented in [36], [38] increases at extended versions, but the gain of converters presented in [10], [28], [30], [33], [39]–[41] remains constant. Among these constant-gain converters, the proposed T_1, T_2 and P_1 topologies have the maximum step-up capability. According to Fig. 7(g), the Average Normalized Standing Voltage (ANSV) of the proposed symmetric converter (P_1) is quite low, while this amount in proposed asymmetric (T_1 and T_2) converters is rather high. Fig. 7(h) shows that the ANSV of converters reduces by an increment of cascaded units. Also, at equal units, the ANSV of proposed T_1, T_2 and P_1 topologies is lower than that of [33], [36], [38], [39], which is desirable. The proposed topology and [30], [31] require an H-bridge to create a bipolar voltage-waveform. Thus, the H-Bridge's switches are exposed to $V_{o,max}$. The negative voltage-level generation in [32] is achieved through a developed-H-bridge, where two switches tolerate $V_{o,max}$. The [34], [35] employ two half-bridges and the [33] inherently produce the negative voltage levels. The number of semiconductors tolerating the maximum output voltage (N_{MVS}) in [33], [34] and [35] are 4, 2 and 0, respectively. The [35] has the least TVS, because none of its semiconductors tolerate the Maximum Voltage Stress (MVS) of $V_{o,max}$.

VIII. LOSS AND EFFICIENCY ANALYSIS

The losses occurred in switches, diodes, and capacitors form the total power loss of the converter. The power dissipation in each component is demonstrated in the following.

A. SWITCHES

The switches of the proposed topology have been realized by MOSFETs, which can be modelled with an on-state resistance ($R_{on,T}$ or $R_{on,H}$). The conduction loss of switches happens at on-state resistances. Also, the switching losses occur during switch on-off transitions. The switching losses depend on voltage stress (V_{stress}), average current (I_{ave}), turn on and off times (t_{on}, t_{off}) and switching frequency (f_s) of a switch. The total switch losses (conduction and switching) can be computed from (18).

$$P_{Loss}^{Switch} = \frac{1}{6} f_s V_{stress} I_{ave}(t_{on} + t_{off}) + R_{on} I_{rms}^2 \tag{18}$$

B. DIODES

The diodes are modelled with a series connection of forward voltage drop (V_{FD}) and on-state resistance ($R_{on,D}$). Thus, the diode losses can be calculated from (19).

$$P_{Loss}^{Diode} = R_{on} I_{rms}^2 + VFD \times I_{ave} \tag{19}$$

C. CAPACITOR

The capacitor losses (including voltage ripple and equivalent series resistance (RESR) losses) is obtained from (20):

$$P_{Loss}^{Capacitor} = \frac{1}{2} f_s C(\Delta V)^2 + (R_{ESR} \times I_{rms}^2) \tag{20}$$

The total power losses, as well as the efficiency (η) of suggested, can be achieved from (21) and (22), respectively.

$$P_{Loss}^{Total} = P_{Loss}^{Switch} + P_{Loss}^{Diode} + P_{Loss}^{Capacitor} \tag{21}$$

$$\eta = \left(P_o/(P_o + P_{Loss}^{Total})\right) \times 100 \tag{22}$$

IX. EXPERIMENTAL RESULTS

Fig. 8 displays the laboratory-scale prototype implemented to verify theoretical analysis and correct performance of suggested basic inverter. Table 5 shows the experimental parameters.

The load power factor is $cos(\varphi) = cos(arctan^{-1}(L\omega/R)) = 0.9336$. According to section 4, the LDI of C_1 and C_2 capacitors are respectively $\theta_{C1} = \pi - 2\theta_4$ and $\theta_{C2} = \pi - 2\theta_3$,

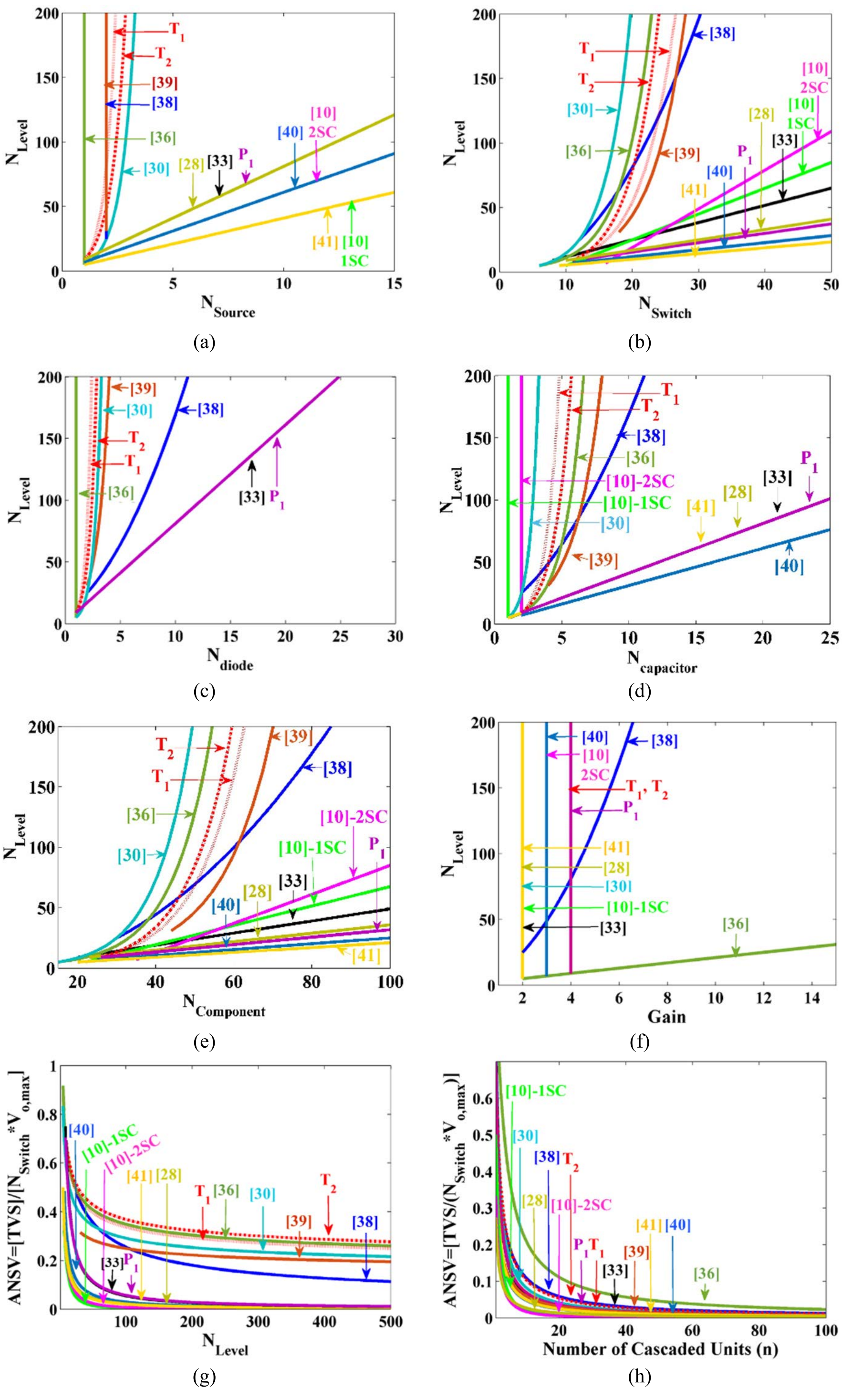


FIGURE 7. Comparison results: (a) N_{Level} Vs. N_{Source}, (b) N_{Level} Vs. N_{Switch}, (c) N_{Level} Vs. N_{Diode}, (d) N_{Level} Vs. $N_{Capacitor}$, (e) N_{Level} Vs. $N_{Component}$, (f) N_{Level} Vs. Gain, (g) ANSV Vs. N_{Level}, (h) ANSV Vs. Number of cascaded units.

where $\theta_4 = 67.5°$ and $\theta_3 = 45°$. So, the duration of LDI of C_1 and C_2 capacitors are, respectively $\theta_{C1} = 45°$ and $\theta_{C2} = 90°$. The C_1-C_2 capacitors have been designed such that to limit the voltage ripples to 5% ($\Delta V_{Ci} = 0.05 V_{Ci}$, $i = 1, 2$). Based on (17), the capacitances should be selected in $C_1 \geq 1822$ [μF] and $C_2 \geq 1682$ [μF]. To satisfy the (17), the C_1 - C_2 have been assumed to be $C_1 = C_2 = 2200$ [μF]. Assuming the input voltage as $V_{dc} = 30$ [V], the voltage stress on C_1 and C_2 capacitors will be 30 [V] and 60 [V], respectively. The employed C_1 and C_2 capacitors have been

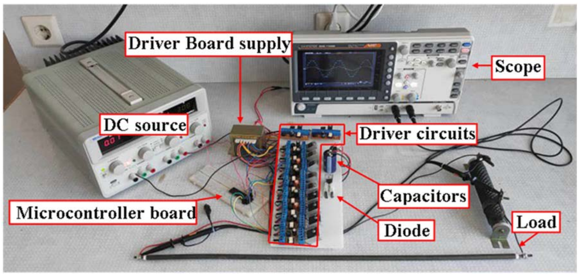
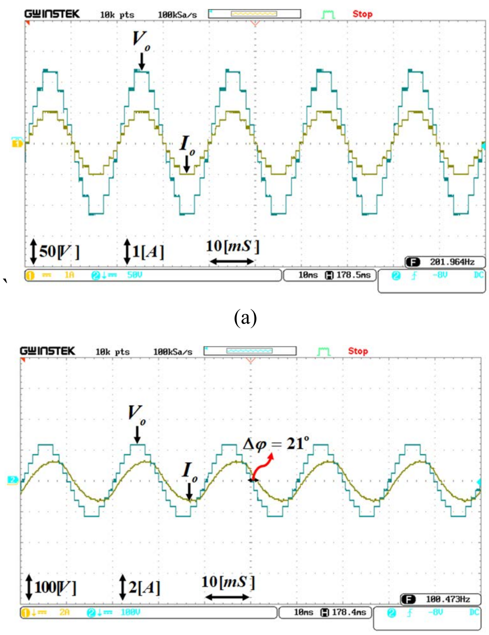


FIGURE 8. Laboratory-scale prototype of the proposed inverter.

TABLE 5. Experimental parameters of proposed topology.

Parameters	Magnitude
Input DC voltage	30 [V]
Load (R, L)	90 [Ω], 110 [mH]
Capacitor C_1	2200 [μF], 50 [V]
Capacitor C_2	2200 [μF], 100 [V]
Diode (D_1)	MUR1560G
Switches (H_1-H_4)	IRFP260NPbF, 200 [V], 50 [A], $R_{DS(on)}$ = 0.04[Ω]
Switches (S_1-S_7)	IRF540, 100 [V], 28 [A], $R_{DS\ (on)}$ = 0.077[Ω]
Fundamental frequency	50 [Hz]



(a)

(b)

FIGURE 9. Experimental results for output voltage-current waveforms (a) R = 90[Ω], (b) R = 90 [Ω] & L = 110 [mH].

selected to withstand up to 50 [V] and 100 [V], respectively, to meet the voltage stress requirement. Based on voltage and current stress of semiconductors, the IRFP260NPbF, IRF540 and MUR1560G have been respectively used for realizing H_1 - H_4, S_1 - S_7 and D_1.

Figs. 9(a) and 9(b) respectively depict the output voltage-current waveforms for (i) R = 90 [Ω] and (ii) R = 90 [Ω] and L = 110 [mH]).

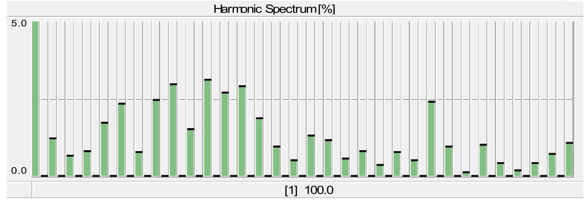
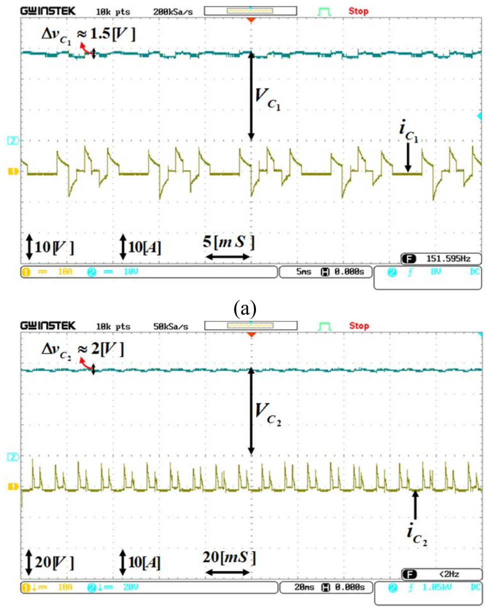


FIGURE 10. Harmonic spectrum of the output voltage.



(a)

(b)

FIGURE 11. Voltage/current waveforms of (a) C_1, (b) C_2, capacitor.

Fig. 9 confirms that the output-voltage waveform includes nine voltage-steps (0, ±30 [V], ±59 [V], ±88 [V], ±118 [V]). The peak value ($V_{o,max}$) is around 118 [V]. Note that the 3 volts difference between theoretical and measured maximum output voltage originates from voltage drops on current flow-path devices. Due to the pure resistive nature of load in Fig. 9(a), the load voltage and current waveforms are stepped and in-phase. The phase-difference of $\varphi = arctan^{-1}(L\omega/R) = 21°$ between V_o and I_o in Fig. 9(b) approves the ability of suggested inverter on feeding resistive-inductive loads. Fig. 10 presents harmonic-spectrum of output-voltage.

As seen from Fig. 10, the even-order harmonics have been eliminated from the output voltage. Among available harmonic orders, the 21th, 17th, 25th and 23th harmonic orders have the highest magnitudes, which are respectively about 3.1%, 2.97%, 2.88% and 2.7% of fundamental harmonic. These high order harmonics can be eliminated through a small filter. The Total Harmonic Distortion (THD) of the suggested 9-level inverter is about 8.53%. Fig. 11 displays the current and voltage waveform of C_1 - C_2 capacitors.

As expected, the voltage across C_1-C_2 capacitors has been naturally balanced on 28 [V] and 58 [V], respectively.

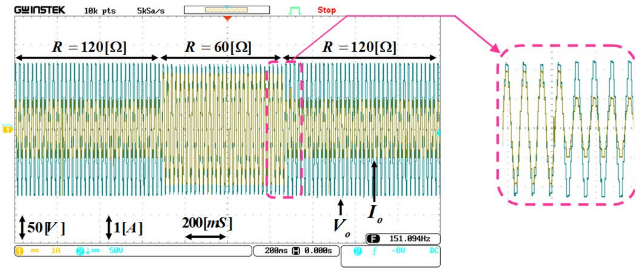


FIGURE 12. Dynamic operation during sudden load changes.

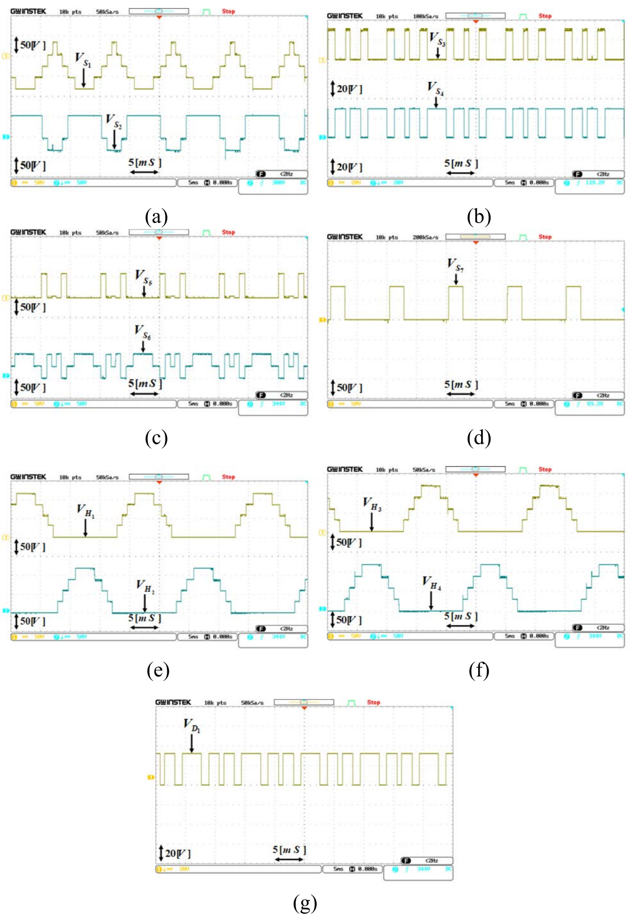
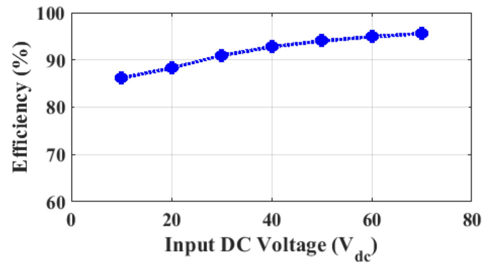


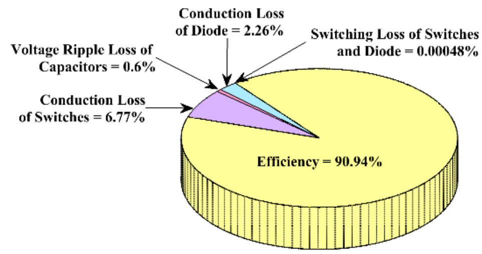
FIGURE 13. Voltage waveforms on semiconductors. (a) S_1, S_2, (b) S_3, S_4, (c) S_5, S_6, (d) S_7, (e) H_1, H_2, (f) H_3, H_4, (g) D_1.

Also, appropriate design of capacitances has suppressed voltage-ripple on C_1 and C_2 to equal or less than 5% ($\Delta V_{C1} = 1.5$ $[V]$, $\Delta V_{C2} = 2$ $[V]$). Note that the experimental results have been obtained in presence of L-D inrush-current limiting cells with small inductances of 50[μH]. Figs. 11(a)-11(b) confirms that the charging current of both C_1 and C_2 capacitors have been suppressed to less than 10[A], which is acceptable.

Fig. 12 indicates the dynamic operation of the suggested topology during sudden load change conditions. It is seen that during decrement of load to half (from 120 [Ω] to 60 [Ω]), the peak load-current is doubled without considerable change in output-voltage. While changing load from 60 [Ω] to 120 [Ω],



(a)



(b)

FIGURE 14. (a) Measured efficiency Vs. input voltage, (b) Loss distribution for $V_{dc} = 30$ [V].

the peak load-current reduces to half, but its voltage remains unaltered. This confirms the appropriate dynamic performance of the suggested topology during sudden load change conditions.

Figs. 13(a)-13(g) show the voltage waveforms of semiconductors. As seen, the voltage-stress of switches and diodes are as: $VS_{S1} = VS_{S7} = 86$ $[V]$ (Figs. 7(a) and 7(d)), $VS_{S2} = VS_{S5} = VS_{S6} = 58$ $[V]$ (Figs. 7(a) and 7(c)), $VS_{S3} = VS_{S4} = 30$ $[V]$ (Fig. 7(b)), $VS_{D1} = 28$ $[V]$ (Fig. 7(g)), and $VS_{H1} = VS_{H2} = VS_{H3} = VS_{H4} = 117$ $[V]$ (Figs. 7(e) and 7(f)). Despite the high voltage stress on H_1 - H_4, their low operation-frequency (fundamental frequency) limits the switching-losses.

Fig. 14(a) illustrates efficiency of suggested topology at various input-voltages. The peak-efficiency is about 95.5% that occurs at $V_{dc} = 70$ $[V]$.

According to Fig. 14(b), the efficiency of converter at the operating point ($P_o = 60$ $[W]$, $V_{dc} = 30$ $[V]$) is about 90.9%, where the conduction-loss of switches/diode are about 4.5 $[W]$ (6.77%) and 1.5 $[W]$ (2.26%), respectively. The ripple-loss of capacitors is about 0.4 $[W]$ (0.6%). The employment of Nearest-Level technique has decreased switching-loss of semiconductors to 0.00048%, which is negligible.

X. CONCLUSION

This paper has proposed a basic switched-capacitor 9-level inverter that is extendable to higher levels. The single-source nature, quadruple voltage-boosting ability, capacitors' natural charge-balancing, increased levels per device, and capability of feeding low power factor (resistive-inductive or inductive) load types are the main advantages of the suggested topology. The H-bridge switches tolerate $V_{o,max}$, but due to their fundamental-frequency operation, their switching-loss is suppressed. The capacitors' impulse-charging current has been reduced by a small-inductance-based L-D network. The output voltage THD of the suggested topology is about 8.5%. The comparative analysis confirms that the suggested topology has higher ratios of a number of levels and gain to devices, which is an important advantage. The efficiency of an implemented laboratory-scale prototype of the suggested topology for $V_{dc} = 30$ $[V]$ is about 90.9%, which is acceptable. Two extended versions of the suggested basic topology have been introduced to achieve more levels and voltage-gains. The experimental outcomes validate the proper performance of the suggested switched-capacitor 9-level inverter topology.

REFERENCES

[1] M. Vijeh, M. Rezanejad, E. Samadaei, and K. Bertilsson, "A general review of multilevel inverters based on main submodules: Structural point of view," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9479–9502, Oct. 2019.

[2] M. Karimi, P. Kargar, and K. Varesi, "An extendable asymmetric boost multi-level inverter with self-balanced capacitors," *Int. J. Circuit Theory Appl.*, vol. 50, no. 4, pp. 1297–1316, Apr. 2022.

[3] F. Esmaeili and K. Varesi, "A novel single-phase multi-level inverter topology based on bridge-type connected sources with enhanced number of levels per number of devices," *J. Energy Manage. Technol.*, vol. 4, no. 3, pp. 37–47, 2020.

[4] S. Deliri, K. Varesi, and S. Padmanaban, "An extendable single-input reduced-switch 11-level switched-capacitor inverter with quintuple boosting factor," *IET Gener., Transmiss. Distrib.*, to be published.

[5] A. Ashraf Gandomi, K. Varesi, and S. H. Hosseini, "Control strategy applied on double flying capacitor multi-cell inverter for increasing number of generated voltage levels," *IET Power Electron.*, vol. 8, no. 6, pp. 887–897, Jun. 2015.

[6] F. Esmaeili, H. R. Koofigar, and H. Qasemi, "A novel single phase multi-level high gain inverter with low voltage stress," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Apr. 14, 2022, doi: 10.1109/JESTPE.2022.3166233.

[7] H. K. Jahan, H. Tarzamni, P. Kolahian, S. H. Hosseini, F. Tahami, and F. Blaabjerg, "A switched-capacitor inverter with optimized switch-count considering load power factor," in *Proc. 45th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Oct. 2019, pp. 4959–4964.

[8] M. Karimi, P. Kargar, K. Varesi, and P. Sanjeevikumar, "Power quality improvement by a double-source multilevel inverter with reduced device and standing voltage on switches," in *Power Quality in Modern Power Systems*. Amsterdam, The Netherlands: Elsevier, 2021, pp. 245–282.

[9] S. Deliri, K. Varesi, Y. P. Siwakoti, and F. Blaabjerg, "Generalized diamond-type single DC-source switched-capacitor based multilevel inverter with step-up and natural voltage balancing capabilities," *IET Power Electron.*, vol. 14, no. 6, pp. 1208–1218, 2021.

[10] S. S. Lee, K.-B. Lee, I. M. Alsofyani, Y. Bak, and J. F. Wong, "Improved switched-capacitor integrated multilevel inverter with a DC source string," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7368–7376, Jan. 2019.

[11] T. Roy and P. K. Sadhu, "A step-up multilevel inverter topology using novel switched capacitor converters with reduced components," *IEEE Trans. Ind. Electron.*, vol. 68, no. 1, pp. 236–247, Jan. 2020.

[12] T. Roy, P. K. Sadhu, and A. Dasgupta, "Cross-switched multilevel inverter using novel switched capacitor converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8521–8532, Nov. 2019.

[13] S. A. Hosseini and K. Varesi, "Hybrid switched-capacitor 9-level boost inverter," in *Proc. 12th Power Electron., Drive Syst., Technol. Conf. (PEDSTC)*, Feb. 2021, pp. 1–4.

[14] F. Esmaeili and K. Varesi, "An asymmetric multi-level inverter structure with increased steps per devices," in *Proc. 11th Power Electron., Drive Syst., Technol. Conf. (PEDSTC)*, Feb. 2020, pp. 1–5.

[15] N. Sandeep and U. R. Yaragatti, "Operation and control of an improved hybrid nine-level inverter," *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5676–5686, Nov./Dec. 2017.

[16] F. Esmaeili, K. Varesi, and S. Padmanaban, "A solar energy-based multi-level inverter structure with enhanced output-voltage quality and increased levels per components," *Green Energy, Solar Energy, Photovolt., Smart Cities*, pp. 469–493, Dec. 2020.

[17] S. Majumdar, B. Mahato, and K. C. Jana, "Implementation of an optimum reduced components multi-cell multilevel (MC-MLI) inverter for lower standing voltage," *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 2765–2775, May 2019.

[18] M. Karimi, P. Kargar, and K. Varesi, "Two novel switched-capacitor based multi-level inverter topologies," in *Proc. Int. Power Syst. Conf. (PSC)*, Dec. 2019, pp. 391–396.

[19] S. R. Raman, Y. C. Fong, Y. Ye, and K. W. Eric Cheng, "Family of multiport switched-capacitor multilevel inverters for high-frequency AC power distribution," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4407–4422, May 2018.

[20] M. D. Siddique, S. Mekhilef, S. Padmanaban, M. A. Memon, and C. Kumar, "Single phase step-up switched-capacitor based multilevel inverter topology with SHEPWM," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 3107–3119, Jun. 2020.

[21] S. D. Khatoonabad, K. Varesi, and S. Padmanaban, "Photovoltaic-based switched-capacitor multi-level inverters with self-voltage balancing and step-up capabilities," *Green Energy, Sol. Energy, Photovolt., Smart Cities*, pp. 549–582, Dec. 2020.

[22] A. Taghvaie, J. Adabi, and M. Rezanejad, "A self-balanced step-up multilevel inverter based on switched-capacitor structure," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 199–209, Jan. 2017.

[23] P. Kargar, M. Karimi, and K. Varesi, "A novel boost switched-capacitor based multi-level inverter structure," in *Proc. 11th Power Electron., Drive Syst., Technol. Conf. (PEDSTC)*, Feb. 2020, pp. 1–6.

[24] S. Deliri, K. Varesi, Y. P. Siwakoti, and F. Blaabjerg, "A boost type switched-capacitor multi-level inverter for renewable energy sources with self-voltage balancing of capacitors," *Int. J. Energy Res.*, vol. 45, no. 10, pp. 15217–15230, Aug. 2021.

[25] E. Babaei, H. Tarzamni, F. Tahami, H. K. Jahan, and M. B. B. Sharifian, "Multi-input high step-up inverter with soft-switching capability, applicable in photovoltaic systems," *IET Power Electron.*, vol. 13, no. 1, pp. 133–143, Jan. 2020.

[26] N. Vosoughi, S. H. Hosseini, and M. Sabahi, "A new single phase transformerless grid connected inverter with boosting ability and common ground feature," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9313–9325, Nov. 2019.

[27] K. Varesi, M. Karimi, and P. Kargar, "A new basic step-up cascaded 35-level topology extendable to higher number of levels," in *Proc. 10th Int. Power Electron., Drive Syst. Technol. Conf. (PEDSTC)*, Feb. 2019, pp. 291–296.

[28] S. S. Lee, "Single-stage switched-capacitor module (S3CM) topology for cascaded multilevel inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8204–8207, 2018.

[29] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, Feb. 2011.

[30] E. Babaei and S. S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4614–4621, Sep. 2014.

[31] Y. M. Ye, K. W. E. Cheng, J. F. Liu, and K. Ding, "A step-up switched-capacitor multilevel inverter with self-voltage balancing," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6672–6680, Dec. 2014, doi: 10.1109/TIE.2014.2314052.

[32] E. Zamiri, N. Vosoughi, S. H. Hosseini, R. Barzegarkhoo, and M. Sabahi, "A new cascaded switched-capacitor multilevel inverter based on improved series–parallel conversion with less number of components," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3582–3594, Jun. 2016.

[33] R. Barzegarkhoo, M. Moradzadeh, E. Zamiri, H. M. Kojabadi, and F. Blaabjerg, "A new boost switched-capacitor multilevel converter with reduced circuit devices," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6738–6754, Aug. 2018.

[34] Y. Nakagawa and H. Koizumi, "A boost-type nine-level switched capacitor inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6522–6532, Jul. 2018.

[35] N. Sandeep, J. S. M. Ali, U. R. Yaragatti, and K. Vijayakumar, "Switched-capacitor-based quadruple-boost nine-level inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7147–7150, Aug. 2019.

[36] B.-B. Ngo, M.-K. Nguyen, J.-H. Kim, and F. Zare, "Single-phase multilevel inverter based on switched-capacitor structure," *IET Power Electron.*, vol. 11, no. 11, pp. 1858–1865, Sep. 2018.
[37] S. D. Khatoonabad and K. Varesi, "A novel dual-input switched-capacitor based 27-level boost inverter topology," in *Proc. 28th Iranian Conf. Electr. Eng. (ICEE)*, Tabriz, Iran, Aug. 2020, pp. 1–5.
[38] M. Ghodsi and S. M. Barakati, "A generalized cascade switched-capacitor multilevel converter structure and its optimization analysis," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4306–4317, Dec. 2019.
[39] A. Ahmad, M. Anas, A. Sarwar, M. Zaid, M. Tariq, J. Ahmad, and A. R. Beig, "Realization of a generalized switched-capacitor multilevel inverter topology with less switch requirement," *Energies*, vol. 13, no. 7, p. 1556, Mar. 2020.
[40] M. D. Siddique, S. Mekhilef, N. M. Shah, J. S. M. Ali, and F. Blaabjerg, "A new switched capacitor 7L inverter with triple voltage gain and low voltage stress," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 7, pp. 1294–1298, Aug. 2019.
[41] N. Sandeep, J. S. M. Ali, U. R. Yaragatti, and V. Krishnasamy, "A self-balancing five-level boosting inverter with reduced components," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6020–6024, Jul. 2018.

KAZEM VARESI was born in Ilkhchi, Tabriz, Iran, in 1985. He received the B.Sc. degree in power electrical engineering from the University of Tabriz, Tabriz, in 2008, the M.Sc. degree (Hons.) in power electrical engineering from the K. N. Toosi University of Technology, Tehran, Iran, in 2011, and the Ph.D. degree (Hons.) in power electrical engineering from the University of Tabriz, in 2017.

Since 2017, he has been working as an Assistant Professor with the Faculty of Electrical Engineering, Sahand University of Technology, Tabriz. He has authored or coauthored more than 60 journal articles, book chapters, and conference papers. He holds one patent in the area of power electronics. His research interests include dc–dc converters, multilevel inverters, hybrid electric vehicles, and renewable energy systems. He was a recipient of the Best Paper Award in 11th International Smart Grid Conference (SGC) in 2021 and the Best Young Researcher Award of the Sahand University of Technology in 2020.

FATEMEH ESMAEILI was born in Abhar-Zanjan, Iran, in 1997. She received the B.Sc. degree in electrical engineering from the Sahand University of Technology (SUT), Tabriz, Iran, in 2020. She is currently pursuing the master's degree with the University of Isfahan through the Merit-Based Scholarship.

Her research interests include power electronics, multilevel voltage source inverters, switched-capacitor converters, and renewable energy systems.

Ms. Esmaeili was a recipient of the Best B.Sc. Thesis Award from the Power Electronics Society of Iran in 2020. She is also selected in the IEEE Iran Section for designing and implementing a multilevel inverter for renewable energy applications.

SAEID DELIRI was born in Tabriz, Iran, in 1996. He received the B.Sc. degree in electrical control engineering and the M.Sc. degree in power electrical engineering from the Sahand University of Technology, Tabriz, in 2018 and 2020, respectively.

His research interests include multilevel inverters, and switched capacitor inverters and its applications in renewable energy systems.

HADI TARZAMNI (Student Member, IEEE) was born in Tabriz, Iran, in 1992. He received the B.Sc. and M.Sc. degrees (Hons.) in power electrical engineering from the Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, in 2014 and 2016, respectively. He is currently pursuing the Ph.D. degree in power electronics engineering under a Dual-Degree Doctoral Program with the Department of Electrical Engineering, Sharif University of Technology, Tehran, Iran, and the Department of Electrical Engineering and Automation, Aalto University, Finland. He has authored or coauthored more than 25 journals and conference papers. He also holds six patents in the area of power electronics. Since January 2021, he has been a Researcher at the Department of Electrical Engineering and Automation; and the Department of Electronics and Nanoengineering, Aalto University. His research interests include power electronic converters analysis and design, dc–dc and dc–ac converters, high step-up power conversion, soft-switching and resonant converters, and reliability analysis. He was a recipient of the Best Paper Award in the 10th International Power Electronics, Drive Systems and Technologies Conference (PEDSTC) in 2019. He has received a three-year Aalto ELEC Doctoral School Grant in 2021.