

Received 1 June 2022, accepted 17 June 2022, date of publication 27 June 2022, date of current version 12 July 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3186312

# Sliding-Mode Control of a Quadratic Buck Converter With Constant Power Load

CARLOS ANDRÉS TORRES-PINZÓN<sup>1</sup>, FREDDY FLORES-BAHAMONDE<sup>2</sup>, (Member, IEEE),  
JUAN ANTONIO GARRIGA-CASTILLO<sup>3</sup>, (Member, IEEE),  
HUGO VALDERRAMA-BLAVI<sup>4</sup>, (Member, IEEE), REHAM HAROUN<sup>4</sup>, (Member, IEEE),  
AND LUIS MARTÍNEZ-SALAMERO<sup>4</sup>, (Senior Member, IEEE)

<sup>1</sup>Modelling-Electronics and Monitoring Research Group (MEM), Faculty of Electronic Engineering, Universidad Santo Tomás, Bogotá 110311, Colombia

<sup>2</sup>Department of Engineering Science (DCI), Universidad Andres Bello, Providencia, Santiago 8370134, Chile

<sup>3</sup>Department of Computer Science and Industrial Engineering, University of Lleida, 25003 Lleida, Spain

<sup>4</sup>Group of Automatic Control and Industrial Electronics, Rovira i Virgili University, 43007 Tarragona, Spain

Corresponding author: Reham Haroun (reham.haroun@urv.cat)

This work was supported in part by the Universidad Santo Tomás, Colombia, Proyecto Semillero, under Contract 2054506; in part by the Spanish Ministerio de Ciencia e Innovación under Grant PID2019-111443RB-I00; and in part by the Agencia Nacional de Investigación y Desarrollo (ANID) through projects FONDECYT Iniciación and SERC Chile, under Grant 11220863 and Grant CONICYT/FONDAP/15110019, respectively.

**ABSTRACT** This paper analyzes for the first time a two-loop sliding-mode control (SMC) of a high-order converter supplying a constant power load (CPL). The converter is a single-switch quadratic buck structure (QBC) interfacing a domestic 380 V DC bus to a CPL requiring a regulated voltage of 48 V DC. The converter is unstable in the absence of control and even after the insertion of an inner loop based on SMC of the input inductor current. The addition of an appropriate linear outer loop establishing the reference to the inner loop stabilizes the system and provides output voltage regulation. The regulated QBC shows a fast recovery of the output voltage with negligible overshoot in response to step-type changes of the output power or the input voltage. It is also shown that the implemented regulator for CPL supply can be used directly in the case of a constant current load (CCL) or a constant resistance load (CRL) resulting in similar performance to the CPL case. PSIM simulations and experimental results in a 400 W prototype are in good agreement with theoretical predictions.

**INDEX TERMS** High-order converters with constant power load, buck quadratic converter, sliding-mode control.

## I. INTRODUCTION

Power converters play an important role in industry enabling the electric energy transformation in low, medium and high power systems. To that end, academia and industry are actively working to develop more reliable and efficient converters [1]. This effort is particularly relevant in the case of DC-DC switching converters, which for several decades have been successfully applied as power electronic interfaces in many systems [1]–[4]. Moreover, the interest on DC-DC converters has been recently supported by the considerable progress of DC-based power architectures for micro-grids (MGs) [5], [6] and electric vehicles (EVs) [7], while

The associate editor coordinating the review of this manuscript and approving it for publication was Yuh-Shyan Hwang<sup>1</sup>.

traditionally it has been motivated by the need of efficient power supplies for telecommunications [8]. As a matter of fact, the electrical architecture of all those systems is composed by DC-buses with different voltage levels and degrees of regulation, in which DC-DC converters are the key elements for the required power processing. The latter usually involves specifications regarding high-quality power performance, high conversion range, fast dynamic response and robustness [9]. In this context, DC-DC switching converters with high conversion ratio have been recently used in efficient lighting and micro-inverter design [10]–[12]. In some cases, they are implemented with two energy conversion stages or with a high-frequency (HF) transformer with a high turns ratio. However, their benchmark in terms of efficiency is not complete yet [13], [14]. Besides, the use of two conversion

stages or HF transformers adds extra complexity and cost to the design due to the high number of components or the use of bulky devices, which eventually results in a waste of power. To cope with the problem of high conversion ratio design, some theoretical proposals were reported [15], and more recently solutions based on a single switch-quadratic concept have attracted engineers' attention. Although this concept goes back in time to 1989, when it was introduced by Maksimovic and Cuk [16], it has not been until lately that some applications have been found in photovoltaic systems (PV) for high-gain voltage stepping-up grid-connected micro-inverters [17].

Furthermore, the increasing use of 380 VDC in domestic and industrial microgrid buses indicates that this level will become a standard value soon. In that scenario, telecom equipment requiring 48 VDC supply will need an interface to step-down the bus voltage.

In this paper, we tackle the problem of designing a quadratic buck converter (QBC) to pass from 380 VDC to 48 VDC. This means that only one active switch is involved, but the resulting performance is electrically comparable to that of two buck converters in cascade connection [16], [18]–[20].

In terms of control, DC-DC converters have been commonly regulated with very good performance through classical linear techniques using pulse width modulation (PWM). However, it is well-known that the good behavior of linear controllers is limited to a small neighborhood around a specific equilibrium point. Thus, large variations of load or sudden changes of the load nature often result in stability problems, which requires the addition of ad-hoc regulation loops or an important effort in tuning the controller. This problem can emerge in converters supplying constant power loads (CPLs), which are frequently found in MGs, EVs and power supplies for telecom. There, the cascade connection of a power converter acting as a source with a converter behaving as a load is equivalent in certain cases to a single converter feeding a CPL, i.e., a converter loaded by a device absorbing a constant value of power.

Recently, many works have been conducted describing different strategies on the control of switching converters loaded by a CPL as reported in [21]. For the linear controller case, it was shown that an unstable transfer function has to be compensated due to the effect of the negative incremental resistance imposed by the CPL [22], [23]. Other solutions based on non-linear controls have been reported, such as sliding mode control (SMC) [24], PWM input-output linearization [25], and PWM adaptive control [26].

SMC is an efficient solution for many open problems in power converters [27] by offering robustness in face of parametric uncertainty, fast response and a systematic approach in the control design [28], [29]. The latter feature lies on the definition of the switching surface and the subsequent establishment of the existence conditions for sliding motions, which eventually results in a relatively simple analysis in most cases. In a clear-cut contrast, a PWM nonlinear approach requires

the definition of the control law of the duty cycle, which is more often than not, the most difficult step of the design. This contrast gets particularly worse in the case of a high-order converter such as the QBC loaded with a CPL. The lack of information on the QBC dynamic behavior in closed-loop operation when it is loaded by a conventional device becomes a difficult problem when considering the nonlinear behavior of the CPL.

For all these reasons, it is sensible to start exploring the dynamic behavior of the QBC using SMC with switching surfaces of the type  $S(x) = x_i - k$ , where  $x_i$  can be any of the state variables of the converter [30]. The underlying idea is to find the switching surface that results in a stable equilibrium point, and then regulate indirectly the output voltage of the QBC by means of an ad-hoc loop that will establish the value of  $k$ . It is worth noting the use of a SMC controller in a quadratic buck converter with resistive load presented in [31]. That paper analyzes and simulates a pulse width modulation (PWM) –based nonlinear control strategy of the QBC with a resistive load using a sliding-mode approach. The switching surface used in the preliminary analysis is a linear combination of output voltage error and inductor  $L_1$  current error plus their respective integrals. However, the work does not study the stability of the final closed-loop implemented system, which is equivalent to a PWM –based control with both feedback and feedforward loops. No separated analysis between fast and slow variables is carried out either, and hence, no information about a potential implementation of a cascade control can be finally inferred.

Therefore, we propose in this paper a comprehensive analysis of a cascade control for a QBC connected to a CPL. In addition, as in DC distribution systems, different types of loads are considered [32], and the robustness of the controller is explored in all cases, namely, for constant power load (CPL), constant resistance load (CRL) and constant current load (CCL). For all cases, the regulation system consist in an inner loop based on SMC with a switching surface of the type mentioned above, and an outer loop made-up of a proportional-integral (PI) controller [33].

The rest of the paper is organized as follows. Section II introduces the switched-model of the QBC loaded with a resistor. A short review of basic notions of sliding-mode control and the selection of the appropriate switching surface for the inner control loop is given in Section III for the case of resistive load. The extension of the resistive load solution to the CPL case is analyzed in Section IV bringing to the light the difficulty of the problem. After showing that the QBC with CPL and the selected inner control loop is still unstable, the design of the outer loop for both output voltage regulation and system stabilization is described in depth. PSIM simulations and experimental results verifying the theoretical predictions are given in Section V. A PSIM simulation-based comparison of the proposed controller with a conventional two-loop linear control is illustrated in Section VI and the conclusions of the paper are presented in Section VII.

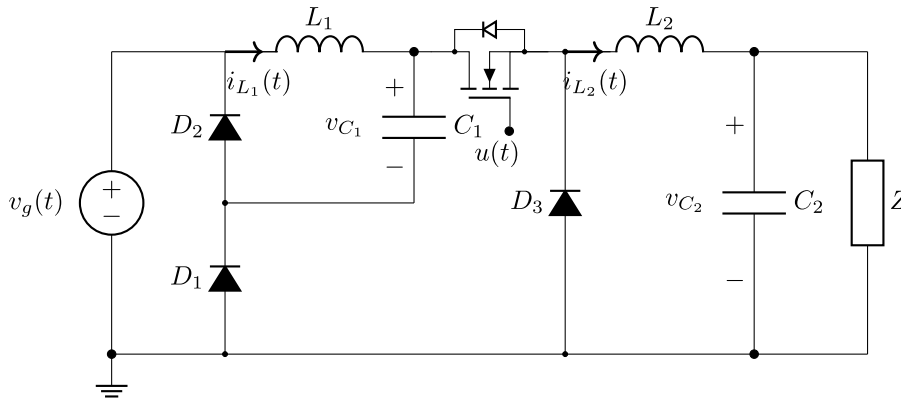


FIGURE 1. Schematic circuit diagram of a quadratic buck converter converter.

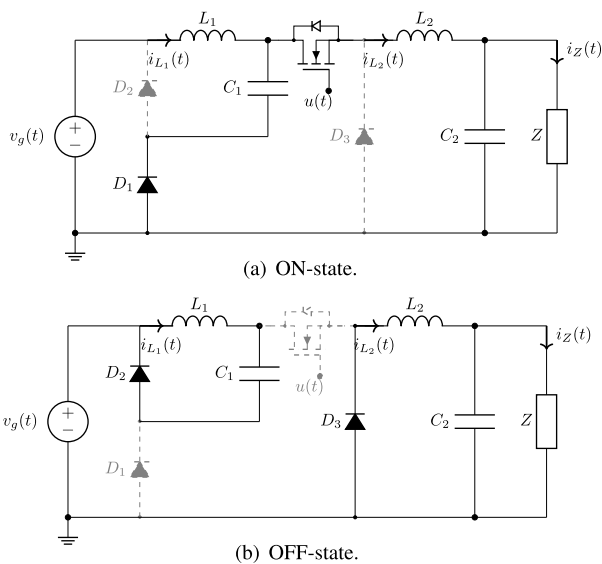


FIGURE 2. Quadratic buck circuit configurations.

## II. SWITCHED-MODEL OF THE QUADRATIC BUCK CONVERTER

Figure 1 shows the circuit scheme of the quadratic buck converter (QBC). This circuit provides a wider conversion ratio than the conventional buck converter, since the dc gain between output voltage  $v_o(t)$  and input voltage  $v_g(t)$  is a quadratic function [19], given by (1).

$$\frac{v_{C_2}}{v_g} = D^2 \quad (1)$$

The (QBC) is composed of only one active switch to perform the conversion voltage, which is equivalent to two cascaded buck converters. In the circuit diodes  $D_1$  and  $D_2$  are in the first conversion stage, whereas the MOSFET and diode  $D_3$  belong to the second stage. Note that the load is presented as a generic one defined by  $Z$ .

Thus, through the control signal  $u(t) = \{0, 1\}$  two configurations are obtained for continuous conduction mode operation (CCM). Figure 3 (a) shows the ON-state configuration

associated to  $u(t) = 1$ , and Figure 3 (b) the OFF-state configuration, corresponding to  $u(t) = 0$ .

The state vector of the converter is given in (2). Consequently, the bilinear expression for the QBC, that describes the ON and OFF operation, is written in (3) considering  $Z = R$ .

$$\begin{aligned} x(t) &= [i_{L_1}(t)v_{C_1}(t)i_{L_2}(t)v_{C_2}(t)]^T \quad (2) \\ \frac{di_{L_1}}{dt} &= -\frac{v_{C_1}}{L_1} + \frac{v_g}{L_1}u \\ \frac{dv_{C_1}}{dt} &= \frac{i_{L_1}}{C_1} - \frac{i_{L_2}}{C_1}u \\ \frac{di_{L_2}}{dt} &= \frac{v_{C_1}}{L_2}u - \frac{v_{C_2}}{L_2} \\ \frac{dv_{C_2}}{dt} &= \frac{i_{L_2}}{C_2} - \frac{v_{C_2}}{RC_2} \quad (3) \end{aligned}$$

## III. SLIDING-MODE OPERATION ANALYSIS

The design of SMC allows forcing the converter dynamics to reach and remain on a switching surface in order to provide a desired asymptotic behavior. SMC is the natural way to control variable structure systems defined as follows:

$$\dot{x}(t) = f(x, t) + g(x, t)u(t) \quad (4)$$

where  $x(t) \in \mathbb{R}^n$  and  $u(t) \in \mathbb{R}^m$  are states and input variables respectively, while  $f(x, t) \in \mathbb{R}^n$  and  $g(x, t) \in \mathbb{R}^{n \times m}$  represent smooth vector fields.

Some of its main advantages are: design simplicity, system order reduction, and low sensitivity to disturbances and plant parameters variations [28]. The design of sliding-mode controllers in switching converters can be based on a suitable Lyapunov function and Filippov's method (equivalent control method) [29]. By using the bilinear expression (3), system dynamics (4) can be written as

$$\dot{x}(t) = \left( \underbrace{Ax(t) + \delta}_{f(x,t)} \right) + \left( \underbrace{Bx(t) + \gamma}_{g(x,t)} \right) u(t) \quad (5)$$

where

$$A = A_2, \delta = B_2, B = A_1 - A_2, \gamma = B_1 - B_2$$

The vector  $u(t)$  represents the discontinuous control inputs of the system which is given by:

$$u_i(t) = [u_1(t) \ u_2(t) \ \dots \ u_i(t)]^T$$

$$= \begin{cases} u_i^+ & \text{for } S_i(x) > 0 \\ u_i^- & \text{for } S_i(x) < 0 \\ u_i^+ \neq u_i^- & \end{cases} \quad (6)$$

where  $u_i^+$  and  $u_i^-$  are either scalar values or scalar functions of  $x(t)$ ; and  $S(x)$  are the switching functions describing the sliding surfaces. The switching surface  $S_i(x)$  can be expressed as a linear combination of the weighted values of the converter state variables as:

$$S_i(x) = \sum_{i=1}^m c_i x_i(t) \quad (7)$$

where  $c_i$  defines the set of the control parameters known as sliding coefficients and  $x_i(t) \in x(t)$ .

The function  $S(x)$  with the associated switching law must ensure that the system reaches the state  $S(x) = 0$  from a non-zero initial condition, and that, once on the surface can remain there. This condition can be expressed as:

$$\lim_{S(x) \rightarrow 0^-} \dot{S}(x) > 0, \quad \lim_{S(x) \rightarrow 0^+} \dot{S}(x) < 0 \quad (8)$$

In this way, the system is in sliding mode on the surface  $S(x)$  if the control continuously switches between  $u^+$  and  $u^-$  fulfilling the conditions of equation (8). In this context, the ideal sliding dynamics is characterized by the invariance conditions:

$$S(x) = 0 \quad \dot{S}(x) = 0 \quad (9)$$

which implies the existence of an equivalent control  $u_{eq}(x)$ . Hence, the vector  $u(t)$  is substituted by a continuous function  $u_{eq}(x)$ , which represents the control strategy that describes the behavior of the system restricted to the switching surface  $S(x)$ . This function is expressed as

$$u_{eq}(x) = -\frac{\langle \nabla_S, Ax(t) + \delta \rangle}{\langle \nabla_S, Bx(t) + \gamma \rangle} \quad (10)$$

where  $\nabla_S$  corresponds to the gradient of the switching surface  $S(x)$ , and  $\langle \cdot, \cdot \rangle$  represents the scalar product. From (10), the necessary condition for the existence of the sliding mode is deduced as:

$$\left\langle \nabla_S, Bx(t) + \gamma \right\rangle \neq 0 \quad (11)$$

The expression (11) is known as the transversality condition, which implies that  $Bx(t) + \gamma$  cannot be tangent to the sliding surface [33].

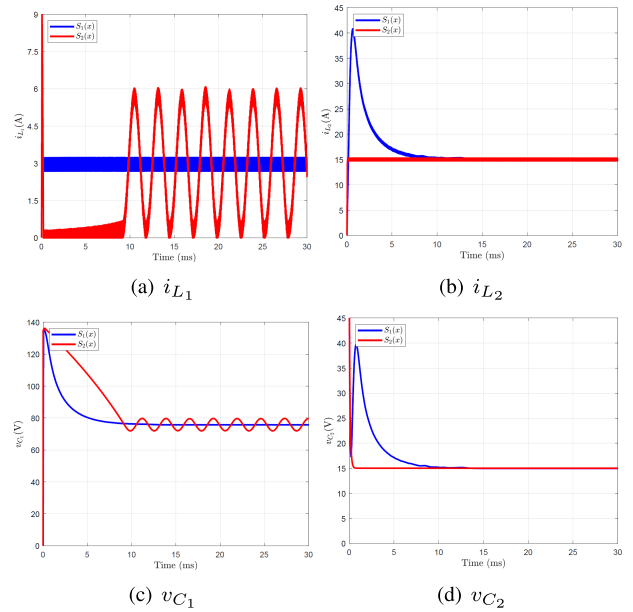


FIGURE 3. Currents and voltages waveforms corresponding to the SM control under  $S_1(x)$  and  $S_2(x)$ .

### A. SELECTING THE SLIDING SURFACE FOR THE QBC

Based on the SMC theory described above, the main idea of the following analysis is to select an appropriate sliding surface to drive first the state variables of the QBC to an equilibrium point and then regulate indirectly the output through some of the parameters of the surface. The proposed surface structure is of the form  $x_i(t) = K$ , which has already been successfully implemented in power switched converters [30].

Hence, to control the output voltage  $v_{C2}$ , three sliding surfaces based on the corresponding state variables are analyzed, i.e., for  $v_{C2}(t) = K$ ,  $i_{L1}(t) = K$ , and  $i_{L2}(t) = K$ , represented by  $S_0(x)$ ,  $S_1(x)$  and  $S_2(x)$ , respectively. The surface selected has to guarantee the control objective, but also ensure the stability for each of the variables of QBC. The following analysis is conducted through the Routh Hurwitz criteria, where the stability of the corresponding characteristic polynomials are studied. In order to simplify the analysis presented in this section a unity resistive load is considered, i.e.,  $Z = R = 1\Omega$ .

Therefore, the state-space model of the quadratic buck converter is rewritten as (12). Then, considering the invariance and transversality conditions, defined in (9) and (11), respectively, and the state-space model (12) it is possible to obtain the existence of sliding mode, the equivalent control, the ideal sliding dynamics and, the corresponding equilibrium points for the different proposed surfaces  $S_0(x)$ ,  $S_1(x)$  and  $S_2(x)$ . The corresponding results are detailed in Table 1.

From Table 1, it is possible to observe that  $S_0(x)$  does not fulfill the transversality condition. Conversely, the surfaces  $S_1(x)$  and  $S_2(x)$  have the conditions to induce a sliding regime. However, to guarantee the local stability of all the variables of the system, the characteristic polynomial derived from

TABLE 1. Sliding regime analysis results.

$S_i(\mathbf{x})$	Transversality Condition	Equivalent Control ( $u_{eq}$ )	Ideal Sliding Dynamic	Equilibrium point ( $x^*$ )	Conditions for local stability
$S_0(\mathbf{x}) = v_{C_2}(t) - K$	0	-	-	-	-
$S_1(\mathbf{x}) = i_{L_1}(t) - K_1$	$\frac{v_g}{L_1} \neq 0$	$\frac{v_{C_1}}{v_g}$	$\frac{dv_{C_1}}{dt} = \frac{K_1}{C_1} - \frac{i_{L_2} v_{C_1}}{C_1 V_g}$ $\frac{di_{L_2}}{dt} = \frac{v_{C_1}^2}{L_2 V_g} - \frac{v_{C_2}}{L_2}$ $\frac{dv_{C_2}}{dt} = \frac{i_{L_2}}{C_2} - \frac{v_{C_2}}{RC_2}$	$\begin{bmatrix} \frac{K_1}{\sqrt[3]{K_1 R V_g^2}} \\ \frac{\sqrt[3]{K_1^2 V_g}}{R} \\ \frac{\sqrt[3]{K_1^2 R^2 V_g}}{K_1} \end{bmatrix}$	$m_2 > 0$ $m_1 > 0$ $m_0 > 0$ $\frac{m_2 m_1 - m_0}{m_2} > 0$
$S_2(\mathbf{x}) = i_{L_2}(t) - K_2$	$\frac{v_{C_1}}{L_2} \neq 0$	$\frac{v_{C_2}}{v_{C_1}}$	$\frac{di_{L_1}}{dt} = -\frac{v_{C_1}}{L_1} + \frac{V_g v_{C_2}}{L_1 v_{C_1}}$ $\frac{dv_{C_1}}{dt} = \frac{i_{L_1}}{C_1} - \frac{K_2 v_{C_2}}{C_1 v_{C_1}}$ $\frac{dv_{C_2}}{dt} = \frac{K_2}{C_2} - \frac{v_{C_2}}{RC_2}$	$\begin{bmatrix} \frac{\sqrt{K_2^3 R}}{V_g} \\ \sqrt{K_2 R V_g} \\ K_2 \\ K_2 R \end{bmatrix}$	$n_2 > 0$ $n_1 > 0$ $n_0 > 0$ $\frac{n_2 n_1 - n_0}{n_2} > 0$

each surface is analyzed. Therefore, for  $S_1(x)$  and  $S_2(x)$ ,  $p_1(s)$  and  $p_2(s)$  are developed, respectively. Thus, considering the expressions in equation (13), and using the parameters shown in Table 2 (with  $R = 1 \Omega$ ), it can be verified that the expression  $\left(\frac{n_2 n_1 - n_0}{n_2}\right)$  of  $p_2(s)$  is negative, showing that the equilibrium point associated to surface  $S_2(x)$  is unstable.

$$\frac{d}{dt} \begin{bmatrix} i_{L_1} \\ v_{C_1} \\ i_{L_2} \\ v_{C_2} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{L_1} & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{RC_2} \end{bmatrix}}_A \begin{bmatrix} i_{L_1} \\ v_{C_1} \\ i_{L_2} \\ v_{C_2} \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_\delta + \underbrace{\begin{bmatrix} 0 \\ -\frac{i_{L_2}}{C_1} \\ \frac{v_{C_1}}{L_2} \\ 0 \end{bmatrix}}_{Bx} u + \underbrace{\begin{bmatrix} \frac{v_g}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}}_\gamma u \quad (12)$$

$$\begin{cases} p_1(s) = s^3 + m_2 s^2 + m_1 s + m_0 \\ p_2(s) = s^3 + n_2 s^2 + n_1 s + n_0 \end{cases} \quad (13)$$

where:

$$m_2 = \left( \frac{1}{RC_2} + \sqrt[3]{\frac{K_1^2}{RC_1^3 V_g^2}} \right)$$

$$n_2 = \left( \frac{1}{RC_2} - \frac{K_2}{C_1 V_g} \right)$$

$$m_1 = \left( \sqrt[3]{\frac{K_1^2}{R^4 C_1^3 C_2^3 V_g^2}} + \frac{1}{L_2 C_2} + 2 \sqrt[3]{\frac{K_1^2 R^2}{L_2^3 C_1^3 V_g^2}} \right)$$

$$n_1 = \left( \frac{2}{L_1 C_1} - \frac{K_2}{RC_1 C_2 V_g} \right)$$

$$m_0 = \left( 2 \sqrt[3]{\frac{K_1}{V_g R^2 C_1^3 C_2^3 L_2^3}} + \sqrt[3]{\frac{K_1^2}{RC_1^3 C_2^3 L_2^3 V_g^2}} \right)$$

$$n_0 = \frac{2}{RL_1 C_1 C_2}$$

The instability problem of  $S_2(x)$  is verified in Figure 3, where it is shown the waveforms of the state variables for both surfaces,  $S_1(x)$  and  $S_2(x)$  for the set of parameters  $L_1 = 1.2 \text{ mH}$ ,  $L_2 = 300 \mu\text{H}$ ,  $C_1 = 300 \mu\text{F}$ ,  $C_2 = 100 \mu\text{F}$ ,  $R = 1 \Omega$ ,  $V_g = 380 \text{ V}$ ,  $K_1 = 3 \text{ A}$ , and  $K_2 = 15 \text{ A}$ . The instability is reflected in the oscillatory behavior of  $i_{L_1}$  and  $v_{C_1}$  when the sliding surface is  $S_2(x)$ .

#### IV. SMC ANALYSIS OF A QUADRATIC BUCK CONVERTER CONNECTED TO A CPL

By simple analysis of (3) in the case of a CPL, it is found that the output voltage of the QBC can be expressed in (14), as shown at the bottom of the next page.

It can be observed that (14) is a nonlinear differential equation, which results in an unbounded behavior of voltage  $v_{C_2}$  for either  $u = 1$  or  $u = 0$ .

As shown in the sequel, the prediction of unstable behavior persists when the dynamic behavior of the output capacitor voltage in (3) is linearized around its equilibrium point and substituted by the equation

$$\frac{dv_{C_2}}{dt} = \frac{i_{L_2}}{C_2} - \frac{v_{C_2}}{R_0 C_2}, \quad (15)$$

where  $R_0 = V_{C_2}^2/P$  and  $V_{C_2}$  is the desired output voltage at the equilibrium point.

From the literature, it is well-known that the CPL exhibits a positive instantaneous impedance behavior, but also a negative incremental impedance effect. Regarding the incremental behavior of the CPL, Figure 4 depicts the approximation of the static non-linearity by the tangent to the curve at the operating point  $(V_{C_2}, P/V_{C_2})$  in the case of a constant power of 400 W and output voltage of 48 V. The substitution of the CPL by its incremental resistance of negative slope has been the traditional way of analyzing converters with CPL but this approach is only valid for small excursions around the operating point.

Now, the output voltage dynamics can be expressed in (16), as shown at the bottom of the next page, and the corresponding characteristic equation is given by (16), as shown at the bottom of the next page, which has roots in the right-half

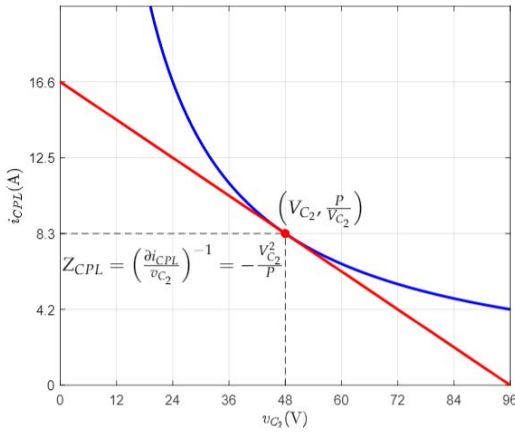


FIGURE 4. CPL characteristic for  $P = 400$  W.

plane for either  $u = 1$  or  $u = 0$  certifying the instability of both on and off trajectories of the QBC in open-loop.

It can be expected that the combination of both on and off trajectories irrespective of the duty cycle value will result in an open unbounded trajectory.

However, the combination of the mentioned unstable trajectories with an appropriate switching policy could drive the converter to a desired equilibrium point (EP) following a stable trajectory. This is the role of the sliding-mode control, i.e. proposing a switching surface that will serve to combine the unstable on and off trajectories using a switching law that turns on the converter when the state vector trajectory is below the switching surface and turns it off when the trajectory is above. The proposed control scheme based on SMC for the QBC loaded with a CPL consists of two cascade control loops. It makes sense to explore first the performance of  $S_1(x)$  for the inner loop and check whether the stable behavior observed in the case of a resistive load is still guaranteed in the case of a CPL.

**A. INNER CURRENT CONTROL LOOP**

Assuming the switching surface  $S_1(x) = i_{L1} - K$ , the ideal sliding dynamics for the QBC loaded with a CPL will be

given by

$$\begin{aligned} \frac{dv_{C1}}{dt} &= \frac{K}{C_1} - \frac{i_{L2}}{C_1} \frac{v_{C1}}{V_g} \\ \frac{di_{L2}}{dt} &= \frac{v_{C1}^2}{L_2 V_g} u - \frac{v_{C2}}{L_2} \\ \frac{dv_{C2}}{dt} &= \frac{i_{L2}}{C_2} - \frac{P}{C_2 v_{C2}} \end{aligned} \tag{18}$$

The corresponding equilibrium point of (18) is

$$X^* = (K, \sqrt{V_g V_2^*}, \frac{P}{V_2^*}, V_2^*)^T \tag{19}$$

and the characteristic polynomial after linearization of (18) around  $X^*$  can be expressed as

$$\begin{aligned} s^3 + \frac{C_2 V_2^* P - C_1 V_g P}{C_1 C_2 V_g V_2^{*2}} s^2 + \frac{C_1 V_g V_2^{*3} - L_2 P^2 + 2 C_2 V_2^{*4}}{L_2 C_1 C_2 V_g V_2^{*3}} s + \\ - \frac{P}{L_2 C_1 C_2 V_g V_2^*} \end{aligned} \tag{20}$$

which corresponds to an unstable system.

Therefore, the insertion of the inner loop that ensures stability in the case of CRL or CCL cannot stabilize the system when the QBC is loaded with a CPL. The outer loop processing the output voltage error must ensure the closed-loop stability and provide voltage regulation. With this aim, reference  $K$  is considered now as a time-varying reference, i.e., the switching surface becomes  $S_1(x) = i_{L1} - k(t)$ , where  $k(t)$  is provided by the outer control loop trough a PI compensator as illustrated in Figure 5, in which the inner loop is implemented with a hysteresis comparator. It is worth mentioning that the switching surface is reached in finite time as demonstrated in the Appendix.

Introducing the invariance conditions  $S(x) = 0$  and  $\frac{dS(x)}{dt} = 0$  in (3) [28] results in the equivalent control  $u_{eq}(x)$ , which is bounded by both maximum and minimum values of  $u$ , such as follows:

$$0 < \left[ u_{eq}(x) = \frac{L_1 \frac{dk}{dt} + v_{C1}}{V_g} \right] < 1 \tag{21}$$

$$\begin{aligned} \frac{d^4 v_{C2}}{dt^4} - \frac{P}{C_2 v_{C2}^2} \frac{d^3 v_{C2}}{dt^3} + \left( \frac{1}{L_2 C_2} + \frac{u^2}{L_2 C_1} + \frac{1}{L_1 C_1} \right) \frac{d^2 v_{C2}}{dt^2} + \frac{6P}{C_2 v_{C2}^3} \frac{dv_{C2}}{dt} \left( \frac{d^2 v_{C2}}{dt^2} - \frac{1}{v_{C2}} \left( \frac{dv_{C2}}{dt} \right)^2 \right) \\ - \frac{dv_{C2}}{dt} \left( \frac{u^2}{L_2 C_2 C_1} + \frac{1}{L_1 C_2 C_1} \right) \frac{P}{v_{C2}^2} + \frac{v_{C2}}{L_1 L_2 C_2 C_1} = \frac{V_g u^2}{L_1 L_2 C_2 C_1} \end{aligned} \tag{14}$$

$$\begin{aligned} \frac{d^4 v_{C2}}{dt^4} - \frac{d^3 v_{C2}}{C_2 R dt^3} + \left( \frac{1}{L_2 C_2} + \frac{u^2}{L_2 C_1} + \frac{1}{L_1 C_1} \right) \frac{d^2 v_{C2}}{dt^2} - \frac{dv_{C2}}{dt} \left( \frac{u^2}{L_2 C_2 C_1 R} + \frac{1}{L_1 C_2 C_1 R} \right) + \frac{v_{C2}}{L_1 L_2 C_2 C_1} \\ = \frac{V_g u^2}{L_1 L_2 C_2 C_1} \end{aligned} \tag{16}$$

$$s^4 - \frac{1}{C_2 R} s^3 + \left( \frac{1}{L_2 C_2} + \frac{u^2}{L_2 C_1} + \frac{1}{L_1 C_1} \right) s^2 - \left( \frac{u^2}{L_2 C_2 C_1 R} + \frac{1}{L_1 C_2 C_1 R} \right) s + \frac{1}{L_1 L_2 C_2 C_1} \tag{17}$$

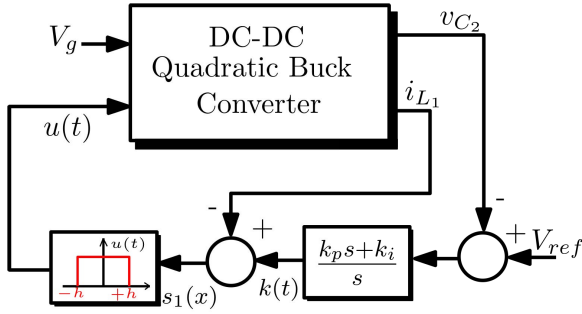


FIGURE 5. Proposed control scheme for the quadratic buck converter.

Now, substituting  $u$  by  $u_{eq}(x)$  in (3) and taking into account expression (14) result in the following ideal sliding dynamics:

$$\begin{aligned} \frac{dv_{C_1}}{dt} &= \frac{k}{C_1} - \frac{L_1}{C_1} \frac{i_{L_2}}{V_g} \frac{dk}{dt} - \frac{i_{L_2}}{C_1} \frac{v_{C_1}}{V_g} = g_1(x) \\ \frac{di_{L_2}}{dt} &= \frac{L_1}{L_2} \frac{v_{C_1}}{V_g} \frac{dk}{dt} + \frac{v_{C_1}^2}{L_2 V_g} - \frac{v_{C_2}}{L_2} = g_2(x) \\ \frac{dv_{C_2}}{dt} &= \frac{i_{L_2}}{C_2} - \frac{P}{C_2 v_{C_2}} = g_3(x) \end{aligned} \quad (22)$$

In order to regulate the output voltage, an outer loop is introduced in cascade with the sliding-mode current controller. Therefore, we have to characterize the dynamic behavior of the converter plus the inner loop around the equilibrium point of (22).

We assume that the reference of the switching surface can be expressed as the sum of two terms, i.e.  $k = k^* + \tilde{k}$ , where  $k^*$  is a constant representing the desired value of current  $i_{L_1}$  in steady-state while  $\tilde{k}$  describes the perturbation superimposed to that constant when the system is temporarily separated from the equilibrium point. Hence, for  $k = k^*$ , the equilibrium point of (22) will be given by

$$\begin{aligned} x^* &= [i_{L_1}^* \ v_{C_1}^* \ i_{L_2}^* \ v_{C_2}^*]^T \\ &= \left[ \frac{P}{\sqrt{V_{ref} V_g}} \ \sqrt{V_{ref} V_g} \ \frac{P}{V_{ref}} \ V_{ref} \right]^T \end{aligned} \quad (23)$$

where  $k^* = \frac{P}{\sqrt{V_{ref} V_g}}$ , which expresses the expected POPI behavior, i.e. input power = output power [34]. Taking into account (22) and (23), the ideal sliding dynamics can be linearized as:

$$\begin{aligned} \frac{d\tilde{v}_{C_1}}{dt} &= a_{11}\tilde{v}_{C_1} + a_{12}\tilde{i}_{L_2} + a_{13}\tilde{v}_{C_2} + b_{11}\tilde{k} + c_{11} \frac{d\tilde{k}}{dt} \\ \frac{d\tilde{i}_{L_2}}{dt} &= a_{22}\tilde{v}_{C_1} + a_{21}\tilde{i}_{L_2} + a_{23}\tilde{v}_{C_2} + b_{21}\tilde{k} + c_{21} \frac{d\tilde{k}}{dt} \\ \frac{d\tilde{v}_{C_2}}{dt} &= a_{33}\tilde{v}_{C_1} + a_{32}\tilde{i}_{L_2} + a_{33}\tilde{v}_{C_2} + b_{31}\tilde{k} + c_{31} \frac{d\tilde{k}}{dt} \end{aligned} \quad (24)$$

where the superscript ( $\sim$ ) stands for the increments of the variables around the corresponding equilibrium values. Besides, the expressions  $a_{ij}, b_{ij}, c_{ij}$ , ( $i, j \in \{1, \dots, 3\}$ ) are described as:

$$\begin{aligned} a_{11} &= \left. \frac{\partial g_1(x)}{\partial v_{C_1}} \right|_{x^*} = -\frac{P}{C_1 V_g V_{ref}} & a_{12} &= \left. \frac{\partial g_1(x)}{\partial i_{L_2}} \right|_{x^*} = -\frac{1}{C_1} \sqrt{\frac{V_{ref}}{V_g}} \\ a_{13} &= \left. \frac{\partial g_1(x)}{\partial v_{C_2}} \right|_{x^*} = 0 \\ b_{11} &= \left. \frac{\partial g_1(x)}{\partial k} \right|_{x^*} = \frac{1}{C_1} & c_{11} &= \left. \frac{\partial g_1(x)}{\partial k} \right|_{x^*} = -\frac{L_1}{C_1} \frac{P}{V_g V_{ref}} \\ a_{21} &= \left. \frac{\partial g_2(x)}{\partial v_{C_1}} \right|_{x^*} = \frac{2}{L_2} \sqrt{\frac{V_{ref}}{V_g}} & a_{22} &= \left. \frac{\partial g_2(x)}{\partial i_{L_2}} \right|_{x^*} = 0 \\ a_{23} &= \left. \frac{\partial g_2(x)}{\partial v_{C_2}} \right|_{x^*} = -\frac{1}{L_2} \\ b_{21} &= \left. \frac{\partial g_2(x)}{\partial k} \right|_{x^*} = 0 & c_{21} &= \left. \frac{\partial g_2(x)}{\partial k} \right|_{x^*} = \frac{L_1}{L_2} \sqrt{\frac{V_{ref}}{V_g}} \\ a_{31} &= \left. \frac{\partial g_3(x)}{\partial v_{C_1}} \right|_{x^*} = 0 & a_{32} &= \left. \frac{\partial g_3(x)}{\partial i_{L_2}} \right|_{x^*} = \frac{1}{C_2} \\ a_{33} &= \left. \frac{\partial g_3(x)}{\partial v_{C_2}} \right|_{x^*} = \frac{P}{C_2 v_{C_2}^2} & c_{31} &= \left. \frac{\partial g_3(x)}{\partial k} \right|_{x^*} = 0 \\ b_{31} &= \left. \frac{\partial g_3(x)}{\partial k} \right|_{x^*} = 0 \end{aligned}$$

By applying the Laplace transform to (24), the transfer function (25) is obtained:

$$G_{vk}(s) = \frac{\tilde{v}_{C_2}(s)}{\tilde{k}(s)} = \frac{\beta_2 s^2 + \beta_1 s + \beta_0}{s^3 + \alpha_2 s^2 + \alpha_1 s + \alpha_0} \quad (25)$$

where

$$\begin{aligned} \beta_2 &= a_{32} c_{21} \\ \beta_1 &= a_{32} (c_{11} a_{21} - a_{11} c_{21}) \\ \beta_0 &= a_{32} b_{11} a_{21} \\ \alpha_2 &= (-a_{11} - a_{33}) \\ \alpha_1 &= (a_{11} a_{33} - a_{23} a_{32} - a_{12} a_{21}) \\ \alpha_0 &= (a_{11} a_{23} a_{32} + a_{12} a_{21} a_{33}) \end{aligned}$$

$G_{vk}(s)$  relates the output voltage variations to the variations of  $k$ .

### B. OUTER CONTROL DESIGN

Using the control to output transfer function (25), a proportional-integral compensator is designed for the outer control loop. Thus, following the classical technique of pole assignment, the system loop gain can be expressed as:

$$T(s) = G_{vk}(s) \cdot \left( K_p + \frac{K_i}{s} \right) \quad (26)$$

and the characteristic equation of the system will be given by

$$\begin{aligned} 1 + T(s) &= s^4 + \underbrace{(\alpha_2 + \beta_2 K_p)}_{\lambda_3} s^3 + \underbrace{(\alpha_1 + \beta_1 K_p + \beta_2 K_i)}_{\lambda_2} s^2 + \\ &+ \underbrace{(\alpha_0 + \beta_0 K_p + \beta_1 K_i)}_{\lambda_1} s + \underbrace{\beta_0 K_i}_{\lambda_0} \end{aligned} \quad (27)$$

To ensure a good performance of the PI controller, a stability region is identified by means of the Routh-Hurwitz criteria, as shown in the green oval region in Figure 6.

Hence,  $K_p$  and  $K_i$  must remain within that region to guarantee the stability of the controlled system. Once the boundaries are obtained, the values  $K_p$  and  $K_i$  are derived using classical Bode's techniques. Consequently, 51° of phase margin and

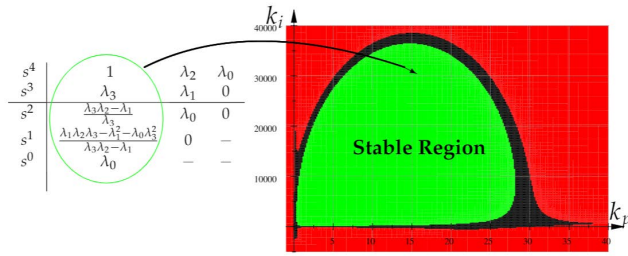


FIGURE 6. Local stability region in the  $K_p$ - $K_i$  plane applying routh-hurwitz criterion.

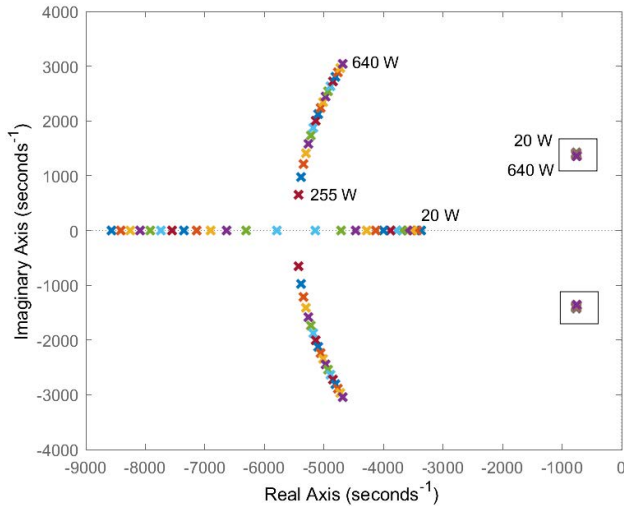


FIGURE 7. Location poles for a constant input voltage and a variable output power.

10 dB of gain margin are established to ensure the performance of the controller. Finally, with sisotool/MATLAB the controller is tuned, leading to

$$PI(s) = 0.95251 + \frac{952.51}{s} \quad (28)$$

Since the transfer function  $G_{vk}(s)$  has been derived from the linearization of the ideal sliding dynamics, the numerator and denominator coefficients will have a clear dependence on the equilibrium point coordinates due to the presence of  $P$  and  $V_g$ . Figure 7 shows the pole location of  $1 + T(s)$  for a constant input voltage of 380 V, a regulated value of 48 V in the output voltage and values of output power changing from 20 to 640 W with steps of 20 W.

On the other hand, Figure 8 shows the pole location of  $1 + T(s)$  for a constant output power of 400 W using input voltage values changing from 380 to 330 V with steps of 12.5 V. It is worth noting that the QBC loaded by CPL is stable over the entire proposed operating range, i.e.,  $P = [20, 640]$  W and  $V_g = [330, 380]$  V.

In order to verify the robustness of the controller, load power and input voltage perturbations are applied considering the operation of the converter at different equilibrium points of its working range. The perturbation will be applied for

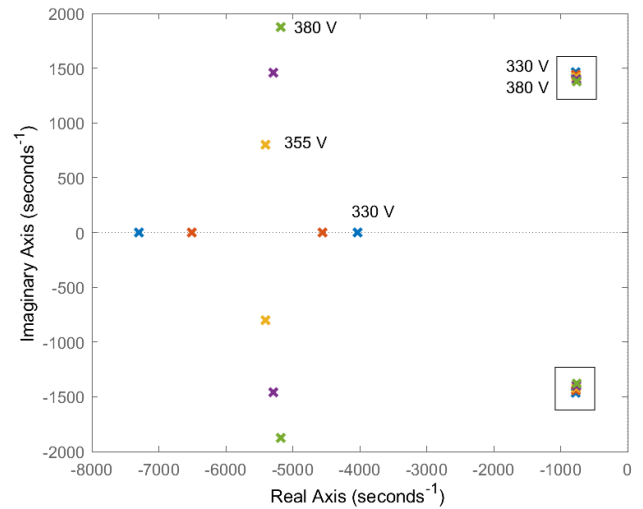


FIGURE 8. Location poles for a constant output power and a variable input voltage.

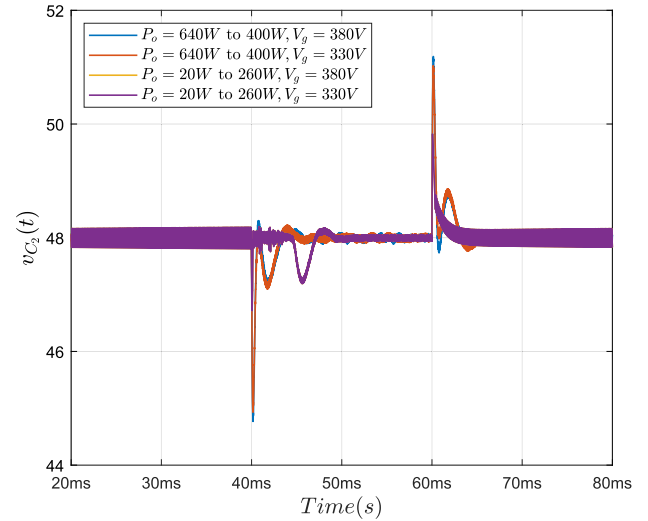
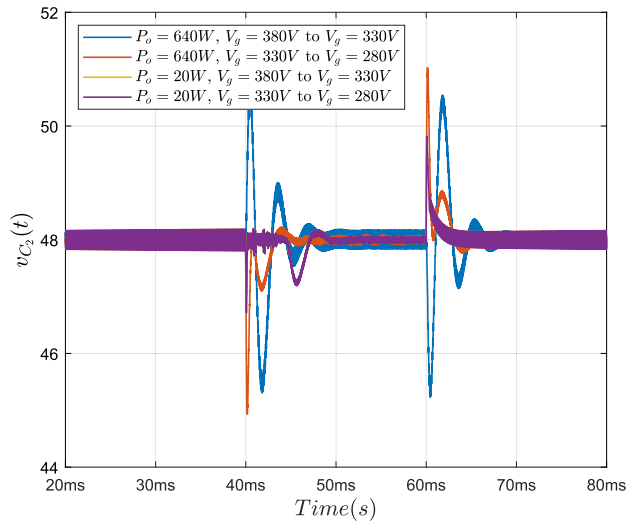


FIGURE 9. Output voltage responses of a QBC loaded by CPL for 240 W step variations of the output power in the extreme values of the converter operational range.

four different operating points at different load powers and input voltages. Figure 9 shows the voltage behavior of  $v_{C2}$  under a step perturbation of 240 W for 20 ms. Note that the perturbation of the load power produces a transient deviation of  $v_{C2}$  below 6.5%, which is totally rejected in less than 10 ms for the worst case.

Also, a 50 V step-type input voltage disturbance is applied to the converter. It can be seen from Figure 10 that the disturbances are rejected in approximately 10 ms showing a maximum transient voltage deviation of less than 6.5% for all cases. The above results demonstrate that the converter is capable of rejecting important disturbances in the input voltage and output load without significant deviations and also guaranteeing stability over the entire proposed operating range.





**FIGURE 10.** Output voltage responses of a QBC loaded by CPL for 50 V step variations of the input voltage in the extreme values of the converter operational range.

**TABLE 2.** Quadratic Buck converter parameter values.

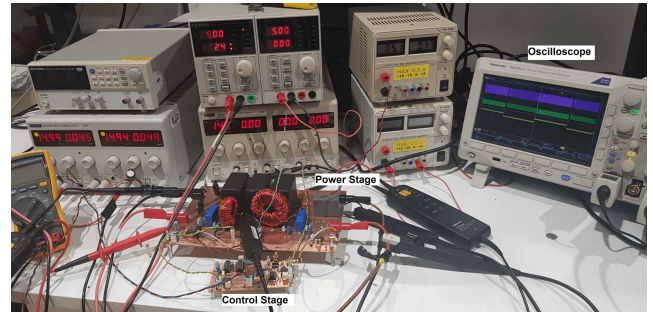
$V_g$	$V_{ref}$	$L_1$	$L_2$	$C_1$	$C_2$	P	$f_{sw}$
380V	48V	1.2 mH	300 $\mu$ H	300 $\mu$ F	100 $\mu$ F	400 W	30kHz

**V. SIMULATION AND EXPERIMENTAL RESULTS**

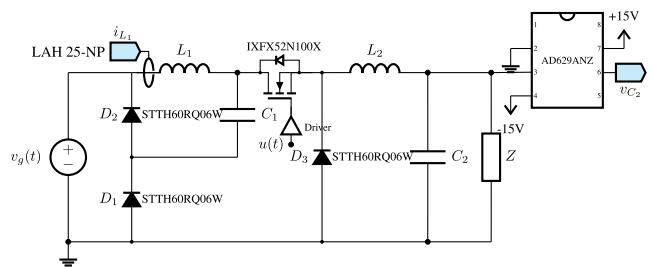
Validation of the theoretical analysis using numerical simulations and experimental results is reported in this section. The system consists of a quadratic buck converter supplied by a dc voltage source and loaded by a constant power load (CPL). The experimental setup has been implemented in the laboratory, as depicted in Figure 11. Two prototypes have been implemented, one for the power stage and another one for the control circuit. The power stage is depicted in Figure 12 and consists of two inductors ( $L_1, L_2$ ) implemented in the laboratory, two capacitors  $C_1$  (VISHAY 1848C MKP) and  $C_2$  (KEMET R60 MKT), three DIODES (sth60rq06w), and one MOSFET (IXFX52N100X). The inductor current is sensed using a current sensor (LAH25-NP), while the output voltage is sensed using a differential operational amplifier (AD629ANZ). The scheme of the sliding mode control circuit illustrated in Figure 13 and has been implemented using standard operational amplifiers, one comparator, and one flip-flop. An electronic load EA-EL-9750-75 has been used in the experiments working in three different modes, namely, CPL, CCL, and CRL. A power supply SPS 800  $\times$  13 is used as input voltage source for the QBC. The numerical simulation is performed using PSIM<sup>©</sup> software [35]. The parameter values used in both numerical simulations and experimental setup are shown in Table 2.

**A. QBC LOADED BY A CPL**

The QBC is loaded first by a CPL and checked under load variations in numerical simulations and experiments as shown in Figures 14-15. The load power has been stepped up from



**FIGURE 11.** Experimental Setup.



**FIGURE 12.** Power stage circuit scheme.

400 W to 640 W during 20 ms, which implies that the load current of the converter changes from 8.33 A to 13.33 A during that lapse of time while the load voltage is regulated.

Figure 14 shows that both inductor currents provide the increment of current demanded by the load while the output voltage  $v_{C_2}$  remains constant at 48 V as depicted in Figure 15. Note that the output voltage recovers the steady-state value after a fast transient regime with a settling time of 0.45 ms and an overshoot of 7.64%. A state-space trajectory in the plane ( $i_{L_2}, v_{C_2}$ ) under load change is shown in Figure 16, where two equilibrium points are observed i.e. point A for  $P = 400$  W and point B for  $P = 640$  W. Note that the existence of sliding conditions leads the state trajectory to slide on the switching surface and the equilibrium point locus in the two points. Moreover, high voltage regulation is guaranteed, and a high matching between the numerical simulation and experimental results is remarkable in Figures 14-16.

The QBC has been also tested for a step change of input voltage under fixed load power of 400 W. The input voltage has been stepped down from 380 V to 330 V during 50 ms as shown in Figures 17 and 18. The former shows the response of both inductor currents to the input voltage disturbance. When the input voltage decreases, both currents increase to feed the load with the same required power. However, the capacitor voltage  $v_{C_1}$  decreases, while the output voltage remains constant at 48 V as shown in Figure 18. It can be observed that the output voltage  $v_{C_2}$  presents a settling time of approximately 2.65 ms and an overshoot of 8.2%. Therefore, the results demonstrate the high regulation of the output voltage and the fast response of the switching regulator under both input voltage and output power disturbances.

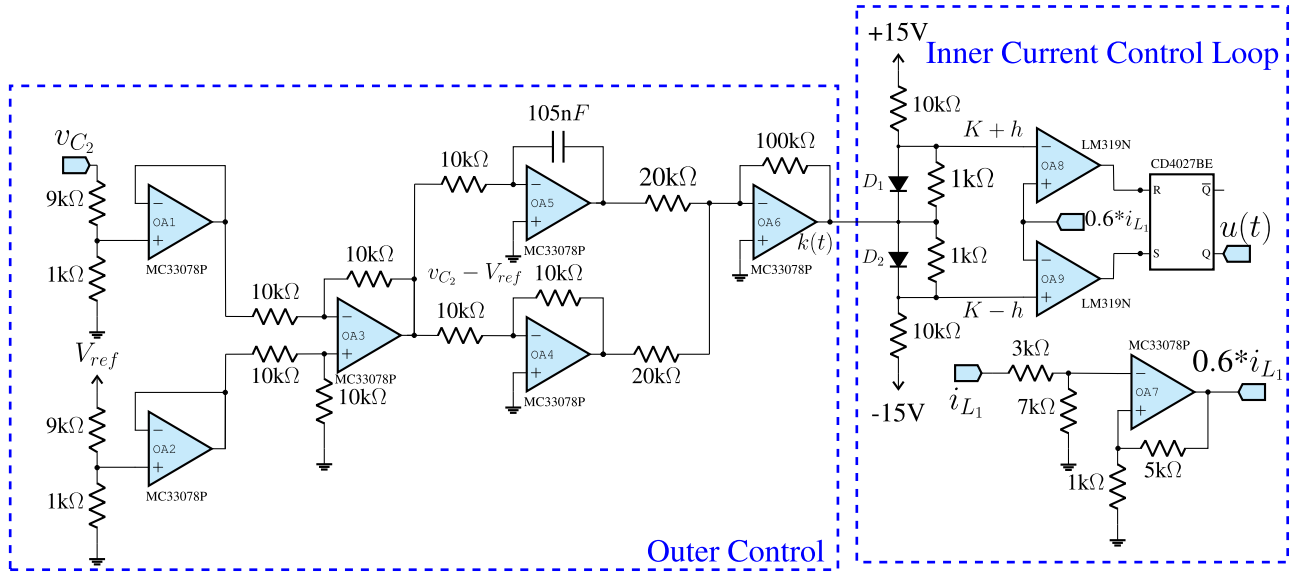
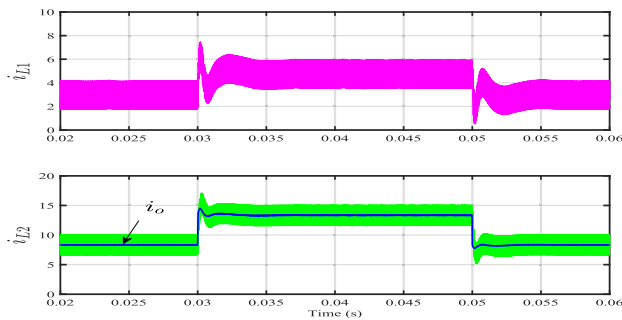
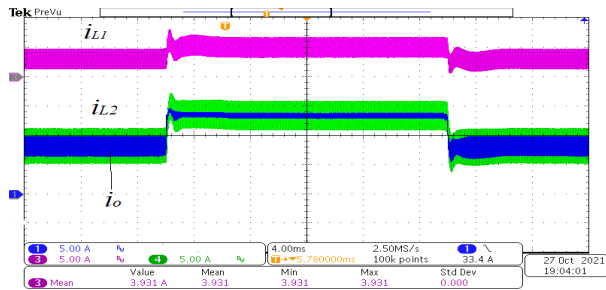


FIGURE 13. The schematic diagram of the implemented sliding control circuit.

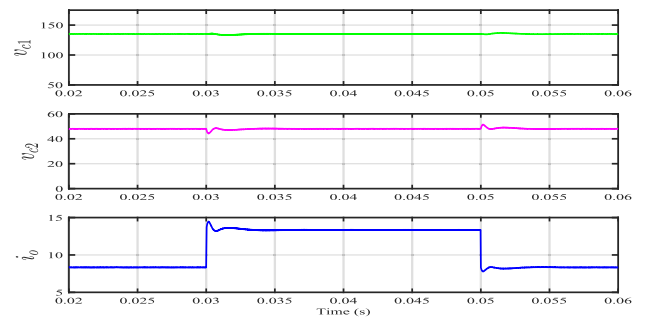


(a)

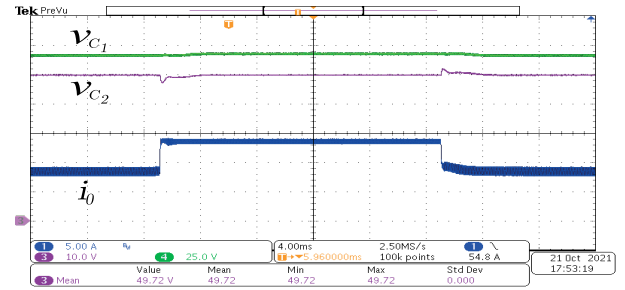


(b)

FIGURE 14. Inductor current behavior ( $i_{L1}$ ,  $i_{L2}$ ) of a QBC loaded by CPL for 5 A step variations of the output current (a) Numerical simulation. (b) Experimental results.



(a)



(b)

FIGURE 15. State variable response of a QBC loaded by CPL for an output current transients of 5 A. (a) Numerical simulation. (b) Experimental results.

### B. QBC UNDER DIFFERENT LOADS

More experimental results have been obtained considering two more different loads, a CCL and a CRL, to show the proposed control robustness. For a CCL type, the dynamic response of the QBC loaded by a CCL under load change from 8.3 A to 13.3 A is shown in Figures 19 (a-b). It can be observed that the system maintains a good regulation of the

output voltage, while the inductor currents and the capacitor voltage  $v_{C1}$  increase. Figures 19 (c-d) shows the response under input voltage variations between 380 V to 330 V. The results also show a good response regulation of the output voltage, while the inductor currents increase and capacitor voltage  $v_{C1}$  decreases.

On the other hand, for a CRL type, the dynamic response of the QBC loaded by a CRL under load resistance change

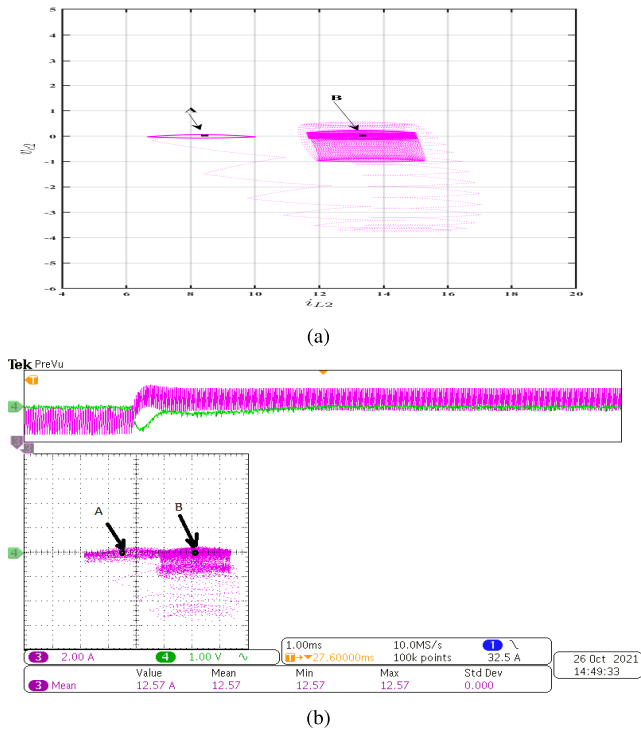


FIGURE 16. Trajectory of the system in the plane  $(i_{L2}, v_{C2})$  under load change of 5 A. (a) Numerical simulation. (b) Experimental results.

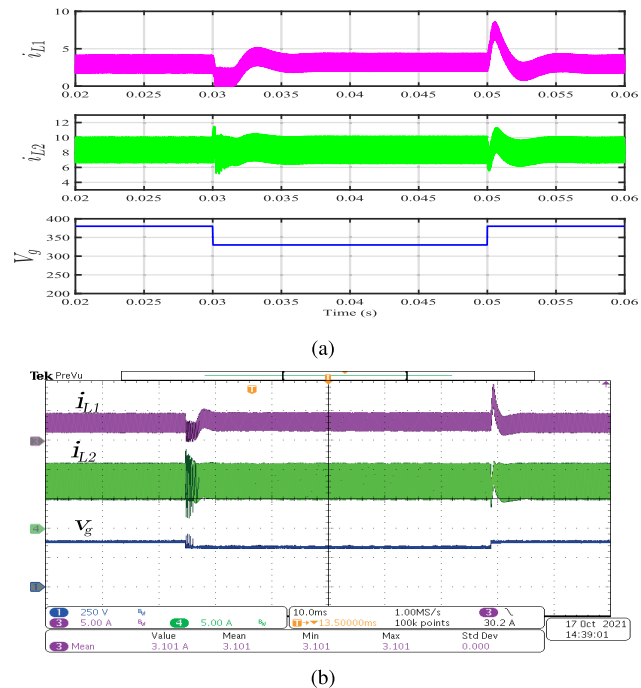


FIGURE 17. Inductor current behavior  $(i_{L1}, i_{L2})$  of a QBC loaded by CPL under input voltage transients from 380 V to 330 V. (a) Numerical simulation. (b) Experimental results.

from 5.76  $\Omega$  to 3.6  $\Omega$  is shown in Figures 19 (e-f). It can be observed that the system maintains a good regulation of the output voltage, while the inductor currents and the capacitor

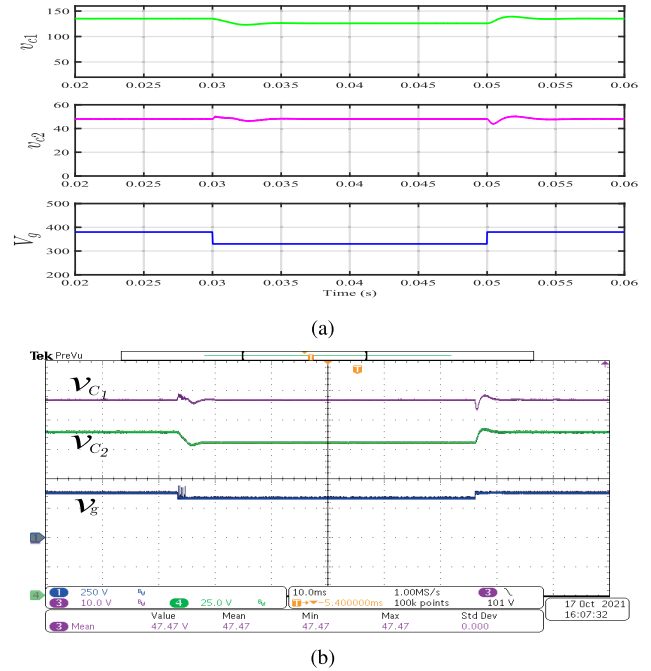


FIGURE 18. State variables response of a QBC loaded by CPL under input voltage transients from 380 V to 330 V. (a) Numerical simulation. (b) Experimental results.

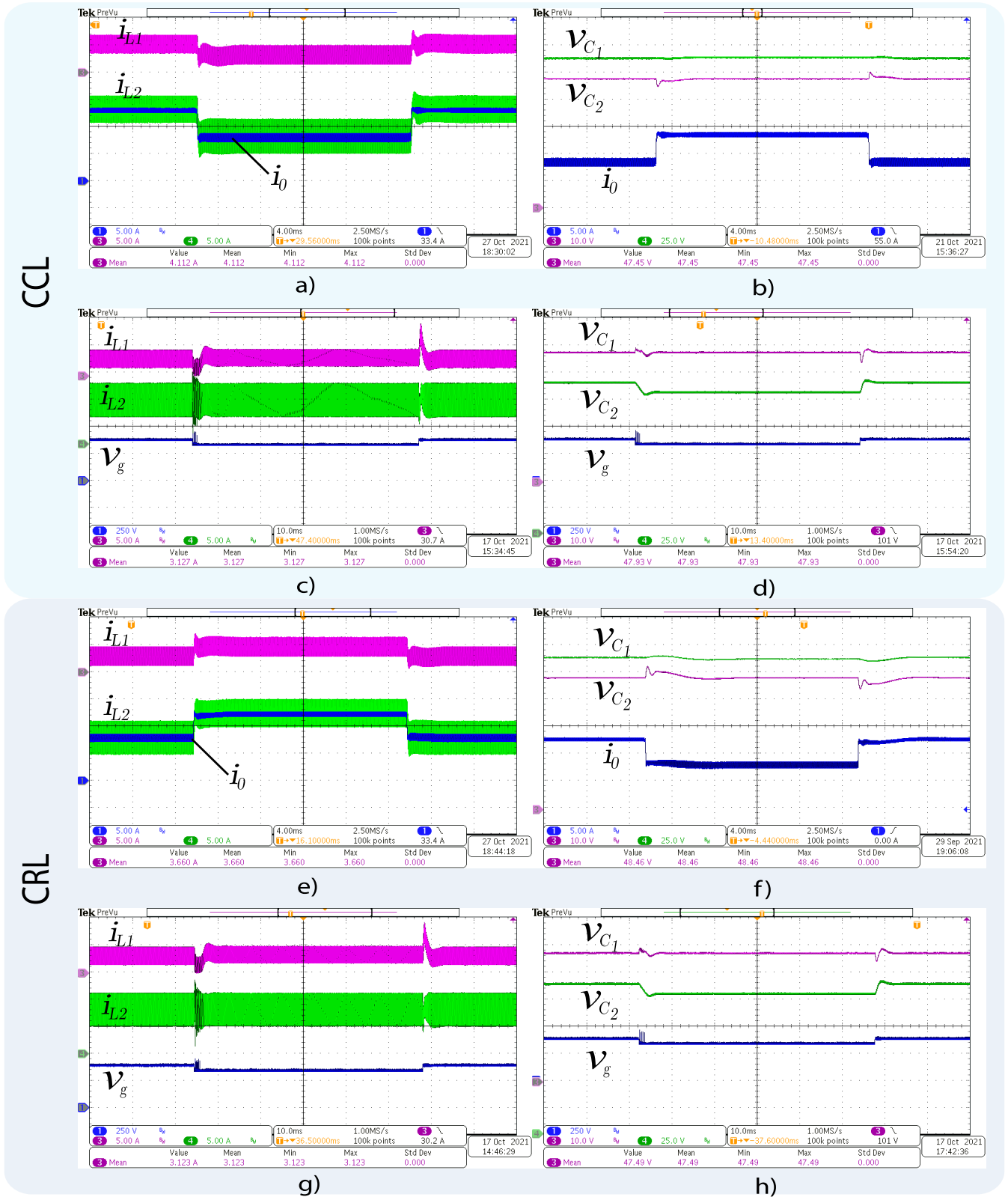
voltage  $v_{C1}$  increase. Figures 19 (g-h) shows the response under input voltage variations between 380 V to 330 V. The results also show a good response regulation of the output voltage, while the inductor currents increase and capacitor voltage  $v_{C1}$  decreases. Despite the disturbance, it can be observed that the output voltage and the state variables of the QBC exhibit practically the same regulation performance.

## VI. COMPARISON WITH A CLASSICAL LINEAR CONTROL

In this section, the performance of the proposed sliding-mode strategy is compared by means of PSIM simulations with a conventional linear approach based on a cascaded control [36] in which the inner loop is a peak-current control and the outer loop is a PI compensator processing the output voltage error as illustrated in Figure 20.

Figures 21 and 22 show the simulation results of the QBC in both cases assuming identical operating conditions, i.e. start-up and same disturbances in either input voltage or load power. The response of the sliding-mode controller is depicted in blue while that of the linear controller is illustrated in red.

It is apparent that no differences can be observed in the responses of both controllers when the converter is in steady-state  $[i_{L1} = 3 \text{ A}, v_{C1} = 135 \text{ V}, i_{L2} = 8, 25 \text{ A}, v_{C2} = 48 \text{ V}]$  and a disturbance of step type penetrates into the system. This is shown in Figure 21 for an input voltage variation from 380 V to 330 V at 30 ms, and then from 330 V to 380 V at 50 ms, and in Figure 22 for a load power change from 400 W to 640 W at 30 ms and back to 400 W at 50 ms. Now, the comparison is performed during start-up, which is



**FIGURE 19.** Experimental results of the QBC loaded by a CCL and a CRL. (a)-(b) state variables response under load current step of 5 A for a CCL load. (c)-(d) state variables response under input voltage transient from 380 V to 330 V for a CCL load. (e)-(f) State variable response under load step from 5.76  $\Omega$  to 3.6  $\Omega$  for a CRL load. (g)-(h) State variable response under input voltage transient from 380 V to 330 V for a CRL load.

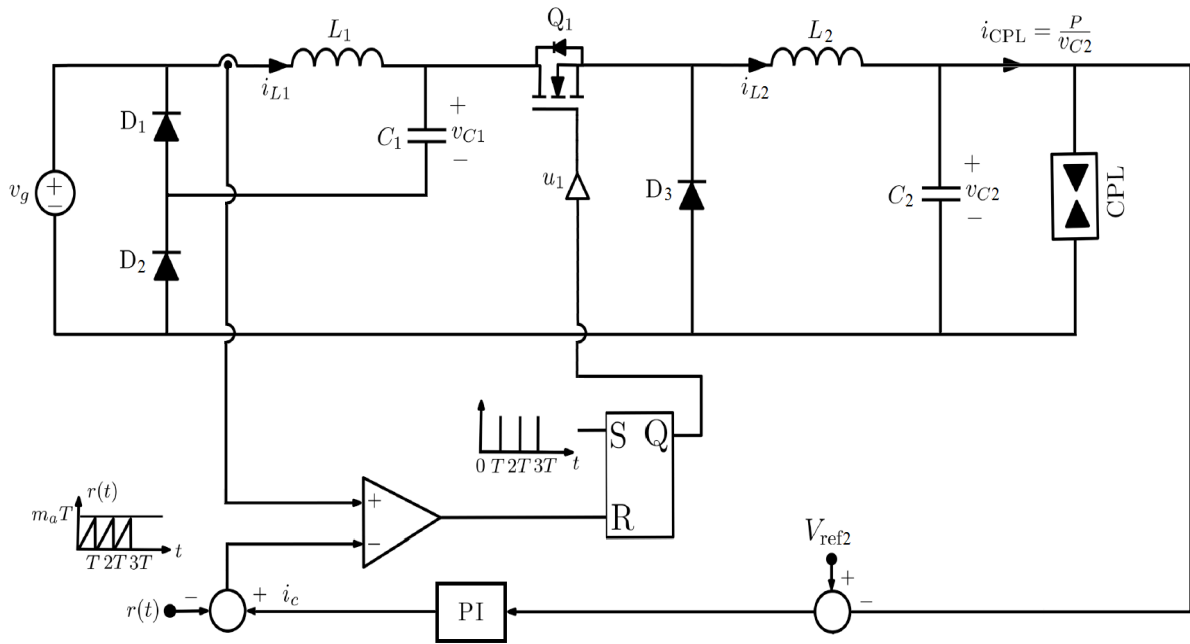


FIGURE 20. Block diagram of two-loop linear controller using peak-current control for the inner loop.

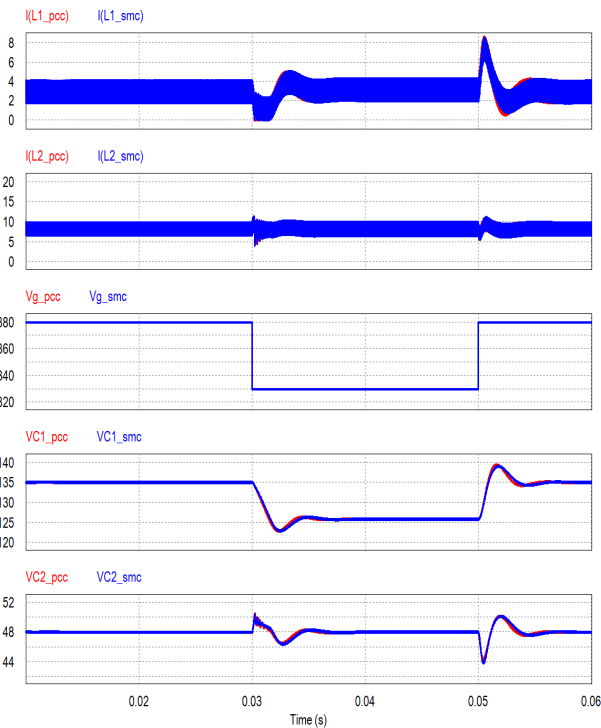


FIGURE 21. Response of the QBC with SMC (blue) and with linear two-loop control (red) for an input voltage disturbance.

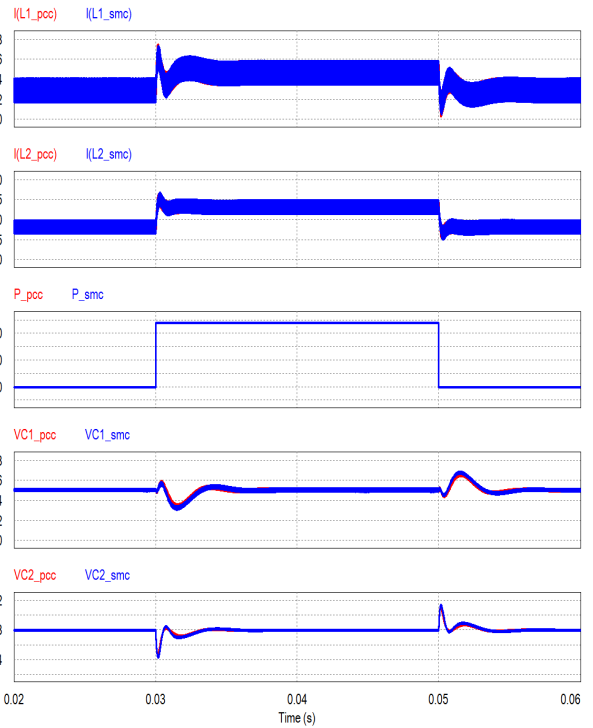


FIGURE 22. Response of the QBC with SMC (blue) and with linear two-loop control (red) for an output power disturbance.

carried out in both cases with a resistive load of  $5.75 \Omega$  that is replaced by the CPL when the system is in steady-state. A clear difference is observed in the peak of both inductor currents, which is around 25% higher in the case of the

two-loop linear controller as illustrated in Figure 23, in which zero initial conditions  $[i_{L1} = 0, v_{C1} = 0, i_{L2} = 0, v_{C2} = 0]$  are considered and the load resistance of  $5.75 \Omega$  dissipating

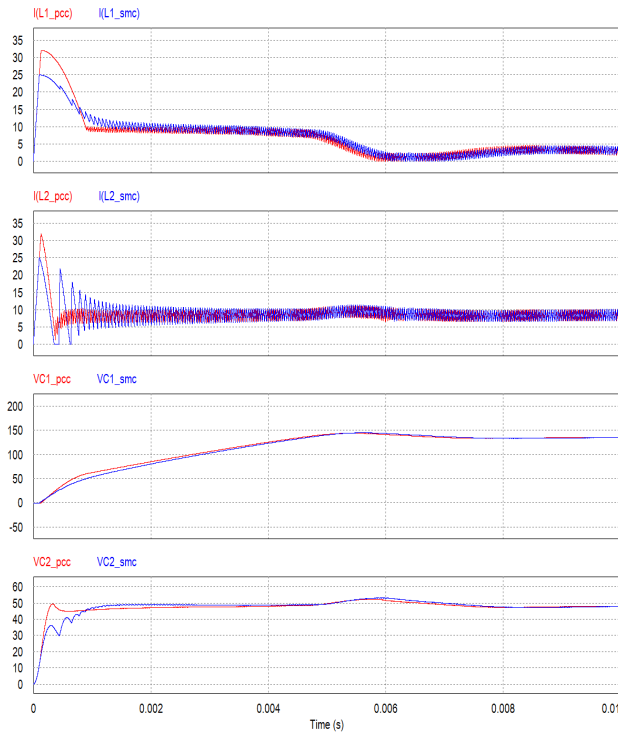


FIGURE 23. Start-up of the QBC with SMC (blue) and with linear two-loop control (red).

400W at 48 V is replaced at  $t = 10\text{ ms}$  by a CPL absorbing the same amount of power.

VII. CONCLUSION

This paper has shown that transferring energy from a 380 V DC bus to different types of load requiring a regulated voltage of 48 V DC can be carried out successfully with a single converter of QBC type. The one-way transference of energy is supervised by a cascade control, in which the inner loop operates in SMC and the outer loop is of PI type. The external loop performs indirectly the output voltage regulation by establishing the reference to the internal loop.

It has been demonstrated that the most appropriated inner loop is based on the SMC of the input inductor current because it leads all the state variables to a stable equilibrium point in the case of resistive load. This fact has opened the way to regulate the output voltage in the worst case of loading, i.e. when the QBC feeds a CPL. In that situation, however, the insertion of the inner control loop does not stabilize the system, this requiring the contribution of the outer loop for that purpose. The addition of a PI controller in the outer loop has required a detailed analysis of stability of the linearized model around the desired equilibrium point of the QBC. The analysis has combined the action of the SMC and the outer compensator in a single description.

A region of stability and robustness in terms of the PI parameters has been subsequently found and the final coefficients of the controller have been selected accordingly.

By means of PSIM simulations and an experimental prototype, the correct operation of the regulated QBC has been verified by showing a fast recovery of the output voltage in response to large variations of step-type in the input voltage and output power.

The results show the robustness of the designed controller under different types of loads and disturbances. It can be observed in the CPL case a settling time of 2.65 ms with an overshoot of 8.2% for the output voltage under a 13.16% of input voltage disturbance. Similarly, under a 60% of disturbance at the output current a settling time of 0.44 ms is observed together with an overshoot of 7.64% for the output voltage. It is worth mentioning that for both cases the under/overshoot is below 10%. Similar results have been obtained for other loads like CRL and CCL.

A comparison of the proposed control with a conventional alternative based on a cascade linear control has shown similar dynamic performance in the mitigation of the disturbances in both input voltage and CPL power penetrating into the system when the QBC is in steady-state. A better performance of the proposed control is observed during start-up exhibiting a lower level of inrush current.

Finally, it has to be pointed out that chattering here is inherent to the nature of switching conversion. The fast repetitive action of absorbing energy from the DC input source to store it in the inductors magnetic field and then transfer it to the DC output load constitutes the basic mechanism of power conversion but it is also the way that chattering (ripple) is produced. Power converters are variable structure systems where conventional SMC is the natural way to regulate them. In a clear-cut contrast, chattering reduction is an important objective in fixed structure systems like electrical drives in which high-order SMC is increasingly used [37].

Further research contemplates the study of the QBC as power gyrator [38] and its potential use in paralleling DC-DC switching converters [39].

APPENDIX

The sliding-mode existence conditions can be written as follows:  $S_1\dot{S}_1 \leq -m|S_1|$ ,  $m > 0$ , where  $m \leq \frac{|S_1(0)|}{T}$  is selected to guarantee a given reaching time  $T$

On the other hand,  $\frac{dS_1}{dt}$  can be expressed as:

$$\begin{aligned} \frac{dS_1}{dt} &= \frac{di_{L1}}{dt} - \frac{dk(t)}{dt} \\ \frac{dS_1}{dt} &= \frac{di_{L1}}{dt} - K_p \frac{i_{L2}}{C_2} + K_p \frac{P}{C_2 v_{C2}} - K_i (V_{ref} - v_{C2}) \end{aligned} \tag{A1}$$

Introducing the expression of  $\frac{di_{L1}}{dt}$  given by (12) in (A1) results in:

$$\frac{dS_1}{dt} = -\frac{v_{C1}}{L_1} + \frac{V_g u}{L_1} + \frac{K_p}{C_2} \left( \frac{P}{v_{C2}} - i_{L2} \right) - K_i (V_{ref} - v_{C2}) \tag{A2}$$

$S_1 > 0 \implies_{u=0} \frac{dS_1}{dt} \leq -m$ , and therefore

$$-\frac{v_{C1}}{L_1} + \frac{K_p}{C_2} \left( \frac{P}{v_{C2}} - i_{L2} \right) - K_i (V_{ref} - v_{C2}) \leq -m \quad (A3)$$

We define  $M_1$  as follows:

$$M_1 \geq \left| \frac{K_p}{C_2} \left( \frac{P}{v_{C2}} - i_{L2} \right) - K_i (V_{ref} - v_{C2}) \right| \quad (A4)$$

(A3) will be satisfied provided that  $-\frac{v_{C1}}{L_1} + M_1 \leq -m$ .

Equivalently,

$$m \leq \frac{v_{C1}}{L_1} - M_1 \quad (A5)$$

Similarly, for  $S_1 < 0$

$$\implies_{u=0}$$

$\frac{dS_1}{dt} \leq m$ , and therefore

$$\frac{V_g - v_{C1}}{L_1} + \frac{K_p}{C_2} \left( \frac{P}{v_{C2}} - i_{L2} \right) - K_i (V_{ref} - v_{C2}) \leq m \quad (A6)$$

(A6) is fulfilled if

$$\frac{V_g - v_{C1}}{L_1} + M_1 \leq m \quad (A7)$$

From (A5) and (A7) we conclude that

$$\frac{V_g - v_{C1}}{L_1} + M_1 \leq m \leq \frac{v_{C1}}{L_1} - M_1 \quad (A8)$$

which guarantees the reachability of the switching surface in finite time.

## REFERENCES

- [1] L. F. Costa and M. Liserre, "Failure analysis of the DC-DC converter: A comprehensive survey of faults and solutions for improving reliability," *IEEE Power Electron. Mag.*, vol. 5, no. 4, pp. 42-51, Dec. 2018.
- [2] J. D. Paez, D. Frey, J. Maneiro, S. Bacha, and P. Dworakowski, "Overview of DC-DC converters dedicated to HVdc grids," *IEEE Trans. Power Del.*, vol. 34, no. 1, pp. 119-128, Feb. 2019.
- [3] S. A. Gorji, H. G. Sahebi, M. Ektesabi, and A. B. Rad, "Topologies and control schemes of bidirectional DC-DC power converters: An overview," *IEEE Access*, vol. 7, pp. 117997-118019, 2019.
- [4] M. Forouzesh, P. Y. Siwakoti, A. S. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC-DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143-9178, Dec. 2017.
- [5] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC microgrids—Part I: A review of control strategies and stabilization techniques," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4876-4891, Jul. 2016.
- [6] T. Dragicevic, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC Microgrids—Part II: A review of power architectures, applications, and standardization issues," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3528-3549, May 2016.
- [7] S. Rivera and B. Wu, "Electric vehicle charging station with an energy storage stage for split-DC bus voltage balancing," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2376-2386, Mar. 2017.
- [8] P. Lindman and L. Thorsell, "Applying distributed power modules in telecommunication systems," *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 365-373, Mar. 1996.
- [9] O. López-Santos, Y. A. Aldana-Rodríguez, G. Garcia, and L. Martínez-Salamero, "A unified multimode control of a DC-DC interlinking converter integrated into a hybrid microgrid," *Electronics*, vol. 8, no. 11, p. 1314, Nov. 2019, doi: 10.3390/electronics8111314.
- [10] A. Leon-Masich, H. Valderrama-Blavi, J. M. Bosque-Moncusí, J. Maixe-Altes, and L. Martínez-Salamero, "Sliding-mode-control-based boost converter for high-voltage-low-power applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 229-237, Jan. 2015.
- [11] A. León-Masich, H. Valderrama-Blavi, J. M. Bosque-Moncusí, and L. Martínez-Salamero, "Efficiency comparison between Si and SiC-based implementations in a high gain DC-DC boost converter," *IET Power Electron.*, vol. 8, no. 6, pp. 869-878, Jun. 2015.
- [12] H. Valderrama-Blavi, E. Rodríguez-Ramos, C. Olalla, and X. Genaro-Muñoz, "Sliding-mode approaches to control a microinverter based on a quadratic boost converter," *Energies*, vol. 12, no. 19, p. 3697, Sep. 2019.
- [13] Q. Zhao and F. C. Lee, "High-efficiency, high step-up DC-DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 65-73, Jan. 2003.
- [14] I. Barbi and R. Gules, "Isolated DC-DC converters with high-output voltage for TWTA telecommunication satellite applications," *IEEE Trans. Power Electron.*, vol. 18, no. 4, pp. 975-984, Jul. 2003.
- [15] L.-S. Yang, T.-J. Liang, and J.-F. Chen, "Transformerless DC-DC converters with high step-up voltage gain," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3144-3152, Aug. 2009.
- [16] D. Maksimovic and S. Cuk, "Switching converters with wide DC conversion range," *IEEE Trans. Power Electron.*, vol. 6, no. 1, pp. 151-157, Jan. 1991.
- [17] O. L. Santos, "Contribution to the DC-AC conversion in photovoltaic systems: Module oriented converters," *Electr. Power.*, INSA de Toulouse, 2015.
- [18] L. dos R. Barbosa, J. B. Vieira, L. C. de Freitas, M. da Silva Vilela, and V. J. Farias, "A buck quadratic PWM soft-switching converter using a single active switch," *IEEE Trans. Power Electron.*, vol. 14, no. 3, pp. 445-453, May 1999.
- [19] E. E. Carbajal-Gutierrez, J. A. Morales-Saldana, and J. Leyva-Ramos, "Modeling of a single-switch quadratic buck converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 41, no. 4, pp. 1450-1456, Oct. 2005.
- [20] J. A. Reyes-Malanche, N. Vázquez, and J. Leyva-Ramos, "Switched-capacitor quadratic buck converter for wider conversion ratios," *IET Power Electron.*, vol. 8, no. 12, pp. 2370-2376, Dec. 2015.
- [21] B. A. Martínez-Treviño, "Nonlinear control of DC-DC switching converters with constant power load," Ph.D. dissertation, Dept. Electron. Eng., Electr. Autom., Rovira i Virgili Univ., Tarragona, Spain, 2019.
- [22] A. M. Rahimi and A. Emadi, "Active damping in DC/DC power electronic converters: A novel method to overcome the problems of constant power loads," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1428-1439, May 2009.
- [23] Y. Li, K. R. Vannorsdel, A. J. Zirger, M. Norris, and D. Maksimovic, "Current mode control for boost converters with constant power loads," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 198-206, Jan. 2012.
- [24] B. A. Martínez-Treviño, A. El Aroudi, E. Vidal-Idiarte, A. Cid-Pastor, and L. Martínez-Salamero, "Sliding-mode control of a boost converter under constant power loading conditions," *IET Power Electron.*, vol. 12, no. 3, pp. 521-529, 2019.
- [25] B. A. Martínez-Treviño, A. E. Aroudi, A. Cid-Pastor, and L. Martínez-Salamero, "Nonlinear control for output voltage regulation of a boost converter with a constant power load," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10381-10385, Nov. 2019.
- [26] B. A. Martínez-Treviño, A. E. Aroudi, H. Valderrama-Blavi, A. Cid-Pastor, E. Vidal-Idiarte, and L. Martínez-Salamero, "PWM nonlinear control with load power estimation for output voltage regulation of a boost converter with constant power load," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2143-2153, Feb. 2021.
- [27] L. Martínez-Salamero, *Sliding Mode Control of Power Converters in Renewable Energy Systems*. Printed Edition of the Special Issue Published in *Energies*, 2020.
- [28] J. S. J. Utkin and V. Guldner, *Sliding Mode Control in Electromechanical Systems*, 2nd ed. Boca Raton, FL, USA: CRC Press, 2000.
- [29] L. Martínez-Salamero, A. Cid-Pastor, R. Giral, J. Calvente, and V. Utkin, "Why is sliding mode control methodology needed for power converters?" in *Proc. 14th Int. Power Electron. Motion Control Conf. (EPE-PEMC)*, 2010, pp. 25-31.
- [30] H. Sira-Ramirez, "Sliding motions in bilinear switched networks," *IEEE Trans. Circuits Syst.*, vol. CS-34, no. 8, pp. 919-933, Aug. 1987.
- [31] R. T. Yadlapalli and A. Kotapati, "A fast-response sliding-mode controller for quadratic buck converter," *Int. J. Power Electron.*, vol. 6, no. 2, pp. 103-130, 2014.

- [32] R. Haroun, A. El Aroudi, A. Cid-Pastor, E. Vidal-Idiarte, H. Valderrama-Blavi, and L. Martínez-Salamero, "Modelling and control of modular DC-nanogrids based on loss-free resistors," *IEEE Access*, vol. 8, pp. 33305–33317, 2020.
- [33] L. Martínez-Salamero, A. Cid-Pastor, A. El Aroudi, R. Giral, J. Calvente, and G. Ruiz-Magaz, "Sliding-mode control of DC–DC switching converters," *IFAC Proc. Volumes*, vol. 44, no. 1, pp. 1910–1916, 2011.
- [34] S. Singer and R. W. Erickson, "Canonical modeling of power processing circuits based on the POPI concept," *IEEE Trans. Power Electron.*, vol. 7, no. 1, pp. 37–43, Jan. 1992.
- [35] *PSIM User's Guide, Version 9.0*, Power Smart Control SL, Madrid, Spain, 2010.
- [36] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Springer, 2007.
- [37] I. Boiko, L. Fridman, A. Pisano, and E. Usai, "Performance analysis of second-order sliding-mode control systems with fast actuators," *IEEE Trans. Autom. Control*, vol. 52, no. 6, pp. 1053–1059, Jun. 2007.
- [38] A. Cid-Pastor, L. Martínez-Salamero, C. Alonso, B. Estibals, J. Alzieu, G. Schweitz, and D. Shmilovitz, "Analysis and design of power gyrators in sliding-mode operation," *IEE Proc.-Electr. Power Appl.*, vol. 152, no. 4, pp. 821–826, Jul. 2005.
- [39] A. Cid-Pastor, L. Martínez-Salamero, C. Alonso, R. Leyva, and S. Singer, "Paralleling DC–DC switching converters by means of power gyrators," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2444–2453, Nov. 2007.



**CARLOS ANDRÉS TORRES-PINZÓN** received the bachelor's and master's degrees in electrical engineering from Universidad Tecnológica de Pereira (UTP), Pereira, Colombia, in 2006 and 2008, respectively, and the master's and Ph.D. degrees in electronic engineering from Universitat Rovira i Virgili, Tarragona, Spain, in 2010 and 2012, respectively. He was a Lecture Assistant at Universidad Tecnológica de Pereira from 2006 to 2007. He is currently an Associate

Professor with the Facultad de Ingeniería Electrónica, Universidad de Santo Tomás, Bogotá D.C., Colombia. His main research interests include robust control, sliding-mode control, DC-DC converters design, and control and energy management systems.



**FREDDY FLORES-BAHAMONDE** (Member, IEEE) was born in Osorno, Chile, in 1983. He received the M.Sc. and Ph.D. degrees in electronics engineering from Universitat Rovira i Virgili (URV), Tarragona, Spain, in 2009 and 2013, respectively. In 2015, he joined as a Postdoctoral Fellow at the Advanced Center for Electrical and Electronic Engineering (AC3E), Universidad Técnica Federico Santa María (UTFSM), Valparaíso, Chile. In 2017, he was in-charge of the energy area in the technology transfer unit of the AC3E developing and managing industrial projects related to energy and electric power systems. He is currently an Assistant Professor with the Engineering Sciences Department, Universidad Andrés Bello, where he is also a Researcher with the Center for Energy Transformation. His main research interests include the design and control of power converters for renewable energies, automotive power systems, and DC microgrids.



**JUAN ANTONIO GARRIGA-CASTILLO** (Member, IEEE) received the B.Sc. degree (Ingeniero Técnico) in telecommunications engineering from the Polytechnic University of Catalonia (UPC), in 1989, the engineering degree (Ingeniero en Electrónica) from the University of Barcelona (UB), in 2005, the MSc. degree in electronic engineering and the Ph.D. degree from the University Rovira i Virgili (URV), in 2013 and 2020, respectively. He is a member of the Robotics and

Signal Processing Research Group, University of Lleida (UdL). His research interests include the design and control of DC/DC converters for energy harvesting applications.



**HUGO VALDERRAMA-BLAVI** (Member, IEEE) received the graduate and Ph.D. degrees in ingeniero de telecomunicación from the Polytechnic University of Catalonia Barcelona, Spain, in 1994 and 2001, respectively. From 2001 to 2002, he was a Postdoctoral Researcher at LAAS-CNRS, Toulouse, France, working in multilevel conversion and renewable energy systems. Since 1997, he has been working with the Departament d'Enginyeria Electrònica, Elèctrica i Automàtica, Escola Tècnica Superior d'Enginyeria, Universitat Rovira i Virgili, Tarragona, Spain, where he is currently Associate Professor. Since 2018, he has been directs the Master's Degree Program of Universitat Rovira i Virgili in electric vehicle technologies. He has conducted of several research projects sponsored by the Spanish Ministry of Science and Innovation, and he has coauthored more than 30 journal articles and many conference papers. He is a member of the Group of Automatic Control and Industrial Electronics (GAEI), Rovira i Virgili University. His current research interests include power electronics, power conditioning for electric vehicles, microgrids, multilevel inverters, electric vehicle battery modeling, battery fast charging systems, photovoltaics systems, and other renewable energy sources.



**REHAM HAROUN** (Member, IEEE) was born in Egypt, in 1982. She received the graduate degree in power and electrical engineering and the master's degree from Aswan Faculty of Engineering, South Valley University, Aswan, Egypt, in 2004 and 2009, respectively, and the Ph.D. degree from Universitat Rovira i Virgili, Tarragona, Spain, in 2014. She was a Lecture Assistant at South Valley University, from 2004 to 2009. She was a member of the Aswan Power Electronics Application

Research Center (APEARC) Group. She is currently a Researcher with the Group of Automatic Control and Industrial Electronics (GAEI), Rovira i Virgili University. Her research interests include power electronics applications including dc–dc switched power supplies and ac–dc converters with power factor correction (PFC).



**LUIS MARTÍNEZ-SALAMERO** (Senior Member, IEEE) received degree in ingeniero de telecomunicación and the Ph.D. degree from Universidad Politècnica de Catalunya, Barcelona, Spain, in 1978 and 1984, respectively.

From 1978 to 1992, he taught circuit theory, analog electronics and power processing at the Escuela Técnica Superior de Ingenieros de Telecomunicación, Barcelona. From 1992 to 1993, he was a Visiting Professor at the Center for Solid State Power Conditioning and Control, Department of Electrical Engineering, Duke University, Durham, NC, USA. From 2003 to 2004, from 2010 to 2011, and from March 2018 to September 2018, he was a Visiting Scholar at the Laboratory of Architecture and Systems Analysis (LAAS), National Agency for Scientific Research (CNRS), Toulouse, France. Since 1995, he has been a Full Professor with the Department of Electrical Electronic and Automatic Control Engineering, School of Electrical and Computer Engineering, Rovira i Virgili University, Tarragona, Spain, where he managed the Research Group in Automatic Control and Industrial Electronics (GAEI) from 1998 to 2018. His research interests include structure and control of power conditioning systems, electrical architecture of satellites and electric vehicles, nonlinear control of converters and drives, and power conditioning for renewable energy.

...