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A Low-Power Wide-Load-Range Output-Capacitorless Low-Dropout Voltage Regulator With Indirect-Direct Nested Miller Compensation

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ABSTRACT This paper presents the design of an output-capacitorless low-dropout voltage regulator (OCL-LDO) capable of driving a wide range of load capacitance and supplying a wide range of load current while maintaining excellent load and line regulations, thanks to the combined indirect-direct nested Miller compensation which ensures stability and maintains a high loop gain over the whole range of load condition. Fabricated in a 0.18-μm CMOS process and consuming 14 μA of quiescent current, the OCL-LDO, while supplying the load current between 0 mA to 100 mA, is capable of driving the load capacitance in the range of 0-1 nF; with a minimum load current of 1 mA, however, the OCL-LDO can drive up to 10 nF of load capacitance. Over such wide load-current and load-capacitance ranges, the OCL-LDO achieves DC load and line regulations of 0.025 mV/mA and 0.5 mV/V, respectively.

INDEX TERMS Output-capacitorless, low-dropout voltage regulator, wide load range, load regulation, line regulation, low-power regulator, nested Miller compensation, system-on-chips, power management circuits.

I. INTRODUCTION

In the past several decades, the world has witnessed technological revolution at a rate unparalleled in the previous history of mankind, thanks to the advent of system-on-chips (SoCs) that provides ubiquitous computing power to almost all aspects of human life. Integrated with many functionalities in a very small footprint, SoCs make possible various computing tasks ranging from high-speed number crunching in mainframe computers down to sensing, processing, and communication normally performed in wireless low-power sensor interfaces [1]–[4].

In low-power sensor interfaces, supplying power to the SoC's core is normally performed by a low-dropout voltage regulator (LDO) generating a clean power supply from rippled DC voltage produced by a switching DC-DC converter. In applications requiring very small footprint such as radio-frequency identification (RF-ID) tags [5]–[7] or wirelessly-powered medical implants [8]–[11], LDO, especially the ones requiring no off-chip capacitor to stabilize its operation (output-capacitorless LDO or OCL-LDO in short), may often be the sole component providing power to the SoC's core as it eliminates off-chip passive components normally required in most switching DC-DC converters. In recent years, research on OCL-LDO has gained increasing popularity, with a major emphasis on improving the OCL-LDO's response to fast changes in the load current [12]–[16], especially from high-speed on-chip digital and RF circuits—in other words, making the OCL-LDO behave more like an ideal voltage source over as high a bandwidth as possible. As OCL-LDO employs feedback to regulate its output voltage to a certain reference, a fast-response OCL-LDO normally requires a very large loop bandwidth, which leads to higher quiescent power. However, employing a high-speed OCL-LDO can be an overkill in some low-power SoC's architectures in which the high-speed circuits are powered

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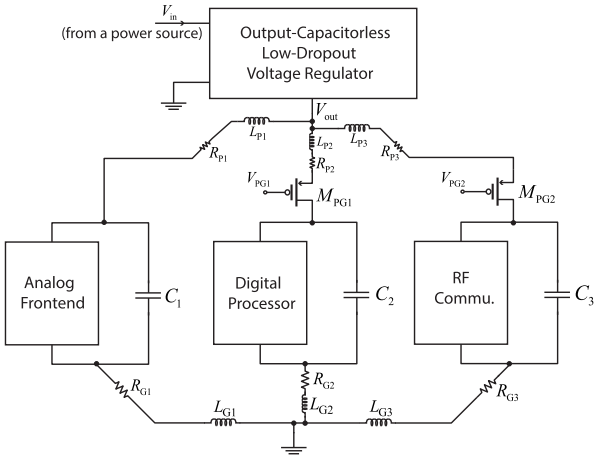

FIGURE 1. The concept of SoC with power gating that inspires this work.

off most of the time to save power, and powered on only briefly to perform necessary tasks. In addition, it might not be practical in such applications to leave the supply regulation of the high-speed circuits solely to the OCL-LDO since, no matter how ideal is the OCL-LDO, significant voltage spikes can still develop from the IR drop across parasitic resistance and inductance in the supply lines and also across the ON resistances of the power-gating transistors. Hence, in practical SoCs housing high-speed circuits, supply decoupling capacitors, mostly in the form of MOS capacitor due to its high-density capacitance, are normally placed in close proximity and connected to the supply nodes of these circuits to help smooth out their supply voltages.

To appreciate this, consider a scenario depicted in Fig. 1 in which an OCL-LDO is to power a low-power SoC's core that consists of many modules—sensitive low-power analog frontend, high-speed digital processor, and radio-frequency (RF) communication module. The main task of this SoC is to continuously but slowly senses the input data from the environment, store it in a local memory, and then process and wirelessly transmit the stored data to a receiver outside. To save power from the leakage and standby current, the digital and RF modules may be powered down most of the time—with the power-gating transistors M_{PG1} and M_{PG2} to help minimize leakage current—-and powered up only briefly to quickly process and transmit data to an off-chip receiver. Each block has its own local capacitor, C_1-C_3, close by to help smooth out its supply voltage. Due to the fast switching nature of the digital processor and the speed of the RF module, their on-chip supply-decoupling capacitors are normally much larger—often in the nanofarad range [17], [18]—compared to that of the analog frontend. We can now envision that—most of the time when the digital and RF modules are powered down and cut off from the OCL-LDO by M_{PG1} and M_{PG2}—the OCL-LDO will see only the small C_1 (possibly around tens of pF) and needs to supply only small load current (possibly around tens of μA). However, during the brief periods when both the digital and RF modules are powered up and connected to the OCL-LDO's output via M_{PG1} and M_{PG2}, the OCL-LDO will see very large capacitive load from C_2 and C_3 (possibly from hundreds of pF's to a few nF's) and may need to supply a very large load current (tens of milliamps). Therefore, the OCL-LDO designed for such applications should be guaranteed stable over the load current ranging from a few μA's to several tens of mA's and a load capacitance ranging from a few pF's to a few nF's. Furthermore, in applications such as the RF-ID tag, the input voltage into the OCL-LDO may vary appreciably depending on the state of its power source—e.g., the distance between an RF-ID tag and its reader. Hence, the OCL-LDO not only needs to provide a very accurate output voltage across a wide load current range (good DC load regulation), it also does for a wide input voltage range (good DC line regulation).

To achieve good DC load and line regulations, conventional LDOs are usually implemented as three-stage feedback circuits—two-stage error amplifier (EA) followed by an output stage comprising a power transistor—to provide very large loop gain. The wide load current and load capacitance ranges make stabilization of a three-stage LDO very challenging. Hence, most conventional LDOs employ a very large off-chip capacitor (normally in the μF's range) at the output to make the output pole dominant regardless of the load current and load capacitance; the equivalent series resistance (ESR) within the off-chip capacitor also helps improve stability by creating a left-half-plane (LHP) zero that helps cancel the effect of the first non-dominant pole within the LDO [19]–[25]. However, such a large off-chip output capacitor is not available for an OCL-LDO. Therefore, stabilization of an OCL-LDO often requires creating the dominant pole out of an internal node within the circuit.

There are many realizations of this principle. The simplest category is the class of OCL-LDOs that employ only two gain stages in feedback for ease of compensation. Stabilization of such topology is achieved by ensuring that the dominant pole is associated with the internal node (i.e., the gate of the power MOSFET, which normally exhibits large capacitance) and not the output node (i.e., by requiring minimum load current and/or maximum load capacitance). The popular flipped-voltage-follower-based (FVF-based) OCL-LDOs [26]–[30] can be categorized in this class along with those employing differential opamp-based error amplifiers (EA) [15], [31], [32]. Lacking an explicit frequency-compensation scheme, the FVF-based OCL-LDOs in [26]–[30] often require a certain minimum load currents or maximum load capacitances to ensure that the output pole is beyond the unity-gain bandwidth to guarantee stability, thus, making the load current and capacitance ranges quite narrow. Also, due to their meager loop gains, these two-stage OCL-LDOs normally exhibit inferior DC load/line regulations compared to other topologies with higher loop gain.

Improving the load/line regulations can be achieved by an addition of another gain stage within the LDO's feedback loop, making it a three-stage feedback circuit. The FVF-based OCL-LDO in [33] and differential EA-based OCL-LDOs

in [34]–[36] are some examples. With three gain stages in their feedback loops, these OCL-LDOs often employ a Miller compensation approach to ensure stability as in the design of three-stage opamps. However, compensation of a three-stage OCL-LDO is much more difficult than that of a three-stage opamp due to the OCL-LDO's output pole occupying a very wide range as the load condition changes: if not prudently compensated, the LDO may exhibit closed-loop poles that are nicely damped at a certain load conditions but become very underdamped (have a high Q-factor) at other load conditions. Many methods were proposed to limit the Q-factor in three-stage LDOs—e.g., [34] employs a damping-factor control circuit to create a dominant pole at the output of the first gain stage; [12] proposes a current feedback scheme to reposition an internal pole based on the load current; [37] proposes a topology that is automatically configured as a two-stage or three-stage feedback depending on the load current; and [14], [36], [38] use some forms of the nested Miller compensation to progressively reposition the open-loop poles/zeros without degrading the DC loop gain. However, the aforementioned LDOs are still not quite suitable for our application because they: i) still require quite a sizable minimum load current which often increases as the load capacitance increases ([14], [34]); ii) sacrifice the loop gains at a certain ranges of the load current ([12], [37]) to ensure stability, which hurts the load/line regulations; iii) require a very large on-chip compensation capacitance to ensure stability ([36]).

In this work, we propose the design of a three-stage OCL-LDO capable of operating over wide ranges of load current (0-100 mA) and load capacitance (0-1 nF under zero load current), while providing very good DC load and line regulations over the entire range of the load current. To stabilize the OCL-LDO while keeping the Q-factor of the complex poles low at all the load conditions, we employ a nested Miller compensation consisting of both the direct and indirect (cascode) feedback paths [39]; the indirect paths are responsible for the normal pole-splitting operation while the direct path helps constrain the Q-factor of the complex poles. In addition, the analysis of three-stage OCL-LDOs employing nested Miller compensation is often very complicated, especially for OCL-LDOs with very wide load-current and load-capacitance ranges. The analyses presented in the literature usually involve solving for the overall closed-loop transfer functions, which are very complicated and lacking the design insights into the roles different circuit components play in stabilizing the OCL-LDO. Hence, in this work, we employ a graphical feedback viewpoint in compensating the OCL-LDO, with the hope of shedding some lights into how to best attempt the design to ensure stability over all the load conditions of interest.

The paper is organized as follow: Section II and III provide an overview of the proposed OCL-LDO's architecture and the detailed mathematical analysis of the indirect-direct nested Miller compensation method; Section IV then applies the result from Section III to graphically visualize the effects of the compensation at various load conditions. Section V then presents the detailed implementation of the OCL-LDO while Section VI and VII validate the proposed design with simulation and experimental results. Finally, Section VIII concludes the paper.

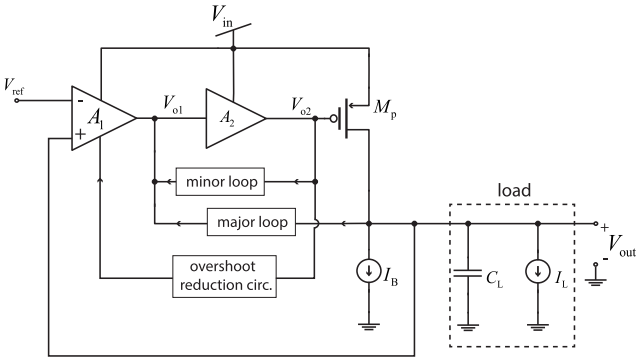

FIGURE 2. High-level architecture of the proposed OCL-LDO.

II. OVERVIEW OF THE PROPOSED OCL-LDO

Unlike conventional LDOs with large off-chip capacitors to help stabilize the output voltage during large changes in the load current, OCL-LDOs rely solely on their internal feedback mechanisms to regulate their output voltages. Thus, for fast response to change in the load current, an OCL-LDO is normally designed with a much higher loop bandwidth than those of the conventional LDOs. However, to avoid severe degradation in the loop gain at very high load current while still preserving low dropout voltage, a wide-load-range OCL-LDO normally employs a large power transistor to ensure its operation in the saturation region. Even then, the loop gain still depends quite strongly on the load current as the power transistor's $g_m r_o$ product, which determines the gain of the output stage, is inversely proportional to the load current. Hence, to achieve a good load/line regulations, it's important to ensure that the EA's gain remains high over the entire load-current range to compensate for the drop in gain of the output stage at high load current.

Fig. 2 shows the conceptual diagram of our proposed OCL-LDO. Instead of sacrificing the EA's gain through the current-feedback mechanism [12] or switching between the two and three-stage topologies as the load current changes [37], we choose to keep the proposed OCL-LDO as a three-stage feedback circuit and the gain of its EA high throughout the entire load-current range; as will be explained in Section V, the EA is implemented as a two-stage amplifier, the first gain stage (A_1) employing a folded-cascode topology to provide a very high gain while the second gain stage (A_2) employing a common-source topology to provide an additional gain. Using the common-source topology with a moderate gain as a second stage also helps separate the very high-impedance output node of the first gain stage from the large parasitic capacitance at the gate of the power transistor, thus extending the OCL-LDO's unity-gain bandwidth. To stabilize the OCL-LDO over the entire load-current and

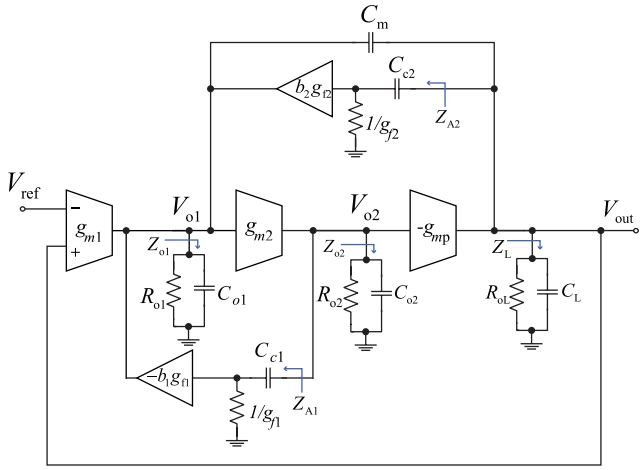

FIGURE 3. Indirect-direct nested Miller compensation scheme of the proposed OCL-LDO (with the overshoot reduction circuit ignored to simplify the analysis).

load-capacitance ranges, we employ a nested Miller compensation seen as the minor loop and the major loop in Fig. 2, with the major loop consisting of both an indirect capacitive-feedback path and a direct capacitive feedback path while the minor loop consisting only of an indirect capacitive-feedback path. The details on how such combined feedback scheme helps stabilize the OCL-LDO over the whole load ranges will be provided in Section IV. To help speed up the OCL-LDO's response to abrupt change in the load current without wasting static power, we also incorporate an overshoot reduction circuit, which detects the change of the power transistor's gate voltage to appropriately increase the bias current of the EA, thus temporarily extending the OCL-LDO's overall bandwidth.

III. THE COMBINED INDIRECT-DIRECT FREQUENCY-COMPENSATION METHOD

To achieve a high loop gain over wide load-current and input-voltage ranges, we propose a frequency-compensation scheme shown in Fig. 3—with the overshoot reduction circuit removed to simplify our analysis—in which the three gain stages are explicitly displayed. The error amplifier comprises the first two gain stages, represented as the operational transconductance amplifiers (OTAs) g_{m1} and g_{m2}, respectively. The power transistor M_p in Fig. 2 comprises the third gain stage, denoted as the OTA g_{mp} in Fig. 3. Shown in Fig. 3 are also two compensation feedback loops: the major loop consisting of the capacitors C_{c2} and C_m and the minor loop consisting of the capacitor C_{c1}. As will be discussed in Section V, the capacitors C_{c1} and C_{c2} form cascode compensation networks, in which their left plates feed to the source terminals of two PMOS transistors within the error amplifier, which help buffer the feedback currents to the output node of the first gain stage—i.e., node V_{o1} in Fig. 3. We then model the PMOS cascode buffers as the OTAs labelled b_1g_{f1} and b_2g_{f2} in Fig. 3; each OTA exhibits an effective transconductance of b_ig_{fi} and an input resistance of $1/g_{fi}$, $i \in \{1, 2\}$—intuitively, g_{fi} is the source conductance of the respective PMOS transistor while b_i, a positive value less than unity, represents the fraction of the fed-back current through C_{ci} that is buffered by the PMOS transistor to the node V_{o1}. The capacitor C_m in the major feedback path is a traditional Miller compensation capacitance whose purpose is to limit the Q-factor of the complex poles resulting from the cascode compensation [40]. Providing a direct feedthrough path from V_{o1} to V_{out}, the capacitor C_m, if its value is too large, may introduce a right-half-plane (RHP) zero in the OCL-LDO's loop transfer function, thus degrading its stability. Therefore, it is important to appropriately choose the value of C_m to ensure low Q-factor while avoiding the RHP zero. We will explain using a graphical method how to intuitively determine the values of various circuit components to stabilize the OCL-LDO across the entire load ranges in Section IV.

A. SMALL-SIGNAL MODELLING

Before we develop a small-signal feedback diagram for analyzing the operation of the proposed OCL-LDO in Fig. 3, let's define

$$\begin{aligned} Z_{A1} &= \frac{1}{sC_{c1}} + \frac{1}{g_{f1}} \\ Z_{A2} &= \frac{1}{sC_{c2}} + \frac{1}{g_{f2}} \end{aligned} \tag{1}$$

as the impedances seen into the two current buffers through C_{c1} and C_{c2}, respectively, and

$$\begin{aligned} Z_{o1} &= R_{o1} \parallel \frac{1}{sC_{o1}} \\ Z_{o2} &= R_{o2} \parallel \frac{1}{sC_{o2}} \\ Z_L &= R_{oL} \parallel \frac{1}{sC_L} \end{aligned} \tag{2}$$

as the output impedances of the first, second, and third gain stages, respectively. Then, applying the Kirchoff's current law (KCL) at the nodes V_{o1}, V_{o2}, and V_{out} yields

$$-g_{m1}(V_{ref} - V_{out}) + \frac{b_1}{Z_{A1}}V_{o2} + \frac{b_2}{Z_{A2}}V_{out} + sC_m(V_{out} - V_{o1}) = \frac{V_{o1}}{Z_{o1}}, \tag{3}$$

$$g_{m2}V_{o1} = \frac{V_{o2}}{Z_{o2} \parallel Z_{A1}}, \tag{4}$$

and

$$-g_{mp}V_{o2} = \frac{V_{out}}{Z_{A2} \parallel Z_L} + sC_m(V_{out} - V_{o1}), \tag{5}$$

respectively.

The expressions in (3)-(5) can be directly translated to the block diagram in Fig. 4(a) in which the minor feedback loop is nested inside the major feedback loop. Here, let's make a few simplifications to transform this diagram into a form suitable for our graphical analysis. First, let's consider the effect of

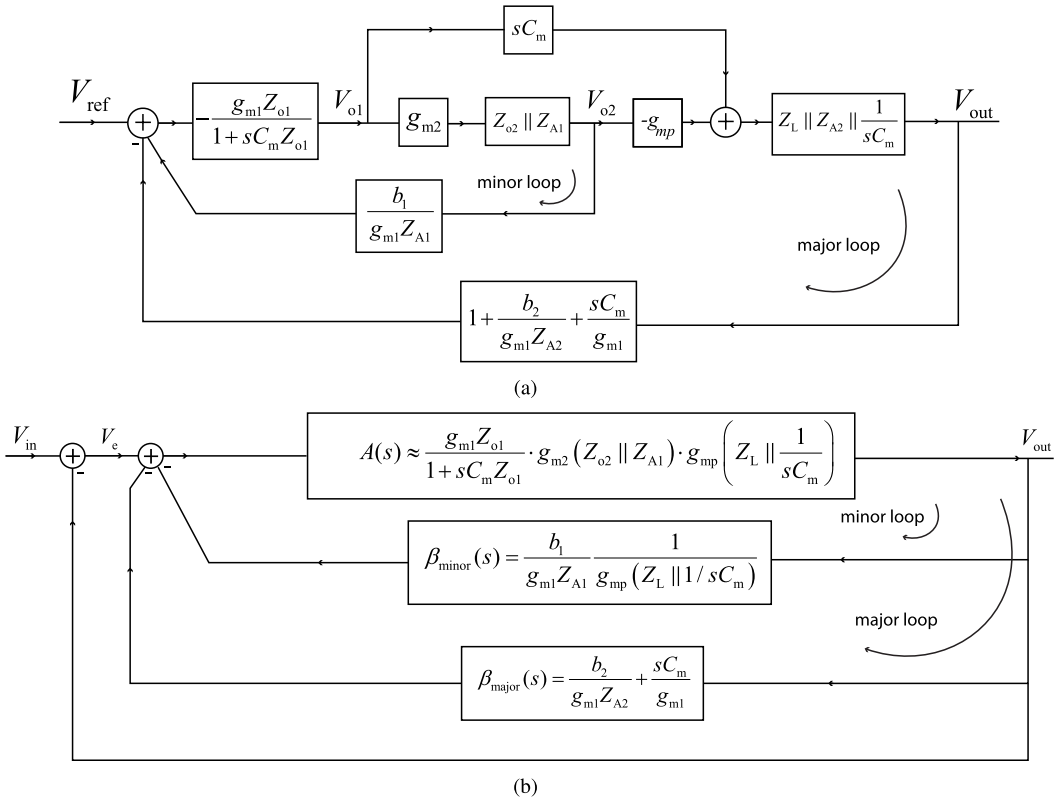

FIGURE 4. (a) Original feedback block diagram of the proposed OCL-LDO. (b) Simplified block diagram.

the compensation capacitance C_m connecting between the node V_{o1} and V_{out} in Fig. 3. This compensation capacitance introduces the feedthrough current path, with an admittance of sC_m, from the node V_{o1} to the output node V_{out}. Normally, as intuited from the block diagram in Fig. 4(a), such feedthrough path often introduces a right-half-plane (RHP) zero at the frequency at which the magnitude of the sC_m term is equal to that of the $g_{m2}(Z_{o2} \parallel Z_{A1})g_{mp}$ term. However, if we make C_m small enough and the loaded gain of the second gain stage ($g_{m2}(Z_{o2} \parallel Z_{A1})$) high enough, we can push the resulting RHP zero to a high enough frequency such that it can be ignored. Our next simplification concerns the term $Z_L \parallel Z_{A2} \parallel 1/sC_m$—i.e., the impedance seen by the output stage. Since the load capacitance C_L also includes the parasitic drain capacitance of the large power MOSFET, its value, even with the OCL-LDO's explicit load capacitance excluded, is much larger than the compensation capacitance C_{c2} (which is a part of Z_{A2}). Hence, we can safely conclude that the magnitude of the $Z_L \parallel 1/sC_m$ term is much smaller than that of Z_{A2}, thus allowing us to approximate $Z_L \parallel Z_{A2} \parallel 1/sC_m$ as just $Z_L \parallel 1/sC_m$. Another simplification that we shall make is to move the feedback path originating from V_{o2} (of the minor loop) to from V_{out}; this manipulation requires that we divide the feedback term $b_1/(g_{m1}Z_{A1})$ in Fig. 4(a) by the gain from V_{o2} to V_{out} ($-g_{mp}(Z_L \parallel 1/sC_m)$). Finally, we denote the unity factor of the major feedback path as a standalone feedback path to arrive at the simplified block diagram in Fig. 4(b).

Fig. 4(b) offers three main benefits in understanding the small-signal operation of the OCL-LDO. First, the diagram depicts how the OCL-LDO actually employs feedback to regulate its output V_{out}: it compares V_{out} to the reference voltage V_{in} to produce the error voltage $V_e = V_{in} - V_{out}$, which must be minimized by the high loop gain of the OCL-LDO. Second, the diagram makes evident the roles of different parts of the OCL-LDO in regulating V_e: the forward-path transfer function $A(s)$ captures the overall gain of the three gain stages including their loading effects; the feedback-path transfer functions $\beta_{minor}(s)$ and $\beta_{major}(s)$ show how the two feedback compensation networks in Fig. 3 provide feedback compensation for the overall OCL-LDO. Finally, the diagram is in a very simple feedback form in which all the feedback paths originating from the output are to be subtracted from the input. With such simple form, the overall loop transfer function of the OCL-LDO is simply

$$L(s) = \frac{V_{out}}{V_e}(s) = \frac{A(s)}{1 + A(s)\left(\beta_{minor}(s) + \beta_{major}(s)\right)} \quad (6)$$

To minimize the error signal V_e, we must make the magnitude of $L(s)$ large while still keeping the overall feedback loop nicely stable. However, architecting $L(s)$ to achieve good stability margins is often made difficult due to little insights offered from the complicated expression of $L(s)$ if solved directly from (6). Hence, in this work, we resort to the use of a graphical technique to help visualize different components of $L(s)$ such that we can design different components to achieve

a satisfactory $L(s)$. To do so, let's start by writing (6) in a more amenable form for our graphical visualization technique:

$$L(s) = A(s) \parallel \frac{1}{\beta(s)}, \tag{7}$$

where $1/\beta(s) = (1/\beta_{\text{major}}(s)) \parallel (1/\beta_{\text{minor}}(s))$. Since the stability margins of a feedback loop is mostly determined by the behavior of its loop transfer function at the unity-gain crossover, our task in the frequency compensation of the OCL-LDO is to architect $L(s)$ such that its unity-gain crossover behavior is close to being first-order. By writing $L(s)$ as a parallel combination of two transfer functions as in (7), we can approximate $L(s)$ by the fact that the transfer function with the lowest magnitude dominates the parallel combination. In other words, by comparing the magnitudes of $A(s)$ and $1/\beta(s)$ on the same Bode plot, we can take the lower portions of the two curves to represent the magnitude of $L(s)$, hence obtaining an approximated form of $L(s)$. To proceed with such approach, let's find simple closed-form expressions of $A(s)$ and $1/\beta(s)$ for use in our graphical approximation.

B. APPROXIMATION OF A(s) AND 1/β(s) FOR GRAPHICAL ANALYSIS

First, let's start with the forward-path transfer function of Fig. 4(b)

$$A(s) \approx \frac{g_{m1}Z_{o1}}{1+sC_mZ_{o1}} \cdot g_{m2}\left(Z_{A1} \parallel Z_{o2}\right) \cdot g_{mp}\left(Z_L \parallel \frac{1}{sC_m}\right). \tag{8}$$

Substituting the expressions of Z_{A1}, $Z_{o1,2}$, and Z_L from (1) and (2) into (8), we can explicitly write $A(s)$ as

$$A(s) \approx \frac{A_{oL}\left(1+sC_{c1}/g_{f1}\right)}{\left(1+\frac{s}{\omega_{o1}}\right)\left(1+\frac{s}{\omega_{o2,1}}\right)\left(1+\frac{s}{\omega_{o2,2}}\right)\left(1+\frac{s}{\omega_{oL}}\right)}, \tag{9}$$

where

$$\begin{aligned} A_{oL} &= g_{m1}R_{o1}g_{m2}R_{o2}g_{mp}R_{oL} \\ \omega_{o1} &= 1/R_{o1}\left(C_{o1}+C_m\right) \\ \omega_{o2,1} &\approx g_{f1}/\left(C_{c1}+g_{f1}R_{o2}\left(C_{c1}+C_{o2}\right)\right) \\ \omega_{o2,2} &\approx \left(1+g_{f1}R_{o2}\left(1+\frac{C_{o2}}{C_{c1}}\right)\right)/R_{o2}C_{o2} \\ \omega_{oL} &= 1/R_{oL}\left(C_{oL}+C_m\right). \end{aligned} \tag{10}$$

From (9), A_{oL} represents the overall low-frequency gain of the three gain stages, ω_{o1} the pole associated with the first gain stage (as introduced by Z_{o1}), and ω_{oL} the pole associated with the output node. The poles at $\omega_{o2,1}$ and $\omega_{o2,2}$ and the zero at g_{f1}/C_{c1} arise from the impedance $Z_{A1} \parallel Z_{o2}$ associated with the output node of the second gain stage. In simplifying (8) into (9), we have made an assumption that the two poles of $Z_{A1} \parallel Z_{o2}$ are real and that $\omega_{o2,1} \ll \omega_{o2,2}$ such that we can approximate $\omega_{o2,1}$ and $\omega_{o2,2}$ as in (10) (see the Appendix).

For our proposed OCL-LDO, the values of ω_{o1} and $\omega_{o2,1}$ are quite low (well below the unity-gain frequency of $A(s)$) while the value of $\omega_{o2,2}$ is quite high (often above the unity-gain frequency of $A(s)$). The value of ω_{oL}, however, varies widely depending on the load condition (C_L and I_L). On one extreme, at very low I_L (in which R_{oL} becomes large due to the large r_o of the power transistor) and very large C_L, ω_{oL} becomes the dominant pole of $A(s)$. Such a load condition normally places ω_{oL}, ω_{o1}, and $\omega_{o2,1}$ below the unity-gain frequency of $A(s)$ while placing the rest of the corner frequencies above it. As a result, $A(s)$ behaves as a third-order transfer function at its unity-gain crossover frequency. On the other extreme, when I_L becomes very large such that R_{oL} becomes much smaller, the value of ω_{oL} becomes so large that it is well above the unity-gain frequency of $A(s)$. As a result, only ω_{o1} and $\omega_{o2,1}$ are below the unity-gain frequency of $A(s)$, making $A(s)$ a second-order transfer function at its unity-gain frequency. Such wide-ranging behavior of $A(s)$ at its unity-gain frequency dictates that, instead of relying on $A(s)$, we must carefully devise $1/\beta(s)$ to ensure that the loop transfer function ($L(s)$ in (7)) behave as a first-order transfer function at its unity-gain crossover. Hence, we shall find a simple closed-form expression of $1/\beta(s)$ next.

To find $1/\beta(s)$, let's write the expressions of $1/\beta_{\text{major}}(s)$ and $1/\beta_{\text{minor}}(s)$ as

$$\begin{aligned} \frac{1}{\beta_{\text{major}}(s)} &= \frac{g_{m1}Z_{A2}}{b_2} \parallel \frac{g_{m1}}{sC_m} \\ \frac{1}{\beta_{\text{minor}}(s)} &= \frac{g_{m1}Z_{A1}}{b_1} \cdot g_{mp}\left(Z_L \parallel \frac{1}{sC_m}\right). \end{aligned} \tag{11}$$

Substituting Z_{A1}, Z_{A2}, and Z_L from (1) and (2) into (11) and performing some algebraic manipulations, we obtain

$$\frac{1}{\beta_{\text{major}}(s)} = K_{\text{major}}\frac{1}{s} \cdot \frac{1+sC_{c2}/g_{f2}}{1+s/\omega_{\text{major}}} \tag{12}$$

and

$$\frac{1}{\beta_{\text{minor}}(s)} = K_{\text{minor}}\frac{1}{s} \cdot \frac{1+sC_{c1}/g_{f1}}{1+s/\omega_{oL}}, \tag{13}$$

where

$$\begin{aligned} K_{\text{major}} &= \frac{g_{m1}}{b_2\left(C_{c2}+C_m/b_2\right)} \\ K_{\text{minor}} &= \frac{g_{mp}R_{oL}}{b_1} \cdot \frac{g_{m1}}{C_{c1}} \\ \omega_{\text{major}} &= g_{f2}/\left(\frac{C_m}{b_2} \parallel C_{c2}\right). \end{aligned} \tag{14}$$

In our design, we try to make the zero frequencies of (12) and (13) very close to each other such that we can define $\omega_z = g_{f1}/C_{c1} = g_{f2}/C_{c2}$. In practice, there is inevitably mismatch in the values of the two zeros but, as long as the two zero frequencies are close enough with each other, the errors resulting from such approximation can be thought of as introducing additional singularities at very high frequencies such that, for the purpose of our analysis, they can be ignored. Finally, with the approximation involving ω_z, we can derive $1/\beta(s)$ as a parallel combination of $1/\beta_{\text{major}}(s)$ in (12) and $1/\beta_{\text{minor}}(s)$ in (13) as

$$\frac{1}{\beta(s)} = \frac{K_{\text{major}} \parallel K_{\text{minor}}}{s} \cdot \frac{1+s/\omega_z}{1+s/\omega_p} \tag{15}$$

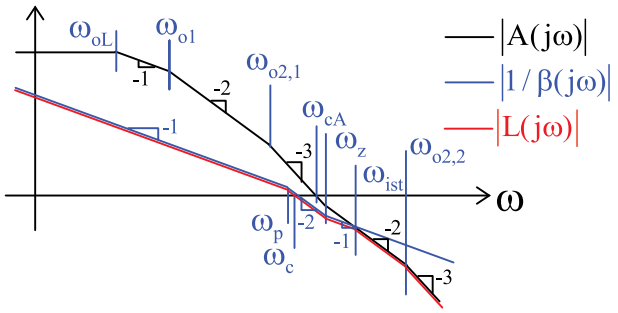

FIGURE 5. Theoretical Bode magnitude plots of $A(s)$ and $1/\beta(s)$ for approximating $L(s)$ for Case 1 ($\omega_{oL} < \omega_{o1}, \omega_{o2,1}$).

where

$$\omega_p = \omega_{major}\left(1+\frac{K_{major}}{K_{minor}}\right) \parallel \omega_{oL}\left(1+\frac{K_{minor}}{K_{major}}\right). \quad (16)$$

IV. GRAPHICAL COMPENSATION

Having obtained the expressions of $A(s)$ and $1/\beta(s)$, we are now ready to graphically compensate $L(s)$ to ensure good stability margins over wide load conditions. Since the load condition directly affects the value of ω_{oL}, we will divide our discussion into three cases based on how the value of ω_{oL} is relative to those of ω_{o1} and $\omega_{o2,1}$. As seen from (16), the value of ω_{oL}—along with the circuit parameters determining K_{major}, K_{minor}, and ω_{major} in (14)—will determine the value of ω_p relative to that of ω_z of $1/\beta(s)$ in (15), which, in turn, will determine the behavior of $L(s)$ at its unity-gain crossover frequency and, hence, the OCL-LDO's stability.

A. CASE 1: $\omega_{oL} < \omega_{o1}, \omega_{o2,1}$

This case corresponds to when I_L is very small while C_L very large. The small I_L results in a very large R_{oL} which, together with a large C_L, makes ω_{oL} in (10) small compared to ω_{o1} and $\omega_{o2,1}$. As ω_{oL}, ω_{o1}, and $\omega_{o2,1}$ are concentrated at low frequencies, the resulting $A(s)$ behaves as a third-order transfer function at its unity-gain frequency (ω_{cA}), making the frequency compensation of the OCL-LDO quite challenging. Fig. 5 shows the asymptotic Bode magnitude plots of $A(s)$ and $1/\beta(s)$ to help visualize $L(s)$ in which we have assumed that the magnitude of $1/\beta(s)$ is much lower than that of $A(s)$ for frequencies lower than where the two curves intersect (ω_{ist}). Therefore, for $\omega < \omega_{ist}$, we can assume that $L(s) \approx 1/\beta(s)$. We have also assumed, from (16), that the small ω_{oL} results in ω_p being lower than ω_z, and that ω_{oL} is so low that it makes ω_p smaller than ω_c, the unity-gain frequency of $L(s)$.

Ideally, to provide the OCL-LDO with a good phase margin, we should make ω_p as large as possible, preferably larger than ω_c, such that $L(s)$ behaves as a first-order transfer function at its unity-gain frequency. Fortunately, despite the low ω_{oL} imposed by the load condition, the value of ω_p can be indeed much larger than ω_{oL}, the reason of which can be explained using (16). Since ω_{major} from (14) is itself already much larger than ω_{oL}—as $g_{f2} \gg 1/R_{oL}$ and $C_m \ll C_L$—what determines the value of ω_p is usually the ω_{oL} term of

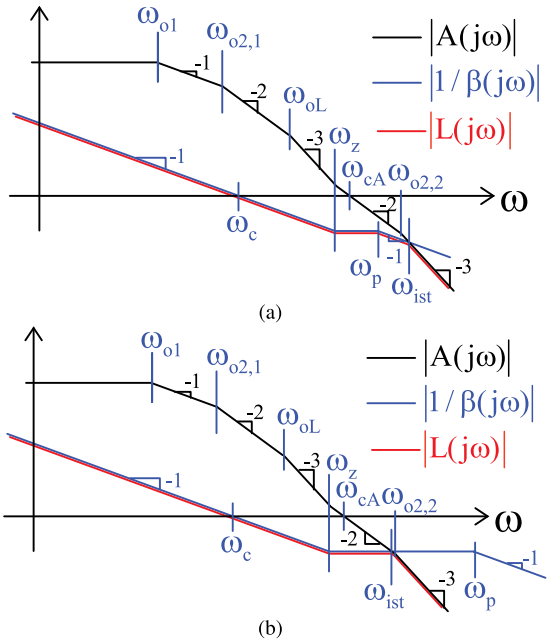

FIGURE 6. Theoretical bode magnitude plots of $A(s)$ and $1/\beta(s)$ for approximating $L(s)$ for Case 2 ($\omega_{o1}, \omega_{o2,1} < \omega_{oL} < \omega_{cA}$): (a) $\omega_p < \omega_{ist}$. (b) $\omega_p > \omega_{ist}$.

the parallel combination in (16). As low I_L makes $g_{mp}R_{oL}$ large, we can see from (14) that K_{minor} should be much larger than K_{major}. Therefore, ω_{oL} in (16) is multiplied by $1+K_{minor}/K_{major}$, a factor much larger than 1, before coming in parallel with the ω_{major} term, resulting in ω_p that is much larger than ω_{oL}.

However, with a severe load condition—in which I_L becomes very low and C_L very large—the very low ω_{oL} may result in ω_p that is lower than ω_c as depicted in Fig. 5, resulting in $L(s)$ with a second-order unity-gain crossover behavior and a poor phase margin. In such case, the left-half-plane zero at ω_z of $1/\beta(s)$ can help alleviate the degradation of the phase margin somewhat as it contributes positive phase to $L(s)$ at ω_c. With the help of such zero, the proposed OCL-LDO may still be functional even while providing a very low load current and driving a large load capacitance as will be demonstrated in Section VI-A.

B. CASE 2: $\omega_{o1}, \omega_{o2,1} < \omega_{oL} < \omega_{cA}$

Now we consider the case of intermediate I_L and C_L, which makes the value of ω_{oL} only a little higher than ω_{o1} and $\omega_{o2,1}$. As I_L is not very high, ω_{oL} is still smaller than ω_{cA}, the unity-gain frequency of $A(s)$, making $A(s)$ still a third-order transfer function at its unity-gain crossover. Nevertheless, since the value of ω_{oL} in this case is much larger than that in case 1, the ω_{oL} term in (16) is no longer a limiting factor of ω_p. As a result, ω_p is pushed to a frequency higher than the unity-gain frequency (ω_c) and the zero frequency (ω_z) of $1/\beta(s)$. As will be discussed next, how high ω_p is relative to ω_z also affects the overall stability of the OCL-LDO, which, fortunately, can be controlled by a careful choice of

the capacitance value C_m. To understand this aspect, let's consider the plots of $|A(j\omega)|$, $|1/\beta(j\omega)|$, and the resulting $|L(j\omega)|$ for two cases of ω_p (relative to ω_{ist}, the frequency of intersection between $|A(j\omega)|$ and $|1/\beta(j\omega)|$): 1) Fig. 6(a) for $\omega_p < \omega_{ist}$ and 2) Fig. 6(b) for $\omega_p > \omega_{ist}$.

For both cases, the relatively high value of ω_p guarantees that $L(s)$ behaves as a first-order transfer function at its unity-gain frequency, thus ensuring a good phase margin. However, for this load condition, what determines the OCL-LDO's stability is no longer the phase margin, but the gain margin as determined by the magnitude peaking due to the high-Q complex poles of $L(s)$ near ω_{ist}. We can intuit on this statement graphically by noticing the slopes of $|A(j\omega)|$ and $|1/\beta(j\omega)|$ at ω_{ist}. In Fig. 6(a) in which $\omega_p < \omega_{ist}$, depending on the slope of $|A(j\omega)|$ at the intersection, the slope of $|L(j\omega)|$ may either change from -20 dB/decade to -40 dB/decade if $\omega_{o2,2} > \omega_{ist}$, or from -20 dB/decade to -60 dB/decade if $\omega_{o2,2} < \omega_{ist}$ (this case is illustrated in Fig. 6(a)). In the first case, we can intuit that, as the change in the $|L(j\omega)|$'s slope at ω_{ist} is only -20 dB/decade, there should be only one real pole there and, hence, no magnitude peaking in $|L(j\omega)|$ near ω_{ist}. In the second case, however, the change in the $|L(j\omega)|$'s slope at ω_{ist} is -40 dB/dec, indicating that there are complex poles and, hence, there can be magnitude peaking in $|L(j\omega)|$ near ω_{ist}. However, if ω_p is made much smaller than ω_{ist}, the value of $|L(j\omega)|$ at ω_{ist}, despite the possible presence of magnitude peaking, can be made much less than 1, and a good gain margin for $L(s)$ can be guaranteed. On the contrary, if $\omega_p > \omega_{ist}$ as in Fig. 6(b), the change in the $|L(j\omega)|$'s slope is either -40 dB/decade or -60 dB/decade depending on the relative position of $\omega_{o2,2}$ to ω_{ist}, hence, indicating the presence of high-Q complex poles around ω_{ist}. What makes this case worse than when $\omega_p < \omega_{ist}$ is that the value of $|L(j\omega)|$ near ω_{ist} can be quite close to unity (as it has not yet been attenuated by the pole at ω_p). As a result, any magnitude peaking near ω_{ist} can severely degrade the gain margin of $L(s)$ or even cause the OCL-LDO to go unstable.

To reduce the Q of the complex poles near ω_{ist}—hence, improving the gain margin—we can incorporate the direct compensation path as provided by the capacitor C_m shown in Fig. 3. To understand the effect of C_m in reducing the Q, we shall resort to the root-locus technique to help visualize how the poles of $L(s)$ arise from the open-loop transfer function of the compensation feedback loop—i.e., $L_{fc}(s) = A(s)\beta(s)$. From the expression of $A(s)$ in (9) (with $g_{f1}/C_{c1} \equiv \omega_z$) and $\beta(s)$ as the inverse of (15), we can write

$$L_{fc}(s) \approx \frac{A_{oL}}{K_{major} \parallel K_{minor}} \cdot \frac{s(1+s/\omega_p)}{(1+\frac{s}{\omega_{o1}})(1+\frac{s}{\omega_{o2,1}})(1+\frac{s}{\omega_{oL}})(1+\frac{s}{\omega_{o2,2}})} \quad (17)$$

We can see from (17) that $L_{fc}(s)$ has four left-half-plane poles and two zeros, one at the origin and the other at $s = -\omega_p$. For this intermediate I_L and C_L case, we shall assume that $\omega_{o1} < \omega_{o2,1} < \omega_{oL}$ while $\omega_{o2,2}$ and ω_p are above these pole frequencies. Since the closed-loop poles of the feedback

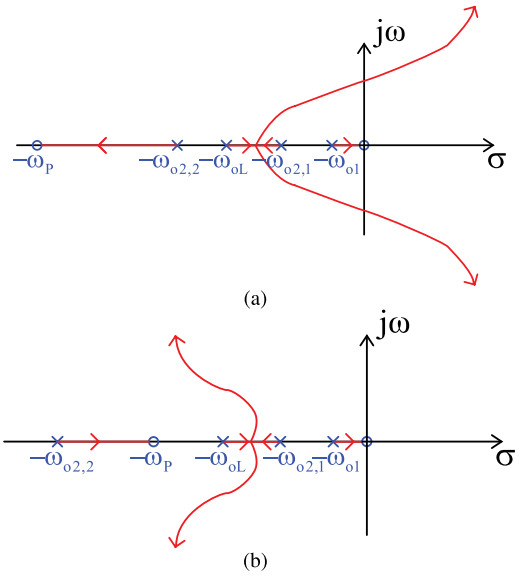

FIGURE 7. Root-locus plots showing the effects of the direct-compensation capacitor C_m on the Q of the complex poles for: (a) $\omega_p > \omega_{o2,2}$ (b) $\omega_p < \omega_{o2,2}$.

compensation loop (whose loop transfer function is $L_{fc}(s)$) are the poles of the OCL-LDO's loop transfer function $L(s)$, we can use the root-locus technique to illustrate how the position of the zero at $s = -\omega_p$, which is affected by C_m, relative to that of the pole at $s = -\omega_{o2,2}$ affects the Q of the complex poles of $L(s)$.

First, let's consider the scenario in which C_m is very small, which makes the value of ω_{major} in (14) very large, thus allowing us to approximate ω_p in (16) as $\omega_p \approx \omega_{oL}(1 + K_{minor}/K_{major})$. For this intermediate I_L case, the value of $g_{mp}R_{oL}$ is still much larger than 1, thus resulting in $K_{minor} \gg K_{major}$ as suggested in (14). In addition, a relatively large I_L, which results in a relatively small R_{oL}, makes ω_{oL} quite substantial compared to $\omega_{o2,2}$. These combined effects, as seen from (16), result in ω_p being significantly larger than $\omega_{o2,2}$—i.e., the Bode plot of Fig. 6(b). Fig. 7(a) shows the root-locus plot of $L_{fc}(s)$ in this case as its DC loop gain $(A_{oL}/\left(K_{major} \parallel K_{minor}\right))$ increases. We can see in this plot that the zero at the origin attracts the closed-loop pole originating from $s = -\omega_{o1}$ toward it while the closed-loop poles originating from $s = -\omega_{o2,1}$ and $s = -\omega_{oL}$ move toward each other and break off the real axis to become complex. Also, the zero at $s = -\omega_p$, which situates at a much higher frequency than the pole at $s = -\omega_{o2,2}$, attracted the closed-loop pole originating from $s = -\omega_{o2,2}$ toward it. Hence, from the average-distance rule of the root-locus technique, such leftward movement of the pole has an effect of pushing the two complex poles toward the right half of the complex plane. In severe circumstances in which the loop gain of $L_{fc}(s)$ is sufficiently high, it is possible that the complex poles be pushed into the right half of the complex plane, making the overall OCL-LDO unstable.

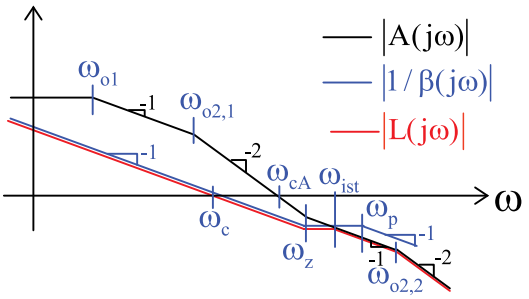

FIGURE 8. Theoretical bode magnitude plots of $A(s)$ and $1/\beta(s)$ for approximating $L(s)$ for Case 3 ($\omega_{oL} \gg \omega_{o1}, \omega_{o2,1}, \omega_{cA}$).

After seeing how the movement of the closed-loop pole originating from $s = -\omega_{o2,2}$ affects the complex poles' Q, we can envision that by forcing such movement to be left-to-right instead of right-to-left as in the $\omega_p > \omega_{o2,2}$ case, we can thwart the rightward movement of the complex poles, thus reducing their Q. Fig. 7(b) shows the root-locus plot of $L_{fc}(s)$ for such concept—here, $\omega_p < \omega_{o2,2}$, which corresponds to the Bode plot of Fig. 6(a). Instead of moving to the left as in the case of $\omega_p > \omega_{o2,2}$, the closed-loop pole originating from $s = -\omega_{o2,2}$ must move rightward toward the zero at $s = -\omega_p$. From the average-distance rule of the root-locus technique, such rightward movement of the closed-loop pole helps pull the complex poles away from the $j\omega$ axis, thus reducing their Q.

In summary, we can help limit the Q of the complex poles of the OCL-LDO's loop transfer function, $L(s)$, by ensuring that $\omega_p < \omega_{o2,2}$. This can be achieved by a selection of a sufficiently large C_m such that, even in the case when ω_{oL} term in (16) becomes very large due to a large I_L, the ω_{major} term in (16) still helps limit ω_p to a value smaller than $\omega_{o2,2}$.

C. CASE 3: $\omega_{oL} \gg \omega_{o1}, \omega_{o2,1}, \omega_{cA}$

This case corresponds to when I_L becomes very large, making R_{oL} very small, which results in ω_{oL} becoming so large that it can be ignored from our analysis. Fig. 8 shows the Bode magnitude plots for estimating $L(s)$ of this load condition. Due to the large ω_{oL}, ω_p, as seen from (16), is pushed to a frequency higher than ω_c, making $L(s)$ behave as a 1st-order transfer function at its unity-gain crossover frequency, hence achieving a good phase margin. To ensure the stability of the feedback compensation loop for the load condition in Case 2, we will assume that the value of C_m is chosen such that $\omega_p < \omega_{o2,2}$.

Whether the load condition for this very high I_L case risks the presence of high-Q complex poles can be seen from the behavior of $L(s)$ at ω_{ist} where the curves $|A(j\omega)|$ and $|1/\beta(j\omega)|$ intersect. If the difference in the slopes of both curves at ω_{ist} is only 20 dB/decade, it can be approximated that $L(s)$ exhibits one real pole near ω_{ist}, without the presence of high-Q complex poles. Assuming that $\omega_{ist} > \omega_c$, we can reason from the plot in Fig. 8 that, due to both $A(s)$ and $1/\beta(s)$ containing a zero at ω_z, the difference in the slopes of $|A(j\omega)|$ and $|1/\beta(j\omega)|$ at $\omega = \omega_{ist}$ is always 20 dB/decade, regardless of where ω_{ist} is relative to ω_z. For instance, if $|A(j\omega)|$ intersects with $|1/\beta(j\omega)|$ before ω_z ($\omega_{ist} < \omega_z$), the slopes of $|A(j\omega)|$ and $|1/\beta(j\omega)|$ at ω_{ist} are -40 dB/decade and -20 dB/decade, respectively, making the slope of $|L(j\omega)|$ change by only 20 dB/decade at ω_{ist}. On the other hand, if $|A(j\omega)|$ intersects with $|1/\beta(j\omega)|$ after ω_z but before ω_p ($\omega_z < \omega_{ist} < \omega_p$), the slopes of $|A(j\omega)|$ and $|1/\beta(j\omega)|$ at ω_{ist} are -20 dB/decade and 0 dB/decade, respectively. Again, the change in the slope of $|L(j\omega)|$ in this case is also only 20 dB/decade. It can also be reasoned that, for $\omega_{ist} > \omega_p$, the change in the slope of $|L(j\omega)|$ around $\omega = \omega_{ist}$ is also 20 dB/decade. Therefore, for this very high I_L case, there are no high-Q complex poles and, thus, no magnitude peaking in $|L(j\omega)|$ near $\omega = \omega_{ist}$. The compensation feedback is thus firmly stable and the overall OCL-LDO should exhibit a good gain margin.

V. CIRCUIT IMPLEMENTATION

Fig. 9 shows the transistor-level implementation of the proposed OCL-LDO. Illustrated as g_{m1}, R_{o1}, and C_{o1} in Fig. 3, the first gain stage is implemented as a folded-cascode operational amplifier (OTA) consisting of the transistors M_0-M_8, with M_1 and M_2 acting as the input differential pair. The second gain stage—illustrated as g_{m2}, R_{o2}, and C_{o2} in Fig. 3—is implemented as a moderate-gain common-source stage (M_{11} and M_{12}) with the transistors M_9 and M_{10} providing voltage inversion from the output of the first gain stage to the gate of M_{11}. Finally, the power stage—g_{mp} and R_{oL} in Fig. 3—consists of the power transistor M_p to provide the required current to the load. The capacitor C_{c1} acts as a minor-loop compensation capacitance that senses the voltage at the drains of M_{11} and M_{12} (node V_{o2} in Fig. 3) and returns current to the source of the transistor M_5. Hence, M_5 acts as a current buffer (the $b_1 g_{f1}$ buffer in Fig. 3) to prevent the feedthrough current through C_{c1} from the node V_{o1} to the node V_{o2}—which otherwise might cause a low-frequency RHP zero. Similarly, the capacitor C_{c2} acts as a major-loop compensation capacitance, sensing the voltage at V_{out} and returning the feedback current to the node V_{o1} via the source of the transistor M_6—hence, M_6 acts as a current buffer $b_2 g_{f2}$ in Fig. 3. The capacitor C_m connects directly between the node V_{out} and V_{o1} to help limit the Q of the $L(s)$'s complex poles when the load current becomes large.

To speed up the OCL-LDO's settling time when the load current undergoes abrupt changes, we have incorporated an overshoot/undershoot reduction circuit, which consists of the transistors M_{b1}-M_{b4}, M_{c1}-M_{c5}, and the passive highpass networks formed by R_{B1}, C_{B1} and R_{B2}, C_{B2}. When the load current abruptly changes, the feedback operation of the OCL-LDO results in an abrupt change in the gate voltage of the power transistor M_p. The two highpass networks then sense this abrupt change and dynamically increase the bias current of the first gain stage—i.e., to increase its transconductance, g_{m1}—to speed up the OCL-LDO. The dynamic increase in the first gain stage's bias current is achieved through two sets of the bias transistors: i) M_{b1}-M_{b3} and

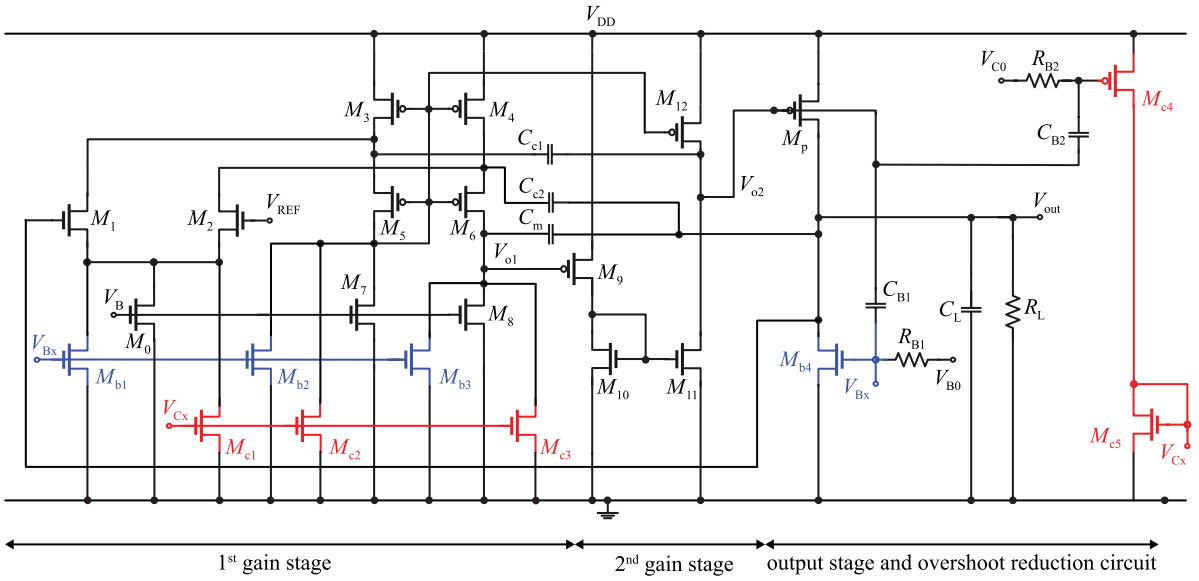

FIGURE 9. Transistor-level implementation of the proposed OCL-LDO.

ii) M_{c1}-M_{c3}, all of which biased to consume negligible drain currents during the OCL-LDO's normal operation. The first set, M_{b1}-M_{b3}, helps increase the bias current when the load current abruptly decreases while the second set, M_{c1}-M_{c3}, helps when it abruptly increases. First, let's consider the scenario when the load current abruptly decreases, which results in a sudden increase of the M_p's gate voltage to reduce its drain current to balance with the reduced load current. The sudden increase in the M_p's gate voltage couples through the highpass network formed by C_{B1} and R_{B1}, raising the gate voltage of M_{b4} (the node V_{Bx}), which, in turn, increases the drain currents of the transistors M_{b1}-M_{b3} to increase the bias current of the first gain stage. In the opposite scenario in which the load current suddenly increases, the OCL-LDO's feedback operation cause the M_p's gate voltage to drop; such sudden voltage drop couples to the gate of M_{c4} through the highpass network C_{B2} and R_{B2}, thus increasing the drain currents of M_{c4} and M_{c5}, which is mirrored to M_{c1}-M_{c3} to increase the bias current of the first gain stage.

Table 1 summarizes the sizes and quiescent currents of all the transistors along with the sizes of the passive components used in the OCL-LDO of Fig. 9.

VI. SIMULATION RESULTS

In this section, we verify the feasibility of our theoretical analyses in Section IV with the stability analyses in SPICE for all the three load conditions. First, we extracted the relevant DC-operating-point parameters of our OCL-LDO in Fig. 9, and used them to calculate $A(s)$ and $1/\beta(s)$ as given in (9) and (15) for different sets of I_L and C_L, with I_L ranging from 0 mA to 100 mA and C_L from 0 to 1 nF. Once obtained, $A(s)$ and $1/\beta(s)$ were used to calculate $L(s)$ in (7), which was then compared to that obtained from the stability analysis in SPICE.

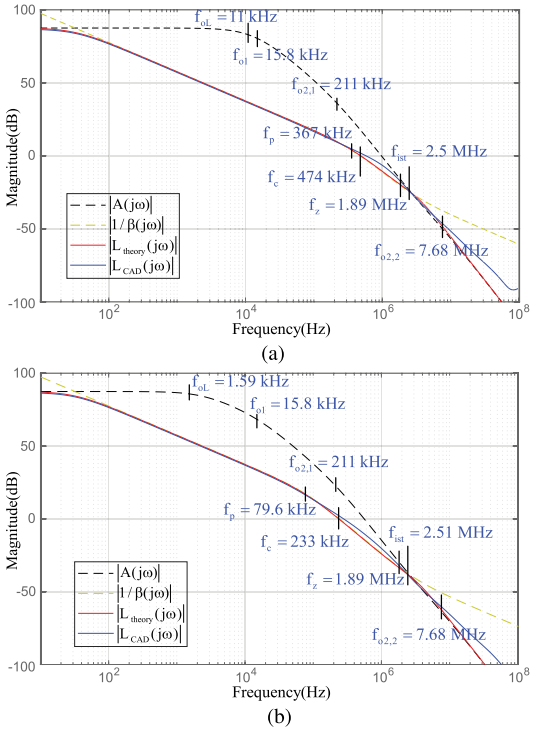

FIGURE 10. Bode magnitude plots for estimating the loop transfer function ($L(s)$) of the proposed OCL-LDO for Case 1 ($\omega_{oL} < \omega_{o1}, \omega_{o2,1}$): (a) $I_L = 0$, $C_L = 200$ pF (b) $I_L = 0$, $C_L = 1$ nF.

A. CASE 1: $\omega_{oL} < \omega_{o1}, \omega_{o2,1}$

First, we shall focus on the loading scenarios with extremely low I_L and very high C_L—i.e., the most difficult condition to compensate. We shall consider two scenarios, both with $I_L = 0$, but one with $C_L = 200$ pF and the other with $C_L = 1$ nF. Fig. 10(a) and Fig. 10(b) show the Bode magnitude plots

TABLE 1. Device sizing and bias currents.

Devices	W (μm)	L (μm)	Bias current (nA)			Devices	W (μm)	L (μm)	Bias current (nA)		
			I_L =0 mA	I_L =1 mA	I_L =100 mA				I_L =0 mA	I_L =1 mA	I_L =100 mA
M_0	8	8	814.9	814.9	814.9	M_{11}	6.96	0.18	3973	4056	4208
M_1	43.2	0.72	465.5	455.6	452.9	M_{12}	21.6	0.18	3973	4056	4208
M_2	43.2	0.72	420.9	421.8	424.6	M_{b1}	1.44	1.08	35.77	35.77	35.77
M_3	3.6	0.36	909.5	908.6	905.9	M_{b2}	0.72	1.08	17.98	17.98	17.98
M_4	3.6	0.36	883.3	883.8	885.1	M_{b3}	0.72	1.08	18.99	18.94	18.79
M_5	3.6	0.36	453	453	453	M_{b4}	180	0.18	8212	8211	8208
M_6	3.6	0.36	462.4	461.9	460.5	M_{c1}	7.2	0.36	26.79	26.79	26.79
M_7	4	8	407.9	407.9	407.9	M_{c2}	7.2	0.36	27.08	27.08	27.08
M_8	4	8	413.1	412.9	412.1	M_{c3}	7.2	0.36	30.27	30.11	29.63
M_9	10.8	0.18	389.7	481	905.7	M_{c4}	1.8	0.72	105.9	105.9	105.9
M_{10}	1.16	0.18	389.7	481.2	905.7	M_{c5}	36	0.36	105.9	105.9	105.9
M_P	2880	0.18	8217	I_L + 8217	I_L + 8217	C_{c1} = 1.2 pF, C_{c2} = 1.5 pF, C_m = 750 fF, $R_{B1,2}$ = 500 kΩ, $C_{B1,2}$ = 1 pF					

of $L(s)$ obtained from our theoretical model ($|L_{theory}(j\omega)|$, red curve) and from SPICE stability analysis ($|L_{CAD}(j\omega)|$, blue curve) for C_L = 200 pF and 1 nF, respectively. In the two figures are also shown the Bode magnitude plots of $A(s)$ and $1/\beta(s)$ used in calculating $L_{theory}(s)$. All the corner frequencies are marked in Hertz—as $f_i = \omega_i/(2\pi)$—instead of in rad/sec as in Section IV. Both Fig. 10(a) and Fig. 10(b) clearly show that $|L_{theory}(j\omega)|$ closely matches $|L_{CAD}(j\omega)|$ up to a frequency close to $f_{o2,2}$, which is well beyond the unity-gain frequency f_c.

In Fig. 10(a) with C_L = 200 pF, we have f_{oL} = 11 kHz, which is below both f_{o1} (15.8 kHz) and $f_{o2,1}$ (211 kHz), making $A(s)$ a third-order transfer function at its unity-gain crossover frequency. Nevertheless, with the help of both compensation networks, $1/\beta(s)$ exhibits a first-order behavior over a wide frequency range. The $1/\beta(s)$'s pole at f_p occurs at 367 kHz, well above f_{oL} and just slightly below the unity-gain frequency f_c = 474 kHz. In theory, the left-half-plane zero at f_z = 1.89 MHz helps introduce a positive phase shift of 14° to the theoretical $L(s)$ at $f = f_c$, resulting in the theoretical phase margin of 39.43°. Nevertheless, SPICE simulation indicates that the pole at f_p of $L_{CAD}(s)$ occurs beyond its unity-gain frequency, making $L_{CAD}(s)$ a first-order transfer function at its unity-gain crossover. As a result, for I_L = 0 and C_L = 200 pF, SPICE stability analysis indicates the phase margin of 42.76°, slightly more than predicted by our theoretical model.

To consider the stability limit of the proposed compensation method, let's turn our attention to the case of I_L = 0 and C_L = 1 nF, whose Bode magnitude plots are shown in Fig. 10(b). Under such severe load condition, f_{oL} is pushed to 1.59 kHz, which is several times lower than its value when C_L = 200 pF, while f_{o1} and $f_{o2,1}$ remain the same. Nevertheless, $A(s)$ still behaves as a third-order transfer function at its unity-gain crossover frequency. Now, let's consider how such large C_L affects f_p, the pole frequency of $L_{theory}(s)$. From the plot, we can see that f_p, originally at 367 kHz when C_L = 200 pF, now drops to 79.6 kHz, which is 2.92 times lower than the unity-gain frequency f_c (233 kHz). As a result, $L_{theory}(s)$ is now strictly second-order at its unity-gain crossover frequency, indicating a poor phase margin. Even then, our theoretical model suggests that the zero at f_z = 1.89 MHz introduces a positive phase shift of around 7.02° to $L_{theory}(s)$ at f_c, which results in a theoretical phase margin of 18.56°. Nevertheless, comparing $|L_{CAD}(j\omega)|$ to $|L_{theory}(j\omega)|$, we observe that $L_{CAD}(s)$ behaves as a first-order transfer function over a slightly wider frequency range, suggesting that f_p of $L_{CAD}(s)$ is at a slightly higher frequency than that of $L_{theory}(s)$. As a result, SPICE stability analysis indicates a slightly better phase margin of 27.46° for this load condition.

Though it may seem that the phase margin of 27.46° is very low, as judged from generally acceptable criteria in circuit design, it should be noted that such large capacitive load under zero load current is very unlikely to occur in practice because a very large load capacitance is normally associated with heavy circuitry being powered by the OCL-LDO. Even if the circuitry being powered is idle, its leakage current alone should be sizeable such that I_L should be significantly higher than zero. Nevertheless, we will shown in Section VII that our OCL-LDO is still stable even with I_L = 0 mA and C_L = 1 nF.

B. CASE 2: $\omega_{o1}, \omega_{o2,1} < \omega_{oL} < \omega_{cA}$

As discussed in Section IV-B, our concern for this load condition is the possible presence of high-Q complex poles near f_{ist} where $|A(j\omega)|$ and $|1/\beta(j\omega)|$ intersect. Hence, a capacitor C_m is needed to limit the Q of the complex poles to guarantee a good gain margin for the OCL-LDO's loop transfer function $L(s)$.

For an illustration, let's consider the scenario in which I_L = 35 mA and C_L = 100 pF, whose Bode magnitude plots are shown in Fig. 11. Due to the high load current and the relatively small load capacitance, f_{oL} is now at 1.26 MHz, now higher than f_{o1} (16.6 kHz) and $f_{o2,1}$ (222 kHz) but still lower than the unity-gain frequency of $A(s)$, making it still a third-order transfer function at its unity-gain crossover as in Case 1. Even then, the now higher f_{oL} pushes f_p (the pole frequency of $1/\beta(s)$, which is now at 4.33 MHz) to a frequency

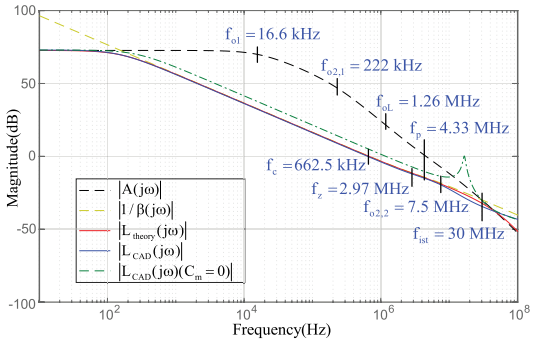

FIGURE 11. Bode magnitude plots for estimating the loop transfer function ($L(s)$) of the proposed OCL-LDO for Case 2 ($\omega_{o1}, \omega_{o2,1} < \omega_{oL} < \omega_{cA}$). In this figure, $I_L = 35$ mA and $C_L = 100$ pF.

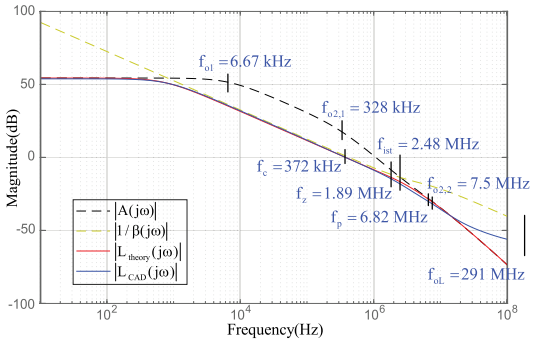

FIGURE 12. Bode magnitude plots for estimating the loop transfer function ($L(s)$) of the proposed OCL-LDO for Case 3 ($\omega_{oL} \gg \omega_{o1}, \omega_{o2,1}, \omega_{cA}$). In this figure, $I_L = 100$ mA and $C_L = 200$ pF.

higher than both f_c (662.5 kHz) and f_z (2.97 MHz). Hence, the OCL-LDO's loop transfer function—as seen in both $L_{\text{theory}}(s)$ and $L_{\text{CAD}}(s)$—crosses over the unity-gain level in a first-order fashion, thus guaranteeing a good phase margin. Notice that even when $f_{oL} = 1.26$ MHz is much higher than its value in Case 1, the value of $f_p = 4.33$ MHz is only slightly higher than $f_z = 2.97$ MHz, thanks to the role of C_m in limiting the value of ω_p as discussed in Section IV-B. Also, recall from the root-locus plot of Fig. 7(b) that making $\omega_p < \omega_{o2,2}$ has a desirable effect of directing the complex poles of $L(s)$ leftward in the complex plane, hence reducing their Q. In this design, we have chosen C_m to be 750 fF to ensure that f_p is always smaller than $f_{o2,2}$ for all the load conditions of interest.

Fig. 11 illustrates that the SPICE-simulated loop transfer function, $L_{\text{CAD}}(s)$, follows our theoretical model, $L_{\text{theory}}(s)$, very closely over a very wide frequency range (up to f_{ist}), and that both transfer functions exhibit no magnitude peaking near f_{ist}, thanks to the Q-limiting effect of C_m. The SPICE-simulated phase and gain margins for this particular load condition are 84° and 20 dB, respectively, indicating that the OCL-LDO is well stabilized. If C_m is removed, however, the SPICE-simulated loop transfer function, $L_{\text{CAD}}(s)$ ($C_m = 0$), exhibits a very high magnitude peaking near f_{ist}. Please also note that the magnitude of $L_{\text{CAD}}(s)$ for $C_m = 0$ is slightly higher than when $C_m = 750$ fF as the absence of C_m increases the value of K_{major} as indicated in (14). For this particular load condition, the peaking near f_{ist} is so high that $|L_{\text{CAD}}(j\omega)(C_m = 0)|$ at its peak almost exceeds unity, indicating that the gain margin is so low and that the feedback compensation loop is close to being unstable.

C. CASE 3: $\omega_{oL} \gg \omega_{o1}, \omega_{o2,1}, \omega_{cA}$

For Case 3, let's consider the load condition in which $I_L = 100$ mA and $C_L = 200$ pF, whose Bode magnitude plots are shown in Fig. 12. With such a high load current, the dropout voltage of 200 mV across M_p—i.e., the source-to-drain voltage of M_p in Fig. 9—is not high enough to keep it in the saturation region. As a result, R_{oL} becomes very small, which significantly degrades the overall magnitude of $L(s)$. Nevertheless, despite M_p operating in the linear region, the Bode magnitude plots in Fig. 12 indicate that the OCL-LDO still achieves a low-frequency loop gain of around 54.4 dB, a reasonable value to provide good load and line regulations. Also, the plots of Fig. 12 indicate that the very small R_{oL} results in f_{oL} being pushed to a very high frequency of 291 MHz, which is well beyond f_{ist} where $|A(j\omega)|$ and $|1/\beta(j\omega)|$ intersect, making $A(s)$ behave as a second-order transfer function at the intersection of the two curves. Nevertheless, despite f_{oL} being pushed so high in frequency, the value of f_p is only 6.82 MHz, an increase of less than two times of its value in the case of $I_L = 35$ mA and $C_L = 100$ pF—thanks to the effect of C_m limiting the value of ω_p. Since the pole of $1/\beta(s)$ at f_p and the zero at f_z are quite close to each other—only a factor of 3.6 apart in frequencies—their effects tend to cancel each other out such that $1/\beta(s)$ behaves approximately as a first-order transfer function in the frequency range $f_z < f < f_p$ where f_{ist} lies. As a result, at $f = f_{ist}$, $L(s)$, which approximately follows $1/\beta(s)$ for $f < f_{ist}$ and $A(s)$ for $f > f_{ist}$, has its slope changed from -20 dB/decade to -40 dB/decade, indicating the presence of one real pole near f_{ist}. Hence, with the absence of complex poles, $L(s)$ exhibits no magnitude peaking near f_{ist}, indicating that the feedback compensation loop is well stabilized. With $L(s)$ behaving as a first-order transfer function at its unity-gain crossover frequency and without the magnitude peaking near f_{ist}, SPICE stability analysis indicates a high phase margin of 87.05° for the OCL-LDO.

VII. EXPERIMENTAL RESULTS

The proposed OCL-LDO was designed and fabricated in a 0.18-μm CMOS process from the United Microelectronic Corp. (UMC). Fig. 13 shows the die micrograph of the OCL-LDO, which occupies an area of 310 μm × 350 μm. For any load current between 0 mA to 100 mA, the OCL-LDO is stable under the load capacitance up to 1 nF, while capable of regulating the output voltage in the range of 1 V to 2.2 V and consuming a total quiescent current of 14 μA. For a larger load current of higher than 1 mA, the OCL-LDO is stable even under the load capacitance of as high as 10 nF. The OCL-LDO employs a total of 5.45 pF for all the on-chip capacitors

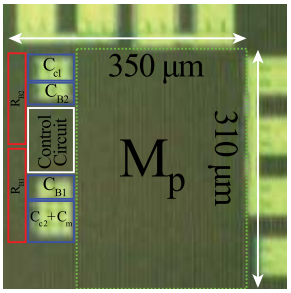

FIGURE 13. Die micrograph of the proposed OCL-LDO.

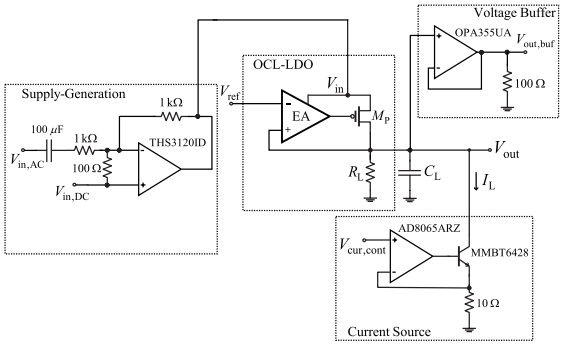

FIGURE 14. Schematic of the proposed OCL-LDO's testbench.

(C_{c1}, C_{c2}, C_m, C_{B1}, and C_{B2} in Fig. 9) and a total of 1 MΩ for all the on-chip resistors (R_{B1} and R_{B2}).

To validate the proposed OCL-LDO's performance, we have built on a printed circuit board (PCB) a test-bench, whose schematic is shown in Fig. 14(a); the proposed OCL-LDO is shown as the combination of the error amplifier (EA) and the power stage (M_p and the resistor R_L). To facilitate the measurements of the line regulation and power supply rejection (PSR), we have built on the PCB the supply-generation circuit—consisting of the low-noise high-output-drive opamp (THS3120ID, Texas Instruments Inc.) and a few passive components—to allow superimposing an AC signal ($V_{in,AC}$) on top of a large-signal component ($V_{in,DC}$) in generating the supply voltage V_{in}. Measuring the PSR of the OCL-LDO can then be performed by determining the small-signal transfer function from $V_{in,AC}$ to the OCL-LDO's output, V_{out}. In addition, by leaving $V_{in,AC}$ opened, we can perform DC sweep on or provide abrupt change to $V_{in,DC}$ to measure the OCL-LDO's line regulation or evaluate its transient behavior, respectively.

To evaluate the effects of the load conditions on the OCL-LDO, we have connected to its output node (V_{out}) an off-chip load capacitance C_L and a voltage-controlled current source built from a high-speed FET-input opamp (AD8065ARZ, Analog Devices Inc.) and a bipolar-junction transistor (MMBT6428, Fairchild Semiconductor). The current source provides the load current I_L to the OCL-LDO, whose value is controlled by the current source's input voltage, $V_{cur,cont}$, according to the relationship $I_L \approx V_{cur,cont}/10\ \Omega$. Also connected to the OCL-LDO's output is a

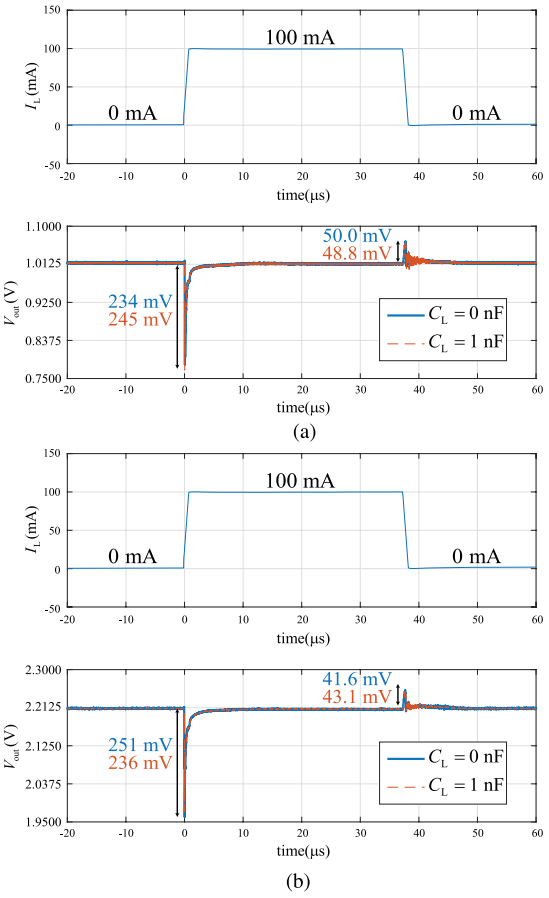

FIGURE 15. The OCL-LDO's transient responses under step changes in I_L between 0 mA and 100 mA: (a) V_{in} = 1.2 V. (b) V_{in} = 2.4 V.

voltage buffer, built from a high-speed operational amplifier (OPA355UA, Texas Instrument Inc.), to help mitigate the loading effect while observing the transient voltage at V_{out}.

A. TRANSIENT RESPONSES TO ABRUPT CHANGES IN THE LOAD CURRENT AND THE LINE VOLTAGE

For this part, we demonstrate the OCL-LDO's performance in handling abrupt changes in the load current. We tested the OCL-LDO under four input-voltage and capacitive-load corners—i) $V_{in} = 1.2$, $C_L = 0$ nF ii) $V_{in} = 1.2$ V, $C_L = 1$ nF iii) $V_{in} = 2.4$ V, $C_L = 0$ nF iv) $V_{in} = 2.4$ V, $C_L = 1$ nF—by stepping the load current I_L over the full range (between 0 mA and 100 mA) with the edge times of 1 μs for both the rising and falling transitions. For all the four corners, the reference voltage V_{ref} is set 200 mV below V_{in} to provide the power transistor M_p with a dropout voltage of 200 mV. Fig. 15(a) shows the OCL-LDO's responses for both values of C_L when V_{in} is set to 1.2 V. At the positive transition of I_L, the response exhibits voltage undershoots of 234 mV and 245 mV for $C_L = 0$ and $C_L = 1$ nF, respectively. Conversely, the negative transition of I_L produces, for $C_L = 0$ and $C_L = 1$ nF, the voltage overshoots of 50 mV and 48.8 mV, respectively. Fig. 15(b) shows the OCL-LDO's responses when V_{in} is set

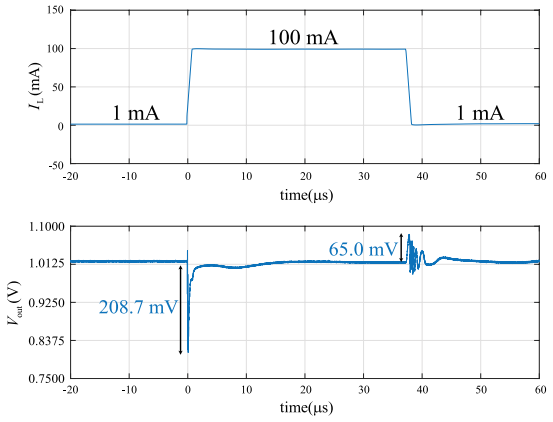

FIGURE 16. The OCL-LDO's transient response under $C_L = 10$ nF and I_L transitioning between 1 mA and 100 mA.

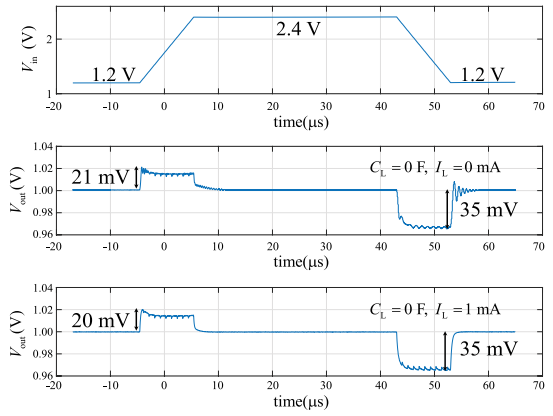

FIGURE 17. Transient responses to step changes in the line voltage.

to 2.4 V. The positive transition of I_L produces the voltage undershoots of 251 mV and 236 mV for $C_L = 0$ and $C_L = 1$ nF, respectively. The negative transition of I_L, on the other hand, produces the voltage overshoots of 41.6 mV and 43.1 mV for $C_L = 0$ and $C_L = 1$ nF, respectively.

The plots of Fig. 15(a) and Fig. 15(b) clearly demonstrate that the steady-state value of V_{out} rarely changes even when the change in I_L is drastic, thus indicating that the proposed OCL-LDO achieves a very good DC load regulation. These plots also demonstrate that the proposed OCL-LDO is stable with $C_L = 1$ nF even under the zero-load-current condition. However, we shall treat this case as the very worst-case condition because, as discussed in Sections I and VI-A, a large load capacitance should correspond to a sizable load current. To see how much load capacitance our OCL-LDO can handle under a sizable load current, we performed an experiment similar to that producing Fig. 15(a) but with $C_L = 10$ nF and I_L transitioning between 1 mA and 100 mA. The result is shown in Fig. 16. Though exhibiting some ringing on both transitions, the response clearly shows that, with the load current of at least 1 mA, the OCL-LDO is stable even under a load capacitance of as high as 10 nF.

Next, we demonstrate the OCL-LDO's performance under abrupt changes in the line voltage V_{in}. For these experiments, we set V_{ref} to 1 V while altering V_{in} between 1.2 V and 2.4 V

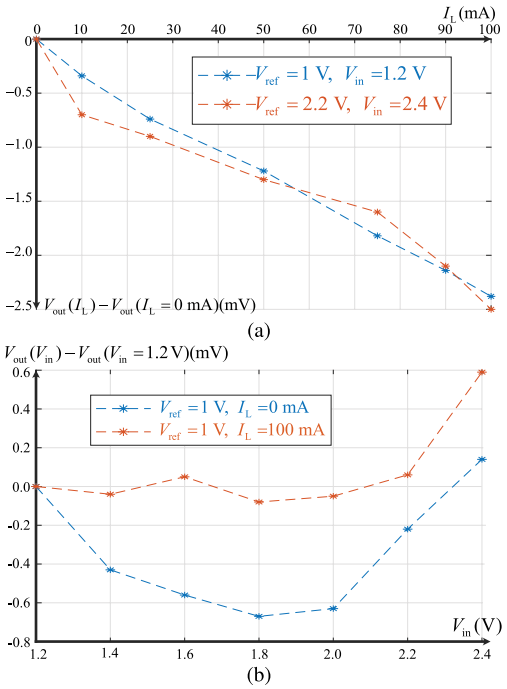

FIGURE 18. (a) Deviation of V_{out} from its value when $I_L = 0$ as I_L changes from 0 to 100 mA (load-regulation plot). (b) Deviation of V_{out} from its value when $V_{in} = 1.2$ V as V_{in} changes from 1.2 V to 2.4 V (line-regulation plot).

with the edge times of 10 μs for both the positive and negative transitions. The value of C_L is set to 0 F as this capacitive-load condition provides the worst line-transient performance as there is no C_L to help attenuate the coupling from V_{in}. The middle and bottom panes of Fig. 17 show the OCL-LDO's response when I_L is set to 0 mA and 1 mA, respectively. We can see from these responses that the OCL-LDO exhibits similar voltage overshoots and undershoots under both values of I_L. However, under $I_L = 0$ mA, the OCL-LDO's response exhibits higher amount of ringing when V_{in} makes the negative transition, probably due to the OCL-LDO's smaller phase margin at very low load current.

In summary, the transient responses of Fig. 15(a), Fig. 15(b), and Fig. 17 confirm that the OCL-LDO is well stabilized across the entire ranges of input voltage (1.2-2.4 V), load current (0-100 mA), and load capacitance (0-1 nF)—and Fig. 16 shows that it is also stable even under $C_L = 10$ nF if I_L remains higher than 1 mA—without the need for adapting the topology of the gain stages to sacrifice the loop gain. As a result, the OCL-LDO's loop gain can be preserved across all the load/input-voltage conditions, which would contribute to excellent load/line regulation performances as will be demonstrated next.

B. LOAD/LINE REGULATIONS AND POWER SUPPLY REJECTION

In this part, we demonstrate the load/line regulation and power-supply-rejection performances of the proposed OCL-LDO. Fig. 18(a) shows, at the two extremes of the input

TABLE 2. Performance summary and comparison to previous works.

Parameters	[12] JSSCC'14	[13] TCAS-I'18	[14] TPEL'18	[15] TCAS-II'19	[16] TCAS-I'20	[32] TCAS-I'12	[37] TCAS-I'13	[41] TPEL'20	This Work
Technology(μm)	0.065	0.065	0.13	0.18	0.065	0.35	0.065	0.065	0.18
Chip area (mm^2)	0.0133	0.0021	0.008	0.031	0.01	0.4	0.017	0.01	0.109
V_{in} (V)	0.75-1.2	1-1.4	1-1.4	1.2-1.8	1.05-1.2	1.2-1.5	1.2	0.95-1.2	1.2-2.4
V_{out} (V)	0.55	0.8	0.8	0.8-1.6	0.9	1	1	0.8	1-2.2
Dropout voltage (mV)	200	200	200	200	150	200	200	150	200
I_Q (μA)	15.9-487	1.6-24.2	112	10.2	65	45	0.9-82.4	14	14
Total on-chip cap. (pF)	4.1	0.6	0.73	0	1.4	41	4.5	6	5.45
C_L range(F)	470p-10n	0-25p	0-25p	0-100p	0-100p	0-1n	0-100p	0-100p	**0-1n**†
Line Reg. (mV/V)	4	0.7	2.25	10	-	-	4.7	12	**0.5**
Load Reg. (mV/mA)	0.18	0.28	0.173	0.081	-	-	0.3	0.09	**0.025**
PSR @1kHz (dB)	-51	-50	-60	-	-52	-	-80	-33	-50
Settling Time (μs)	0.25	3.6	0.19	0.22	0.1	4	6	3.2	7.3
$I_{L,max}$ (mA)	50	25	25	100	20	50	100	100	100
$I_{L,min}$ (mA)	0	0	0.12	1	0.1	1	0	0	0
ΔI_{out} (mA)	50	25	24.88	99	20	49	100	100	100
ΔV_{out} (mV)	113	37	284	200	200	70	68.8	230	252
Edge Time(μs)	0.1	0.1	0.3	0.1	0.005	1	0.3	0.22	1

† For $I_{L,min} = 0$ mA. C_L's range is 0-10 nF for $I_{L,min} = 1$ mA.

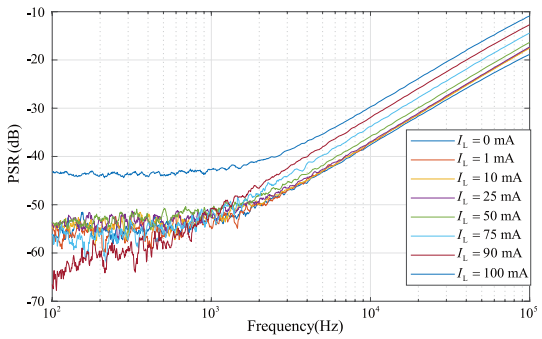

FIGURE 19. Power supply rejection (PSR) as a function of frequency.

voltage V_{in}, the deviation of the OCL-LDO's output voltage from the no-load value ($V_{out}(I_L) - V_{out}(I_L = 0)$) as the load current varies from 0 mA to 100 mA—for both curves, V_{ref} is set 200 mV below V_{in} to provide a dropout voltage of 200 mV across the power transistor. The load regulations for both values of V_{in} appear to be quite similar, but the worst-case value over the entire load-current range happens to be 0.025 mV/mA as calculated from the curve with $V_{in} =$ 2.4 V. For the line regulation, Fig. 18(b) shows the deviation of the OCL-LDO's output voltage as we varied V_{in} from 1.2 V to 2.4 V ($V_{out}(V_{in}) - V_{out}(V_{in} = 1.2$ V)). For this curve, we set I_L to 100 mA to achieve the worst-case line regulation performance as large I_L drives the power transistor into the linear region such that V_{in} has maximal effect on V_{out}. As V_{in} varies, the reference voltage V_{ref} remains at 1 V. Calculating the line regulation from this curve over the entire range of V_{in} yields the value of 0.5 mV/V. Fig. 19 shows the power supply rejection (PSR) of the proposed OCL-LDO at various load currents I_L. For most values of I_L, the PSR at 1 kHz ranges from -50 dB to -55 dB. At $I_L = 100$ mA, however, the PSR at 1 kHz drops to -43 dB due to the power transistor being forced to operate in the linear region.

C. COMPARISON TO PREVIOUS WORKS

Table 2 summarizes the performance of the proposed OCL-LDO compared to those of the previous works. Though implemented in a much larger technology node while utilizing approximately the same quiescent current, the proposed OCL-LDO exhibits the settling time on the same order as those in [13], [37], [41]. Those achieving much better settling times are mostly regulators implemented in smaller technology nodes which also utilizes significantly higher quiescent currents ([12], [14], [16]), except for the work in [15] which is also implemented in a 0.18-μm CMOS process while utilizing a smaller quiescent current. However, compared to the OCL-LDO in [15], which requires a minimum load current of 1 mA to be stable and is capable of driving capacitive load only in the range of 0-100 pF, the proposed OCL-LDO is stable under a much wider capacitive load range (0-1 nF) even with the load current being zero; the OCL-LDO is also stable while driving capacitive load of up to 10 nF for a guaranteed minimum load current of at least 1 mA. In addition, thanks to the proposed compensation methodology, which maintains the high loop gain over a very wide load-current range, the proposed OCL-LDO achieves the best DC load and line regulations compared to the previous works.

VIII. CONCLUSION

In this paper, we have presented the design of an OCL-LDO capable of driving a very wide range of load capacitance and supplying a wide range of load current while maintaining excellent DC load and line regulations. Good DC

regulation performances are achieved through the combined indirect-direct nested Miller compensation method which allows the preservation of the loop gain throughout the entire load-capacitance and load-current ranges. To provide insights into the working of the proposed compensation scheme, we employ a graphical feedback technique to help visualize how stability is achieved at various load conditions. Due to its low quiescent current, good DC regulation performance, and wide load-current and load-capacitance ranges, the OCL-LDO is suitable for SoCs whose loads undergo drastic changes throughout their entire operations such as those employing wakeup and power-gating schemes.

APPENDIX

In this part, we briefly outline the derivation of two pole frequencies of $A(s)$ in (9)—i.e., $\omega_{o2,1}$ and $\omega_{o2,2}$ in (10). These pole frequencies arise from the $Z_{A1} \parallel Z_{o2}$ term of $A(s)$ in (8), which, upon being substituted by Z_{A1} in (1) and Z_{o2} in (2), yields

$$Z_{A1} \parallel Z_{o2} = R_{o2} \frac{1 + sC_{c1}/g_{f1}}{1 + as + bs^2}, \tag{18}$$

where

$$\begin{aligned} a &= \left(C_{c1} + C_{c1} g_{f1} R_{o2} + g_{f1} R_{o2} C_{o2}\right)/g_{f1} \\ b &= R_{o2} C_{o2} C_{c1}/g_{f1}. \end{aligned} \tag{19}$$

We can then estimate the two pole frequencies from the denominator of (18) by assuming that the two poles are real and far apart in frequency such that we can factor the denominator as

$$\begin{aligned} 1 + as + bs^2 &= \left(1 + \frac{s}{\omega_{o2,1}}\right)\left(1 + \frac{s}{\omega_{o2,2}}\right) \\ &= 1 + \left(\frac{1}{\omega_{o2,1}} + \frac{1}{\omega_{o2,2}}\right)s + \frac{s^2}{\omega_{o2,1}\omega_{o2,2}} \\ &\approx 1 + \frac{s}{\omega_{o2,1}} + \frac{s^2}{\omega_{o2,1}\omega_{o2,2}}, \end{aligned} \tag{20}$$

in which the last step arises from the assumption that $\omega_{o2,2} \gg \omega_{o2,1}$. Comparing the coefficients of the result in (20) to those in (19), we then obtain $\omega_{o2,1}$ and $\omega_{o2,2}$ as shown in (10).

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