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Design and Analysis of Extendable Switched-Inductor and Capacitor-Divider Network Based High-Boost DC-DC Converter for Solar PV Application

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ABSTRACT In presented article, an extendable non-isolated high boost converter based on switched-inductor and capacitor-divided (SLCD) network is designed. The high gain, single switch, continuous input current and common ground structure makes it suitable for solar PV applications. The voltage stress across the semiconductor devices is less than the output voltage thus enhancing the efficiency of the converter. The operation in continuous and discontinuous mode of the converter with precise design parameters is presented. A meticulous analysis of voltage gain and efficiency is presented considering the inbuilt resistances of the components and the small-signal model developed evince the stability of the SLCD converter. The proffered converter is weighed against other recent congruent topologies. The theoretical analysis is supported by an experimental set-up of 150W prototype.

INDEX TERMS Renewable energy sources, switched-inductor, capacitor-divider network, single switch.

NOMENCLATURE

V_1	Input Voltage
V_0	Output Voltage
D	Duty Ratio
G_{CCM}	Gain in CCM
G_{DCM}	Gain IN DCM
D'	Duty Ratio in DCM when current becomes zero
Γ	Inductor Time Constant
V_S	Maximum Voltage across switch S
I_S	Maximum Current across switch S
I_0	Output Current
I_1	Input Current
f_S	Switching Frequency
r_S	Switch Internal resistance
r_L	Inductor Internal resistance
r_C	Capacitor Internal resistance
V_{FD}	Forward Voltage Drop
t_{ON}, t_{OFF}	On and Off time of switch
η	Efficiency

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I. INTRODUCTION

The fast depletion of conventional sources of energy has caused rapid advancement in the exploration of renewable energy sources (RES). The use of renewable energy not only helps in fulfilling the growing energy demand but also in providing a much efficient, clean and sustainable alternative. These RES like solar PV cells, fuel cells, etc produce a low terminal voltage, typically 12-24V and for the ease in the utilisation of this energy, the output voltage needs to be stepped up for either directly feeding to the local loads or connecting to the microgrid system as depicted in Fig.1 [1]. The typical boost converter topology is not suitable for this application because for obtaining the desired high gain, an extreme value of duty ratio needs to be applied which deteriorates the performance of the high-boost converter and leads to serious diode reverse recovery problems, electromagnetic interference, a surge in conduction losses and high voltage stress on the switch [2].

There are various converter topologies in literature aiming to achieve high gain with a moderate value of duty ratio [3]. The converters topologies can be branched into two: isolated and non-isolated type of high gain converters. In the isolated converters, the transformer turn ratio is resorted to raise the

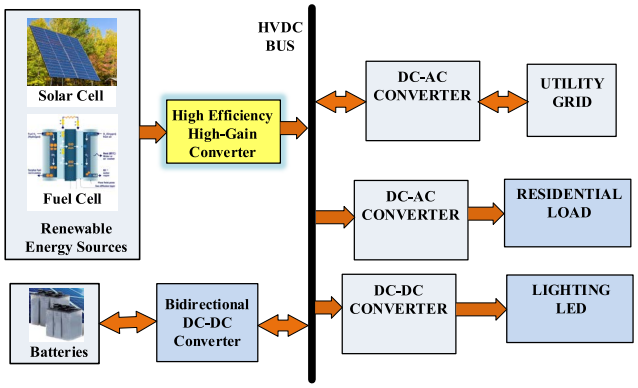

FIGURE 1. Role of High-boost Converter in solar PV system.

gain. The galvanic isolation makes them favourable for high-power applications but the size, cost and bulky nature are its major limitation. The leakage inductance loss and the transformer core saturation are other constraints [4].

The other variety is grouped under the name of non-isolated high-boost converters. In [5], a cascaded boost converter with several individual units of conventional converters connected in series is proposed. Here, the high gain is achieved at a high duty ratio (D>0.8) and thus, the efficiency is decreased due to substantial conduction losses. Moreover, the number of devices is increased which leads to large size, high complexity and escalated losses. With cascading of several converters, cubic and quadratic converters are derived [6]. In [7], a quadratic converter is developed with superior voltage gain in contrast to conventional boost converters but the high current and increased switch voltage stress are serious drawbacks. In this, the quasi-resonant structure required for soft-switching adds up to the complexity of the circuit.

The topologies proposed in [8], [9] use coupled inductors (CIs) to secure the elevated gain. In this, the voltage stress and the current stress subjected to the switch is limited but the leakage inductance loss of the coupled inductor winding impose a major limitation. For regeneration of the leakage energy, an additional clamping circuit is required which complicates the controllability of the converter along with increasing the losses [10]. The topology presented in [11] uses an interleaved structure with two coupled inductors and four switches.

Though the interleaving technique favours the high-power applications and has reduced ripple current but the number of switches used is high considering the gain derived. The other voltage-uplift techniques are switched capacitors, switched inductors, voltage-multiplier units, etc. In [12], the interleaved converter with voltage-multiplier unit yields gain of (1+3D)/(1-D) with considerably high number of components and two switches. The switched capacitor (SC) based topologies are presented in [13], [14]. In these types of converters, the capacitors undergo charging in parallel followed by discharging in series. But in such cases, the voltage regulation is poor and this technique can only be employed when integrated with other methods for the proper regulation of output voltage. It also results in high current spikes. In [15], a switched-capacitor based converter is proposed providing the gain of (3+D)/(1-D). In [16], switched inductor (SI) based converters yields a gain of 2/(1-D) in which the inductors are charging parallelly and discharging serially to enhance the gain but at the cost of an incremented number of switches. Unfortunately, this leads to higher conduction and switching losses.

There are many single-switch converters proposed in the literature. The converters in [17]–[20], use a single switch and provide high gain but the gain of these converters is limited due to the narrow range of duty ratio. (D_{max} =0.5 for [17], [18], D_{max} =0.33 for [19], [20]). There are several other topologies with voltage-multiplier units and its combination with other technique in the literature. The converter in [21], [22] uses active-passive inductor cells with two switches to provide a gain of (1+3D)/(1-D). The converter in [23] provides a gain of 1/D(1-D) with two switches and in [24], [25] three switches are used to attain the high gain. In [24], active-passive inductor cells are used which increases the overall component count and in [25], the parallel inductors are charged with a divided duty ratio. Even though the gain is increased but it is accompanied by a proliferation of switches and a lack of common ground. There are several converters proposed that use only one single switch [26]–[30]. In these converters, various kinds of hybrid boosting VMUs, active-passive switched inductor and capacitor cells are used but the total number of components are also increased with the gain.

Even now, there is sufficient scope for designing an even better high-gain power converter. In this paper, an expandable switched-inductor and capacitor-divider circuit (n-SLCD) with single switch is designed. The propounded converter has a continuous, non-pulsating input current, common-ground structure, high-gain, easier control and low maintenance requirement with low EMI. The proposed converter has a minimum phase nature as there is no right-hand plane zero (RHPZ). This improves the transient voltage response and smoothens high bandwidth control. The propounded converter is stable with all its poles on the left-hand plane (LHP). The voltage stress subjected to the switch is half of the output voltage and the converter can yield high gain for a wide range of duty ratios. The use of only a single switch is cost-effective and the limited stress on the switch allows the use of a lower rating switching device and hence, improves the efficiency.

This article is structured in seven sections. The circuit topology description, extended topology, continuous conduction mode, discontinuous conduction mode and boundary conditions are described in section 2. The circuit parameters design, semiconductor devices' voltage stress and the effect of non-ideal circuit parameters on efficiency and voltage gain are grouped in section 3. The small-signal model of the converter and control is articulated in section 4. To prove the competence of the given converter it is set side by side with other topologies in section 5 and the theoretic inspection is

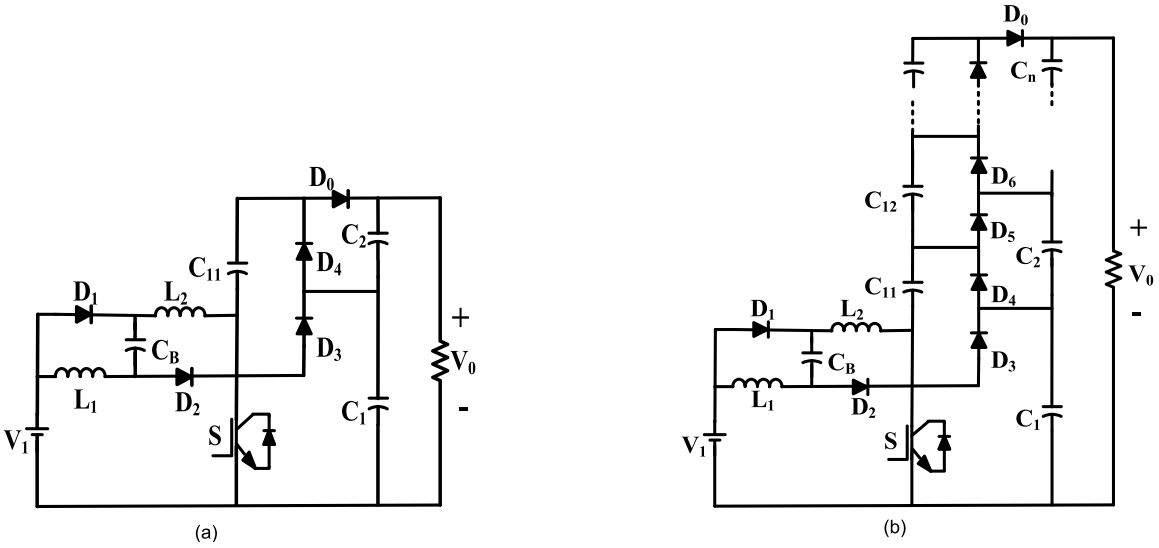

FIGURE 2. (a) Proposed SLCD Converter, (b) Extended SLCD Converter.

verified by experimental set up of 150W in section 6 followed by the conclusion.

II. PROPOSED SLCD CONVERTER

In the proffered converter model, a revamped switched-inductor cell and switched- capacitor are merged in such a way that they override their respective drawbacks. The SLCD converter has two inductors (L_1 and L_2), one boosting capacitor (C_B), one charge storing capacitor (C_{11}), two output voltage divider capacitors (C_1 and C_2), five diodes (D_1, D_2, D_3 and D_4 and one output diode D_0) and one switch (S) as shown in Fig.2(a).

The SCLD converter operates in two modes. When the inductor currents I_{L1} and I_{L2} remain always positive, the converter operates in continuous conduction mode (CCM) and when it reaches zero before the end of the switching off interval, the converter operates in discontinuous conduction mode (DCM). For analytical simplification, a few assumptions are made. They are listed as follow:

- All the devices are considered ideal and lossless.
- The capacitance value is considered ample enough to overlook the ripple voltage.
- The inductance is also large enough to assume a linear variation in inductor current.
- The inductors L_1 and L_2 are identical ($L_1 = L_2 = L$).

A. CCM OPERATION

According to the switching operation, there are two modes of operation identified in CCM.

1) MODE 1

During this mode, S is switched on. The inductor L_1, L_2 and capacitor C_B are charging through diodes D_1, D_2 and switch S as demonstrated in the circuit diagram Fig.3(a). The inductor currents I_{L1} and I_{L2} are increasing linearly with a positive slope. The diodes D_3 and D_0 are reverse biased. The output capacitor C_1 is charging the intermediate capacitor C_{11} through diode D_4 and the output capacitors C_1 and C_2 are feeding the load. The response of the inductor, capacitor voltages and currents waveform for this mode are showcased in Fig.4(a). The inductor voltages, currents and capacitor voltage are given by the following equation:

$$V_{L_1} = V_{L_2} = V_1 \tag{1}$$

$$V_{CB} = V_1 \tag{2}$$

$$I_{L_1MIN} = I_{L_2MIN} = I_{LMIN} \tag{3}$$

$$I_{L_1} = I_{L_2} = I_L = \frac{V_1}{L} DT_S + I_{L(Min)} \tag{4}$$

2) MODE 2

During this mode, switch S is switched off and the energies garnered in the inductors L_1, L_2 and capacitors C_1 and C_2 are released to load in series along with V_1. The series discharge of energy of all the passive elements upsurges the gain of the converter. The equivalent circuit operation diagram is demonstrated in Fig.3(b). The inductor currents decline linearly with a negative slope but they do not reach zero value and remains continuous. The diode D_3 limits the voltage stress across the switch to equal to voltage across C_1 which is half of output voltage. The inductor voltages and currents are given by the following equations:

$$V_1 + V_{L1} + V_{CB} + V_{L2} + V_{C11} = V_0 \tag{5}$$

$$V_{L_1} = V_{L_2} = \frac{V_0}{4} - V_1 \tag{6}$$

$$I_{L_1 \max} = I_{L_2 \max} = I_{L \max} \tag{7}$$

$$I_{L_1} = I_{L_2} = I_L = \frac{1}{L}\left(V_1 - \frac{V_0}{2}\right)(1-D)T_S + I_{L \max} \tag{8}$$

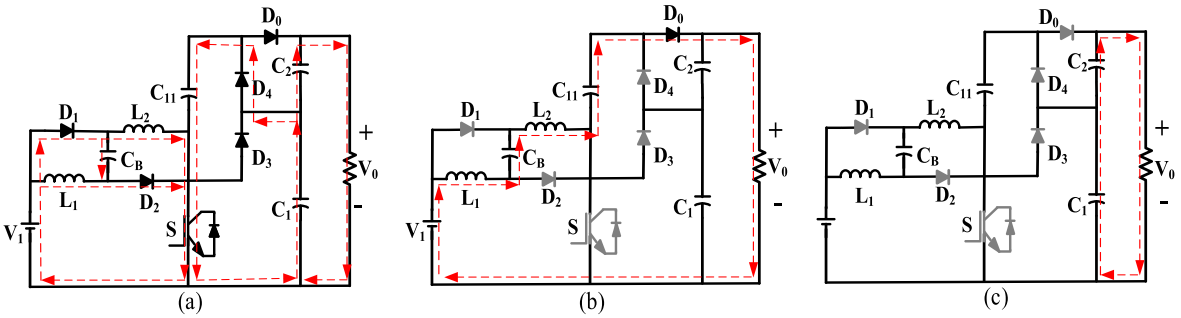

FIGURE 3. (a) Mode 1 of CCM; (b) Mode 2 of CCM; (c) Mode 3 of DCM.

The voltage-second balance equation for V_{L1} is given as,

$$\int_0^{DT_S} V_1 dt + \int_{DT_S}^{T_S} \left(V_1 - \frac{V_0}{4}\right) dt = 0 \tag{9}$$

Thus, the voltage gain G_{CCM} is expressed by the following relation:

$$G_{CCM} = \frac{V_0}{V_1} = \frac{4}{(1-D)} \tag{10}$$

B. EXTENSION OF THE PROPOSED SLCD CONVERTER

The SLCD converter can be expanded to n-stage switched-inductor capacitor-divider network high-boost converter. The n SLCD converter has two inductors (L_1 and L_2), one boosting capacitor C_B, intermediate capacitors ($C_{11}$to $C_{1(n-1)}$), n output capacitors (C_1 to C_n), (2n+1) diodes (D_1 to D_{2n}), one output diode D_0 and one switch (S). The converter circuit is shown in Fig.2(b).

The V_{L1} for mode 1 is given by Eq. (1). For the second mode, the value of $V_{L1}$by Kirchhoff's Law as follow:

$$V_{L1} = \frac{V_0}{2n} - V_1 \tag{11}$$

By voltage-second balance equation using Eq. (9),

$$V_0 = \frac{2n}{(1-D)} V_1 \tag{12}$$

where n is the number of output capacitor in load-end capacitor-divider network.

C. DCM OPERATION

In this DCM operation, the current through the inductors L_1 and L_2 reduce to zero before the expiration of the switching-off time of the switch. Therefore, the DCM operation is divided into three operating modes. The first and second modes resemble the CCM operation as shown in the operating circuit of Fig.3(a) and Fig.3(b). In the third mode of DCM, the switch is already turned off and the inductors L_1 and L_2 act as a constant current source and hence the voltage across them is zero is sown in Fig.3(c). The waveform of the key elements is depicted in Fig.4(b).

1) MODE 1

This mode is analogous to the first mode of CCM.

2) MODE 2

This mode lasts for a time-frame of D'T_S and the inductor current declines with a negative slope and reaches zero at the instant (D+D')T_S as shown in Fig.3(b). The inductor voltage and current are given below:

$$V_{L1} = V_{L2} = \frac{V_0}{4} - V_1 \tag{13}$$

$$i_{L1} = i_{L2} = \frac{1}{L}\left(V_1 - \frac{V_0}{2}\right) D'T \tag{14}$$

3) MODE 3

In the third mode of operation, the output current will flow from the output capacitor to load and diode D_0 will be non-conducting. The voltage spanning the inductor becomes zero. Fig.3(c) shows an equivalent circuit for this mode.

$$V_{L1} = V_{L2} = 0 \tag{15}$$

Writing the voltage-second balance equation for inductor voltage V_{L1} for DCM,

$$\int_0^{DT_S} V_1 dt + \int_{DT_S}^{(D+D')T_S} \left(V_1 - \frac{V_0}{4}\right) dt + \int_{(D+D')T_S}^{T_S} V_1 = 0 \tag{16}$$

By simplifying the above equation, the DCM voltage gain, G_{DCM} as a function of D and D' will be given by the following equation:

$$\frac{V_0}{V_1} = \frac{4(D+D')}{D'} \tag{17}$$

$$G_{DCM} = 4\left(\frac{D}{D'} + 1\right) \tag{18}$$

D. BOUNDARY CONDITION OF OPERATION

At the boundary operating condition, the gain of both CCM and DCM modes are identical. Hence, by equating Eq.10 and Eq.16, the normalized inductor time constant can be derived. For boundary conditions, the inductor current falls to zero just at the end of switching off instant. The DCM waveform is analysed for deriving the boundary conditions.

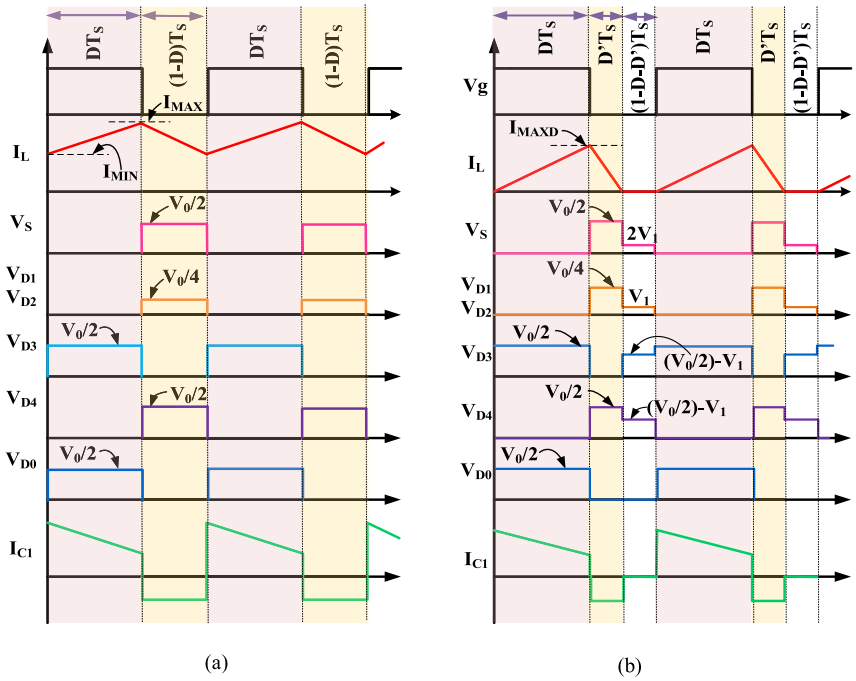

FIGURE 4. Waveform of the key factors for operation in (a) CCM, (b)DCM.

As it can be seen in the waveform from Fig.4(b), for the converter to operate in CCM, and for the inductor current to be continuous, half of the total ripple inductor current should be more than the inductor current I_L. Therefore, for analysis, the value of ξ_{iL1} is more than equal to 1.

$$\xi_{i_{L1}} = \frac{(\Delta i_{L_1}/2)}{I_L} \geq 1 \tag{19}$$

And,

$$I_1 = \frac{4}{(1-D)} I_0 \tag{20}$$

Replacing the value of I_L in Eq.17,

$$\xi_{i_{L1}} = \frac{\Delta i_{L_1}(1-D)}{16 I_1} \geq 1 \tag{21}$$

$$\xi_{i_{L1}} = \frac{V_1 D T_S (1-D)}{16 L I_0} \geq 1 \tag{22}$$

And,

$$\Gamma = \frac{L f_S}{R} \tag{23}$$

Here, Γ is the time constant for the inductor. For boundary operation, the variation of Γ with D can be in Fig.5. The boundary-value of Γ is,

$$\Gamma = \frac{D(1-D)^2}{32} \tag{24}$$

Using the above equations,

$$G_{DCM} = \sqrt{\frac{D}{2\Gamma}} \tag{25}$$

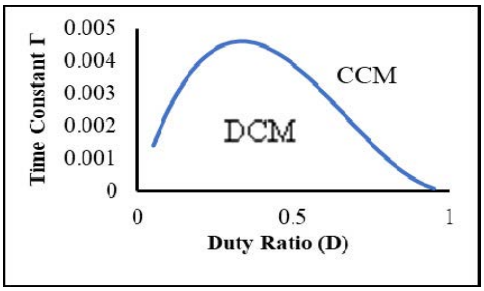

FIGURE 5. Variation of Boundary Inductor time- constant Γ with duty ratio D.

III. PARAMETER DESIGN CONSIDERATION

The design of the circuit components for the SLCD converter is done for a scaled-down system of 150W output power, 10V input voltage. The gate pulses of the switch S has frequency f_S equal to 30kHz.

A. INDUCTOR DESIGN

The inductor value can be found out by the value of maximum allowable ripple current Δi_L. The maximum allowable ripple current is presumed to be 10% of the inductor current value. Both the inductors L_1 and L_2 are equal and can be derived from the following relation [2]:

$$L_1 = L_2 \geq \frac{D V_1}{\Delta i_L f_S} \tag{26}$$

B. CAPACITOR DESIGN

The capacitor C_B and C_{11} are charged for time DT_S when switch S is on and the output capacitors C_1 and C_2 are charged

TABLE 1. Switch and Diodes Voltage Stress in CCM and DCM.

	Operating Mode	V_S	V_{D1}	V_{D2}	V_{D3}	V_{D4}	V_{D0}
CCM	Mode 1	0	0	0	$V_0/2$	0	0
	Mode 2	$V_0/2$	$V_0/4$	$V_0/4$	0	$V_0/2$	$V_0/2$
DCM	Mode 1	0	0	0	$V_0/2$	0	0
	Mode 2	$V_0/2$	$V_0/4$	$V_0/4$	0	$V_0/2$	$V_0/2$
	Mode 3	$2V_1$	V_1	V_1	$(V_0/2)- V_1$	V_1	V_1

for time (1-D)T_S when the switch S is off. With the charge balance equation,

$$C_B\Delta V_{CB} = (I_1 - 2I_L)DT_S \tag{27}$$
$$C_{11}\Delta V_{C11} = I_0 DT_S \tag{28}$$
$$C_1\Delta V_{C1} = C_2\Delta V_{C2} = (I_L - I_0)(1-D)T_S \tag{29}$$

The average inductor current I_L by ampere second balance equation for I_{C2},

$$\int_0^{DT_S} I_{C2} + \int_{DT_S}^{T_S} I_{C2} = 0 \tag{30}$$
$$-\frac{V_0}{R}D + \left(I_L - \frac{V_0}{R}\right)(1-D) = 0 \tag{31}$$
$$I_L = \frac{V_0}{R(1-D)} \tag{32}$$

Using Eq.18, Eq.30 and $I_0 = V_0/R$, the capacitance values are as follow:

$$C_B \geq \frac{2V_0 D}{(1-D)f_S R\Delta V_{CB}} \tag{33}$$
$$C_{11} \geq \frac{V_0 D}{f_S R\Delta V_{C11}} \tag{34}$$
$$C_1 = C_2 \geq \frac{V_0 D}{f_S R\Delta V_{C_{1/2}}} \tag{35}$$

C. VOLTAGE STRESS ACROSS THE SWITCH AND DIDOES

The switch and diode voltage stress in CCM and DCM operation is given in Table 1. The voltage stress, the switch is independent of the duty cycle and is equal to half of the output voltage. The DC voltage gain for the switch and the diodes are given by the equation below:

$$\frac{V_S}{V_1} = \frac{G_{CCM}}{2} \tag{36}$$

The diode voltage gain as a function of gain ratio G_{CCM} can be given as follow:

$$\frac{V_{D1}}{V_1} = \frac{V_{D2}}{V_1} = \frac{G_{CCM}}{4} \tag{37}$$
$$\frac{V_{D3}}{V_1} = \frac{V_{D4}}{V_1} = \frac{V_{D0}}{V_1} = \frac{G_{CCM}}{2} \tag{38}$$

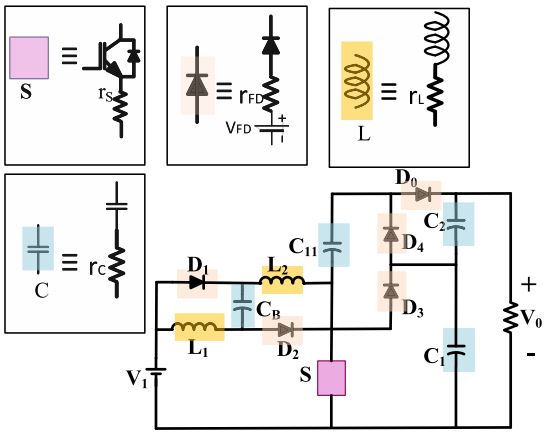

FIGURE 6. SLCD Converter with non-ideal components.

IV. EFFICIENCY INVESTIGATION

A. EFECT OF NON-IDEAL NATURE OF COMPONENTS ON VOLTAGE GAIN AND EFFICIENCY

The converter efficiency is investigated considering the non-ideal nature of the circuit elements. The corresponding circuit of the SLCD converter with non-idealities is depicted in Fig.6. The internal resistances of the inductors L_1 and L_2 are r_{L1} and r_{L2} respectively. The switch S has on-state resistance of r_S. The diodes D_1-D_4 and D_0 have forward voltage drops of V_{FD1}-V_{FD4} and V_{FD0}. The internal resistances of the diodes are r_{D1}-r_{D4} and r_{D0}. The circuit equations for the two modes of operation are as follow:

1) MODE 1

In this mode, the input voltage V_1 is charging the two inductors and capacitor C_1. The equations considering the non-ideal components are as follow:

$$V_{L1} = V_1 - i_{L1}(r_{L1} + r_S + r_{D1}) + V_{FD1} \tag{39}$$
$$V_{L2} = V_1 - i_{L2}(r_{L2} + r_S + r_{D2}) + V_{FD2} \tag{40}$$
$$I_0 = \frac{V_0}{R} \tag{41}$$
$$I_{C2} = -\frac{V_0}{R} \tag{42}$$

2) MODE 2

In this mode, the energy hoarded in the capacitors and inductors are discharging to the load. The governing equations are as follow:

$$V_{L1} = V_{L2} = V_1 + V_{CB} + V_{C11} - V_0 - i_L(r_{L1} + r_{L2} + r_{D0}) + V_{FD0} \tag{43}$$
$$V_{L2} = V_1 - i_{L2}(r_{L2} + r_S + r_{D2}) + V_{FD2} \tag{44}$$
$$I_{C2} = I_L - \frac{V_0}{R} \tag{45}$$

The voltage second balance equation for inductor L_1 is given by the following equation:

$$\int_0^{DT_S} V_{L1} + \int_{DT_S}^{T_S} V_{L1} = 0 \tag{46}$$

Solving the above equation and using Eq.30, the voltage gain of the converter considering the non-ideal nature of the components is given below:

$$V_0 = \frac{V_1 \frac{4}{(1-D)} + 2V_{FD}}{1 + \frac{1}{R}\left[Ar_S + Br_L + -Cr_D\right]} \tag{47}$$

where A=4D/(1-D)^2, B=(2D-1)/(1-D)^2 and C=2/(1-D). The inductors are assumed identical such that their parasitic resistance is equal (r_{L1} =r_{L2} =r_L). The intermediate diodes D_1 to D_4 are also assumed to have equal forward resistance (r_{D1} =r_{D2} =r_{D3} =r_{D4} =r_{D0}) and equal forward voltage drop (V_{FD1} =V_{FD2} =V_{FD3} =V_{FD4} =V_{FD}). The efficiency of the SLCD converter considering the internal resistance of the circuit elements and forward voltage drop of the diodes is given by the following equation:

$$\eta = \eta' - \frac{P_S}{P_i} \tag{48}$$

$$\eta' = \frac{1 + \frac{V_{FD}(1-D)}{2V_1}}{1 + \frac{1}{R}\left[Ar_S + Br_L + -Cr_D\right]} \tag{49}$$

P_S is the switching loss of the switch given by the following equation:

$$P_S = \frac{1}{2} V_{S(\max)} I_{SW} (t_r + t_f) f_S \tag{50}$$

Here, t_r and t_f is the rise time and fall time of the switch mentioned in the datasheet, $V_{S(max)}$ and I_{Sw} are the RMS switch voltage and current and f_S is the switching frequency.

$$P_i = \frac{G_{IDEAL} V_S V_0}{R} \tag{51}$$

P_i is the input power of the converter. Here, G_{IDEAL} is the ideal voltage gain of the converter. The plot showing the variation of voltage gain versus duty ratio for ideal case with loss-free components and for non-ideal case with practical components is plotted using Eq.10 and Eq.45 is shown in Fig.7. The curve for the two voltage gains show variation at higher duty ratio (D>0.75) as the gain in practical conditions declines compared to ideal gain. The efficiency versus duty ratio is plotted in Fig.8 using Eq.46 and Eq.47 after calculating the values of constant A, B and C from datasheet. It shows that the efficiency increases with incrementation in input voltage with output power remaining constant.

B. EFFICIENCY CALCULATION FOR CCM

The efficiency of the DC-DC converter is the paramount feature and the analysis is done here by evaluating the losses

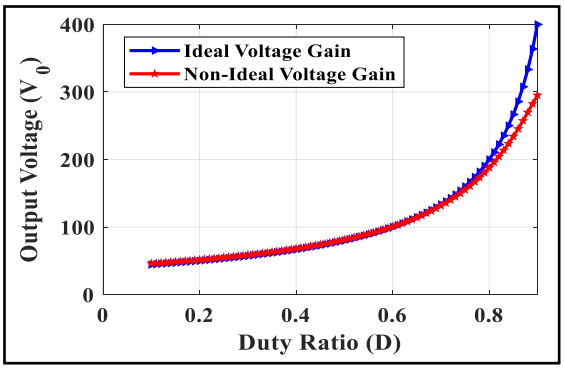

FIGURE 7. Variation of Ideal and Non-Ideal Voltage Gain with Duty Ratio (D).

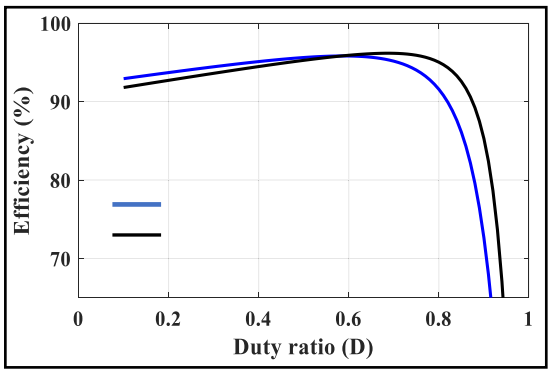

FIGURE 8. Variation of Efficiency (%) versus Duty Ratio (D).

in each element for the given converter. For the switches, switching losses (P_{SWL}) is given by the following formula:

$$P_{SWL} = \frac{1}{2} f_S V_{S(\max)} I_{SW} \left(t_r + t_f\right) = 0.85\text{W} \tag{52}$$

In this equation, $V_{S(max)}$ is the maximum voltage stress on the switches, I_{SW} is the switching current, t_{off} and t_{on} are the device static characteristic and f_S is the switching frequency ($V_{S(max)}$ =60V, f_S =30kHz, I_{SW} =6.1A, t_{on}+t_{off} =153ns). And, the formula governing switch conduction loss (P_{SWC}) is given as follow:

$$P_{SWC} = I_{SW(rms)}^2 R_{DS(on)} = 0.76\text{W} \tag{53}$$

where $I_{SW(RMS)}$ is the RMS value of the switch current and $r_{DS(on)}$ is on-state resistance ($r_{DS(on)}$ =20mΩ). The sum of switching and conduction losses gives the total loss in the switch ($P_{SW(loss)}$).

$$P_{SW(loss)} = P_{SWL} + P_{SWC} = 1.61\text{W} \tag{54}$$

For the diodes, the losses are divided into loss due to forward voltage drop and conduction loss. The forward voltage drop loss ($P_{D(FVD)}$) is given by the following equation:

$$P_{D(FVD)} = \sum_{k=1}^{k=5} I_{Dk(avg)} V_{FD} = 4.75\text{W} \tag{55}$$

where $I_{Dk(avg)}$ is the average current across k^{th} diode and V_{FD} is the forward voltage drop (V_{FD} =0.78V). The conduction losses in the diodes is given by the following equation:

$$P_{D(Cond.Loss)} = \sum_{k=1}^{k=5} I_{Dk(rms)} r_D = 0.74\text{W} \tag{56}$$

where $I_{Dk(rms)}$ is the RMS current across k^{th} diode and r_D is the diode internal resistance (r_D =17.7mΩ). The total loss occurred due to diodes is equal to,

$$P_D = P_{D(FVD)} + P_{D(Cond)} = 5.40\text{W} \tag{57}$$

The inductor loss is given by,

$$P_L = \sum I^2_{L(rms)} r_L = 1.62\text{W} \tag{58}$$

where $I_{L(rms)}$ is the RMS current across inductor and r_L is the internal resistance of inductor ($I_{L(rms)}$ =4.5A, r_L =20mΩ). And the capacitor loss is given by the following equation:

$$P_C = \sum I^2_{C(rms)} r_C = 0.4\text{W} \tag{59}$$

where $I_{C(rms)}$ is the RMS current across capacitor and r_C is the internal resistance of capacitor (r_C =10mΩ). Based on the above analysis, the efficiency of the converter can be found by:

$$\eta = \frac{P_0}{P_0 + P_{TL}} \tag{60}$$

where P_0 is the total power output and P_{TL} is the total power loss given by sum of all the losses.

$$P_{TL} = P_{SW(loss)} + P_D + P_L + P_C \tag{61}$$

The efficiency of the given converter is computed to be 94% at the given rated power of 150W. And the loss allocation can be found as shown in the Fig. 16(b).

V. SMALL SIGNAL MODELLING OF THE CONVERTER

To inspect the open-loop stability of the converter, state-space modelling and analysis is done. The small-signal model for the system is derived by using the state-space average technique. The state variables are inductor current (i_{L1} and i_{L2}) and capacitor voltages (V_{C1}, V_{C2}, V_{C3} and V_{C4}). And the generalized state-space equation for CCM operation is:

$$\dot{x}(t) = A_k.x(t) + B.u(t) \tag{62}$$
$$y(t) = C_k.x(t) + D.u(t) \tag{63}$$

Here k demonstrates the mode of operation of the converter.

The state, input and output variables are given below:

$$x(t) = [i_{L1}\ i_{L2}\ V_{CB}\ V_{C11}\ V_{C1}\ V_{C2}]^T \tag{64}$$
$$u(t) = [V_1\ i_1] \tag{65}$$
$$y(t) = [V_0(t)] \tag{66}$$

For the first mode of operation, the state space equations can be obtained from the following circuit equations (Fig.3(a)):

$$\left.\begin{aligned} \frac{di_{L1}}{dt} &= \frac{V_1}{L_1} \\ \frac{di_{L2}}{dt} &= \frac{V_1}{L_2} \\ \frac{dV_{CB}}{dt} &= \frac{i_1 - i_{L1} - i_{L2}}{C_B} \\ \frac{dV_{C11}}{dt} &= \frac{V_{C1} + V_{C2}}{R.C_{11}} \\ \frac{dV_{C1}}{dt} &= -\left(\frac{V_{C1} + V_{C2}}{R.C_1}\right) \\ \frac{dV_{C2}}{dt} &= -\left(\frac{V_{C1} + V_{C2}}{R.C_2}\right) \end{aligned}\right\} \tag{67}$$

And for the second mode of operation as shown in Fig.3(b), the circuit equations for determining the state space equation are given below:

$$\left.\begin{aligned} \frac{di_{L1}}{dt} &= \frac{1}{2L}(V_{CB} + V_{C11} - V_{C1} - V_{C2} + V_1) \\ \frac{di_{L2}}{dt} &= \frac{1}{2L}(V_{CB} + V_{C11} - V_{C1} - V_{C2} + V_1) \\ \frac{dV_{CB}}{dt} &= -\frac{i_{L1}}{C_B} \\ \frac{dV_{C11}}{dt} &= -\frac{i_{L1}}{C_{11}} \\ \frac{dV_{C1}}{dt} &= \frac{i_{L1}}{C_1} - \frac{(V_{C1} + V_{C2})}{RC_1} \\ \frac{dV_{C2}}{dt} &= \frac{i_{L1}}{C_2} - \frac{(V_{C1} + V_{C2})}{RC_2} \end{aligned}\right\} \tag{68}$$

The A, B, C and D are the system, input, output and feed-forward matrix. For the first mode of operation, A_1, B_1 and C_1 are derived from Eq.65 and for the second mode of operation, the state matrix is represented by A_2, B_2 and C_2 and can be evaluated from Eq.66.

The state-space average matrixes (A_{avg}, B_{avg}) are given by the following equation:

$$A_{avg} = A_1.D + A_2.(1-D) \tag{69}$$
$$B_{avg} = B_1.D + B_2.(1-D) \tag{70}$$
$$C_{avg} = C_1.D + C_2.(1-D) \tag{71}$$

The state-space matrices are given as follow.

$$A_{avg} = \begin{bmatrix} 0 & 0 & \frac{(1-D)}{2L} & \frac{(1-D)}{2L} & -\frac{(1-D)}{2L} & -\frac{(1-D)}{2L} \\ 0 & 0 & \frac{(1-D)}{2L} & \frac{(1-D)}{2L} & -\frac{(1-D)}{2L} & -\frac{(1-D)}{2L} \\ -\frac{1}{C_B} & -\frac{D}{C_B} & 0 & 0 & 0 & 0 \\ -\frac{(1-D)}{C_{11}} & 0 & 0 & 0 & 0 & 0 \\ \frac{(1-D)}{C_1} & 0 & 0 & 0 & -\frac{1}{RC_1} & -\frac{1}{RC_2} \\ \frac{(1-D)}{C_2} & 0 & 0 & 0 & -\frac{1}{RC_1} & -\frac{1}{RC_2} \end{bmatrix} \tag{72}$$

$$B_{avg} = \begin{bmatrix} \frac{(1+D)}{2L} & 0 \\ \frac{(1+D)}{2L} & 0 \\ 0 & \frac{(1-D)}{C_B} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad (73)$$

$$C_{avg} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \quad (74)$$

By solving the state-space average matrix, the open-loop transfer function of the output voltage with duty ratio (considering the initial condition zero) is obtained:

$$TF = \frac{\hat{v}(s)}{\hat{d}(s)}; (V_0(s) = 0) \quad (75)$$

The transfer function, poles and zeros are calculated using MATLAB code with parameter values given in Table 3. The non-zero poles are: P_1, $P_2 = -373.5.1 \pm 7600.3i$ and $P_3 = -1038.6$ and the non-zero zeros are Z_1, $Z_2 = -742 \pm 14119i$ and $Z_3 = -301$. As there is no right-hand plane zero (RHPZ), the converter system is a minimum phase (MP) system and thus, it is capable of faster response and favourable high-bandwidth control design. All the poles are on the left-hand plane (LHP) and hence, the converter is stable. The bode plot of the TF is shown in Fig.9. The phase margin is 22.4° and the gain margin is infinite which justifies that the system is inherently stable.

From the Fig.9, it can be seen that the circuit operation is inherently stable with infinite gain margin and positive phase margin. For achieving the operation at any desired frequency, a controller loop can be designed. For the closed loop control of the designed SLCD converter, proportional integral (PI) controller can be used. The error signal generated by comparison of the output voltage with the reference output voltage and the error signal e(t) generates the gating pulse $V_{GS}(t)$ with the help of comparator as shown in the Fig.10. The time-constant and gain is obtained for PI controller employing the trade-off method.

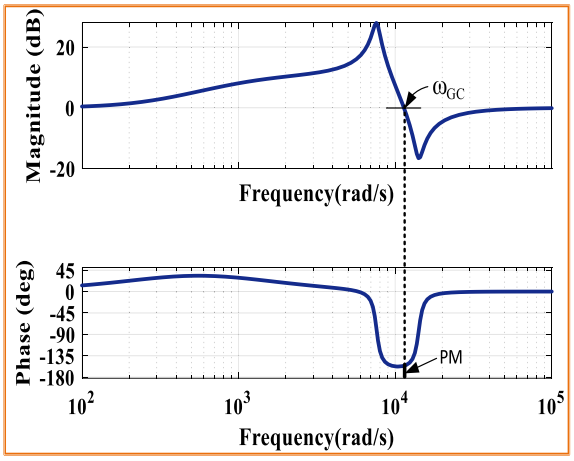

FIGURE 9. Bode Plot of the Open-loop transfer function of the converter.

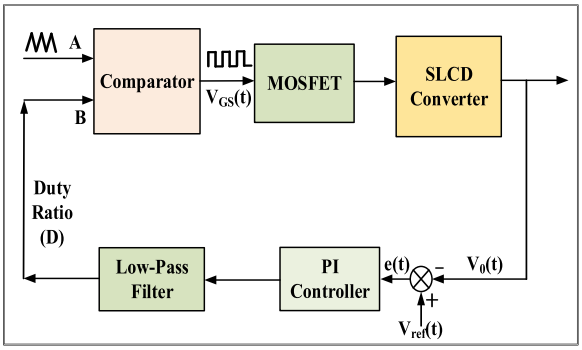

FIGURE 10. (a) Bode Plot of the Open-loop transfer function of the converter; (b) Closed Loop Control of the converter using Duty Ratio control.

VI. COMPARISON OF SLCD CONVERTER WITH OTHER TOPOLOGIES

The SLCD converter is compared with the recent converters as listed in Table 2. The converters use different techniques for achieving the gain like switched inductor, switched capacitor, voltage multiplier units or a hybrid of all these techniques. In [15], switched capacitor technique is used to achieve the gain but the prime limitation is the use of two switches and the requirement of gate driver circuit increasing the losses and cost. Also, the switch voltage stress is immensely large equal to the output voltage. Although the total number of components used is 10, the ratio of gain to total component count is lesser than the proffered converter. The converters in [16], [21], [22] and [23] utilize three switches but the gain achieved is lesser than the SLCD converter. In [16], SL are charged in parallel and discharged in series with a total of eight components but the gain achieved is half of the presented converter. The converters in [21] and [22] achieve a gain of (1+3D/(1-D) which is lesser as shown in Fig.11(a). In [24], an extendable active-passive inductor cell (APICs) based converter is proposed that uses three switches to achieve the high gain. For a better comparison, the ratio of voltage gain to the number of components can be seen in Fig.11(b). The converters [26]–[30] use a single switch. A bipolar voltage multiplier-based hybrid boost converter is proposed in [26] which uses a single switch and single inductor but the gain at a given duty ratio is less. The converter in [27] is a SEPIC based buck-boost converter that utilizes inductors, capacitors and diodes for achieving the higher gain.

Though only a single switch is used, the number of components is high and the key ratio of gain to total component count is lower compared to the proposed converter. The switch voltage stress depends on the duty cycle and is equal to $V_0/3D$. The converter in [28] is a consolidation of the Cockcroft-Walton diode-capacitor voltage multiplier and conventional boost converter. Apart from increasing gain, it increases the number of components considerably. For

TABLE 2. Comparison of SLCD converter with other converters.

Ref.	No. of Components		Voltage Gain (V_0/V_1)	Switch Voltage Stress (V_S/V_0)	Output Diode Voltage Stress (V_D/V_0)	High-Gain Technique	Common Ground
	N_S N_D	N_L N_C					
SLCD Converter	1 5	2 4	$\frac{4}{1-D}$	$\frac{1}{2}$	$\frac{1}{2}$	Switched Inductor and Capacitor Divider Network	Yes
[30]	1 6	2 3	$2\left(\frac{1+D}{1-D}\right)$	$\frac{1}{2}$	$\frac{1}{2}$	Single Switched Impedance Network and SC	No
[29]	1 3	3 5	$\frac{1+2D}{1-D}$	$\frac{2+G}{3G}$	$\frac{2+G}{3G}$	$L^2C^3D^2$ Network with single switch	Yes
[28]	1 5	1 5	$\frac{3}{1-D}$	$\frac{1}{3}$	$\frac{1}{3}$	Cockcroft-Walton Diode Capacitor Multiplier Technique	Yes
[27]	1 3	4 6	$\frac{3D}{1-D}$	$\frac{G+3}{3G}$	$\frac{G+3}{3G}$	LC Multiplier Unit	Yes
[26]	1 4	1 4	$\frac{3-D}{1-D}$	$\frac{G-1}{2G}$	$\frac{G-1}{2G}$	Hybrid Boosting Structure with VMUs	No
[24]	3 3	4 1	$\frac{1+2D}{1-D}$	$\frac{G+1}{2G}$	$\frac{1}{G}$	Active Passive Inductor Cell	No
[23]	2 3	2 2	$\frac{1}{D(1-D)}$	1	1	SC and Inductor Voltage Lift technique	No
[22]	2 7	4 1	$\frac{1+3D}{1-D}$	$\frac{G+1}{2G}$	$\frac{G+1}{G}$	Active-Passive Inductor Cell	No
[21]	2 2	3 3	$\frac{1+3D}{1-D}$	$\frac{G+3}{4G}$	$\frac{G+3}{4G}$	Active SL and Passive SC	No
[16]	2 2	2 2	$\frac{2}{1-D}$	$\frac{1}{2}$	1	Parallel charging of inductors with multiple switches	No
[15]	2 3	2 3	$\frac{3+D}{1-D}$	$\frac{G+1}{4G}$	$\frac{G+1}{2G}$	SC based Converter	No

comparative analysis, three units of ladder circuit are considered (N=3) and the gain is derived as 3/(1-D). Though the voltage stress across switch and diode is less ($V_0/3$), the gain to component count ratio is lesser as compared to the designed converter. The other converter in [29] utilizes the $L^2C^3D^2$ circuit network for achieving the high voltage gain and gives lesser gain with the same number of components as the SLCD converter. In [30], switched inductor impedance network and a SC without common ground is used to achieve the gain which is lesser than the proposed converter. The plot of gain to duty ratio, gain to total component count prove the advantage of the

TABLE 3. Efficiency Comparison of SLCD converter with other single switch converters.

Converter	Number of Components				Total Component Count (TCC)	Duty Ratio (D)*	V_S (V)	V_{D0} (V)	Common Ground	Efficiency η (%) at 150W
	N_S	N_D	N_L	N_C						
Proposed SLCD	1	5	2	4	12	0.65	60	60	✓	94.05%
[30]	1	6	2	3	12	0.71	60	60	×	93.00%
[29]	1	3	3	5	12	0.78	46.67	46.67	✓	92.50%
[28]	1	5	1	5	12	0.75	40	40	✓	93.51%
[27]	1	3	4	6	14	0.8	50	50	✓	92.70%
[26]	1	4	1	4	10	0.818	55	55	×	92.10%

*Duty Ratio is varied to according to the gain equation to obtain the same output voltage and output power with constant input voltage.

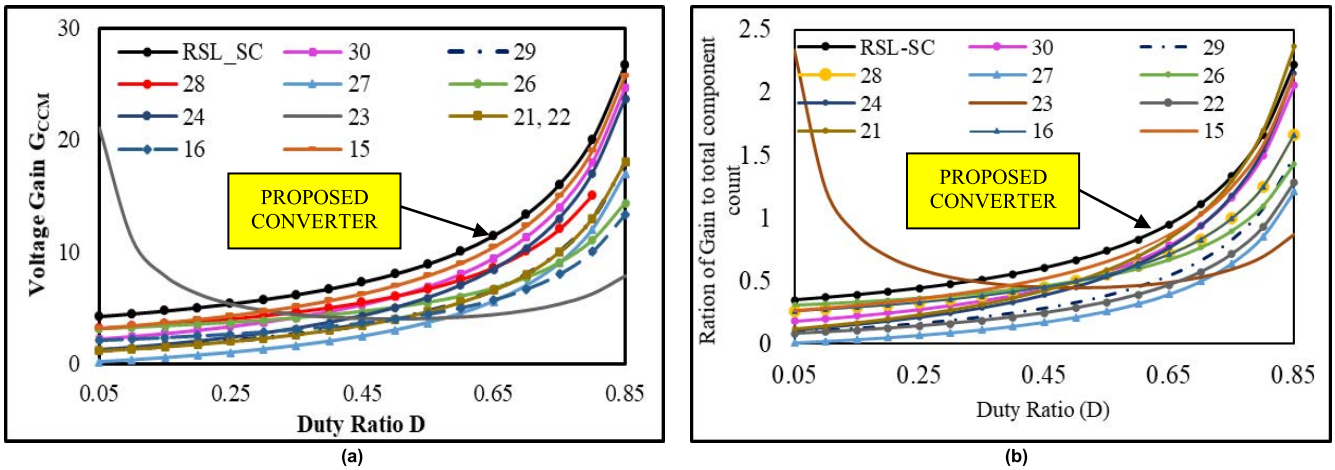

FIGURE 11. (a) Variation of Voltage Gain with Duty Ratio, (b) Variation of Ratio of Gain to Component Count with Duty ratio D.

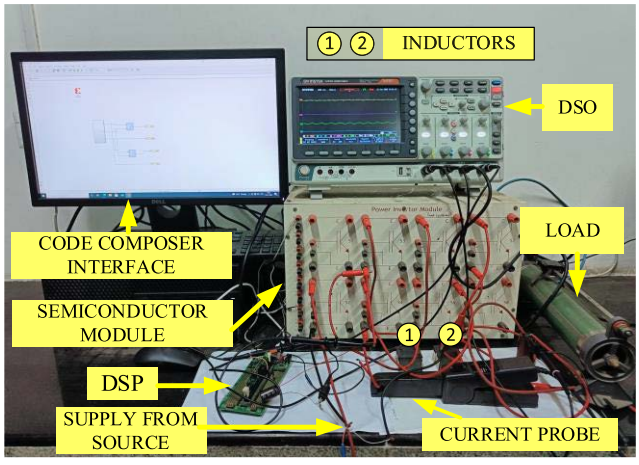

FIGURE 12. Experimental Test Bed.

proposed SLCD converter over other converters is shown in Fig.11(b).

For a better comparison, the efficiency of the proposed SLCD converter and converters in [26]–[30] which uses single switch are computed theoretically using MATLAB Simulink with same input voltage, output voltage and output power. To achieve same the same output voltage with given input, the value of duty ratio D is varied according to the gain equation as displayed in Table 3. As depicted in Table 3, even though the number of diodes in [26], [27] and [29] is lesser, the duty ratio required for a desired gain is high thus escalating the current and hence overall conduction losses. The propounded converter gives higher gain at lower duty ratio with lesser number of components and improved efficiency.

VII. EXPERIMENTAL RESULT

The experimental verification is done with a laboratory prototype of 150W. The circuit is fabricated with elements and values listed in Table 4. The switching pulses of frequency f_S =30kHz are generated by interfacing code composer using DSP controller Texas F28335. The input voltage is 10-12V and the experiment is done for two duty ratios 1) D=0.6 and 2) D=0.68. The optimum value of duty ratio is chosen for better efficiency and desired gain as shown in Fig.8. The experimental test bed is shown in Fig.12.

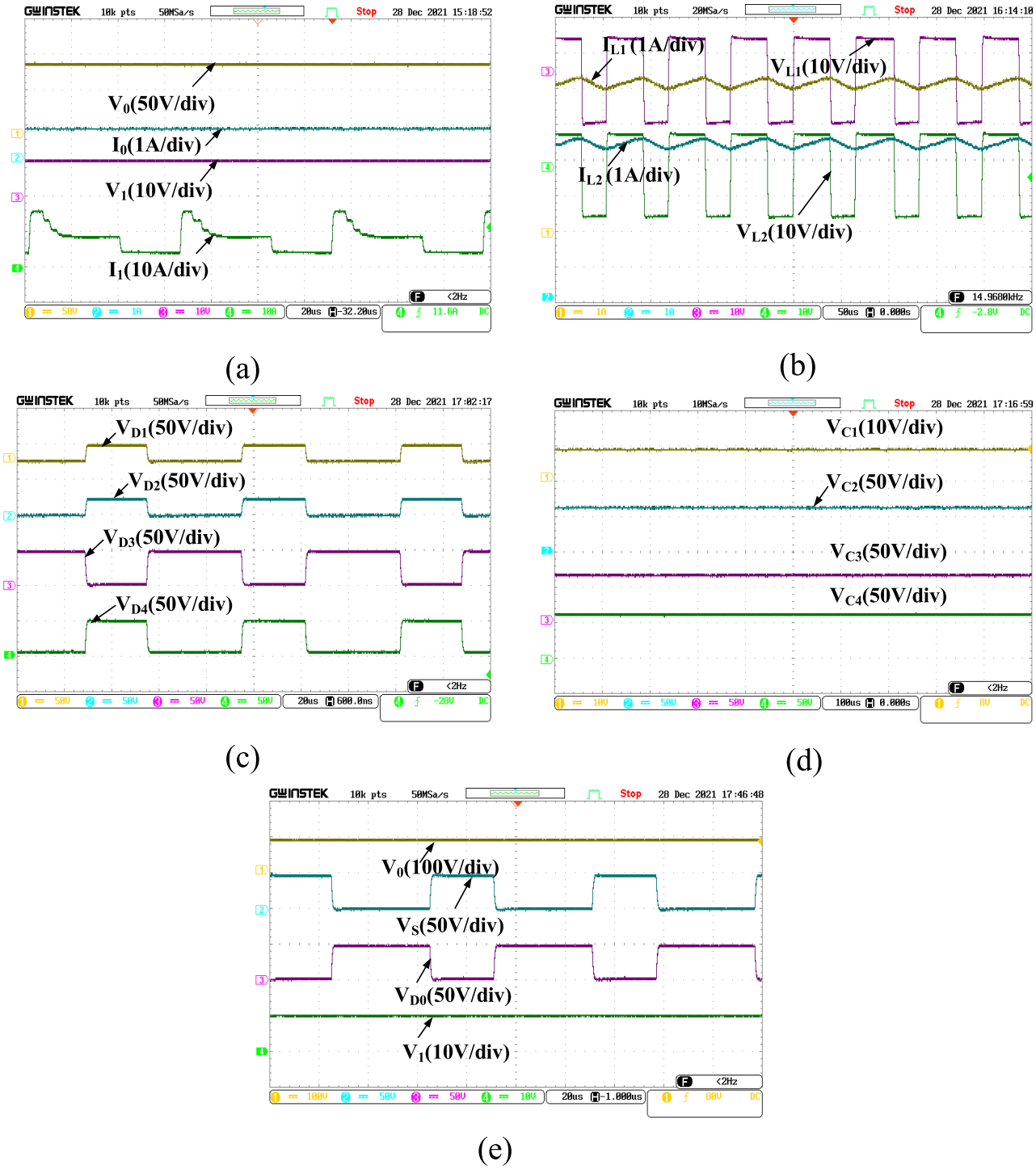

FIGURE 13. Experimental Result for D = 0.6. (a) Output Voltage V_0(V), Output Current I_0(A), Input Voltage V_1(V), Input Current I_1(A), (b) Inductor Current I_{L1}(A), Inductor Current I_{L2}(A), Inductor Voltage V_{L1}(V), Inductor Voltage V_{L2}(V), (c) Diode Voltage V_{D1}, V_{D2}, V_{D3}, V_{D4}(V), (d) Capacitor Voltage V_{C1}, V_{C2}, V_{C3}, V_{C4}(V), (e) Output Voltage V_0(V), Switch Voltage Stress V_S (V), Output Diode Voltage V_{D0}(V), Input Voltage V_1(V).

For D=0.6, a voltage gain of 10 times, V_0 =100V is obtained according to gain equation 4/(1-D). The input voltage 10V and the average value of output current and input current is 0.9A and 10A with load resistance of 110Ω as shown in Fig.13(a). The inductor current is triangular with the linear rise during the on-time of the switch and linear decline during the off-time with an average value of 4.7A. The inductor charges and discharges during the rise and fall time of the inductor current as can be seen in Fig.13(b). The diodes D_1 and D_2 have voltages V_{D1} and V_{D2} equal to 25% of the output voltage, 25V and the voltage stress across V_{D3} and V_{D4} is equal to 50% of output voltage, 50V (Fig.13(c)).

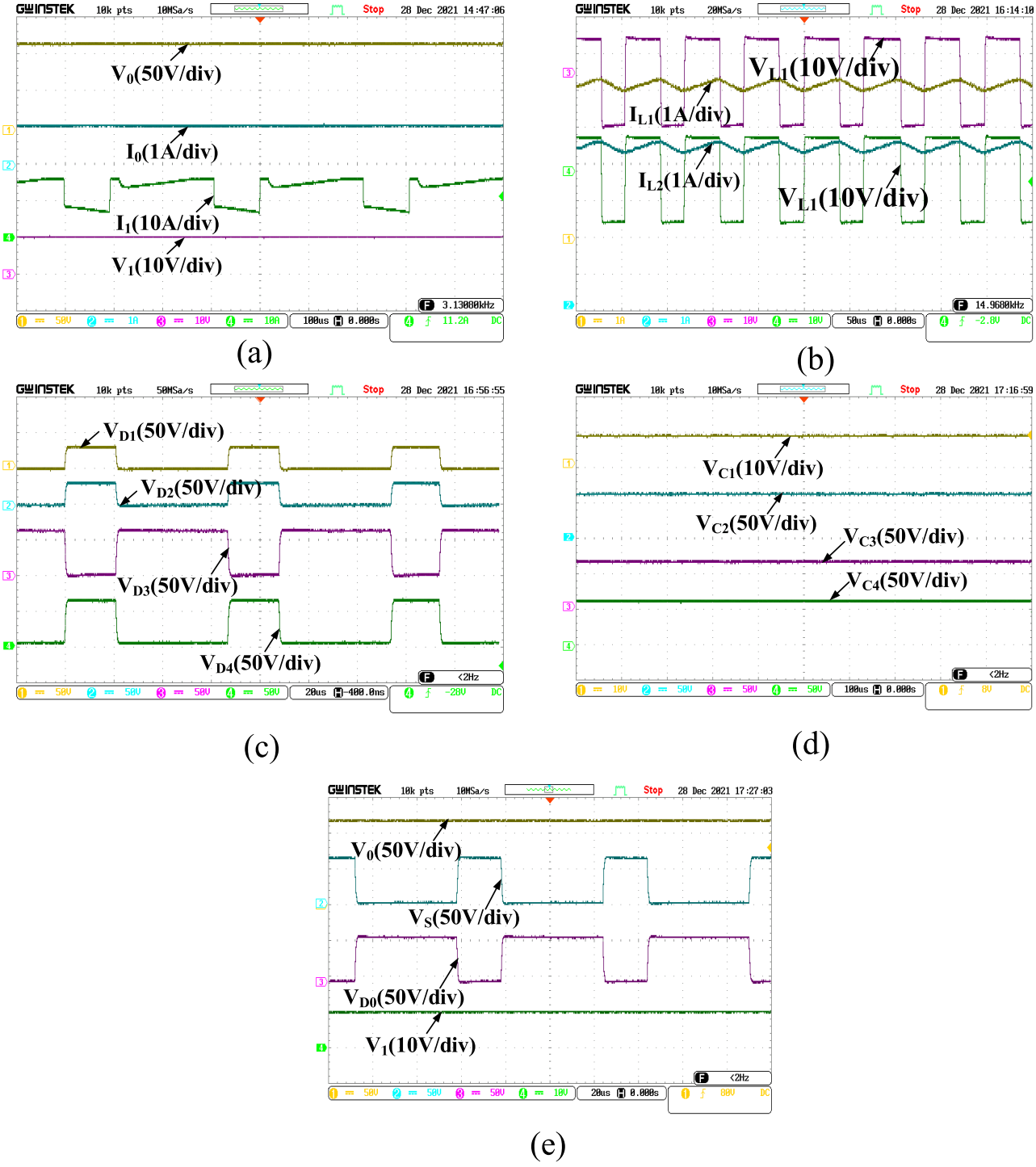

FIGURE 14. Experimental Result for D=0.68. (a) Output Voltage V_0(V), Output Current I_0(A), Input Current I_1(A), Input Voltage V_1(V), (b) Inductor Current I_{L1}(A), Inductor Current I_{L2}(A), Inductor Voltage V_{L1}(V), Inductor Voltage V_{L2}(V), (c) Diode Voltage V_{D1}, V_{D2}, V_{D3}, V_{D4}(V), (d) Capacitor Voltage V_{C1}, V_{C2}, V_{C3}, V_{C4}(V), (e) Output Voltage V_0(V), Switch Voltage Stress V_S (V), Output Diode Voltage V_{D0}(V), Input Voltage V_1(V).

The capacitor voltage V_{CB} and V_{C11} are 10V and 50V respectively according to the analysis as V_{CB} is equal to input voltage V_1 and V_{C11} is equal to half of output voltage. Also, the output capacitor divider voltage V_{C1} and V_{C2} is 50V, half of V_0 shown in Fig.13(d). The value of maximum switch voltage stress is equal to half of the output voltage, 50V irrespective of the value of D. And the output diode stress is also 50V shown in Fig.13(e).

For D=0.68, a voltage gain of 12 times (V_0 =120V) is obtained according to gain equation 4/(1-D). The switch voltage stress is 60V and the load resistance R is 120Ω. The

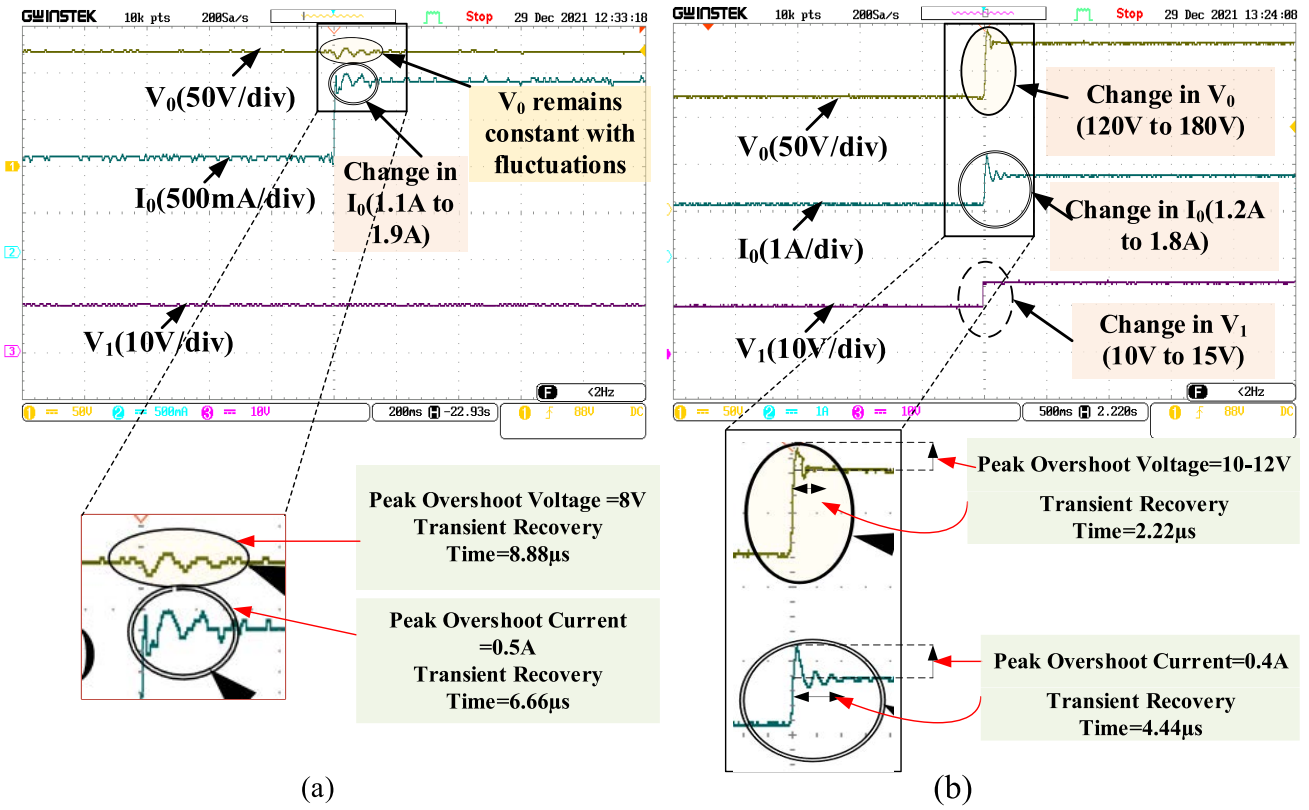

FIGURE 15. Experimental Dynamic Response of the converter for (a) Change in Input Voltage, (b)Change in Load.

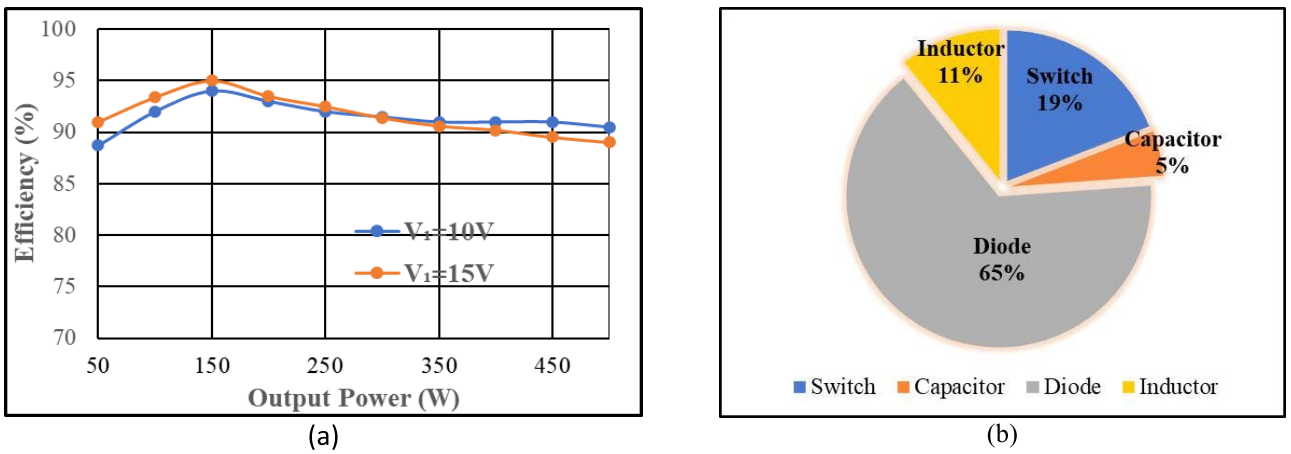

FIGURE 16. (a) Efficiency (%) versus Duty Ratio(D), (b) Loss Distribution.

output and input current obtained is approximately 1A and 10.1A as shown in Fig.14(a). The average value of inductor current is 4.8A and inductor charges to voltage equal to input voltage (Fig.14(b)). The diode voltage V_{D1} and V_{D2} is 30V and V_{D3} and V_{D4} is 60V shown in Fig.14(c).

The capacitor voltages V_{CB}, V_{C11}, V_{C1} and V_{C2} are shown in Fig.14(d) where V_{CB} is equal to input voltage 10V and V_{C11}, V_{C1} and V_{C2} are equal to half of output voltage 60V.The switch voltage stress V_S and output diode stress V_{D0} is shown in Fig.14(e) equal to 60V. When the switch is conducting the diode D_0 is off and when the switch is off in the second mode, the output D_0 conducts.

The dynamic response of the converter is also examined. The response of the converter with the change in load and change in the input voltage is as shown in Fig.15(a) and Fig.15(b). The duty ratio, in this case, is 0.68. When the load resistance is changed (R=110Ω to R=65Ω), the output current I_0 increases (I_0 =1.1A to I_0 =1.9A) with peak overshoot of 0.5A and transient recovery time 6.66μs.

TABLE 4. Components Of SLCD Converter.

Symbol	Quantity	Value
V_I	Input Voltage	10V
V_0	Output Voltage	100V, 120V
L_1, L_2	Inductor	360μH (Ferrite Core)
C	Capacitor	C_1=100μF, C_2=4.7μF, C_3=C_4=10μF
S	Switch	IRF360
D	Diode	MUR1560
f_S	Switching Frequency	30kHz
D	Duty Ratio	0.6, 0.68

The output voltage V_0 remains constant after voltage ripples equal to 8V, thus varying within acceptable limits (V_0 = 180V and I_0 =1.9A) as shown in Fig.15(a). Thus, the converter shows an excellent response to dynamic conditions. When the input is changed from 10V to 15V, the output voltage changes from 120V to 180V according to the gain equation with peak overshoot of 10-12V and transient recovery time of 2.22μs. The output current I_0 increases from 1.2A to 1.8A with R=100Ω, D=0.68, peak overshoot current equal to 0.4A and settling time 4.44μs. The output voltage and output current ripples are seen but their magnitude remains well within acceptable limits as exhibited in Fig.15(b). The efficiency of the converter is investigated at different output power is investigated for two different input voltages (V_1 =10V and V_1 =15V) as shown in Fig.16(a). It exhibits an efficiency of 94% for V_1 =10V and 95% for V_1 =15V at P_0 =150W. The variation of efficiency with load is shown in Fig.16(a) and the loss distribution is displayed in Fig.16(b). The maximum loss of 65% is contributed by the diodes. And the switch contributes 19% of the losses. The inductor and capacitor losses are 11% and 5%.

VIII. CONCLUSION

In this article, a single-switch high-boost SLCD converter is explicitly designed. The SLCD converter is capable of achieving high gain without applying an extreme value of duty ratio and without using coupled inductor or transformers. Due to the employment of only a single switch, the control of the converter or applying any MPPT algorithm is simple. The stress on the switch is limited to half of output voltage which permits utilization of low rating device and minimizing the switching losses. Also, a higher gain achieved at comparably low duty ratio ensures lower conduction losses improving overall efficiency. The small-signal modelling assures the stable operation of the system and the minimum phase nature of the converter shows that the response to changes in input is not delayed and the converter maintains its stable operation. A detailed explanation of the converter operation, stress analysis, the effect of the non-ideal nature of components on efficiency and voltage gain is investigated. The presented SLCD converter is compared with other recent converters and it evidently provides a better trade-off between the gain to the total component count ratio, better reliability and higher gain for a wide range of duty ratios. For verification of theoretical analysis, an experimental prototype of 150W is developed and an efficiency of approximately 94% is achieved. Thus, it can be concluded that this SLCD converter possesses the potential as a significant high-boost DC-DC converter candidature for solar photovoltaic applications.

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