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Low Voltage and Low Power Front Panel Design for 12 Lead ECG

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ABSTRACT The use of portable devices is increasing day by day. Mainly these devices play a vital role in medical field when the doctors are unavailable. In that one of the important emergency medical portable systems is Electro Cardiogram (ECG). ECGs are used to measure the abnormalities of the heart by performing electrical activities. It can be done by attaching electrodes on the body for few minutes. To collect the information from electrodes data acquisition system is used in ECGs or in any biomedical systems. The major challenge in implementing data acquisition system is the increase in power dissipation due to the excessive contact impedance of electrodes. As a solution to this, A CMOS 12 lead ECG data acquisition circuit is designed by using analog multiplexers is proposed in this paper. The proposed system is designed by using improved DTMOS based analog multiplexers and these works with a power supply of ± 0.2 V with a dynamic voltage range from 1uv to 200mv with the Power dissipation of 140 nW.

INDEX TERMS Analog multiplexer, DTMOS, ECG, data acquisition system, noise analysis, signal transmission.

I. INTRODUCTION

Portable biomedical instruments are playing an essential role in the medical system. Electrocardiogram (ECG) is one of the instruments which is very helpful for cardiac patients. During cardiac cycle, ECG graphically displays time-variant voltages that are produced by the myocardium [1]. Biomedical signals are usually picked from the electrodes located at different places of the human body; therefore, these multiple signals have to be acquired and analyzed by the multi-channel system [2], [3]. In twelve lead ECG, 12 different channels with deferent frequencies and amplitudes are used. All these conditions will make a different task to implement a data acquisition system [4]. There are several techniques proposed for the data acquisition system. One of the methods is using Analog to digital converters [5], but ASIC implementation of these circuits is very complex [6], [7]. The alternate solution for this is the analog Multiplexers [8]. Pass transistor logic is one method to implement analog multiplexers [9], but the threshold voltage of pass transistor logic is high compared with supply voltage. Transmission gate switches are also one of the approaches to implement analog multiplexers [10]. These analog multiplexers utilize NMOS and PMOS transistors to implement switches, in which all these switches are connected to design the multiplexer logic [11]. CMOS transistors have high threshold voltage, and it is challenging to design a circuit with a low voltage supply; therefore, CMOS transistors are replaced with Dynamic Threshold MOSFET(DTMOS) transistors [12]. This paper proposes a analog front panel design using DTMOS switches, which will work at low ON resistance and high OFF resistance with a better dynamic range [13], [14]. In regular operations ECG signals amplitude ranging from a few uv to 5 mV [15] and the bandwidth of ECG signals ranges from 0.1 Hz to 150 Hz. The proposed work is executed by using the CADENCE virtuso tool.

The remaining paper is organized as follows. Section II represents the 12 lead ECG signal interpretations. Section III discuss about the forward body biased analog DTMOS switch. Section IV describes Analog front panel design with analog multiplexers. Section V describes the noise and power analysis of the front panel design and finally the work is concluded in Section VI.

II. ECG 12 LEAD INTERPRETATION

12 lead ECG is required to measure the heart information from different parts of the human body by using electrodes [9]–[11]. ECG leads are two types. One is hex

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TABLE 1. 12 lead ECG information.

Lead Name	Connected to inverting terminal of instrumentation amplifier	Connected to NON- inverting terminal of instrumentation Amplifier
BIPOLAR LIMB LEADS		
LEAD- I	RA	LA
LEAD- II	RA	LL
LEAD- III	LL	LL
UNIPOLAR LIMB LEADS		
aVR	LL+LA	RA
aVL	LL+RA	LA
aVF	LA+RA	LL
UNIPOLAR CHEST LEADS		
V1	LA+RA+LL	Fourth inter coastal space at right sterna margin
V2	LA+RA+LL	Fourth inter coastal space at left sterna margin
V3	LA+RA+LL	Midway betweenV2 and V4
V4	LA+RA+LL	Fifth inter coastal space at mid clavicular line
V5	LA+RA+LL	Same level as V4 on anterior auxiliary line
V6	LA+RA+LL	Same level as V4 on mid auxiliary line

axial leads another one is precordial leads. Limb leads and augmented leads are hex axial leads, and chest leads from V1 to V6, these are precordial leads. Bipolar Limb leads are Lead I, Lead II, Lead III. Unipolar Augmented leads are aVR, aVL, aVF. Here aV represents augmented voltage. Precordial leads are placed on the top of the chest.V1 is placed at the right side of the sternum fourth inter coastal space, V2 is placed at the left side of the sternum fourth inter coastal space, V3 is placed between V4 and V2, V4 is placed at left mid clavicles line fifth inter coastal space.V5 is placed at inter coastal axial line and V6 at the middle of the arm line. The front panel of the 12 lead ECG depends on the interpretation of all these leads. Lead information amplified by the instrumentation amplifier (IA). Electrodes are connected to inverting, and non-inverting terminals of the instrumentation amplifier are shown in the Table 1. All Non-inverting terminal electrodes are processed by a 12:1 analog multiplexer and inverting terminal electrodes are processed by the 7:1 analog multiplexer circuit.

III. DESIGN OF DTMOS SWITCH

Based on working principle these are classified as forward and reverse body bias DTMOS switches. Body effect is one of the second-order effects in a MOS transistor which plays a crucial role in determining the MOSFET threshold voltage. In general, the source and substrate are tied to the ground. Introducing voltage differences between the source and substrate terminals, the MOS transistors threshold voltage can be diminished electrically without any technical modifications. Traditionally in circuit design, designer treats MOSFET as a three-terminal device, in which source and substrate are short-circuited. It indicates that the MOSFET can also operate in zero-biased threshold voltage. Since MOSFET has four terminals, including body or substrate, then applying a voltage to the body makes it possible to bias the source and substrate into forward bias, reducing the threshold voltage. The body bias can be accomplished by short-circuiting gate and substrate terminals. The threshold voltage includes the component voltage, which determines the number of carriers in the channel. The threshold voltage (with zero source and substrate voltage) can be written as,

$$V_{TH0} = V_{fb} + \phi_s + \frac{Q_B}{C_{ox}} \tag{1}$$

Here C_{ox} represents the Oxide Capacitance. Flat band voltage V_{fb} is represented as follows

$$V_{fb} = \phi_{gs} - \frac{Q_f}{C_{ox}} \tag{2}$$

where ϕ_{gs} is difference between poly silicon gate work functions and silicon substrate, ϕ_f is fixed oxide charge present in the oxide and at the $Si - SiO_2$ interface, the second term ϕ_s is surface potential, which is double the substrate Fermi potential at threshold. The voltage across the parallel plate capacitor with the charge on the capacitor Q_B is

$$Q_B = \sqrt{2q\epsilon_{si}N_a\phi_s} \tag{3}$$

where ϵ_{si} is the silicon permittivity, q is charge of electrons, N_a is accepter concentration. The electrostatic potential with respect to Si bulk at the silicon surface is described by ϕ_s. The depletion region charge at strong inversion, with no body bias ($V_{SB} = 0$), Q_{BO} is given by

$$Q_{BO} = \sqrt{2qN_a\epsilon_{si}| - 2\phi_f|} \tag{4}$$

In existence of non-zero source /substrate voltage, the stored corresponding charge in depletion capacitance Q_B, is given by

$$Q_B = \sqrt{2qN_a\epsilon_{si}| - 2\phi_f + V_{SB}|} \tag{5}$$

Hence, the threshold voltage is varied by

$$\Delta V_{TH} = \gamma_n(\sqrt{\phi_s + V_{SB}} - \sqrt{\phi_s}) \tag{6}$$

Here γ_n represents the body effect coefficient. The effective threshold voltage in the existence of body-effect V_{TH} is given by

$$V_{TH} = V_{TH0} + \gamma_n(\sqrt{\phi_s + V_{SB}} - \sqrt{\phi_s}) \tag{7}$$

With proper polarity of substrate voltage, threshold can be increased or decreased. As the gate and substrate terminals are short circuited, then there is a transition in the gate voltage due to the non-zero V_{SB}. Reverse polarity of non-zero V_{SB} will introduce change in the threshold voltage.

The Complementary-MOSFET (CMOS) consists of P and N-channel MOSFETs. CMOS switch can be obtained by connecting the PMOS and NMOS devices in parallel form. This combination reduces the on-resistance, and also produces a resistance which varies much less with signal voltage.

The ideal analog switch has zero time delay, infinite off-impedance and no on-resistance. In practice, a CMOS analog switch doesn't meet any of these criteria [16]. In ON

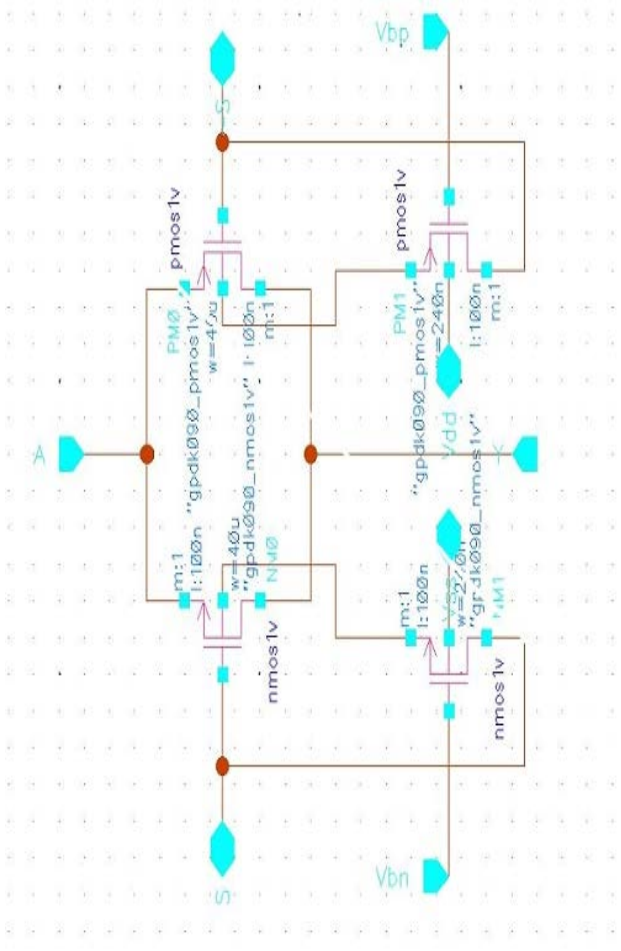

FIGURE 1. DTMOS Analog Switch.

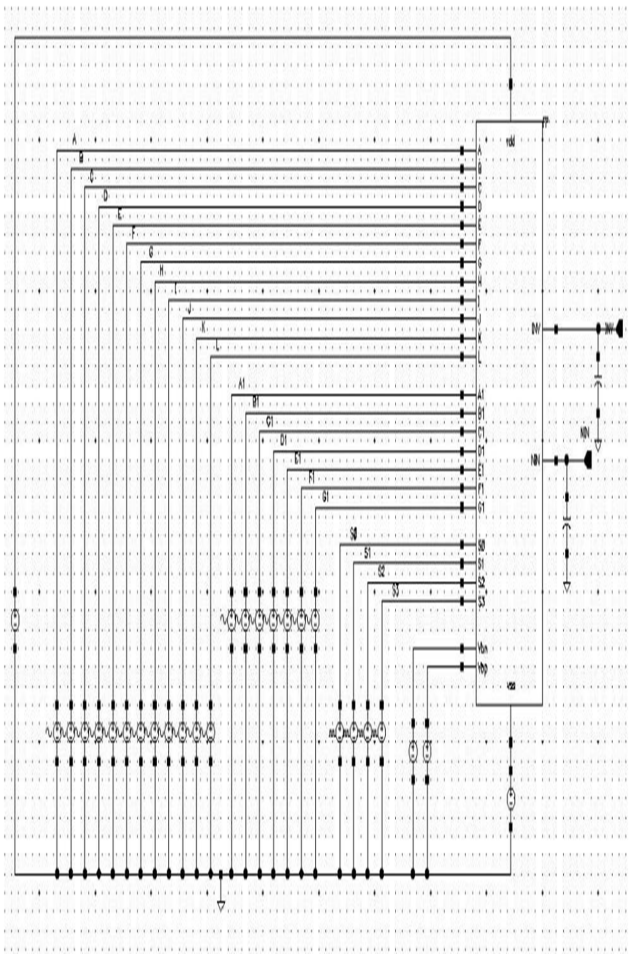

FIGURE 2. A Test bench circuit for front panel design.

state, its resistance is few ohms but in OFF state it increases to several mega ohms [4], [18]. MOSFET transistors are bilateral i.e. they can operate as a switch between positive and negative voltages and conduct positive and negative currents with equal ease.

When the gate voltage is HIGH, the substrate of n-channel MOSFET is connected to VDD and substrate of p-channel MOSFET is connected to VSS. Both the transistors source substrate junctions are forward biased. Now the transmission gate is ON, when it is LOW, the body bias of n-MOSFET is switched to VSS and p-MOSFET switched to VDD. When the source-substrate junctions of both the transistors are reversed biased, the transmission gate is fully ''off''. In new DTMOS proposed switch shown in figure 1, gate to body voltage is controlled by a two more switches. If the gate and body directly tied with same voltage the threshold voltage will vary.

IV. FRONT PANEL FOR 12 LEAD ECG

Implementation of the front panel is done using two analog multiplexers. Test bench circuit of 12 lead ECG front panel design circuit shown in figure 2 and its internal circuits are shown in figure 3. Here, 12 to 1 analog multiplexer is designed using 12 DTMOS switches shown in figure 5. Inverting inputs are selected by the selection procedure called a decoder. Here, 4 to 12 decoder is intended for 12:1 analog multiplexer which is shown in figure 4. The non inverting inputs 7:1 analog multiplexer designed in with the same DTMOS switches and 3 to 7 decoder selection procedures are represented in figure 6. A selector circuit is implemented to process the selection inputs between the two multiplexers, among which one multiplexer needs three selection lines, and another multiplexer needs four selection lines [17]. To solve this problem, a selector circuit is designed by NAND gates which are shown in Figure 4.

The output of the decoder allows the switch to pass any one of the input signals. A decoder converts the n coded binary information in to 2^n unique outputs [19]. In 2^n outputs, if any output is at high state then the remaining outputs will be at low state [20]. In 12:1 Multiplexer, shown in Figure 5 have four selection inputs and are applied to the decoder and hence produce 12 unique outputs. These outputs act as control signals to the 12 different switches, allowing one switch to be in the ON-state, and the corresponding input of the switch is

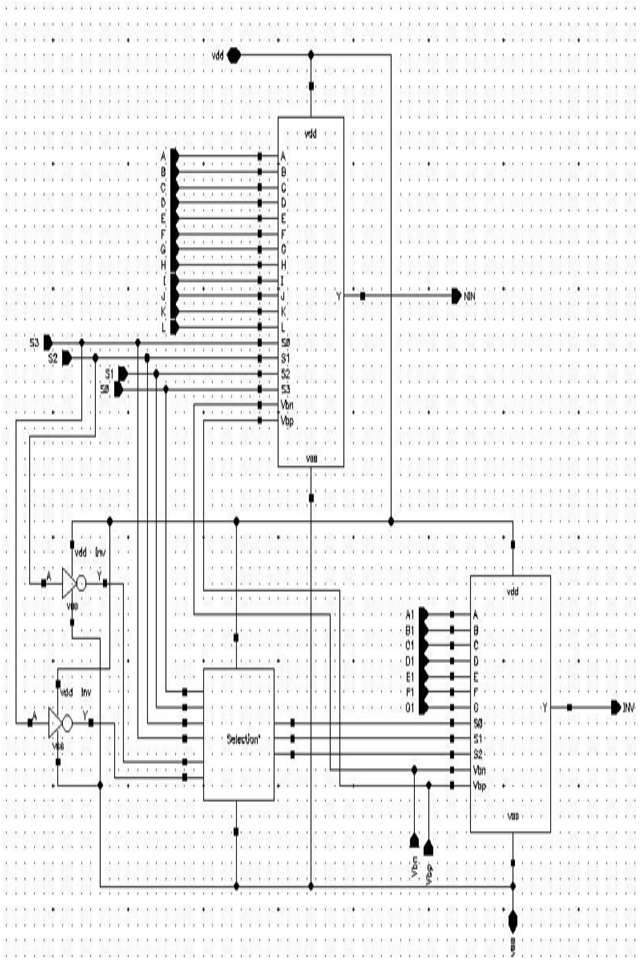

FIGURE 3. 12:1 and 7:1 Analog Multiplexers with selector block.

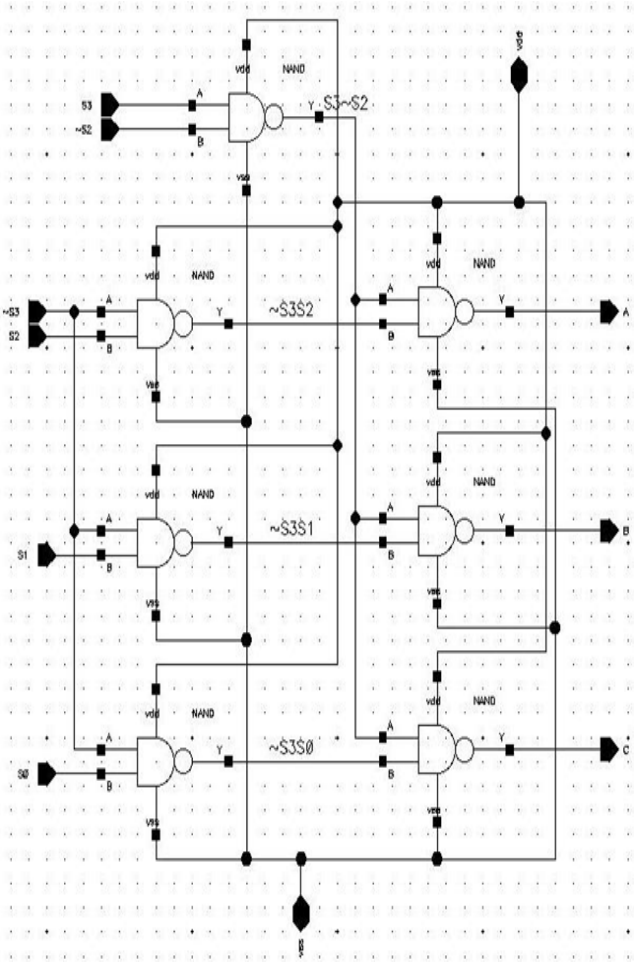

FIGURE 4. Selector circuit for selection lines.

collected by the output terminal [21], [22]. These outputs acts as control signals to the 12 different switches, allowing one switch to be in the ON-state and the corresponding input of the switch is collected by the output terminal.

Similarly 7:1 analog Multiplexer, for which three selection inputs are applied to the decoder, produce seven unique outputs is shown in figure 6.

V. RESULT AND ANALYSIS

From the proposed DTMOS analog switch, front panel design, 12:1 and 7:1 analog multiplexers, it is observed that the implemented architectures works with a power supply of ±0.2 V with a dynamic voltage range from 1uv to 200mv with the Power dissipation of 140 nW. The detailed result analysis with CMOS Analog switch response and output waveforms are represented in following figures 7, 8, 9.

Figure 7 depicts the wave form of Dynamic threshold MOSFET for 100HZ frequency. As shown in the figure, the waveforms of 12 lead ECG inverting and non inverting inputs are selected by multiplexers from the dynamic range of 1uV to 200mV.

Figure 8 represents the transient responses of signals with different voltages along with the time and also the waveforms of 12 lead ECG inverting and non inverting inputs are selected by multiplexers from the dynamic range of 1uV to 200mV.

The various dynamic voltage output signals for 12:1 and 7:1 multiplexers with various dynamic inputs are plotted in Figure 9. The detailed power and noise analysis of proposed architectures are explained as follows.

A. POWER ANALYSIS

Power dissipation of a circuit mainly depends on three parameters, load capacitor C_L, supply voltage V_{dd}, and switching frequency $f_{switching}$.

$$P = C_L V_{dd}^2 f_{switching} \tag{8}$$

From the equation 8, it is observed that, if switching frequency increases the power consumption also increases. Power analysis of the 12 lead ECG front panel at various frequencies is shown in Figure 10.

Figure 10 shows the power analysis for various frequencies like 1K, 10K, 100K, and 1M Hzs. In that the leakage power and static power are constant for all frequencies but

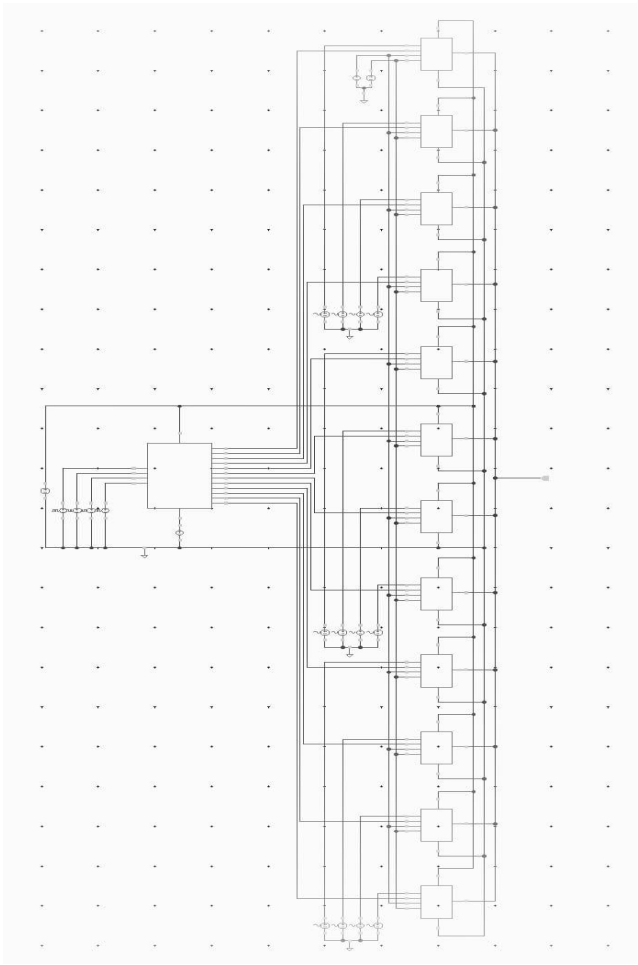

FIGURE 5. 12:1 Analog Multiplexer with 12 switches.

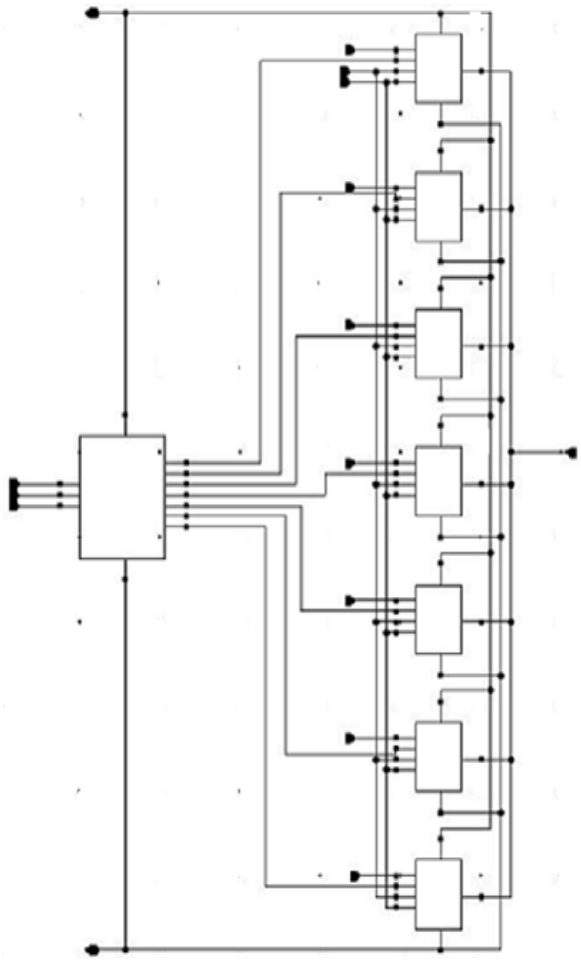

FIGURE 6. 7:1 Analog Multiplexer using 7 DTMOS switches.

dynamic power increases when frequency increases; hence, the total power dissipation increases. For 1M frequency, the dynamic power increased to 140uw with total power dissipation 310uW. The utilization of switches in various logics is depicted in Figure 11.

From the figure 11, it is observed that the proposed method produces the efficient results with less number of switches compared to the existing methods represented in [5], [18].

B. NOISE ANALYSIS

Electrical noise always affects the performance of the system, and it degrades the signal quality. In MOSFET, three types of noise are associated: thermal noise, flicker noise (fc) and shot noise. The shot noise is neglected in reverse body bias because the number of carriers that are crossing the P-N junction and source substrate are tiny. The noise analysis graph is shown in Figure 12.

In Figure 12, the CMOS analog front panel output noise is plotted between the frequency and voltage noise. From this we can observe that the voltage noise is reverse proportional to the input frequency and the flicker noise at corner with frequency 6 kHz is equal to 13.3145nV/$\sqrt{HZ}$.

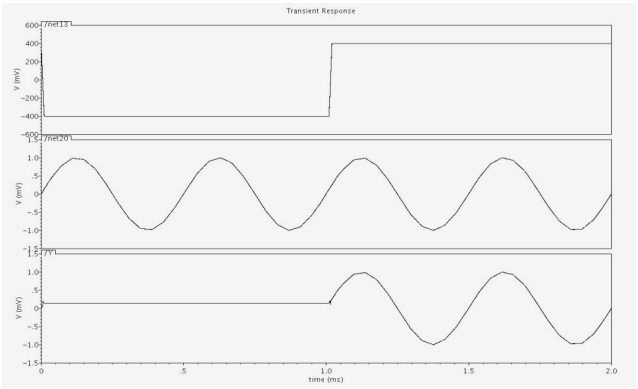

FIGURE 7. CMOS Analog switch response.

C. PVT CORNER ANALYSIS

PVT means the Process, Voltage and Temperature. In order to make the proposed chip to work after the fabrication in all the possible conditions, we pretend it at different corners of process, Voltage and Temperature. These conditions are called corners. Process corner represented by two letters where first letter shows N-channel MOSFET and second one

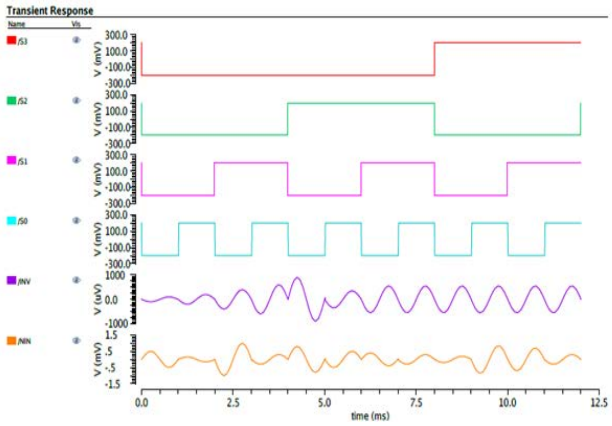

FIGURE 8. Output waveforms of front panel circuit.

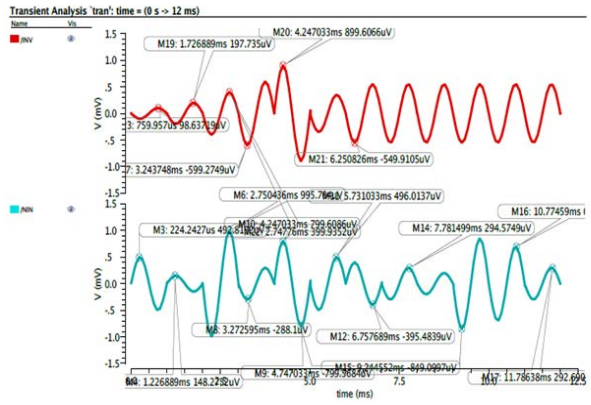

FIGURE 9. Output wave forms of 12:1 and 7:1 Multiplexers for various dynamic inputs.

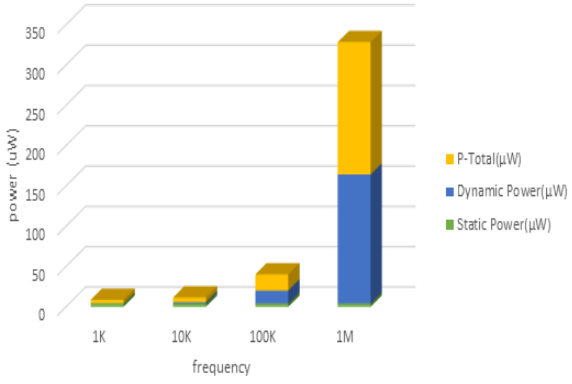

FIGURE 10. Switching frequency Vs Power dissipation.

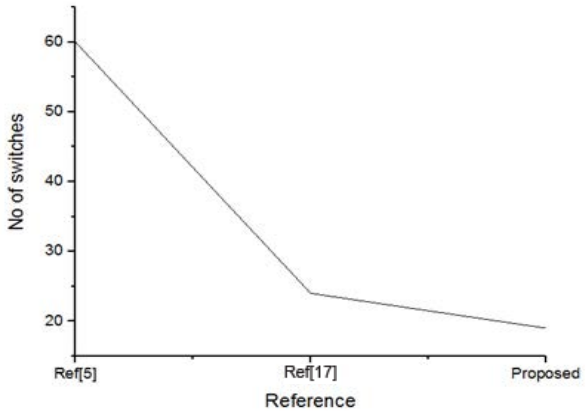

FIGURE 11. Number of switches utilization.

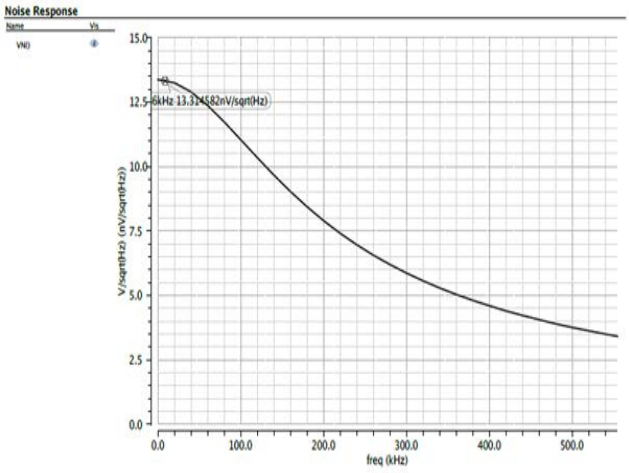

FIGURE 12. Noise analysis for front panel design.

TABLE 2. Corner analysis of DTMOS Analog front panel at input voltage of 1mV.

	FF		
VDD	$-40°C$	$27°C$	$125°C$
0.3V	975mv	989mv	979mv
0.35V	973mv	990mv	980mv
0.4V	973mv	988mv	979mv

TABLE 3. Corner analysis of DTMOS Analog front panel at input voltage of 1mV.

	SS		
VDD	$-40°C$	$27°C$	$125°C$
0.3V	981mv	998mv	995mv
0.35V	981mv	995mv	995mv
0.4V	980mv	996mv	993mv

represent P-channel MOSFET. Here we have total 5 corners those are SS(slow slow), FF (Fast Fast), TT(Typical Typical), SF(Slow Fast), FS(Fast Slow). Example SS means slow N- channel MOSFET and slow P-channel MOSFET. Here we considered SS, FF and TT. These three corners are called even corners because the N and P channel transistors behaves evenly. All these three parameters directly affect the detention of the cell.The Corner analysis of DTMOS Analog front panel at input voltage 1mv is shown in table 2,3,4.

From the tables 2, 3, 4 it has been observed that there is no drastic change in input voltage at various supply voltages and temperatures. From the corner analysis, it is observed that the power consumption and number of switches used

TABLE 4. Corner analysis of DTMOS Analog front panel at input voltage of 1mV.

	TT		
VDD	-40^oC	27^oC	125^oC
0.3V	960mv	965mv	928mv
0.35V	964mv	966mv	927mv
0.4V	962mv	965mv	926mv

are reduced with the proposed CMOS 12 lead ECG data acquisition circuit with improved DTMOS based analog multiplexers. It also gives the efficient results compare to existing architectures [5], [8], [18].

VI. CONCLUSION

This paper presents the implementation of 12 lead ECG front panel with 90 nm CMOS technology. To implement this **CADENCE virtuso tool** has been used. Here 12:1 and 7:1 analog multiplexers are designed to optimize the circuit. Compare to transmission gate logic, the proposed logic consumes less power and uses less number of switches. Dynamic threshold MOSFET is more affected in threshold voltage and leads to reduced supply voltage and circuit operation with a low voltage of 0.2V. With the effect of this, the Power dissipation for the circuit is achieved for 140 nW. The proposed method gives an efficient solution for many biomedical signal acquisition systems.

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