Fully-Integrated Timers for Ultra-Low-Power Internet-of-Things Nodes—Fundamentals and Design Techniques

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ABSTRACT Driven by the momentum toward compact and low-power Internet-of-Things (IoT) systems, the research on fully-integrated and energy-efficient kHz-to-MHz timers increased explosively. This article examines recent publications on timers and classifies them into two major categories: open-loop-based and close-loop-based timers. Upon introducing the basic parameters for characterizing a timer, we perform an extensive investigation to gain insights into recent state-of-the-art works. We also discuss in detail the comparison between the two classes of timers. With the aid of the state-of-the-art, we present a comprehensive review from multiple perspectives, such as *Energy Efficiency*, *Temperature Coefficient*, *Temperature Range, Figure-of-Merit*, etc.

I. INTRODUCTION

Compact wireless systems experienced massive growth in emerging microsystems that benefit many applications, such as healthcare monitoring, environmental investigation, and smart sensors [1], [2]. Lifetime and power consumptions constraints of the different blocks within the System-on-Chip (SoC) solution are the major bottlenecks to further promote the deployment of wireless systems [3]. The well-known duty-cycling technique minimizes the power consumption of the power-hungry radio. Allowing the system to alternate between sleep and active mode periodically, significantly reduces the total power consumption. Therefore, an accurate timer to precisely wake up the radio is compulsory. As there is no synchronization between the radio and the master device in the idle state, the frequency accuracy of the timer amid

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environmental variations (e.g., supply voltage and temperature variation) is decisive. Also, since the timer is always-on, it must operate at ultra-low power (sub-μW) while maintaining performance accuracy [4], [5].

Crystal oscillator is the *de facto* standard for the kHz-to-MHz range timer due to its excellent frequency accuracy and reliable performance [6]–[8]. Yet, the bulky off-chip crystal (e.g., 3.2×2.5 mm^2) contradicts the integration of compact system design, especially in Internet of Things (IoT) applications [9]. Although we can fully integrate the LC-tank-based timer, the on-chip inductor limits its application toward high operating frequency due to a size constraint [10]. Alternatively, fully-integrated RC timers that can generate clock signals with moderate frequency accuracy with low-power consumption exhibit potential in replacing the bulky crystal oscillator [1]–[3], [6], [11]–[14]. With the resistors and capacitors handily integrated on-chip, it favors hardware miniaturization for the IoT device.
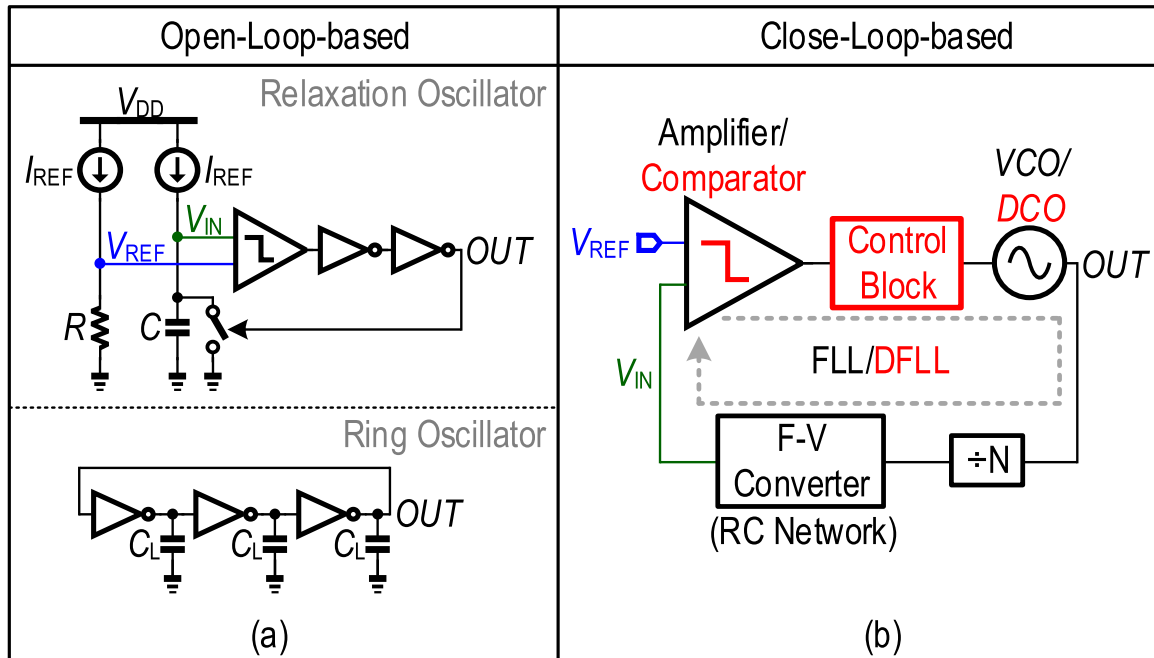
FIGURE 1. General view of timer: (a) open-loop-based. (b) close-loop-based.
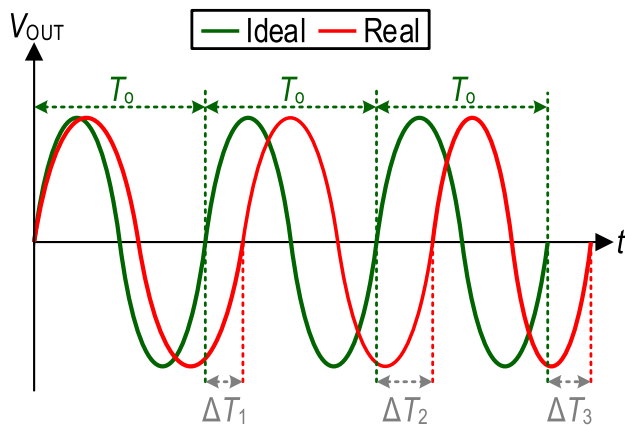
FIGURE 2. Sinusoidal waveform of Ideal vs Real.

FIGURE 3. Frequency spectrum of Ideal (left) vs Real (right) oscillator [18].

(i.e. resistor, capacitor, voltage reference, etc.). Yet, Process, Voltage, and Temperature (PVT) variation influence the frequency stability of the oscillator. For instance, considering the relaxation oscillator illustrated in Fig. 1(a), ideally, the output signal OUT ought to toggle once $V_{IN} > V_{REF}$. Yet, the delay of the comparator and the logic gates contributes in prolonging the clock period. In addition, as the delay changes amid PVT variation, it aggravates the frequency stability of the timer.

This article reviews the fundamentals of designing the fully-integrated timers as wakeup timer for ULP IoT nodes, particularly in a CMOS process. Section II introduces the essential parameters to characterize the timer. Section III describes a review of recent architectures based on two types of design topology: open-loop-based and close-loop-based timers. Section IV compares the design of open-loop-based and close-loop-based timers from different perspectives, performance summary and tradeoffs with recently reported publications. Section V concludes this review.
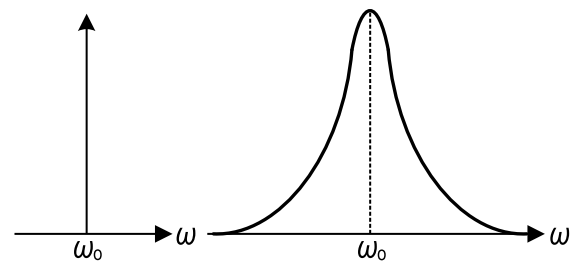
We can classify the architecture of the fully-integrated timer into two major types: open-loop-based (e.g., relaxation oscillator and ring oscillator) and close-loop-based timer (e.g., frequency-locked loop, FLL), as depicted in Fig. 1. Relaxation oscillator (RxO) is preferred for a kHz-to-MHz range timer, whereas the ring oscillator is usually designed for higher frequency application [15]–[17]. For an open-loop-based timer, the oscillator operates in a free-running mode. The closed-loop-based timer also consists of an oscillator to generate the oscillation signals, however, it has its frequency locked by another timing element (e.g., RC-network in the FLL). Theoretically, the periods of the oscillations for both type of timers solely depend on the desired circuit elements
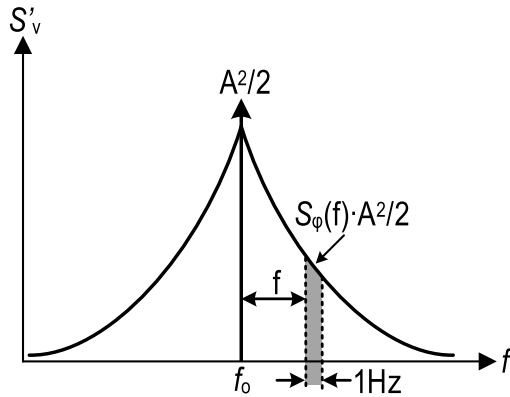
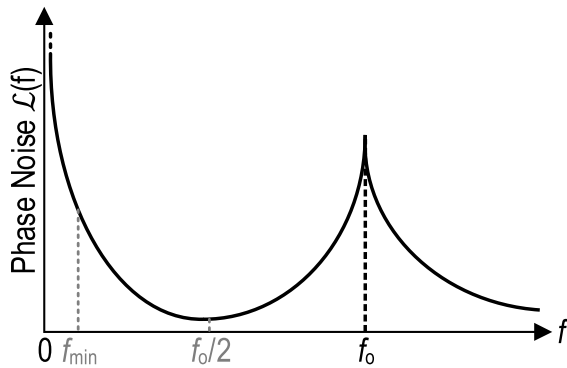**FIGURE 4.** Relation between voltage spectrum and PSD of timer [19].

FIGURE 5. Phase noise integration limit [19].

II. ESSENTIAL PARAMETERS OF TIMERS

It is crucial to discuss the parameters to characterize the performance of the timer. In this section, several common performance parameters in benchmarking the timers are elaborated.

A. JITTER AND PHASE NOISE

The goal of a timer is to generate a stable reference timing. Ideally, the timer provides the oscillating signals with identical periods in every cycle. Due to the presence of noise from the circuits, the period deviates from its ideal value. As shown in Fig. 2, the signal's period exhibits a perturbation every cycle (ΔT_1, ΔT_2, ΔT_3, etc.). This perturbation is known as *absolute jitter*, which is the difference between the ideal period and the measured period of a clock cycle. Practically, it is improbable to obtain the ideal period as it is unknown. As such, the parameter *Period jitter* can be utilized, which portrays the difference in the measured period of a clock cycle and the average period of multiple clock cycles. The period jitter can be characterized by root-mean-square or peak-to-peak value to manifest the clock's performance.

On the other hand, the clock's jitter incurs phase diffusion to the signal. Hence, the spectrum of the clock spreads around ω_o, as shown in Fig. 3 [18]. Such perturbation is known as *phase noise*. To understand phase noise, we must observe the Power Spectral Density (PSD) of the timer around the oscillating frequency (f_o) (Fig. 4). Interestingly, the PSD of
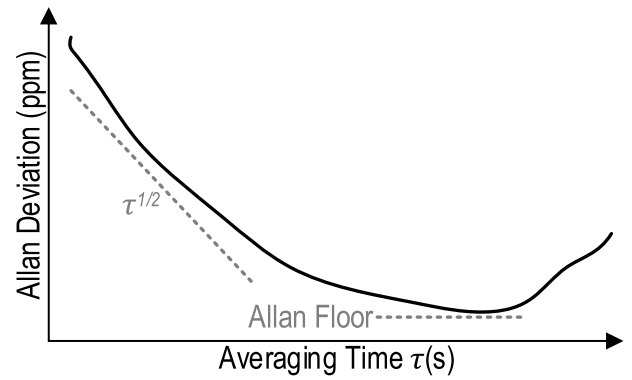

FIGURE 6. Common form of Allan deviation.

the timer correlates to the PSD of the jitter. The PSD of jitter can be determined as [19]

$$S_\varphi\left(f\right) = \frac{S'_v\left(f_o + f\right)}{A^2/2}, \tag{1}$$

where f is the offset from f_o. With (1), we can obtain the phase noise of the timer

$$\mathcal{L}\left(f\right) = \frac{1}{n^2} \cdot \frac{S'_v\left(nf_o + f\right) \text{ in } 1Hz \text{ bandwidth}}{\text{Power of } n^{th} \text{ harmonic}}, \tag{2}$$

where n is the number of harmonics. The relationship between the RMS absolute jitter and the phase noise is expressed as

$$\sigma_a = \sqrt{\frac{2}{\omega_o^2} \int_{f_{min}}^{f_o/2} \mathcal{L}\left(f\right) df}, \tag{3}$$

where σ_a is the RMS absolute jitter. Note that the upper limit of the integration is $f_o/2$ to prevent double count of the phase noise around the 2nd harmonic, whereas the lower limit f_{min} is usually determined by the observation time (Fig. 5).

B. ALLAN DEVIATION

For duty-cycling purposes, the timer is turned on for a relatively long period. The timer output will be counted continuously. Hence, the period jitter of each individual cycle is averaged out and it is inadequate to show the performance of the timer over an extended integration time. In this regard, the *Allan deviation*, which measures the long-term stability of the oscillator, is a more appropriate indicator. The Allan deviation characterizes the frequency stability of the oscillator over a timespan of τ. It depicts the expected timing deviation between two subsequent sleeping periods of the duration τ [20].

To understand Allan deviation, we must first define $y(t)$ as a normalized, fractional frequency of the timer from the nominal frequency f_o. It can be expressed as [21]

$$y\left(t\right) = \frac{f\left(t\right) - f_o}{f_o} = \frac{1}{2\pi f_o} \frac{d\varphi\left(t\right)}{dt}, \tag{4}$$

where $f(t)$ is the oscillating frequency at time t and $\varphi(t)$ is the instantaneous phase fluctuation. From [22], the

Allan variance is determined as

$$\sigma_y^2(\tau) = \frac{1}{2(M-1)} \sum_{i=1}^{M-1} [\bar{y}_{i+1} - \bar{y}_i]^2, \qquad (5)$$

where M is the number of frequency measurements of a sampling time τ_o and $\bar{y}_i$ is the ith of M fractional frequency values averaged over τ. The mathematical equation for $\bar{y}_i$ can be determined as

$$\bar{y}_i(\tau) = \frac{1}{\tau} \int_{t_i}^{t_i+\tau} y(t) \, dt. \qquad (6)$$

Note that, τ_o is the data sampling or measurement interval for the timer, while τ (also known as observation interval) is the analysis or average time taken for the measurement and is commonly expressed as a multiple of τ_o ($\tau = n\tau_o$, where n is the averaging factor). Finally, the definition of Allan deviation is expressed as the square root of Allan variance $\sigma_y(\tau) = \sqrt{\sigma_y^2(\tau)}$.

Fig. 6 exemplifies the typical profile of Allan deviation of a timer. For a short gating time, the Allan deviation decreases at a rate of $\sqrt{\tau}$ as the period jitter is averaged out. Subsequently, the Allan deviation will reach a minimum due to the presence of the $1/f$-noise. As the power of the $1/f$-noise increases with decreasing frequency, extending τ ceases to improve the Allan deviation. This lower bound is called Allan noise floor. If we keep increasing τ, the Allan deviation increases due to temperature and environmental effects as part of the drift process [13].

C. FREQUENCY DEVIATION

Apart from the noise, the oscillator's frequency is also affected by the PVT-variation. While the process variation can be trimmed and calibrated after fabrication, the variations due to voltage and temperature exist throughout the operation.

The perturbation in the supply voltage affects the frequency stability of the timer. For instance, for the circuit in Fig. 1(a), ideally, the output will be flipped once $V_{\text{IN}} > V_{\text{REF}}$. Section I highlights that the delay from the comparators and logic gates extends the periods. Normally, the delay of the logic gates is inversely proportional to its supply voltage. Hence, the frequency of the timer tends to shift with the supply voltage. The frequency deviation caused by the voltage variation is characterized as *line sensitivity*, which is defined as the fraction of frequency variation per volt.

Similarly, the frequency of the timer deviates amid temperature variations [23]. Primarily, the deviation is due to the temperature dependence of resistors and transistors. Consider the circuit in Fig. 1(a) again, where the resistance R changes with temperature. Hence, even with an ideal I_{REF}, $V_{\text{REF}} = R \cdot I_{\text{REF}}$ drifts, thereby affecting the frequency accuracy. The frequency deviation caused by temperature variation is characterized as *temperature coefficient (TC)*, which depicts the ratio of fractional change in frequency to the temperature range. Usually, the *TC* is reported in the unit of part per million per degree Celsius, or ppm/°C.

D. FIGURE-OF-MERIT (FoM)

Figure-of-Merit (*FoM*) is a numerical indicator for any system to express its performance and efficiency. There are several *FoM* for timer benchmarking. One of the most commonly used *FoM* in regards to the phase noise and power consumption is expressed as [24]:

$$FoM_1 = \left| \mathcal{L}(f) + 20log\left(\frac{\Delta f}{f_0}\right) + 10log\left(\frac{P}{1mW}\right) \right|, \qquad (7)$$

where Δf is the offset frequency and P is power consumption. However, FoM_1 does not consider the timer's stability within the operating temperature range. Hence, an alternative *FoM* is proposed as [12]

$$FoM_2 = 10\log\left(\frac{f_0 \cdot T_{range}}{P \cdot TC}\right), \qquad (8)$$

where T_{range} is the temperature range of the timer. FoM_2 considers the tradeoff between frequency, temperature, power, and *TC* and subsequently expresses the performance in numerical value. Another indicator that is commonly used is the *energy efficiency* of the timer, which is expressed as

$$Energy \; Efficiency = \frac{P}{f_0} \qquad (9)$$

As the dynamic power of circuits generally is proportionate to its operating frequency, the energy efficiency is a simple yet powerful indicator to depict the energy consumption of the timer in each cycle, which perfectly suits the performance evaluation for low-frequency oscillators [9].

III. RECENT STATE-OF-THE-ART TIMERS

In this section, a review of recent state-of-the-art timers is provided. Based on the architecture, we can generally classify the timer into open-loop-based and close-loop-based timers. For an open-loop-based timer, the oscillating signal is generated by a free-running oscillator. For instance, consider a relaxation oscillator, the output signal is generated by alternately (dis-)charging the capacitor. Although there might be certain error compensation components to ameliorate the frequency accuracy [25], the frequency of the oscillator's output merely depends on its timing element. Here, we shall stress that although we used the term open-loop, the core oscillator itself (i.e. relaxation oscillator and ring oscillator) is still constructed in a loop. The term open-loop only refers to whether an auxiliary loop regulates the oscillator's output frequency.

Alternatively, for the closed-loop-based timer, a voltage-controlled oscillator (VCO) is integrated within a feedback loop. The output of the VCO is fed to a frequency-to-voltage (F-V) converter (e.g., RC network), which senses the output frequency and converts it to a voltage signal. Then, an amplifier/comparator compares this voltage to a reference voltage signal and provides a corresponding output. After filtering out the out-of-band noise by a low-pass filter, the output signal is fed to the VCO to tune its frequency. Provided that the loop gain is sufficient, the output frequency will only
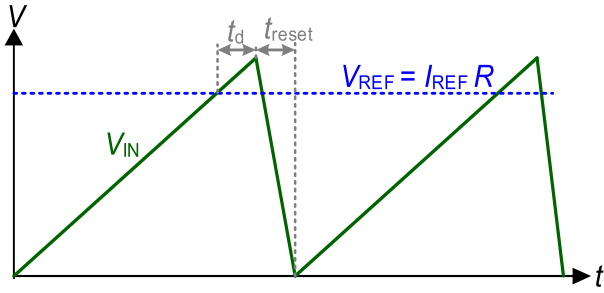
FIGURE 7. General RxO waveform.

be affected by the reference voltage signal and the conversion gain of the F-V converter. If the VCO's output frequency deviates amid VT-variations, the F-V converter tracks this deviation via the loop and makes an appropriate adjustment. As such, the frequency of the timer is being "locked" and kept constant.

In terms of architecture, the closed-loop-based timer has a more complicated pattern than the open-loop-based counterpart as it is constructed with a continuous feedback path using multiple blocks. Comparatively, the design process of the open-loop-based timer is much more straightforward. In the subsequent subsections, we will elaborate on the recent open-loop-based and close-loop-based timers respective to their performance parameters.

A. OPEN-LOOP-BASED TIMERS

The open-loop-based timer is primarily implemented using a free-running oscillator acting as a frequency generator. Fig. 1 shows the general architecture of the RxO [26], [27]. Two matched current source are utilized; one injects the current into a resistor to generate a reference voltage $V_{REF} = I_{REF}R$, and the other charges/discharges the capacitor. The voltage on the capacitor (V_{IN}) is compared with V_{REF} through a comparator. Initially, the capacitor is reset to the ground. Then, it is charged by I_{REF}, where V_{IN} can be formulated as $I_{REF}t/C$, assuming I_{REF} is constant with time. Once $V_{IN} > V_{REF}$, the output of the comparator changes, and a reset signal will be sent out and discharges the capacitor [11]. The process iterates for every cycle. The ideal period of the timer is thus RC. Ideally, the capacitor starts to discharge once $V_{IN} > V_{REF}$, and the discharge process will be completed instantly. Yet, the actual period is affected by the delay of the comparator and logic gates and thus subjected to PVT variations [28]–[31]. Such waveform is depicted in Fig. 7, where there is an additional delay of t_d (comparator delay, buffer delay, etc.) and t_{reset} (capacitor discharging time) in a cycle on top of the desired capacitor charging time. To minimize t_d, a high-speed comparator is required, which implies high power consumption and contradicts to low power design preference for IoT devices.

To eliminate unnecessary discharging time of the capacitor, an improvised architecture using two sets of charging capacitors with respective comparators has been implemented [32]–[34]. This RxO has an additional capacitor path
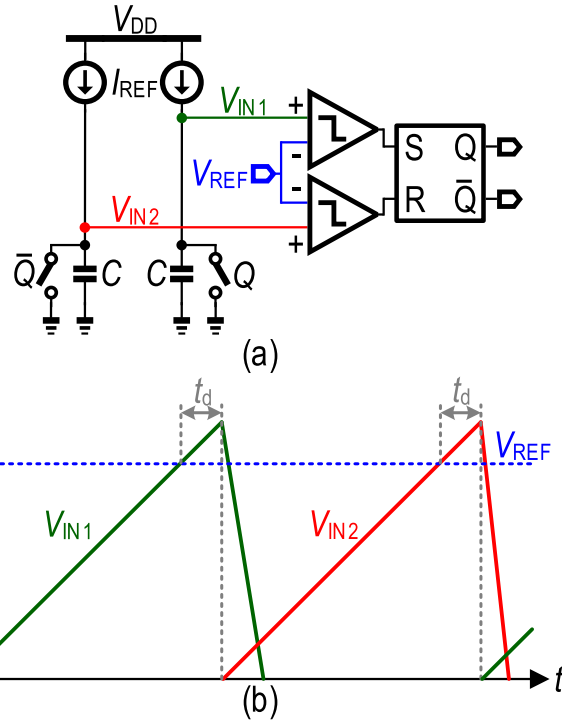

FIGURE 8. Dual comparator RxO (a) schematic and (b) waveform.

for charging/discharging process and comparator to compare V_{REF} and $V_{IN1(2)}$ [Fig. 8(a)]. Although the charging/discharging processes are the same, this architecture eliminates t_{reset} by alternating the charging process between two capacitors [Fig. 8(b)]. Hence, this RxO has higher immunity against PVT variations since fewer components contribute to the cycle period, thereby improving the frequency stability.

As aforementioned, the thermal noise and *1/f*-noise induce jitter on the timers. For the RxO, by using "first-crossing approximation," the jitter due to thermal noise can be determined as [24]

$$\sigma_{\Delta T}^2 \propto \frac{\sigma_{V_n}^2}{slope_{V_{IN}}^2}, \tag{10}$$

where $\sigma_{V_n}^2$ is the noise variance referred to the input of the comparator and $slope_{V_{IN}}^2$ is the slope of V_{IN} in proximity to the threshold. To improve the jitter performance, we can either minimize $\sigma_{V_n}^2$ or maximize $slope_{V_{IN}}^2$. The former implies that a low-noise comparator must be used. In maximizing $slope_{V_{IN}}^2$, a higher I_{REF} and V_{REF} are required provided that the oscillation period is unchanged. Both approaches increase the power consumption and impose a tradeoff between jitter and power.
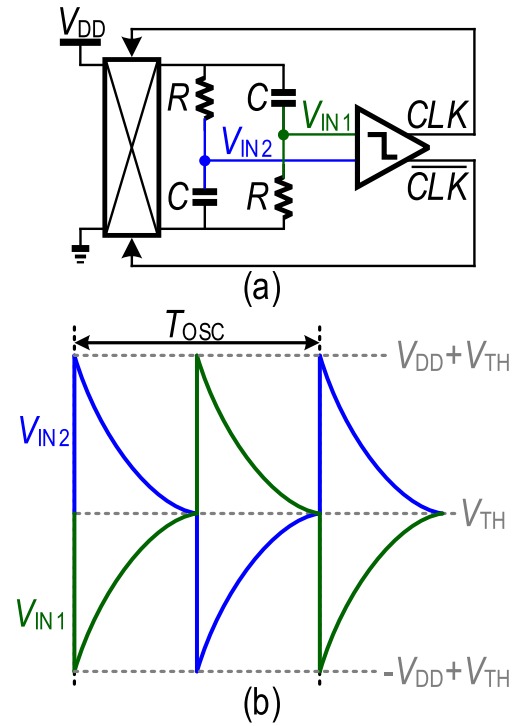
1) SWING-BOOSTING

Swing-boosting technique proves effective in improving the jitter performance of the RxO. Several works adopting swing-boosting RC networks have been reported in the literature in the past few years [12], [24], [35]–[37]. Zhou *et al.* [35]
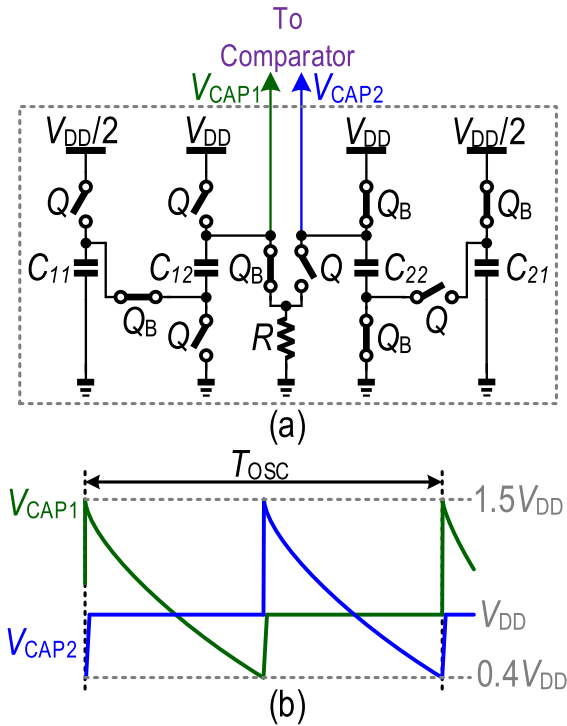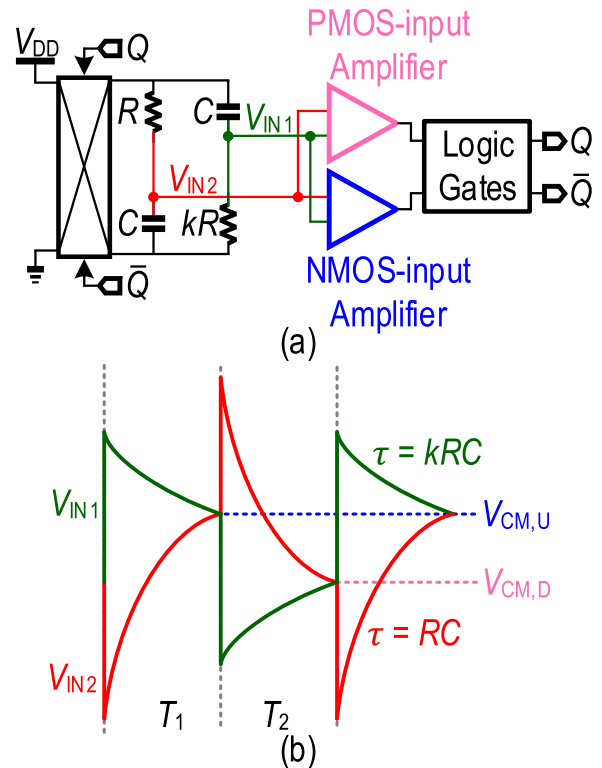
FIGURE 9. (a) Switch-capacitor swing boosting RC network and (b) waveform [35].

FIGURE 10. (a) Symmetrical swing-boosted RxO and (b) waveform [21].

introduced a swing-boosting capacitor charging/discharging method that allows the capacitor voltage swing to exceed V_{DD}. The RC network is shown in Fig. 9(a), while its corresponding waveform is shown in Fig. 9(b). It is assumed an initial condition for all switches Q are open, while all switches Q_B are closed. C_{22} and C_{21} are disconnected and charged to V_{DD} and $0.5\,V_{DD}$, respectively. Concurrently, C_{11} and C_{12}, which are initially charged to $0.5\,V_{DD}$ and V_{DD} respectively, are connected in series and start to discharge from $1.5\,V_{DD}$ (explained below) to the ground via R. Once V_{CAP1} drops below V_{REF}, the output switches to the next half-cycle, where all switches are flipped. As the charges stored in C_{21} and C_{22} are conserved and the bottom plate of C_{22} is connected to C_{21}, which was previously charged to $0.5\,V_{DD}$, V_{CAP2} is boosted to $1.5\,V_{DD}$ and discharges to the ground via R. Meanwhile, C_{11} and C_{12} will be charged to $0.5\,V_{DD}$ and V_{DD} respectively. The operation repeats itself after another cycle. As the swings at the capacitors increases to $1.1\,V_{DD}$, the jitter of the RxO can be improved [38]. This improvement inevitably comes at the penalty of higher capacitor count and larger chip area, incurring higher manufacturing cost.

With the same initiative, Lee et al. [24] proposed the differential swing-boosting technique with fewer component counts and a higher boosting range. The proposed RxO is shown in Fig. 10(a), where Fig. 10(b) displays the corresponding waveform. As opposed to [35], the bottom plates of the capacitors alternate between V_{DD} and ground in different phases of the cycles by the chopper, while the top plates are connected to the input of the comparator. With the

FIGURE 11. (a) Asymmetrical swing-boosted RC network and (b) waveform [12].

differential operation, the peak-to-peak swing across the comparator increases to $2\,V_{DD}$, further improving the jitter of the RxO. Benefitting from the differential operation, this

architecture avoids the voltage reference, which is subjected to VT-variation. It scores a jitter performance of 9.86 ps$_{rms}$ (0.01% of its period). The large swing is achieved at the expense of high power consumption. In addition, as the voltage swing is higher than V_{DD} at the input of the comparator, it may cause long-term reliability issues to the transistors, particularly for advanced deep-submicron process with breakdown voltage <1 V.

The V_{DD} of the RxO could be reduced to pursue ultra-low-power operation. Lei *et al.* introduced an ultra-low-voltage RxO with an asymmetric swing-boosted RC network (Fig. 11) [12]. It operates with sub-0.5V supply voltage to be compatible with the low output voltage of energy harvesters [39], [40] while maintaining the overall performance. The proposed work has a similar architecture to [24], except that the resistance in two RC branches of the RC-network are unequal. This arrangement leads to different charging/discharging rates of the capacitor. As such, the common-mode voltages where V_{IN1} crosses V_{IN2} alternate between $V_{CM,U}$ and $V_{CM,D}$ instead of 0.5 V_{DD} as in [24]. It eases the low-voltage operation since $V_{CM,U}$ and $V_{CM,D}$ can be maneuvered to fit the operation of the subsequent dual-path comparator (NMOS-input and PMOS-input). It achieves the state-of-the-art energy efficiency of 667 fJ/cycle and FoM_2 of 181 dB.

2) TEMPERATURE-DEVIATION COMPENSATION

Various compensation methods have been reported to alleviate the frequency deviation of the RxO due to temperature variation [12], [13], [41]–[44]. The techniques can be mainly characterized into two groups. The first is to compensate through the resistors of the RC network. By adapting series resistors with positive and negative TC (e.g., silicide/non-silicide poly and diffusion resistor), a composite resistor with specific TC can be obtained and providing first-order TC compensation [13], [41], [42], [45]. As the delay from the comparator and logic gates is also temperature-sensitive, a non-zero TC of the resistor can be utilized to nullify the overall TC [43].

The second compensation method is active tracking of the delay by the comparator and logic gates. For instance, a delay generator is introduced in [12] to track and compensate for the delay by modifying the time constant of the RC-network. The delay generator is biased with the same current as the comparators. If the bias current decreases (e.g., temperature decreases), the delay increases, so the width from the output of the delay generator also increases. At the same time, the time constant of the RC-network is halved to compensate for this delay. A replica of the comparator and logic gates can also be used to track the delay, as proposed in [44]. It replicates the main branch to measure the delay and compensate for it by halving the time constant at the same time.

3) DESIGN CONSIDERATION

For designers, it is important to determine the design priority based on different applications, as most parameters exhibit
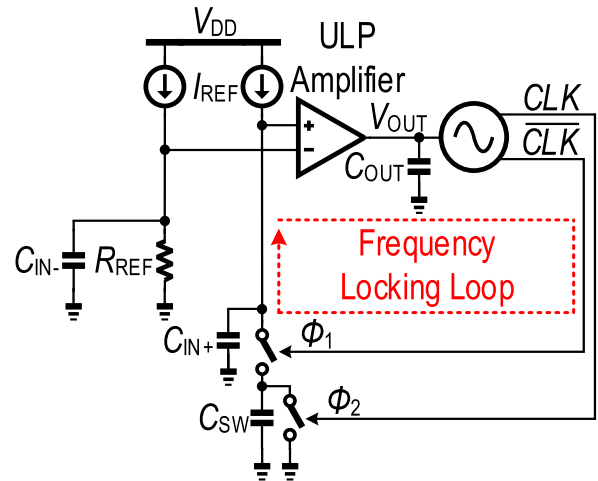

FIGURE 12. Resistive frequency locked oscillator [11].

tradeoff in performance. With the same FoM, reducing the power would result in an increase in phase noise (7) and temperature coefficient TC (8). One of the persistent goals of the research on IoT timer is to reduce the power consumption. This can be realised by minimizing either the supply voltage V_{DD} or total current consumption [46]. For such ultra-low-voltage applications, swing-boosting technique proves to be a promising solution [12]. Apart from reducing the power consumption by achieving state-of-the-art energy efficiency, the work also exhibits a promising frequency stability against PVT variation. A total current reduction can be realised by implementing duty-cycled dynamic components that only turn on when required. The toggling is achieved through the use of logic gates. In comparing [12] and [43], both works achieve ultra-low-voltage supply compatibility of 0.35 V and 0.4 V, respectively. The work [12] implemented a dual-path comparator to suit the low voltage operation, while [43] adopted a two-stage comparator with the first stage reusing part of the reference circuits and the second stage is heavily duty-cycled with sub-threshold operation.

Note that, by reducing the supply voltage, usually it comes with a tradeoff with other parameters such as jitter performance. As referred to (10), the input noise of the comparator is inversely proportional to the voltage swing slope. With reduced V_{DD}, the allowable voltage swing would reduce and exhibits a lower slope, resulting in an increment in noise. For instance, with an identical swing boosted technique, [12] achieved the lowest voltage supply and an outstanding energy efficiency with a penalty in jitter performance of 800 ps$_{rms}$, while [24] exhibits jitter performance of 9.86 ps$_{rms}$ using $4\times$ higher supply voltage, with $31\times$ larger energy per cycle. The designers are recommended to modify the components accordingly based on their design constraints.

B. CLOSE-LOOP-BASED TIMERS

In a basic RxO, one cycle period contains multiple uncertain delays, mainly due to dynamic comparator, buffers and
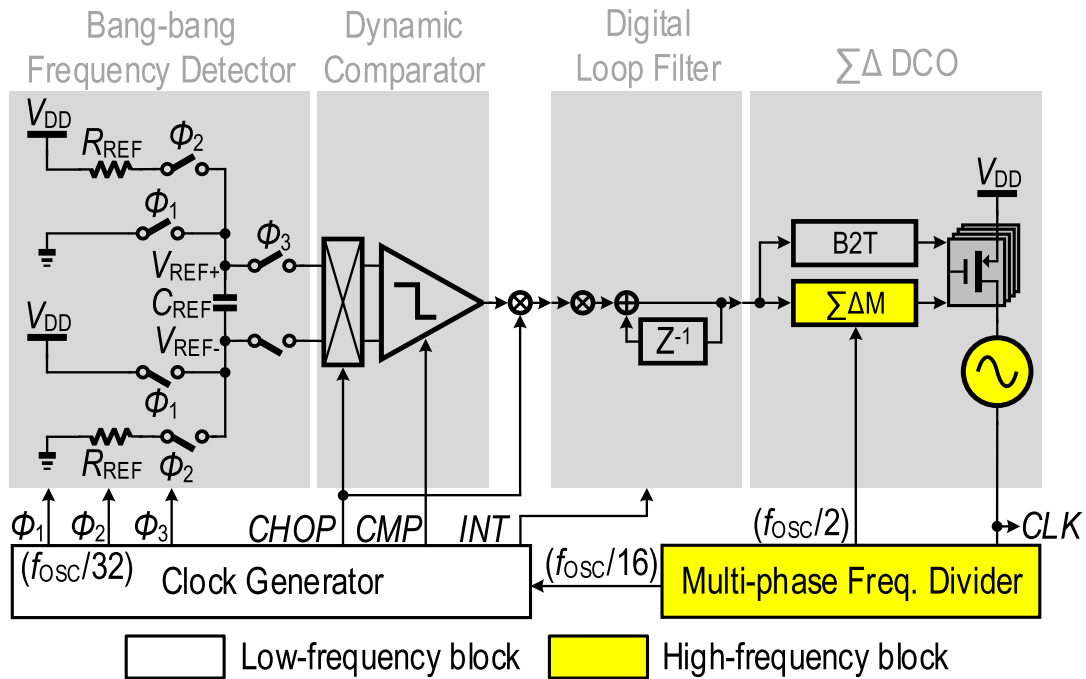
FIGURE 13. DFLL wakeup timer [53].

charging reset. Few techniques have been reported to increase the frequency stability by delay elimination methods [12], [13], [41]–[44], [47]. Alternatively, close-loop-based timer such as FLL, has better immunity against the VT-variations of the system. In principle, the output frequency of the FLL is only governed by the timing element such as the RC-network and the VCO is only used to provide an oscillation signals, which the frequency is locked by the loop [48]. The basic structure is shown in Fig. 1(b).

In contrast to RxO, FLL is constructed with multiple components connected in a feedback loop. Although different methodologies have been developed based on design priorities, the FLL share similar architecture as described in [49]. The output of the VCO is fed into an optional frequency divider. The purpose of this frequency divider is to step down the frequency and reduce the operating speed of other blocks and thus the power consumption [50], [51]. Another compulsory component block for FLL is the Frequency-to-Voltage (F-V) Converter or Frequency Detector (FD), which is implemented through RC network. The F-V converter should be resilient against PVT deviation and provide a stable frequency reference point to the FLL for locking purpose. A comparator/amplifier will then be used to detect and correct the frequency shifting.

1) POWER REDUCTION TECHNIQUES

In RxO, the dynamic comparator contributes most of the delay, hence affecting the frequency performance of the timer as it is sensitive to temperature and supply [52]. In order the reduce its delay, the power consumption must be increased,
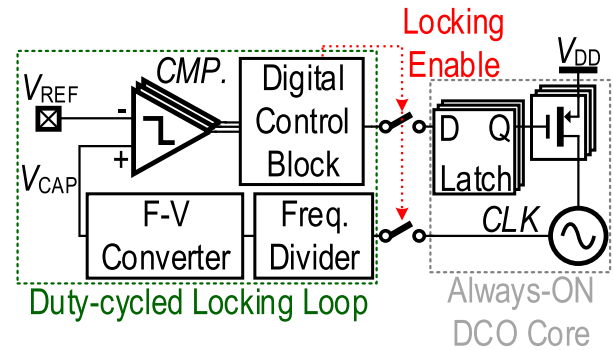


FIGURE 14. Duty-cycled digital FLL [50].

thereby burdening the power budget. In this regard, the work [11] adopts the FLL structure and uses a low power amplifier for signal comparison (Fig. 12). By using FLL, frequency stabilityimproves due to the feedback and lock mechanism. Together with the low power amplifier, not only the total dynamic power is reduced significantly, the FLL structure also shows superior long-term stability compared to the open-loop-based timer [11].

Following the FLL architecture, Ding et al. [53] proposed a digital-intensive FLL that exploits the advantage of advance CMOS technology nodes. It allows the implementation of a low area, low power, and low supply voltage timer (Fig. 13). In this topology, the signal generated by the digitally-controlled oscillator CLK is fed into multi-phase divider, which steps down the frequency from f_{osc} to $f_{osc}/16$. The step-down frequency is then sent to the non-overlap clock generator to distribute the corresponding signals into
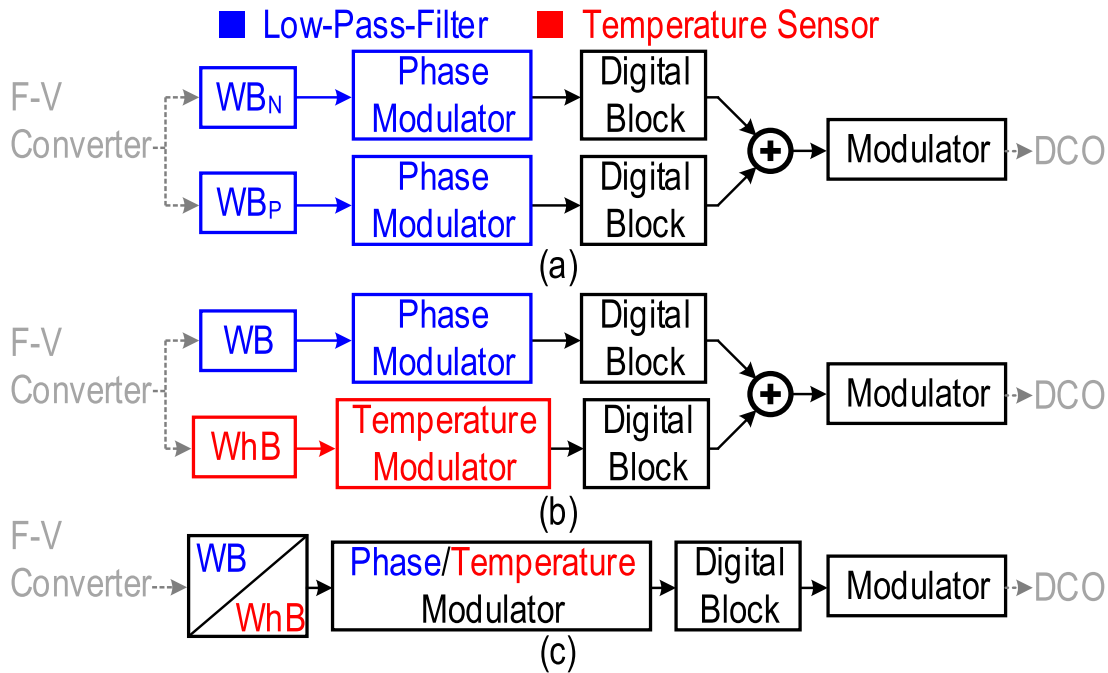
FIGURE 15. Block diagram of frequency references (a) using 2 LPF [54], (b) using 1 LPF and 1 Temeperature sensor [55] and (c) combined LPF and Temperature sensor [56].
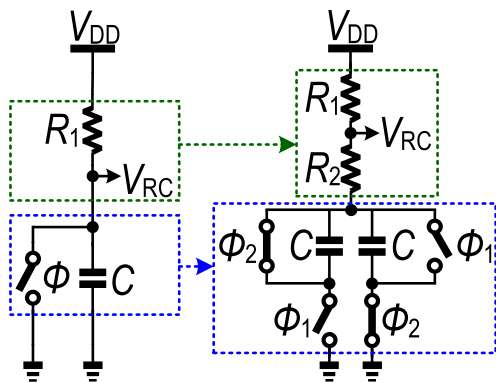
FIGURE 16. Temperature-compensated R-RC configuration [57].

different components. The frequency of the FLL is governed by a differential Frequency Detector (FD) formed by *RC* network as aforementioned. Such differential topology ensures the stability of performance respective to the supply and temperature variation. The resistor of FD is implemented with a series combination of non-silicided p-poly and n-poly resistors with opposite temperature coefficients (*TC*). Such implementation provides first-order compensation in temperature variation [53]. A dynamic comparator compares the output of the FD, which is then fed to a digital filter and locks the frequency of the digitally-controlled oscillator. The power consumption of the comparator is suppressed by reducing its operating frequency by 256×. It achieves an outstanding energy efficiency of 0.43 pJ/cycle, with a *TC* of 106 ppm/°C.

Truesdell *et al.* [50] also report a digital FLL, which locks the Digitally Controllable Oscillator (DCO) to a stable reference voltage V_{REF} (Fig. 14). The frequency generated by

the DCO is divided and fed to the F-V converter, generating V_{CAP} to compare with V_{REF}. For this DFLL, a comparator bank is implemented and a dead-zone (DZ) around V_{REF} is established. When the DCO operates within this DZ, it indicates that the frequency generated by the DCO is stable and the feedback path would be broken such that the DCO will be free-running. As such, the power consumption is minimized as other blocks will be powered down. Certainly, the *DCO* will be subjected to supply and temperature variation if the feedback loop is broken. Hence, the timer is being designed to periodically turn on to lock the frequency by the duty-cycling mechanism. Such approach effectively reduced the power consumption by only consuming 18.8 fJ/cycle. However, this scheme penalizes the frequency accuracy by exhibiting an Allan Deviation of 450 ppm, which is considered high among timers.

2) HIGH PRECISION METHODOLOGIES
With the design preference on frequency stability for FLL, works focusing on high precision have achieved an inaccuracy as low as ±200 ppm across the industrial temperature range. In 2018, Gürleyük *et al.* [54] proposed a Dual-RC Frequency Reference that uses an FLL for high precision signal generation. The FLL features two independent low-pass-filter (LPF), implemented using Wien Bridge filter, to detect their temperature-dependent phase shifts and locks the frequency of *DCO* (Fig. 15(a)). One of the Wien Bridge filters employed silicided p-poly resistors to demonstrate positive temperature phase shift, while the other used non-silicided n-poly resistors. With proper calibration, a temperature-independent frequency signal can be realized, resulting in

an extraordinary *TC* of 2.5 ppm/°C. It is worth noting that instead of using a LPF and temperature sensor for phase shift detection, [54] uses two independent LPF and complex temperature-compensation schemes to achive low *TC*, which leads to a high energy consumption of 110 pJ/cycle. On top of that, it also consumes a chip area of 2.528 mm², which is critical for SoCs.

In the effort to relax calibration complexity, [55] proposed another *RC*-based frequency reference in which the FLL features only one Wien-Bridge (WB) filter, while the temperature phase shift is detected by a Wheatstone-Bridge (WhB) temperature sensor (Fig. 15(b)). In this work, both WB and WhB exhibit similar non-linearity of temperature dependencies, achieving good accuracy using a 2-point trim. Such effort led to a massive decrement in power consumption to 25 pJ/cycle and reduced the area consumption by 8.4×. Although the temperature inaccuracy has been increased to ±400 ppm across the industrial temperature range, it still shows an outstanding *TC* of 6.15 ppm/°C.

Recently, similar inaccuracy of ±400 ppm has been achieved with a single room-temperature trim [56]. Similar to [55], the FLL also constructed based on a WB filter and a WhB temperature sensor. Instead of a separate implementation, [56] combined both WB and WhB into single architecture (Fig. 15(c)). Therefore, not only the number of components are reduced for smaller chip usage, the temperature-compensated phase shift has also been suppressed since p-poly resistors were being shared by both WB and WhB. By reducing both number of trimming points and counts, it exhibits an energy efficiency of 9.9 pJ/cycle (2.5× improvement) and chip area reduction of 2×, with the state-of-the-art *TC* of 5.2 ppm/°C.

Apart from using LPF or temperature sensor for compensation, [57] has proposed a temperature-compensated *R-RC* oscillator that focuses on eliminating possible temperature-caused delay. Based on the differential swing-boosted technique in [24], [57] had performed certain calibration on the *RC* network configuration. In common situation which relies on a single RC network, the charging/discharging rate is fully dependent on the resistance, which is highly susceptible to temperature deviation. Although it's first-order dependency is compensated using a series combination of positive and negative resistor, it's resistance still deviates due to second-order temperature dependency. On top of that, extra reset delay is also expected with the usage of single reset transistor. In this regard, [57] has added another resistor to form a *R-RC* network (Fig. 16). The extra resistor can eliminate the existing second-order temperature-coefficient. As such, second-order temperature dependency is being mitigated by modifying it's initial charging point across different temperature. On top of that, in the effort of achieving temperature-independent operation, the capacitor and reset transistor has been duplicated for dual-phase operation, where transition mode and reset operation is taken in different path. This leads to a fast reset and low leakage transition operation. Although the supply voltage required is relatively high, [57] scores
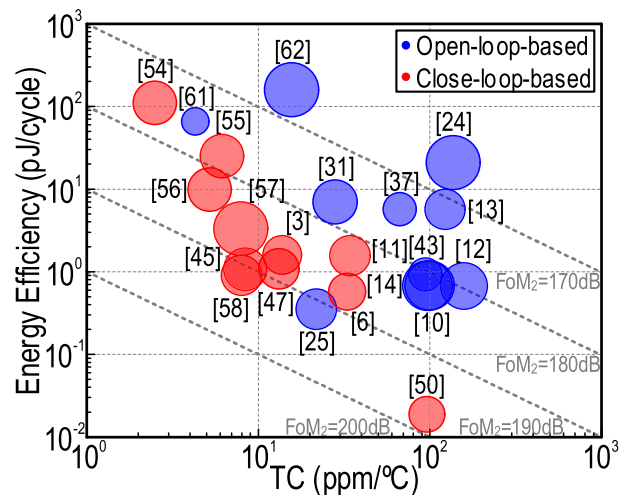
FIGURE 17. The energy efficiency versus the TC of state-of-the-art fully integrated timers. The size of the circle depicts the operating temperature range of the timer.

state-of-the-art *TC* of 7.93 ppm/°C across wide temperature range of −45 °C to 125 °C, while consuming 3.3 pJ/cycle.

3) DESIGN CONSIDERATION

As aforementioned, with a design focus on power reduction, similar considerations can be taken for FLL in minimizing V_{DD} and total current consumption. The reduction of current consumption can be achieved through multiple approaches. The most common one is to reduce the operation speed of the FD, as described in the beginning of this section [6], [54], [55], [58]. Also, duty-cycling part of the modules can reduce the power consumption. For example, the comparator is to demonstrate the frequency shift and this comparison period only occurs around the transition point. Hence, by providing the appropriate clock signal, the comparator can be designed to only operate within the transition period and subsequently sustained in idle mode for the rest of the time period [3]. The same technique can be applied to other blocks, such as biasing circuits [50].

IV. COMPARISON BETWEEN OPEN-LOOP AND CLOSE-LOOP BASED TIMER

Both the open-loop-based and close-loop-based timers serve to provide an accurate frequency reference for timing purposes. A benchmark of the recent state-of-the-art kHz-to-MHz timers for both architectures is described in Table 1. Fig. 17 illustrates their energy efficiencies versus the *TC*, while the circle size represents timer's operating temperature range.

Intuitively, it might be perceived that the close-loop based timer will have higher power consumption compared with the open-loop-based timer due to excessive components. However, from Fig. 17, we can observe that the closed-loop-based timer in general achieves a better *TC* with the same energy efficiency. Despite fewer components in an open-loop based timer, the comparators consume the majority of power to safeguard the *TC* of the timer, which leads to extra power

TABLE 1. Benchmark of recent state-of-the-art kHz-to-MHz timers.

Ref.	Type	Process (nm)	Area (mm²)	V_{DD} (V)	Freq. (Hz)	Power (μW)	Temp. Variation (ppm/°C) / Temp. Range (°C)	V_{DD} Variation	Energy Efficiency (pJ/cycle)	Jitter (ps$_{rms}$)	Allan Floor (ppm)	Settling Time (μs)	FoM₂ (dB)
[3]	CL	180	0.5	0.85-1.4	3k	0.0047	13.8 / -25 to 85	0.48%/V (0.85 to 1.4)	1.6	N/A	63	100000*	187#
[6]	CL	40	0.07	0.8	417k	0.24	33 / -20 to 80	0.53% (0.7 to 0.9)	0.57	N/A	12	68500	187#
[10]	OL	65	0.005	0.9	1.2M	0.82	100 / -25 to 125	0.7%/V (0.9 to 1.8)	0.68	N/A	10 (1s)	10	183
[11]	CL	180	0.26	1.2	70.4k	0.11	34.3 / -40 to 80	0.75%/V (1.2 to 1.8)	1.56	N/A	7 (12s)	2500	184#
[12]	OL	28	0.58	0.35-0.38	2.1M	1.4	158 / -20 to 120	2.3% (0.35 to 0.38)	0.67	800	210	3.6	181
[13]	OL	180	0.028	0.75	8.2M	46.3	123 / -20 to 100	0.91%/0.1V (0.75 to 0.95)	5.65	7.66	1.56 (4s)	N/A	172
[14]	OL	65	0.005	N/A	1.3M	0.92	96 / 0 to 145	0.49%/V (0.9 to 2.0)	0.68	N/A	N/A	10	183
[17]	CL	130	0.28	1.5	43.3M	757	N/A	N/A	0.175	316	N/A	N/A	N/A
[24]	OL	180	0.015	1.4	10.5M	219.8	137 / -40 to 125	0.44%/0.1V (1.4 to 2)	20.9	9.86	2.8	N/A	168
[25]	OL	90	0.027	0.8	51.3M	18	21.8 / -20 to 100	0.53% (0.8 to 1.2)	0.35	89.27	N/A	3.3	192
[31]	OL	65	0.032	1	18.5k	0.13	13.8 to 42.3 / -40 to 90	<5%/V (0.95 to 1.05)	7	N/A	20 (1s)	216 (4 cycle)	178
[37]	OL	65	0.044	1	3M	17.3	66.67 / 0 to 90	0.15% (1.95 to 1.45)	5.7	49.8	N/A	4$	174
[43]	OL	180	0.2	0.4	1.22k	0.0014	94 / -20 to 70	4.3% (0.4 to 0.65)	0.93	N/A	58 (3s)	N/A	179
[45]	CL	65	0.18	1.2	32M	34	8.4 / -40 to 85	80ppm/V (1.1 to 2.3)	1.06	25	2.5 (1s)	N/A	192#
[47]	CL	180	0.16	1.2	32.7k	0.0354	13.2 / -20 to 100	0.44%/V (1 to 1.8)	1.08	N/A	10	2000	189#
[50]	CL	65	0.134	0.5	560k	0.0105	96.1 / 0 to 100	N/A	0.0188	N/A	450 (1ms)	N/A	197#
[54]	CL	180	2.528	1.7-2.0	7M	775	2.5 / -45 to 85	0.18%/V (1.7 to 2.0)	110	23.8	0.33 (3s)	N/A	177#
[55]	CL	180	0.3	1.6-2.0	16M	400	6.15 / -45 to 80	0.12%/V (1.6 to 2.0)	25	39	0.32	N/A	179#
[56]	CL	180	0.14	1.8	16M	158.4	5.2 / -45 to 85	0.2%/V (1.6 to 2.0)	9.9	10.2	0.35	N/A	184#
[57]	CL	180	0.07	1.3	2.3M	7.6	7.93 / -45 to 125	0.51%/V (1.3 to 2.0)	3.3	N/A	9 (0.5s)	N/A	188#
[58]	CL	40	0.07	1-1.4	428k	0.38	8 / -40 to 80	0.27%/V (1 to 1.4)	0.9	N/A	10 (100s)	N/A	192#
[61]	OL	65	0.051	0.98-1.02	1.05M	69	4.3 / -15 to 55	0.17% (0.98 to 1.02)	65.7	160	N/A	8 (Sim)	174
[62]	OL	350	0.032	3.3	1M	160	15.757 / -40 to 125	0.08%/V (3.0 to 4.5)	160	N/A	15	1$	168

CL = Close-loop-based   OL = Open-loop-based   * Estimated from graph
$ Deduced from the number of cycles to start, which may underestimate true startup time.
# Performance cannot be fully evaluated, as it did not take settling time into consideration

usage and deteriorates the energy efficiency [59]. Contrarily, even the close-loop-based timer entails more components, the comparator and the logic gates have minimal impact on the frequency of the timer. Consequently, even with minimal power consumption, the closed-loop-based timer can still yield a stable output amid VT-variations, relaxing the current requirement and maximizing the energy efficiency.

Apart from the *TC*, one of the important parameters to be taken into consideration is the temperature range. In practice, the timer is preferred to be operated in a wide temperature range to cope with the harsh environment [60]. For instance, a common standard is the full-industrial range, which requires the electronics to work from −40 °C to 125 °C. As shown in Table 1, although some of the reported works were able

to achieve a low *TC*, their operating temperature ranges are comparably narrow, while others managed to maintain a moderate *TC* over a wide temperature range. For instance, [61] exhibits a *TC* value of 4.3 ppm/°C within −15 °C to 55 °C. Using open-loop-based architecture, [57] and [62] can function across the full-industrial range but exhibits a higher *TC* of 7.93 ppm/°C and 15.76 ppm/°C, respectively. Hence, it is important to characterize a timer's ability to maintain a moderate *TC* within a reasonable temperature range. Such ability can be expressed using *FoM₂* where an overall performance can be enumerated as defined in (8). Take the open-loop-based timer as example, the work [61] shows the lowest *TC* among all proposed works, but exhibits poor performance in temperature range and energy efficiency, which leads to a moderate overall performance with *FoM₂* of 174 dB. Contrarily, although [25] shows a relatively moderate *TC* of 21.8 ppm/°C, it presents the best *FoM₂* among all competitors with it's exceptional energy efficiency and wide operating temperature range.

One drawback of the close-loop-based timer is in its long settling time. Not only a long settling time results in a longer start-up period, it also suffers in a longer time in attaining steady-state operation amid V_{DD} variation. As summarized in Table 1, the open-loop-based timer shows a significantly lower settling time compared to the close-loop-based timer. To guarantee the loop stability, the loop filter ought to have a cutoff frequency lower than the sampling rate of the comparators, which in turn limits the settling time of the loop response. On the other hand, the settling time of the open-loop-based timer is solely dependent on the settling time of the RC-network, which can be achieved in a couple of cycles. Such characteristic shows potential for application such as energy harvesting, where the supply voltage stability is not ensured.

V. CONCLUSION

Motivated by the uprising trend of ultra-low-power timers, this review article elaborated on the characteristics of fully-integrated timers reported in the literature. We categorized these timers into two types based on their architectures: open-loop-based and close-loop-based. We also explained in detail the basic parameters to characterize and optimize a timer. To differentiate the timers, we found out that the open-loop-based timer depended on a single free-running oscillator to generate the frequency, while the closed-loop-based timer contained a feedback path to lock the output frequency. In general, the open-loop-based timer shows a faster settling time than the close-loop-based timer, but with a penalty on *TC* in effect to the delay from the logic gates and comparators/amplifiers. On the other hand, the closed-loop-based timers show a better *TC* under a similar power budget, benefitting from the closed-loop operation. We recommend the designers to determine the main design priority before finalizing a suitable architecture. We envision that the development of ultra-low-power timers will continue for both types of timers, aligning with the current trend of energy harvesting for IoT nodes.

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