IEEE Access
Multidisciplinary : Rapid Review : Open Access Journal

Received 2 May 2022, accepted 6 June 2022, date of publication 16 June 2022, date of current version 1 July 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3183593

Effect of ALD Processes on Physical and Electrical Properties of HfO_2 Dielectrics for the Surface Passivation of a CMOS Image Sensor Application

HONGGYUN KIM[1], VIJAY D. CHAVAN[1,2], JAMAL AZIZ[1,2], BYOUNGSU KO[3], JAE-SUNG LEE[4], JUNSUK RHO[3,6], TUKARAM D. DONGALE[5], KYEONG-KEUN CHOI[6], AND DEOK-KEE KIM[1,2]

[1]Department of Electrical Engineering, Sejong University, Seoul 05006, South Korea
[2]Department of Electrical Engineering and Convergence Engineering for Intelligent Drone, Sejong University, Seoul 05006, South Korea
[3]Department of Mechanical Engineering, Pohang University of Science and Technology, Pohang, Gyeongbuk 37673, South Korea
[4]Department of Renewable Energy Engineering, Uiduk University, Gyeongju 38004, South Korea
[5]Computational Electronics and Nanoscience Research Laboratory, School of Nanoscience and Biotechnology, Shivaji University, Kolhapur 416004, India
[6]National Institute for Nanomaterials Technology, Pohang University of Science and Technology, Pohang, Gyeongbuk 37673, South Korea

Corresponding authors: Deok-Kee Kim (deokkeekim@sejong.ac.kr) and Kyeong-Keun Choi (choikk@postech.ac.kr)

This work was supported by the Korean Government (MOTIE) and Korea Evaluation Institute of Industrial Technology (KEIT) under Grant 20010574.

ABSTRACT The surface passivation of a CMOS image sensor (CIS) is highly beneficial for the overall improvement of a device performance. We employed the thermal atomic layer deposition (T-ALD) and plasma enhanced (PE-ALD) techniques for the deposition of 20 nm HfO_2 as well as stacked with 3 and 5 nm Al_2O_3 thin films. The HfO_2/Si and Al_2O_3/HfO_2/Si metal-oxide-semiconductor structures were used to analyze the fixed charge density (Q_f) and interface trap density (D_{it}). The as-synthesized samples show high D_{it} and Q_f values (10^{12} cm^{-2}eV^{-1}) and a minority carrier lifetime of 15-300 μs. The finite-difference time-domain simulation of high-k dielectrics confirmed that the Al_2O_3 (top)/HfO_2 stacked structures expected higher quantum efficiency for CIS application. The effect of vacuum annealing (VA) and forming gas annealing (FGA) treatments succeeded with the decomposition of the D_{it} and increase in carrier lifetime. The H_2 ambient FGA samples showed a remarkable decrease in the D_{it} values. To improve the overall performance of the device after passivation, we employed an Al_2O_3/HfO_2 bilayer structure, which showed a low D_{it} of 10^{11} cm^{-2}eV^{-1} and a minority carrier lifetime of ~3,700 μs after 400 °C and 30 min FGA. We believe that this surface passivation strategy will pave way for future CIS technology regarding the development of lower defective surface and superior performance.

INDEX TERMS Atomic layer deposition, carrier lifetime, CMOS image sensor, surface passivation, forming gas, HfO_2, interface trap density.

I. INTRODUCTION

The rapid progress in CMOS circuit technology is expecting a dominant market extension regarding novel electronic devices [1]. CMOS technology plays an important role in the evolution of image sensors as modern low-cost sensors require high resolution, high speed, and low power consumption [2]. However, the performance of the CMOS image sensor (CIS) is highly affected by defects (Si-dangling bonds) and impurities that are linked with Si interfaces and surfaces. Therefore, it is important to passivate the Si surface to achieve better device performance.

The defects at the Si/dielectric interface introduce different energy levels into the Si bandgap, which are generally termed as interface trap density (D_{it}). Therefore, excellent chemical surface passivation is required to suppress the defects at the Si/dielectric interface, which can reduce the D [3]. On the other hand, the fixed charge (Q_f) is the charge accumulation within a few nm of the Si/dielectric interface. The Q_f is the resultant of the surface properties and annealing conditions. The presence of charges in the dielectric film established an electric field at the interface, which can either attract or repel the carriers from the surface [4]. Thus, attracting or repelling one type of carrier from the surface limits the charge recombination rate [5]. Also, the negative charges for the p-type Si and the positive charges for the n-type Si

The associate editor coordinating the review of this manuscript and approving it for publication was Ye Zhou.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

can improve the quality of the field-effect passivation in the entire injection level range. The quality of passivation by the dielectric is commonly examined by the minority carrier lifetime [6]. The minority carrier lifetime depends on the surface recombination and the dark current of the thermally generated electrons at the interface. This results in the excitation of electrons from the valence band to the conduction band level [5].

Up to now, a variety of high-k dielectric materials, such as Al_2O_3, HfO_2, Ta_2O_5, and TiO_2 are of beneficial interest for the surface passivation [7]–[9]. Among these high-k materials, HfO_2 and Al_2O_3 dielectrics are of receiving progressive attention due to their outstanding defect decomposition properties in regard to the CIS applications [10]. Interestingly, the bilayer or laminated structures of the dielectric materials, such as Al_2O_3, HfO_2, SiO_2, and TiO_2 are widely adopted due to their overall surface passivation benefits and improved device performance [7], [8]. However, the high quality of chemical as well as field effect passivation is introduced by Al_2O_3 and HfO_2 which effectively passivates the defects. This is because of the improvement in the interfacial layer due to the bilayer structure of Al_2O_3 and HfO_2. Owing to there excellent interfacial characteristics, these Al_2O_3/HfO_2 bilayer structures are getting more and more attention for the improvement of passivation quality. The synthesis of the dielectric thin films has been implemented by a variety of techniques [11]. Atomic layer deposition (ALD) is a state-of-the-art and crucial technique among the various techniques to synthesize different dielectric materials. The ALD process represents the key features of the as-synthesized films, which include a highly effective uniform deposition, low-temperature process, and layer-by-layer growth. Also, it is most favorable as compared to other techniques due to a self-limited reaction mechanism that is based on the chemisorption of two or more precursors [12], [14].

In this research work, we have investigated the different process parameters as well as the post-metal annealing conditions that realized the decomposition of the D_{it} and increased Q_f for a single HfO_2 structure. However, to increase the carrier lifetime and improve the interface, we have employed the bilayer Al_2O_3/HfO_2 laminate structures. The results show that the H_2 ambient forming gas annealing (FGA) remarkably decreases the D_{it} values than vacuum annealed (VA) samples. The Al_2O_3/HfO_2 bilayer structure may shows better field-effect and chemical passivation effect [18] in an integration of CIS process by minimizing the formation of interfacial layer (Si/dielectric) and improve characteristics of the dielectric properties. Hence, after FGA of Al_2O_3/HfO_2 bilayer structure, the interfacial layer gets improved which results in reduction of D_{it} values and recombination. Also, combining effect of these high-k materials effectively enhances the passivation quality. We believe that this surface passivation strategy will pave a way for future CIS technology regarding the development of lower defective surface and superior performance.

II. EXPERIMENTAL DETAILS

The HfO_2 ALD films were deposited using a tetrakis (ethylmethylaminohafnium) (TEMAHf, $Hf[N(C_2H_5)(CH_3)]_4$) precursor at a temperature range between 100 °C to 400 °C. The p-type Si ((100), 18 Ω-cm) substrates were cleaned using an ammonia peroxide mixture (NH_3:H_2O_2:de-ionized (DI) water with a ratio of 1:1:5 at 70 °C for 10 min) and diluted hydrofluoric acid (50:1, DI H_2O) at room temperature for 1 min before the deposition. The HfO_2 films were then deposited using ALD reactor (Plus 200 system, Quros). The TEMAHf precursor was supplied with O_2 plasma at a 200 sccm flow rate and a power of 100 W, for the sequential surface reactions in the plasma-enhanced ALD (PE-ALD) at a chamber pressure of 0.4 mTorr. Also, H_2O precursor was used in thermal ALD (T-ALD) for the 20-nm-target film thickness instead of the O_2 plasma for PE-ALD deposited films. For comparison of the different HfO_2 films synthesized using different ALD processes, the T-ALD HfO_2 and PE-ALD HfO_2 samples were prepared at different deposition temperatures (250 °C and 280 °C) on the pre-cleaned Si wafer. The post-deposition annealing was performed in a tube furnace at vacuum and forming gas (N_2:H_2 = 95 %:5 %) conditions for all the HfO_2 samples. The annealing temperature was kept constant at 400 °C for 30 min.

To fabricate the standard Al/HfO_2/Si and Al/Al_2O_3/HfO_2/Si MOS capacitor (MOSCAP) like structures, a 300 nm Al top electrode was deposited using thermal evaporation. The custom-made shadow mask with a 150 × 150 μm^2 dimension was used for the dot structure as a gate electrode for all the structures. The capacitance-voltage (C-V) and the current density-voltage (J-V) measurements of the prepared structures were then conducted using the Agilent B1500A parameter analyzer. All the measurements were traced at room temperature with a high frequency (1 MHz) under dark conditions. The dual C-V curves of 10 devices in the forward and backward directions were collected from the accumulation to the inversion region properties of the MOSCAPs. The J–V characteristics were then conducted to investigate the effect of the different passivation layers on the electrical properties of the prepared MOSCAPs.

The D_{it} and Q_f values were estimated using C-V curves from Eqs. 1 and 2, respectively [15].

$$Q_f = \frac{(\varphi_{ms} - V_{FB})C_{ox}}{qA}, \tag{1}$$

where ϕ_{ms} is defined by the difference between the metal and the semiconductor work functions, V_{FB} is the flat band voltage, C_{ox} is the oxide capacitance, q is the electron charge, and A is the electrode area.

$$D_{it} = \frac{2\omega C_{ox}^2 G_{max}}{qA(G_{max}^2 + \omega^2 (C_{ox} - C_m C_{max})^2)}, \tag{2}$$

where G_{max} is the maximum conductance, and C_m is the measured capacitance at the frequency ω.

The thickness and refractive index (n) of the HfO_2 films were determined using spectroscopic ellipsometry (alpha SE,

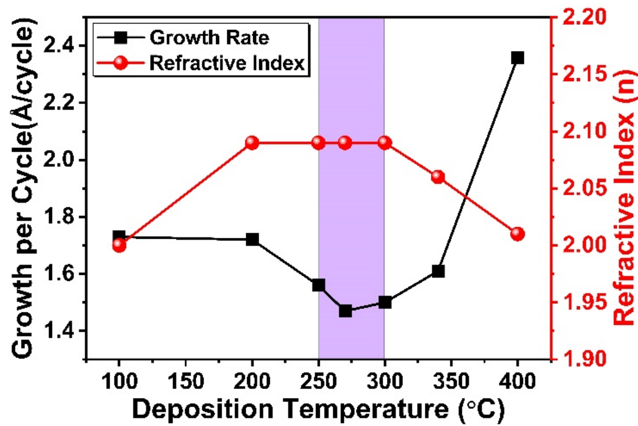

FIGURE 1. Growth per cycle (GPC) (left axis) and the refractive index (n) at 632.8 nm (right axis) of the HfO_2 films on the Si wafer at substrate temperatures between 100 °C and 400 °C.

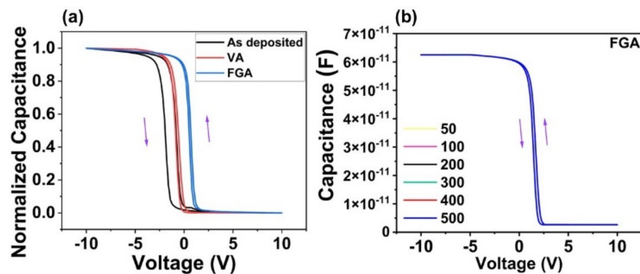

FIGURE 2. The C-V curves of the HfO_2 samples synthesized at 250 ° using plasma enhanced-ALD technique under different annealing conditions (a), and multiple C-V cycles of FGA sample (b).

J. A Woollam co., Ltd). The minority carrier lifetime (injection level-dependent) of the Si-wafers was measured using the quasi-steady-state photoconductance (QSS-PC) method with the lifetime tester (WCT-120, Sinton Instruments) [16]. The minority carrier lifetime was extracted at an intermediate carrier level injection of 1 x 10^{15} cm^{-3}.

III. RESULTS AND DISCUSSION

In this study, the ALD synthesis of the HfO_2 thin films was conducted at a wide temperature range from 100 °C to 400 °C using a TEMAHf precursor to examine the thorough deposition variation. **Fig. 1** illustrates the growth per cycle (GPC) and n of the HfO_2thin films with respect to the deposition temperature. The GPC vs the deposition temperature curve (black) in **Fig. 1** indicates that the GPC decreases at 200 °C and reaches a stable value of about 1.5 Å/cycle in the range of 250 °C to 300 °C. After that, the GPC increased in the temperature range from 300 °C to 400 °C. Thoroughly, the initial temperature range (100-200 °C) possesses minimal activation energy for the formation and growth of the HfO_2 thin films [17]. On the other hand, temperature above 300 °C showed a CVD-type growth performance, which showed a high GPC value [18]. This implies that the temperature range of 250-300 °C is a crucial temperature range for the optimal process window. Additionally, the ellipsometry measurements showed a slanted increase of the n from 100 °C to 200 °C. However, with a further increase in temperature, the n values acquire a stable range from 250 °C to 300 °C, which again decreased for both ALD processes. Thus, the overall results imply that the ALD process window is optimum in the range of 250-300 °C. **Fig. 2(a)** shows the C-V characteristics of the as-deposited PE-ALD HfO_2 samples at 250 °C under different annealing conditions. The arrows indicate the voltage sweep direction in the C-V curves. The obtained C-V curves display hysteresis in the as-prepared HfO_2films. The hysteresis in the C-V curves is related to the existence of a certain amount of interface defects at HfO_2/Si interface. [19], [20]. However, after VA and FGA treatments there is a remarkable reduction in the C-V hysteresis due to a reduction in interface defects [19], [21]. Further, after VA and FGA, the V_{FB} showed a negative value, which reflects the existence of trapped positive oxide charges in the HfO_2 passivation layer. The T-ALD films also exhibited similar characteristics as PE-ALD grown films.

In addition to V_{FB}, the permittivity (K) and other parameters of the as-grown films are summarized in **Table 1**. The *EOT* and the K of the HfO_2 films were extracted using the relation provided below Eqs. 3 and 4. [22]:

$$EOT = \frac{K_{SiO_2} \times \varepsilon_0}{C_{max}/A}, \quad (3)$$

$$K = \frac{K_{SiO_2} \times t_{hk}}{EOT - t_{SiO_2}}, \quad (4)$$

where K_{SiO_2} is the permittivity of SiO_2, A is the area of the Al electrode, C_{max} is the accumulation capacitance, and t_{hk} is the thickness of the HfO_2 films. The annealing effect on the HfO_2 films prepared at 250 °C in PE-ALD showed an increase in the *EOT* and a reduction in K, as illustrated in **Table 1**. For the films prepared at 280 °C (T-ALD), 250 °C (PE-ALD), and 280 °C (PE-ALD), the same trend was observed. It can be concluded that the HfO_2 passivation layer can be attributed to the formation of the interface layer after the annealing [23], [24].

The J-V characteristics of the 280 °C PE-ALD grown films with VA and FGA conditions were measured after applying a negative bias. We observed a very low current density of 4.5 x10^{-7} A/cm^2 at -1 V after the annealing process at 400 °C. Due to the existence of a small number of dangling bonds and an interface charge trapping, the leakage current gets reduced after FGA [22], [25].

Fig. 3 shows the role of VA and FGA on the D_{it}values of the 20-nm-thick HfO_2 thin films deposited using T-ALD and PE-ALD growth techniques. For both synthesis techniques, the as-prepared films possessed high D_{it} values (1.2 ∼ 1.5 x 10^{12} $cm^{-1}eV^{-1}$) before the annealing process. However, T-ALD showed lower D_{it} values as compared to the PE-ALD technique. The Si-dangling bonds and the inferior HfO_2 and Si interface seemed to cause the high D_{it}values for the as-prepared samples [15], [16]. Interestingly, in both ALD processes, the as-prepared HfO_2 films show a remarkable reduction in the D_{it}values (6∼11 x10^{11} $cm^{-1}eV^{-1}$), which

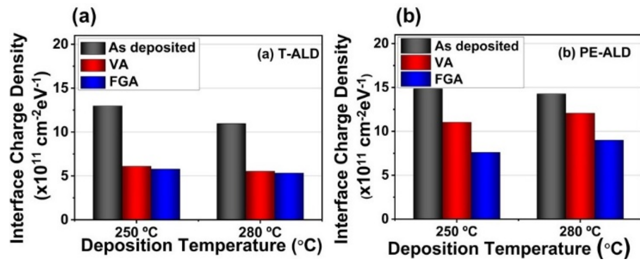

FIGURE 3. Interface trap density (D_{it}) for 20-nm-thick HfO_2 films after annealing at 400 °C for 30 min. (a) thermal-ALD grown HfO_2 films and (b) plasma enhanced-ALD grown HfO_2 films.

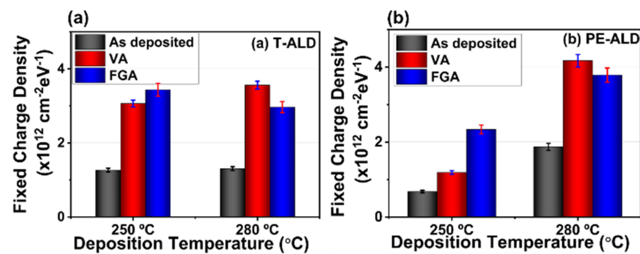

FIGURE 4. Fixed charge density (Q_f) for 20-nm-thick HfO_2 films after annealing at 400 °C for 30 min. (a) thermal-ALD grown HfO_2 films and (b) plasma enhanced-ALD grown HfO_2 films.

visualizes the significant role of the annealing parameters. The device possessed minimal D_{it} values after the FGA process. The obtained results indicate that the H_2 annealing at 400 °C improves the quality of the interface by hydrogenation, which is advantageous for strong chemical passivation of the Si-dangling bonds as opposed to the VA [26], [27]. This visualization depicts the dominant role of the FGA over the VA samples.

In **Fig. 4**, the Q_f values were measured as a function of the different HfO_2 synthesis temperature to study the field-effect passivation [27]. For this analysis we have measured 10 devices. The error bars in **Fig. 4** represents that there is not much significant deviation in the analyzed samples. With the HfO_2, the equivalent series resistance, and other models predict that the positive charges near or at the interface of the metal/semiconductor were present due to oxygen vacancies [8], [27]. The as-prepared T-ALD films demonstrated high Q_f values for low substrate temperatures. However, for PE-ALD grown films, Q_f values get increased at high substrate temperature samples. The FGA samples showed higher Q_f values for T-ALD and PE-ALD methods than as-deposited HfO_2films. The increased Q_f values after VA and FGA conditions may be caused by interfacial layer formation, revealing the better field-effect passivation than as-synthesized HfO_2 films [28].

After the FGA, the D_{it} values decreased, and the Q_f values increased which implies the collective effect of the chemical as well as the field-passivation. This is an ideal phenomenon to possess strong surface passivation [29], [30].

Finite-difference time-domain (FDTD) is used to calculate the reflectance, transmission, interference, diffraction, and

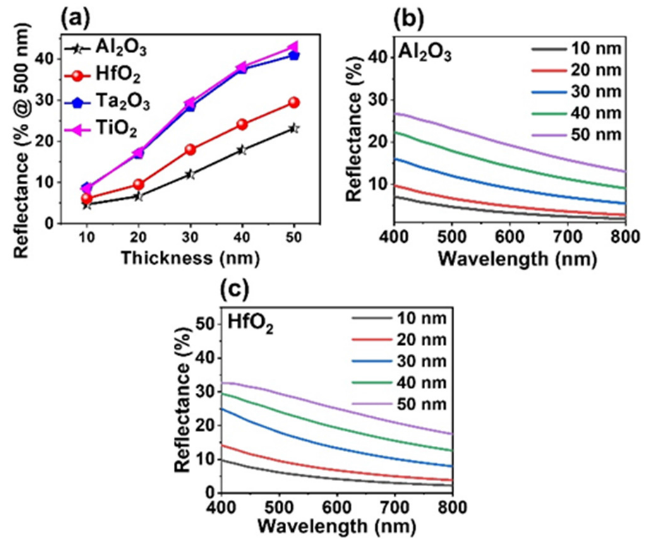

FIGURE 5. Finite-difference time-domain (FDTD) simulation results: (a) reflectance at 500 nm incident wavelength as a function of thickness for each high-k dielectric, (b) reflectance as a function of wavelength for the Al_2O_3 films, and (c) reflectance as a function of wavelength for the HfO_2 films.

absorption of structured or unstructured materials, as well as to study the response to different polarizations and wavelengths of light and demonstrate how light travels through the materials in real-time [31]. **Fig. 5** represents FDTD simulation to evaluate the reflectance measurements of the single-layer and bilayer structures. In **Fig. 5(a)**, the reflectance (%) at a 500 nm wavelength for different thickness of Al_2O_3, HfO_2, Ta_2O_5, and TiO_2 films on the Si substrates is shown. The graphical representation of reflectance at 500 nm was found to be linearly proportional to the thickness in the all-dielectric materials in the simulation. However, the lower reflectance values of the Al_2O_3 and HfO_2 dielectrics result in higher quantum efficiency (QE) values than Ta_2O_5 and TiO_2. Nevertheless, the comparison between the reflectance of Al_2O_3 and HfO_2 reveals that Al_2O_3 results in better QE than HfO_2 films (**Fig. 5(b)** and **Fig. 5(c)**).Furthermore, the Al_2O_3/HfO_2stack structure results in high QE, and it is helpful for the CIS applications with its low reflectance. The reflectance of the Al_2O_3 and HfO_2 dielectrics results in higher quantum efficiency (QE) values than Ta_2O_5 and TiO_2. Nevertheless, the comparison between the reflectance of Al_2O_3 and HfO_2 reveals that Al_2O_3 results in better QE than HfO_2 films (**Fig. 5(b)** and **Fig. 5(c)**). Furthermore, the Al_2O_3/HfO_2stack structure results in high QE, and it is helpful for the CIS applications with its low reflectance.

The generation and recombination of the carriers at the interface due to defects might result in the emergence of a dark current which can demean the QE of the CIS [32]. On the other hand, the reduction of carrier recombination is the key feature in fabricating Si-based high-performance cutting-edge electronic devices [33]. **Figs. 6(a)** and **6(b)** demonstrate the effective carrier lifetime of the as-prepared and the FGA HfO_2devices that were prepared by T-ALD and PE-ALD.

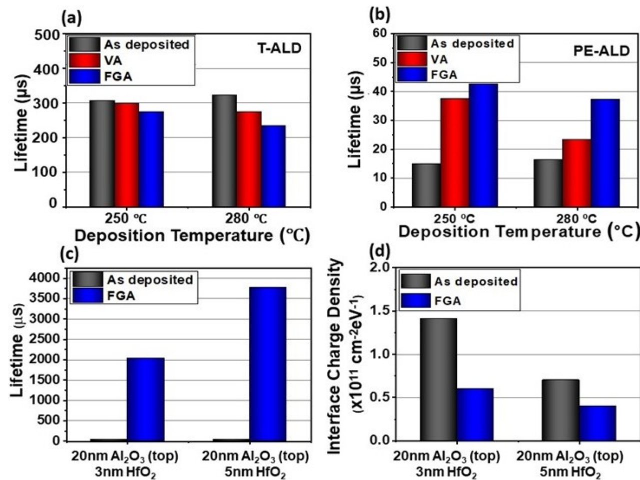

FIGURE 6. Effective carrier lifetime before and after annealing (400 °C for 30 min) of (a) thermal-ALD HfO_2, (b) plasma enhanced-ALD HfO_2, (c) plasma enhanced-ALD 3 nm and 5 nm of the Al_2O_3(top)/HfO_2 stacked structure films, and (d) the interface trap density (D_{it}) measurements of the Plasma enhanced-ALD 3 nm and 5 nm Al_2O_3 (top)/HfO_2 stacked structure films.

In **Fig 6(a)**, T-ALD grown HfO_2 films show similar values under all conditions. However, the as-prepared samples exhibit lower carrier lifetime values as compared to the FGA samples, which is shown in **Fig. 6(b)**. The low lifetime values of the as-prepared samples occur due to the recombination centers induced by the interfacial defects [34]. However, the carrier lifetime value of the single-layer HfO_2films gets improved after the FGA (300 μs). The minimized charge carrier recombination is attributed to the enhanced lifetime after the FGA processing conditions. For further improvement in the carrier lifetime, the bilayer Al_2O_3/HfO_2stacked structure was utilized as predicted by the FDTD simulation (**Fig 5**). **Fig. 6(c)** depicts the carrier lifetime measurements of the Al_2O_3/HfO_2bilayer structures, deposited by PE-ALD with 3-nm and 5-nm thick HfO_2 and 20-nm-thick of Al_2O_3. As predicted, bilayer stacked structures of Al_2O_3/HfO_2 showed a higher carrier lifetime than the single-layer HfO_2samples. The high quality of the chemical passivation can reduce the defects, which can increase the carrier lifetime. Later, both the Al_2O_3/HfO_2bilayer structures were subjected to the FGA processing. The Al_2O_3/3-nm HfO_2 structure showed a carrier lifetime of 2,100 μs. However, the Al_2O_3/5-nm HfO_2structure showed a maximum carrier lifetime of 3,750 μs owing to the better interface caused by the 5-nm-thick HfO_2 with Si. The record performance of the bilayer structures shows that the interface traps or the Si-dangling bonds were banished and effectively passivated by the hydrogenation [34], [35]. Further, **Fig. 6(d)** shows that the Al_2O_3/HfO_2bilayer structure shows lower D_{it} values (1.0×10^{11} cm^{-2}.eV^{-1}) than the single-layer HfO_2 structures (6.0×10^{11} cm^{-2}.eV^{-1}) after the FGA processing conditions. Thus, the enhancement in the carrier lifetime due to hydrogenation after the annealing affects the chemical passivation of Al_2O_3/HfO_2, resulting in the record performance.

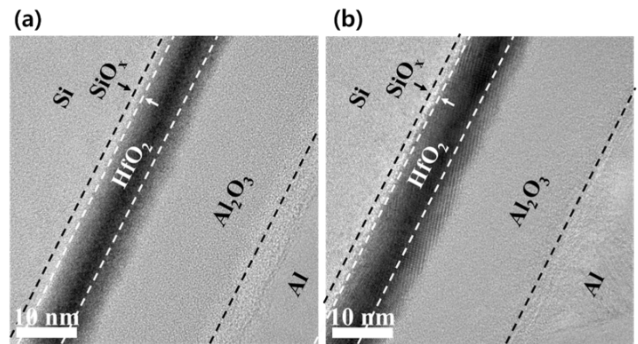

FIGURE 7. Transmission electron microscopic images of the Si/5-nm HfO_2/20-nm Al_2O_3/Al structure (a) before forming gas anneal (FGA) and (b) after FGA.

TABLE 1. Parameters for the HfO_2 and Al_2O_3 /HfO_2 passivation layers include flat band voltage (V_{FB}), permittivity (*K*), equivalent oxide thickness (*EOT*), and leakage current density (J).

Deposition	Annealing	V_{FB}(V)	EOT (nm)	K_{ox}	J_g (A/cm²)
250 °C T-ALD	As-deposited	- 1.9	5.8	20.6	5.0 x 10^{-7}
	VA	- 1.4	8.5	12.0	1.7 x 10^{-7}
	FGA	- 1.3	9.2	10.8	1.8 x 10^{-7}
280 °C T-ALD	As-deposited	- 1.4	5.1	25.6	1.0 x 10^{-6}
	VA	- 1.1	6.6	17.0	3.5 x 10^{-7}
	FGA	- 1.0	9.2	10.9	1.7 x 10^{-7}
250 °C T-ALD	As-deposited	- 2.6	5.9	19.8	1.5 x 10^{-6}
	VA	- 1.8	6.4	17.7	1.3 x 10^{-7}
	FGA	- 0.8	8.1	12.8	1.1 x 10^{-7}
280 °C PE-ALD	As-deposited	- 2.4	6.0	19.7	2.8 x 10^{-6}
	VA	1.1	6.7	16.5	1.6 x 10^{-7}
	FGA	1.0	6.8	16.3	4.5 x 10^{-7}
5nm HfO_2 20nm Al_2O_3	As-deposited	- 0.4	8.6	11.7	-
	FGA	0.4	8.8	11.5	

To study the interface property of Al_2O_3/5-nm HfO_2 bilayer structures, we used cross-sectional transmission electron microscopy (TEM). In **Fig. 7,** the TEM micrographs display the different MOS structures with an interface layer between HfO_2/Si. It was observed that the as-deposited Si/5-nm (target thickness) HfO_2/20-nm Al_2O_3(target thickness)/Al samples showed a clear interface between the Si and HfO_2 with a 6.2-nm-thick HfO_2 and a 20.8-nm-thick Al_2O_3. These calculated values from the TEM are corroborated with the expected thickness from the ALD process. The fully amorphous nature of the oxide layers can be observed in the as-deposited ALD structures.

After FGA processing, the thickness of the interface between the HfO_2 and Si showed an improvement, and crystallinity gets increased as shown in **Fig. 7(b)** [8]. The increased interface thickness is crucial for the reduction of D_{it} values [36]. In addition to this, hydrogenation played a very crucial role in the suppression of the Si dangling bonds, which also accounted for the D_{it} suppression. Thus, the densification of the interface of the bilayer Al_2O_3/HfO_2after FGA will result in decreased *EOT* and increased K_{ox} as shown in **Table 1**.

The overall finding of this study revealed that the defects that are associated with the Si surface and its interfaces with oxides can be potentially controlled by chemical and field-effect passivation, which is emerging with CIS technology as well as Si-based electronic devices.

IV. CONCLUSION

In this study, the plasma-enhanced ALD (PE-ALD) and thermal atomic layer deposition (T-ALD) HfO_2 thin films were prepared. The ALD process window was optimum in the temperature range from 250 °C to 300 °C. The high deposition temperature showed higher fixed charge density (Q_f) values in both ALD techniques. In the case of interface trap density (D_{it}), the values for the T-ALD prepared HfO2 films were lower than the values for the PE-ALD grown films, which indicates that the moderate temperature played a crucial role in the surface passivation for the ALD processes. To improve the overall performance, we studied the Al_2O_3/HfO_2 stack structures. The finite-difference time-domain (FDTD) simulation finding for the Al_2O_3/HfO_2 stack showed higher QE for the CMOS image sensor (CIS) applications. The Al_2O_3/HfO_2 stack layers possessed a minimum D_{it} of $\sim$1.0 x10^{11} cm^{-2}eV^{-1}. The H_2 ambient forming gas anneal (FGA) (400 °C for 30 min) is advantageous for chemical passivation in CIS applications. The bilayer Al_2O_3/HfO_2 stacked structures showed an increased minority carrier lifetime from $\sim$300 μs up to $\sim$3,700 μs. The analyzed structures can help to increase the carrier lifetime as well as decrease the D_{it} values, which also reveal the importance of the FGA, and can assist with the advancement of the upcoming CIS technology.

ACKNOWLEDGMENT

This research was also supported by the MOTIE (Ministry of Trade, Industry, and Energy (20010574, High-k passivation dielectric thin film development for a CMOS image sensor application) and KSRC (Korea Semiconductor Research Consortium) support program for the development of the future semiconductor device. *(Honggyun Kim and Vijay D. Chavan contributed equally to this work.)*

REFERENCES

[1] E. J. Nowak, I. Aller, T. Ludwig, K. Kim, R. V. Joshi, C.-T. Chuang, K. Bernstein, and R. Puri, "Turning silicon on its edge [double gate CMOS/FinFET technology]," *IEEE Circuits Devices Mag.*, vol. 20, no. 1, pp. 20–31, Jan./Feb. 2004, doi: 10.1109/MCD.2004.1263404.

[2] M. Bigas, E. Cabruja, J. Forest, and J. Salvi, "Review of CMOS image sensors," *Microelectron. J.*, vol. 37, no. 5, pp. 433–451, May 2006, doi: 10.1016/j.mejo.2005.07.002.

[3] E. Oudot, M. Gros-Jean, and K. Courouble, "Hydrogen passivation of silicon/silicon oxide interface by atomic layer deposited hafnium oxide and impact of silicon oxide underlayer COLLECTIONS," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 36, pp. 1–116, Jan. 2018, doi: 10.1116/1.4999561.

[4] G. Dingemans and W. M. M. Kessels, "Status and prospects of Al_2O_3-based surface passivation schemes for silicon solar cells," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 30, no. 4, Jul. 2012, Art. no. 040802, doi: 10.1116/1.4728205.

[5] Z. Taghipour, S. Lee, S. A. Myers, E. H. Steenbergen, C. P. Morath, V. M. Cowan, S. Mathews, G. Balakrishnan, and S. Krishna, "Temperature-dependent minority-carrier mobility in p-type InAs/GaSb type-II-superlattice photodetectors," *Phys. Rev. A, Gen. Phys.*, vol. 11, no. 2, Feb. 2019, Art. no. 24047, doi: 10.1103/PhysRevApplied.11.024047.

[6] N. E. Grant and J. D. Murphy, "Temporary surface passivation for characterisation of bulk defects in silicon: A review," *Phys. Status Solidi Rapid Res. Lett.*, vol. 11, no. 11, pp. 1–18, 2017, doi: 10.1002/pssr.201700243.

[7] V. Djara, M. Sousa, N. Dordevic, L. Czornomaz, V. Deshpande, C. Marchiori, E. Uccelli, D. Caimi, C. Rossel, and J. Fompeyrine, "Low dit $HfO_2/Al_2O_3/In_{0.53}Ga_{0.47}$As gate stack achieved with plasma-enhanced atomic layer deposition," *Microelectron. Eng.*, vol. 147, pp. 231–234, Nov. 2015, doi: 10.1016/j.mee.2015.04.102.

[8] H.-K. Kang, Y.-S. Kang, D.-K. Kim, M. Baik, J.-D. Song, Y. An, H. Kim, and M.-H. Cho, "Al_2O_3 passivation effect in $HfO_2 Al_2O_3$ laminate structures grown on InP substrates," *ACS Appl. Mater. Interface*, vol. 9, no. 20, pp. 17526–17535, May 2017, doi: 10.1021/acsami.7b00099.

[9] J. Azadmanjiri, C. C. Berndt, J. Wang, A. Kapoor, V. K. Srivastava, and C. Wen, "A review on hybrid nanolaminate materials synthesized by deposition techniques for energy storage applications," *J. Mater. Chem. A*, vol. 2, no. 11, pp. 3695–3708, 2014, doi: 10.1039/c3ta14034b.

[10] F. Lin, B. Hoex, Y. H. Koh, J. J. Lin, and A. G. Aberle, "Low-temperature surface passivation of moderately doped crystalline silicon by atomic-layer-deposited hafnium oxide films," *Energy Proc.*, vol. 15, pp. 84–90, Jan. 2012, doi: 10.1016/J.EGYPRO.2012.02.010.

[11] J. Azadmanjiri, C. C. Berndt, J. Wang, A. Kapoor, V. K. Srivastava, and C. Wen, "A review on hybrid nanolaminate materials synthesized by deposition techniques for energy storage applications," *J. Mater. Chem. A*, vol. 2, no. 11, pp. 3695–3708, 2014, doi: 10.1039/c3ta14034b.

[12] K.-K. Choi, J. Kee, S.-H. Kim, M.-S. Park, C.-G. Park, and D.-K. Kim, "Filling performance and electrical characteristics of Al_2O_3 films deposited by atomic layer deposition for through-silicon via applications," *Thin Solid Films*, vol. 556, pp. 560–565, Apr. 2014, doi: 10.1016/j.tsf.2014.01.081.

[13] K. K. Choi, C. G. Park, and D. K. Kim, "Electrical characteristics and step coverage of ZrO_2 films deposited by atomic layer deposition for through-silicon via and metal-insulator-metal applications," *Jpn. J. Appl. Phys.*, vol. 55, no. 1, pp. 1–6, 2016, doi: 10.7567/JJAP.55.016502.

[14] K.-K. Choi, J. Kee, C.-G. Park, and D.-K. Kim, "Effects of H_2 plasma and annealing on atomic-layer-deposited Al_2O_3 films and Al/Al_2O_3/Si structures," *Appl. Phys. Exp.*, vol. 8, no. 4, Apr. 2015, Art. no. 045801, doi: 10.7567/APEX.8.045801.

[15] C.-H. Hsu, Y.-S. Cho, W.-Y. Wu, S.-Y. Lien, X.-Y. Zhang, W.-Z. Zhu, S. Zhang, and S.-Y. Chen, "Enhanced Si passivation and PERC solar cell efficiency by atomic layer deposited aluminum oxide with two-step post annealing," *Nanosc. Res. Lett.*, vol. 14, no. 1, pp. 1–10, Dec. 2019, doi: 10.1186/s11671-019-2969-z.

[16] X. Y. Zhang, C. H. Hsu, Y. S. Cho, S. Y. Lien, W. Z. Zhu, S. Y. Chen, W. Huang, L. G. Xie, L. D. Chen, X. Y. Zou, and S. X. Huang, "Simulation and fabrication of HfO_2 thin films passivating SI from a numerical computer and remote plasma ALD," *Appl. Sci.*, vol. 7, no. 12, pp. 1–9, 2017, doi: 10.3390/app7121244.

[17] M. Lapteva, V. Beladiya, S. Riese, P. Hanke, F. Otto, T. Fritz, P. Schmitt, O. Stenzel, A. Tünnermann, and A. Szeghalmi, "Influence of temperature and plasma parameters on the properties of PEALD HfO_2," *Opt. Mater. Exp.*, vol. 11, no. 7, p. 1918, Jul. 2021, doi: 10.1364/ome.422156.

[18] J. C. Hackley, J. D. Demaree, and T. Gougousi, "Growth and interface of HfO_2 films on H-terminated Si from a TDMAH and H_2O atomic layer deposition process," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 26, no. 5, pp. 1235–1240, Sep. 2008, doi: 10.1116/1.2965813.

[19] H. W. Wan, Y. J. Hong, Y. T. Cheng, and M. Hong, "BTI characterization of MBE Si-capped Ge gate stack and defect reduction via forming gas annealing," in *Proc. IEEE Int. Reliab. Phys. Symp.*, May 2019, pp. 1–4, doi: 10.1109/IRPS.2019.8720567.

[20] M. Tapajna, L. Válik, D. Gregušová, K. Fröhlich, F. Gucmann, T. Hashizume, and J. Kuzmlk, "Threshold voltage instabilities in AlGaN/GaN MOS-HEMTs with ALD-grown Al_2O_3 gate dielectrics: Relation to distribution of oxide/semiconductor interface state density," in *Proc. 11th Int. Conf. Adv. Semiconductor Devices Microsyst. (ASDAM)*, vol. 3, Nov. 2015, pp. 103–111, doi: 10.1109/ASDAM.2016.7805881.

[21] T. Hosoi, K. Kutsuki, G. Okamoto, M. Saito, T. Shimura, and H. Watanabe, "Origin of flatband voltage shift and unusual minority carrier generation in thermally grown GeO_2/Ge metal-oxide-semiconductor devices," *Appl. Phys. Lett.*, vol. 94, no. 20, pp. 2007–2010, 2009, doi: 10.1063/1.3143627.

[22] D. Wang, G. He, L. Hao, J. Gao, and M. Zhang, "Comparative passivation effect of ALD-driven HfO_2 and Al_2O_3 buffer layers on the interface chemistry and electrical characteristics of Dy-based gate dielectrics," *J. Mater. Chem. C*, vol. 7, p. 1955, 2019, doi: 10.1039/c8tc05736b.

[23] R. I. Hegde, C. C. Hobbs, L. Dip, J. Schaeffer, and P. J. Tobin, "Impact of metal–oxide gate dielectric on minority carrier lifetime in silicon," *Appl. Phys. Lett.*, vol. 80, no. 20, pp. 3850–3852, May 2002, doi: 10.1063/1.1480883.

[24] R. L. Nigro, E. Schiliro, C. Tudisco, G. G. Condorelli, P. Fiorenza, H. Gargouri, and F. Roccaforte, "Thermal and plasma-enhanced atomic layer deposition of hafnium oxide on semiconductor substrates," in *Proc. IEEE 9th Nanotechnol. Mater. Devices Conf. (NMDC)*, Oct. 2014, pp. 112–115, doi: 10.1109/NMDC.2014.6997435.

[25] Y. C. Chang, M. L. Huang, Y. H. Chang, Y. J. Lee, H. C. Chiu, J. Kwo, and M. Hong, "Atomic-layer-deposited Al_2O_3 and HfO_2 on GaN: A comparative study on interfaces and electrical characteristics," *Microelectron. Eng.*, vol. 88, no. 7, pp. 1207–1210, Jul. 2011, doi: 10.1016/J.MEE.2011.03.098.

[26] R. Puthenkovilakam, M. Sawkar, and J. P. Chang, "Electrical characteristics of postdeposition annealed HfO2 on silicon," *Appl. Phys. Lett.*, vol. 86, no. 20, pp. 1–3, 2005, doi: 10.1063/1.1927273.

[27] Y. Oshima, Y. Sun, D. Kuzum, T. Sugawara, K. C. Saraswat, P. Pianetta, and P. C. McIntyre, "Chemical bonding, interfaces, and defects in hafnium oxide/germanium oxynitride gate stacks on Ge(100)," *J. Electrochem. Soc.*, vol. 155, no. 12, p. G304, 2008, doi: 10.1149/1.2995832.

[28] D. Biswas, A. Chakraborty, and S. Chakraborty, "Role of annealing temperature in the oxide charge distribution in high-κ-based MOS devices: Simulation and experiment," *J. Comput. Electron.*, vol. 15, no. 3, pp. 795–800, Sep. 2016, doi: 10.1007/s10825-016-0829-y.

[29] A. B. Gougam, B. Rajab, and A. Bin Afif, "Investigation of c-Si surface passivation using thermal ALD deposited HfO_2 films," *Mater. Sci. Semicond. Process.*, vol. 95, pp. 42–47, Jun. 2019, doi: 10.1016/j.mssp.2019.02.012.

[30] J. Gope, Vandana, N. Batra, J. Panigrahi, R. Singh, K. K. Maurya, R. Srivastava, and P. K. Singh, "Silicon surface passivation using thin HfO_2 films by atomic layer deposition," *Appl. Surf. Sci.*, vol. 357, pp. 635–642, Dec. 2015, doi: 10.1016/J.APSUSC.2015.09.020.

[31] K. Yee, "Numerical solution of initial boundary value problems involving Maxwell's equations in isotropic media," *IEEE Trans. Antennas Propag.*, vol. AP-14, no. 3, pp. 302–307, May 1966, doi: 10.1109/TAP.1966.1138693.

[32] Q. Y. Zeng, W. J. Wang, J. Wen, P. X. Xu, W. D. Hu, Q. Li, N. Li, and W. Lu, "Dependence of dark current on carrier lifetime for InGaAs/InP avalanche photodiodes," *Opt. Quantum Electron.*, vol. 47, no. 7, pp. 1671–1677, Jul. 2015, doi: 10.1007/s11082-014-0024-y.

[33] M. D. Laurentis and A. Irace, "Optical measurement techniques of recombination lifetime based on the free carriers absorption effect," *J. Solid. State. Phys.*, vol. 2014, pp. 1–19, Jun. 2014, doi: 10.1155/2014/291469.

[34] C. M. Iaru, "Characterization of hafnium oxide thin films for applications in high eciency c-Si solar cells," Student thesis, Oct. 2015.

[35] B. W. H. van de Loo, "On the hydrogenation of Poly-Si passivating contacts by Al_2O_3 and SiNx thin films," *Sol. Energy Mater. Sol. Cells*, vol. 215, Apr. 2020, Art. no. 110592, doi: 10.1016/j.solmat.2020.110592.

[36] R. Prasher, D. Dass, and R. Vaid, "Al/HfO_2/Si gate stack with improved physical and electrical parameters," in *Proc. 29th Int. Conf. VLSI Design 15th Int. Conf. Embedded Syst. (VLSID)*, Jan. 2016, pp. 334–337, doi: 10.1109/VLSID.2016.71.