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A Highly Efficient Time-Based MPPT Circuit With Extended Power Range and Minimized Tuning Switching Frequency

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ABSTRACT This paper presents a highly efficient time-based maximum power point tracking (TB-MPPT) circuit with an enhanced three-dimensional tuning method. In the proposed circuit, firstly, the reconfigurable switched capacitor dc-dc converter with three conversion ratios is used to extend power range. The conversion ratio is selected according to input voltage level to avoid large charge redistribution loss. Secondly, the proposed algorithm can find the maximum power point with the minimum tuning switching frequency and capacitance control knob to reduce power loss, which results in high power conversion efficiency (PCE). The TB-MPPT circuit is fabricated with a 180nm CMOS process and has an active area of 0.42mm^2. The measured results achieve a peak PCE of 90.4%, a peak power tracking efficiency of 99.6%, and the output power of 52μW in an energy harvesting system with four commercial PV cells.

INDEX TERMS Energy harvesting system, extended power range, maximum power point tracking circuit, switched capacitor dc-dc converter.

I. INTRODUCTION

With the recent development of the Internet-of-Everything (IoE), humans, processes, data, and things are intelligently connected in ways that are more relevant and valuable than ever before [1]. The wireless sensor network (WSN) has been created to communicate and process the environment information. In such a network, the distributed sensors (or smart nodes) should be integrated with System-on-Chip (SoC) and wireless transceivers [2]. To power these nodes, several renewable energy sources such as photovoltaic (PV) [3]–[22], thermoelectric generator (TEG) [8], [20]–[28], piezoelectric [4], [21], [29], [30], and radio frequency (RF) energy [31], [32] are used. Among these energy sources, PV is attracting considerable attention as an energy source for smart nodes due to its low cost and high-power density [33]. Fig. 1 shows a block diagram of a typical IoE SoC smart node using an energy harvesting system (EHS) with PV cells. Because the IoE load consists of different types of blocks, such as ADC, DSP, transceiver, and sensor, it is powered by different power sources. Therefore, Multiple-Output Point of Load Conversion (MOPLC) is also required [34]. One of the most important factors in EHS is the maximum power point tracking (MPPT) circuit that guarantees the EHS operates at the maximum efficient power under various light intensities and temperatures. In particular, the MPPT circuit matches the impedance of the sc dc-dc converter and the impedance of the PV cells to find Maximum Power Point (MPP) using the Power Tracking block. Since the sc dc-dc converter is used, there are three control

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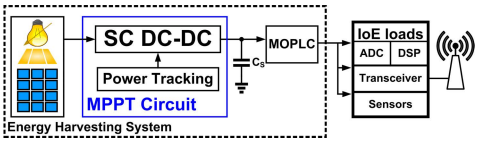


FIGURE 1. Block diagram of IoE SoC smart node with energy harvesting system.

knobs to adjust the impedance of the converter for finding the MPP: conversion ratio (CR), capacitance, and switching frequency [35]. Based on these impedance variables, many MPPT circuits have been exploited to maximize the power efficiency of EHS. Although significant power performance can be achieved, there were different problems depending on the combination of the three control knobs. Here a type of MPPT circuit is addressed that uses an n-Dimensional (e.g., 1-D, 2-D), where n represents the number of simultaneous control knobs that the system utilizes to find MPP. Initially, a 1-D MPPT circuit is proposed using a capacitor bank as a single impedance control knob [14]. The system demonstrates high power conversion efficiency (PCE) because the capacitor bank does not consume standby power. However, the use of a single CR in [14] causes a small input voltage range and large Charge Redistribution Loss (CRL) [5], [8], [13]. In addition, if the MPPT circuit needs to extract more power from the PV cells, a large capacitor size for the converter is usually required. To increase the input voltage range, the [8] adopted a two-dimensional (2-D) MPPT circuit that tunes the CR and switching frequency. Although the input voltage range is extended, the sc dc-dc converter requires a sufficient number of CR to find the MPP accurately, which in turn requires many capacitors and power switches, resulting in a large power loss. Using CR as a control knob in the MPPT procedure also causes a large CRL. Instead, the CR must be defined depending on the ratio between the regulated output voltage of the sc dc-dc converter and the output voltage of PV cells. Moreover, the switching frequency adjustment method increases the switching loss of the converter. In [8], the highest available frequency is applied at the start of the MPPT procedure, resulting in high power loss. A three-dimensional (3-D) MPPT circuit [13] has been reported to solve the problems encountered in the previous two tasks. Several CR are used and selected based on the output voltage level of the PV cells to reduce the CRL and extend the input voltage range. The switching frequency tuning is then used only to regulate the output voltage under different load conditions. The system in [13] uses switch width modulation to obtain high power efficiency in idle mode. By utilizing the three control knobs, the system can have a wide input voltage range and a large output power range while CRL is reduced. One disadvantage of the system with three control knobs is that the energy collected from the PV cells is greater than the energy required by the load side, the system wastes redundant power. Moreover, the design is complicated because the system requires sophisticated

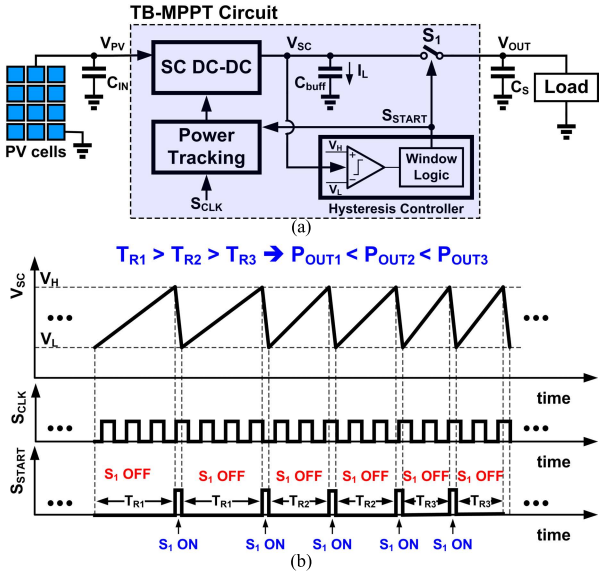


FIGURE 2. (a) Block diagram of EHS with TB-MPPT circuit and (b) its timing diagram.

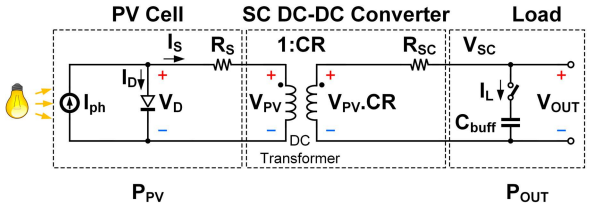


FIGURE 3. Model of PV cell with sc dc-dc converter.

sub-devices such as Digital Processing Unit and switch width modulator.

To overcome the aforementioned challenges, an enhanced 3-D time-based MPPT (TB-MPPT) circuit is proposed with the following characteristics. Firstly, a reconfigurable sc dc-dc converter with three CRs is used to extend the power range. Here, the CR is selected according to the voltage level of the PV cells to avoid large CRL. Secondly, the proposed algorithm finds the MPP with minimum tuning switching frequency and capacitance control knob to reduce the power loss of the system.

The rest of this paper is organized as follows. The proposed MPPT circuit is discussed in Section II. Section III describes the architecture and circuit implementation of the proposed MPPT circuit. Section IV explains the measurement results, and finally, Section V concludes this paper.

II. PROPOSED ENHANCED 3-D TB-MPPT CIRCUIT

A. CONCEPT OF EHS WITH TB-MPPT CIRCUIT

Fig. 2(a) shows the simplified architecture of EHS. It consists of 3 main parts: PV cells, TB-MPPT circuit, and Load [14]. The TB-MPPT circuit is the main part of the EHS, and its operation principle can be described as follow. The sc dc-dc converter converts power from PV cells and provides it to the Load. Meanwhile, the Hysteresis Controller (HC)

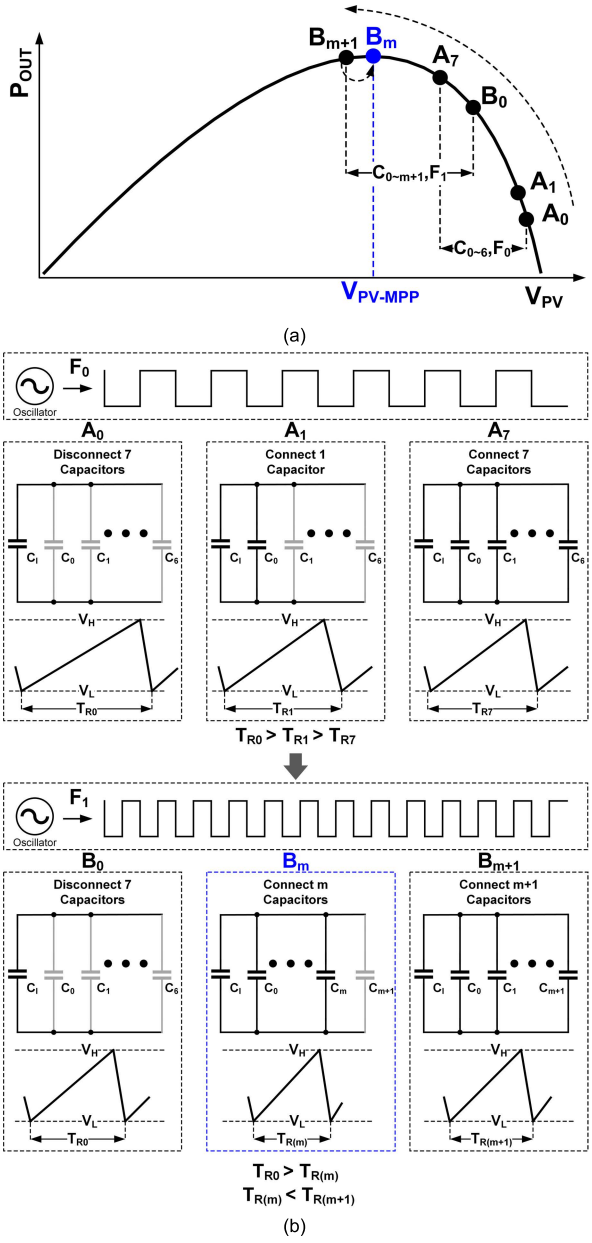


FIGURE 4. (a) Hill climbing algorithm in proposed MPPT circuit and (b) Capacitor bank configuration and switching frequency setting.

regulates the output voltage (through the V_{SC}) according to the reference voltages (V_H and V_L). The timing diagram of the HC is shown in Fig. 2(b). Initially, the V_{SC} is lower than V_L. The comparator operation within the HC will then switch S_1 off. When the V_{SC} is disconnected from the Load, the energy in the PV cells is now charged in the C_{buff}. Therefore, the V_{SC} increases gradually. When the V_{SC} reaches V_H, S_1 is turned on by the S_{START} signal and emits the energy inside the C_{buff} to the Load. The switching operation of S_1 is controlled by the S_{START} signal. This signal is activated when the V_{SC} reaches the high threshold level (V_H) of the comparator and deactivated when the V_{SC} reaches the V_L. This means that the time interval (T_R) between adjacent S_{START} pulses can be used to estimate the charging time required for the C_{buff} from V_L to V_H at the given energy of the PV cells. The charging time varies depending on the power level of the PV cells. Therefore, The T_R represents the power information of PV cells. The MPPT circuit uses T_R to monitor the amount of power currently collected while the impedance of the sc dc-dc converter is adjusted to provide MPP to the Load. Because the voltage and current sensors are avoided and the charging time is only needed to obtain MPP, this architecture is called TB-MPPT. To provide details on the proposed circuit, we will provide an analysis of the relationship between T_R, output power, and the output impedance of the sc dc-dc converter, in the next section.

B. PROPOSED ENHANCED 3-D TB-MPPT CIRCUIT

In this section, the analysis of tuning variables is presented by modeling the EHS. Then, the proposed MPPT circuit will be described. The quantitative relationship between charging time T_R and output power P_{OUT} can be modeled using the steady-state assumption, as shown in Fig 3. PV cells is modeled as a light-controlled current source I_{PH} with a parallel diode and a series resistor R_S. The sc dc-dc converter can be modeled as a DC transformer having a conversion ratio of CR with an output impedance R_{SC}. The Load is modeled as a buffer capacitor C_{buff} and a gated switch with a charging current of I_L. V_{SC} is regulated voltage between a boundary of desired voltage level (V_H, V_L). According to the steady-state assumption, the ripple of V_{SC} between V_H and V_L can be neglected, and V_{SC} equals V_{OUT}. By applying Kirchhoff's voltage law to the input node of the DC transformer, the PV cells output voltage V_{PV} can be modeled as:

$$V_{PV} = V_D - CR_i \times I_L \times R_S = \frac{V_{OUT} + R_{SC} \times I_L}{CR_i} \quad (1)$$

where V_D is the diode voltage. The average current I_L during the entire charging period T_R can be specified as:

$$I_L = \frac{C_{buff} \times (V_H - V_L)}{T_R} \quad (2)$$

In addition, the P_{OUT} can be expressed as:

$$P_{OUT} = V_{OUT} \times I_L = V_{OUT} \times \frac{C_{buff} \times (V_H - V_L)}{T_R} \quad (3)$$

As can be seen from Eq. (3), P_{OUT} is inversely proportional to the T_R. Therefore, T_R can be used to monitor trends in P_{OUT} during the MPPT procedure. From (1) and (2), T_R can be expressed as:

$$T_R = \frac{R_{SC} + CR_i^2 \times R_S}{CR_i} \times \frac{C_{buff} \times (V_H - V_L)}{V_D - \frac{1}{CR_i} \times V_{OUT}} \quad (4)$$

where CR_i, C_{buff}, V_H, V_L, and V_{OUT} are constant. The value of the PV cells source resistance R_S is also constant under a given light intensity or temperature condition. V_D is the dependent variable of the R_{SC}. When considering the constant (or near-constant) variable, the only concerns lie with the variables T_R and R_{SC}, where T_R represents the power information of PV cells as described in the previous

section. Therefore, the MPPT procedure can be performed by monitoring the P_{OUT} via T_R while utilizing the R_{SC} as the control knob. To determine how to adjust the R_{SC}, the R_{SC} must be reviewed. In [35], R_{SC} is a combination of two impedance components: Slow Switching Limit R_{SSL} and Fast Switching Limit R_{FSL}, as follows:

$$R_{SC} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} = \sqrt{\left(\sum_{i\in caps} \frac{\left(a_{c,i}^j\right)^2}{2 \times C_i \times F_{sw}}\right)^2 + \left(\sum_{i\in switches} R_i \times (a_{r,i})\right)^2} \tag{5}$$

where R_i is the on-resistance of each switch, C_i is the capacitance of each capacitor, F_{SW} is the switching frequency, and $a_{c,i}$, $a_{r,i}$ are the capacitor multipliers and the switch multipliers, respectively. The $a_{c,i}$, $a_{r,i}$ are defined by the CR of the sc dc-dc converter. For ultra-low power applications, the sc dc-dc converter in the MPPT circuit operates at a low switching frequency to reduce power loss. Therefore, it can be assumed that the R_{FSL} is very small and negligible. Thus, the R_{SC} can be simplified as:

$$R_{SC} \approx \sum_{i\in caps} \frac{\left(a_{c,i}^j\right)^2}{2 \times C_i \times F_{sw}} \tag{6}$$

Equation (6) shows that there are three parameters of interest ($a_{c,i}$, C_i, F_{SW}) that can be adjusted to change the R_{SC}. To use these three parameters in MPPT operation effectively, each parameter must be analyzed. First, among the three parameters, $a_{c,i}$, which is determined by the CR of the sc dc-dc converter, shows a quadratic relation with R_{SC}. Thus, adjusting CR results in a rapid change in R_{SC}, which acts as a coarse tuning parameter in the design, as reported in [8]. However, using CR tuning for R_{SC} has a disadvantage. In the EHS, the PCE of the sc dc-dc converter is limited by CRL [13]. For a given regulated output voltage, the high PCE of the sc dc-dc converter is obtained only when using the optimal CR, which is determined by the ratio between the regulated output voltage and the input voltage level. Since the CR tuning is used in the MPPT procedure, the MPPT circuit adjusts the CR to obtain the highest power tracking point. In this process, the CRL is ignored because the MPPT procedure only matches the impedance of the PV cells with the sc dc-dc converter. For this reason, the CR captured during the MPPT procedure can cause a large CRL that degrades the PCE, which leads to the choice that the CR must be configured based on the voltage level of the PV cells. Second, after determining the CR, the MPP of the EHS could be obtained by using the capacitance and the switching frequency as fine-tuning parameters. To obtain the large power range, both switching frequency and capacitance should be used in MPPT procedure. The capacitance tuning can be done using a Capacitor Bank which does not consume large power loss. On the other hand, adopting the switching frequency tuning

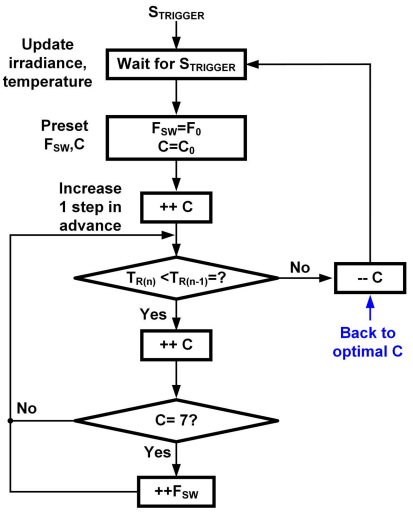


FIGURE 5. Flow chart of hill climbing algorithm in proposed MPPT circuit.

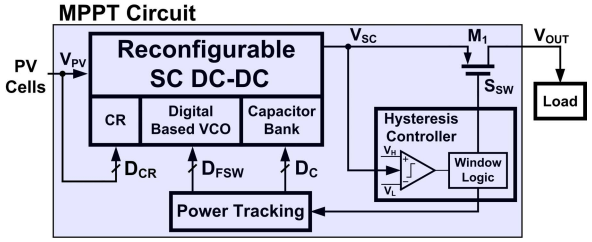


FIGURE 6. Simplified block diagram of proposed MPPT circuit.

option requires a consideration of the relationship between different parameters. Analytical approaches to understand the problems of using switching frequency tuning will be introduced as follow: As can be seen from Eq. (4), T_R is a function of R_{SC}. Then, T_R could be written as follows with reference to Eq. (6):

$$T_R = f\left(\frac{a_{c,i}^2}{2 \times C_i \times F_{SW}}\right) \tag{7}$$

Here, T_R is a time interval between S_{START} pulses in Fig. 2(b), wherein T_R could be defined as the number of pulses of S_{CLK}. Since one cycle period of S_{CLK} is the reciprocal of the switching frequency, the following relationship is established,

$$T_R = N \times \frac{1}{F_{SW}} \tag{8}$$

where N is the number of switching cycles between adjacent S_{START} pulses. Due to the integer multiple relationship between T_R and switching cycle $1/F_{SW}$, the MPPT procedure using the switching frequency tuning parameter shows a sudden jump from one point to another. Therefore, the F_{SW} parameter cannot be used directly as a tuning parameter for the MPPT procedure. To overcome this problem and seamlessly extend the MPPT tracking range, the capacitance tuning is used first in MPPT procedure. If the MPP is out of the range using the specified capacitance value, the system increases the switching frequency to expand the search area

to explore the MPP. To minimize the power consumption of a given system, the minimum switching frequency is initially used for MPP tracking. This process is repeated until the MPPT circuit finds MPP with minimum power consumption. In this work, the programmable ring oscillator provides several different switching frequencies with a simple architecture. It can be concluded that the proposed tuning method uses three parameters to find MPP effectively. The CRL is improved, and the power loss of the system is also minimized.

The hill-climbing algorithm of the proposed system based on the capacitance- switching frequency double-control knob is shown in Fig. 4. The Fig. 4(a) visualizes the entire hill-climbing algorithm starting at the rightmost corner A_0, and Fig. 4(b) shows the Capacitor Bank configuration and switching frequency at each stage along the hill-climbing curve in Fig. 4(a). Initially, the MPPT procedure begins with the minimum capacitance (C_I only) and the minimum switching frequency (F_0), where the current power level extracted from the PV cells is A_0. Capacitors $C_{0\sim6}$ are all disconnected from the Capacitor Bank (denoted in grey color). Then, through the operation of the Hysteresis Controller, the V_{SC} signal represents a serrated signal, and the charging time T_{R0} is evaluated through the internal unit of the Power Tracking in Fig. 2(a). The MPPT procedure starts with the minimum value for each control knob, so the system increases the capacitance value by one step as described to move to the next power point. The system is now in A_1 with a clearly higher power point than the previous one A_0. This could be determined by comparing the charging time of T_{R1} and the previous one T_{R0}. The shorter duration of T_{R1} means that the system will need less time to charge the capacitor C_{buff}, which means the system will move to the MPP. By following this strategy, the system uses the Capacitor Bank to increase the capacitance under a given frequency setting until the A_7 power point is reached. Because the time duration of T_{R7} is still shorter than the previous T_{R6}, the system now extends the power range of the EHS by increasing the frequency of the oscillator by one step (F_1). The Capacitor Bank is now reset and has a minimum capacitance, so the system moves back slightly to point B_0. The MPPT procedure is now repeated from B_0, increasing only the capacitance. To illustrate the situation when the system finds the MPP, it is assumed that the MPP is located in B_m of Fig. 4(a). Once the system reaches the B_m, the $T_{R(m)}$ is still shorter than the previous one $T_{R(m-1)}$. Therefore, the system increases the capacitance one step further and moves to the B_{m+1}. However, B_{m+1} is out of MPP, and accordingly, the period of $T_{R(m+1)}$ is longer than the period of $T_{R(m)}$. By detecting this change, the system verifies that the MPP has been found and disconnects the last capacitor in the Capacitor Bank. A flowchart of the proposed hill-climbing algorithm is shown in Fig. 5. Note that the system is initially idle. When the $S_{TRIGGER}$ signal is provided, the MPPT procedure is started, and the system tunes the capacitance and switching frequency to find the MPP.

The design approach of proposed circuit is shown in Fig. 6. As can be seen, the CR of reconfigurable sc dc-dc converter

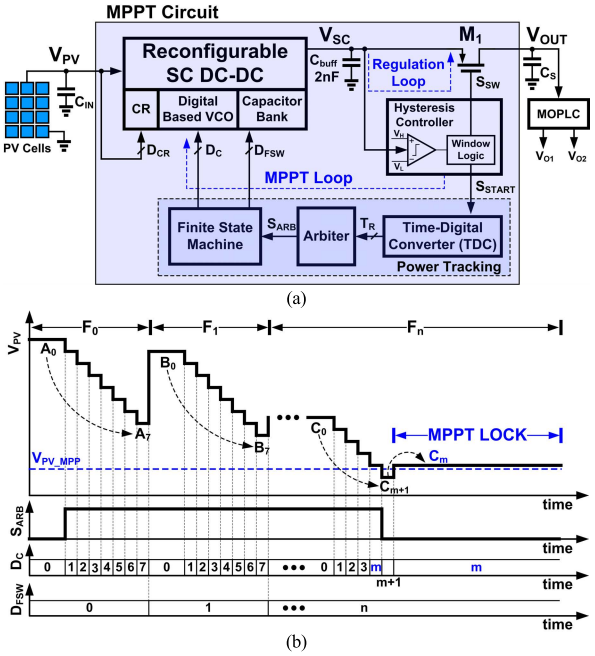


FIGURE 7. (a) Block diagram of EHS with proposed MPPT circuit and (b) its timing diagram.

is first configured according to input voltage level of PV cells, which results in minimizing the CRL. Then, the Power Tracking unit with proposed tuning method finds MPP with minimum switching frequency and extended power range. To adjust the switching frequency and capacitance without large power dissipation, the Digital-Based VCO and Capacitor Bank are used, respectively. By using enhanced 3-D tuning method, the proposed circuit can solve the problems of the previous works and sufficiently improve the performance of EHS. The detail of circuit implementation will be described in Section III.

III. CIRCUIT IMPLEMENTATION

In this section, the detail of circuit implementation and design consideration will be described based on the design approach in Section II. Fig. 7(a) shows the EHS with the proposed enhanced 3-D TB-MPPT circuit. The MOPLC is included in this design to provide two regulated output voltages as mentioned in Section I and it is not the main objective of this work. The Proposed MPPT circuit consists essentially of two control loops: Regulation Loop, and MPPT Loop. The Regulation Loop ensures that the voltage level of the V_{SC} is within the two trip points (V_H and V_L) of the Hysteresis Controller, as described in the previous section. Meanwhile, the MPPT loop uses the output signal from the Hysteresis Controller (S_{START}) to adjust the switching frequency and capacitance to find the MPP in a given working condition of PV cells. The main idea of determining the optimal power point here arises from the simple fact that the time interval between adjacent S_{START} pulses indirectly represents the power information harvested from the PV cells. (The pulse generated from two consecutive S_{START} pulses will be denoted as T_R hereafter).

In the proposed system, a narrower T_R pulse due to a change in switching frequency or capacitance means that the system moves to a better power point. Therefore, the Power Tracking compares the pulse width of successive T_R pulses and determines whether the capacitance or switching frequency should be changed in a particular way. For this function, the Time-Digital Converter (TDC) first generates a T_R pulse based on two consecutive S_{START} signals, and then converts the time duration of the T_R pulse into digital code. The Arbiter then compares the digital code of the current charging time $T_{R(n)}$ pulse width and the previous charging time $T_{R(n-1)}$ pulse width stored in FFs. The main output signal of the Arbiter is a S_{ARB} signal that remains at a logical high level if the $T_{R(n)}$ is less than the $T_{R(n-1)}$. The high level of S_{ARB} allows the Finite State Machine (FSM) to control the frequency of the Digital-Based VCO and the capacitance of Capacitor Bank by changing the D_{FSW} and D_C, respectively. If the system finds an MPP, that is, if the current $T_{R(n)}$ is longer than the previous $T_{R(n-1)}$, the S_{ARB} signal is disabled, and the tracking process is interrupted. Fig. 7(b) shows a detailed timing diagram of the MPPT procedure. The capacitance and switching frequency initially begin with the minimum values ($D_C = D_{FSW} = 0$), and the S_{ARB} is elevated when the first S_{START} signal is received (not shown in the figure). The MPPT loop then adjusts the capacitance value of the Capacitor Bank based on the pulse width comparison between two consecutive T_R pulses. As the system starts with the lowest R_{SC} value due to the minimum capacitance and switching frequency, the capacitance value naturally increases, so the V_{PV} value decreases as the FSM is updated. This will continue as long as the S_{ARB} signal remains high, and the system will explore the power range from A_0 to A_7 as the capacitance changes from minimum to maximum value. If the capacitance step has reached its maximum value (when $D_C = 7$) and the S_{ARB} is still high, this means that the system cannot find the MPP with the combination of the current switching frequency setting and the capacitance range. Therefore, the FSM increases the switching frequency by one step (D_{FSW} from 0 to 1), and resets the capacitance step (D_C returns to 0). The EHS now explores the power range extended from B_0 to B_7. Now we will explain the situation where the output voltage of the PV cells reaches V_{PV_MPP} as the system approaches MPP. At the switching frequency step (F_n) and capacitance step (C_{m+1}), the V_{PV} exceeds V_{PV_MPP}. At this point, the system passes through the MPP, and the corresponding pulse width is wider than the previous T_R. The Arbiter then finds an MPP and pulls the S_{ARB} lower, causing the capacitance value to return one step back, making the V_{PV} the closest value to the V_{PV_MPP}. The EHS then locks the MPP and turns off the Power Tracking to save power while using the MPP.

A. RECONFIGURABLE SC DC-DC CONVERTER

The energy harvesting from the PV cells is performed through the sc dc-dc converter, where there are three main parts: Reconfigurable sc dc-dc converter, Digital-based VCO, and Capacitor Bank. Fig. 8(a) shows a simplified sc dc-dc converter with three conversion ratios (2x, 3x, 4x) and the configuration of power switches. Details of the Capacitor Bank, and the Digital-based VCO with its simulation result are shown in Fig. 8(b) and (c), respectively. In the proposed system, a sc dc-dc converter with three CRs is used to prevent CRL as mentioned previously. Moreover, by adaptively selecting the optimal CR, the system can accommodate a wide range of input voltage from PV cells, leading to improved PCE. The switching algorithm of the sc module is optimized to reduce switching loss and bottom-plate

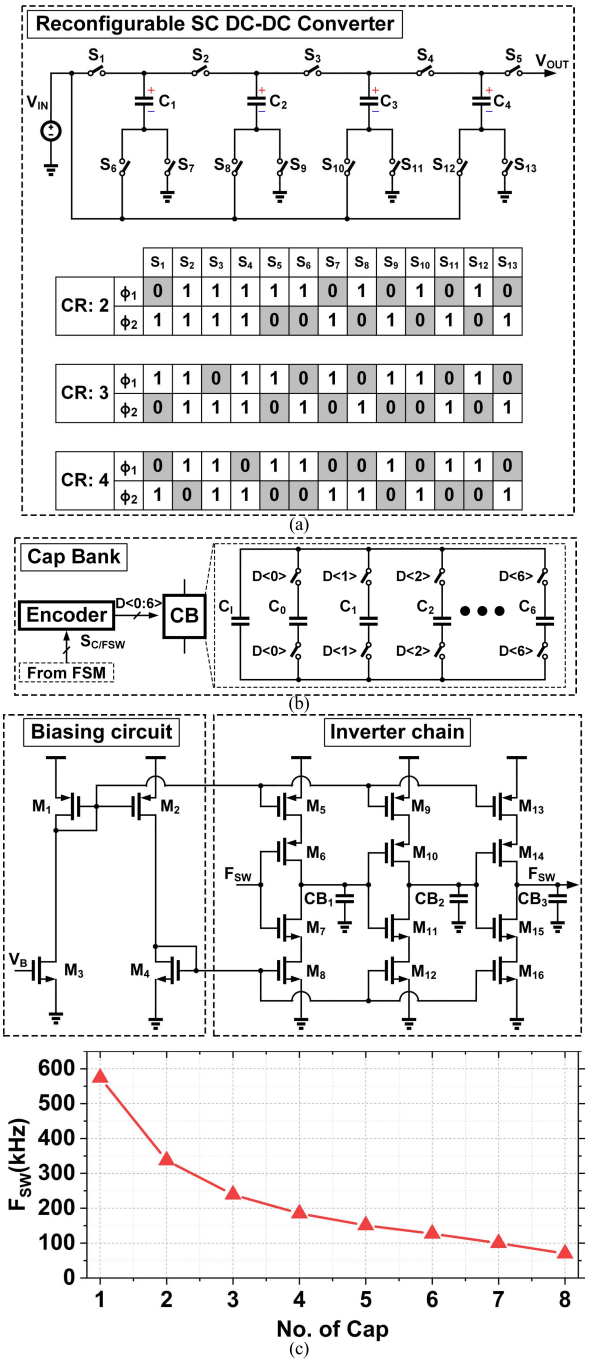


FIGURE 8. (a) Schematic of sc dc-dc converter, (b) Capacitor bank, and (c) Digital-based ring oscillator with its simulated result.

capacitor loss. The Capacitor Bank acts as a unit capacitor of the sc module. As shown in Fig. 8(b), the digital code from the FSM is encoded into the switch control signal (D<0:6>) of the unit Capacitor Bank (CB), wherein the unit CB has eight identical capacitors (C_I, $C_0 \sim C_6$). The capacitor C_I is the default capacitor, and the other capacitors are used as variable capacitors by its control signal. When all capacitors are used, the total capacitance is 57.6 pF which means that the capacity of a single capacitor is 7.2 pF. The total capacitance value is determined by considering the input voltage range of MPPT circuit while the single capacitor value is selected to meet tracking accuracy requirement. The Capacitor Bank is used to adjust the capacitance of the sc dc-dc converter, while the Digital-based VCO is used to control the switching frequency of other MPP tracking options. The Digital-based VCO circuit consists of a biasing circuit and an inverter chain. The biasing circuit provides an appropriate voltage level for the inverter chain. The inverter chain comprises three stacked inverters connected in series, with the upper and lower transistors gaining control voltage from the biasing circuit and the center two transistors operating as the inverter chain. A programmable Capacitor Bank is placed between the two inverters (CB_x) to control the oscillation frequency of the Oscillator. The structure of Capacitor Bank is similar as CB block in Fig. 8(b). The total capacitance of the capacitor array is 1.6 pF when all capacitors are connected, where the capacitance of the unit capacitor ($C_{0\sim6}$) is 200 fF. A three-stage ring oscillator having a capacitor array can generate an output signal in a frequency range of 70 kHz to 600 kHz as shown in the Fig. 8(c). With this degree of frequency variation, the proposed EHS can handle the throughput power range from 10 μW to 52 μW.

B. HYSTERESIS CONTROLLER

The Hysteresis Controller regulates the V_{SC} level within two boundary voltages, V_H and V_L. Detailed circuit implementation and timing diagram are shown in Fig. 9. The Hysteresis Controller consists of two comparators (A_1, A_2) followed by a flip-flop and logic gates. Here's how the Hysteresis Controller works: Initially, the V_{SC} is 0, so $S_{START} = S_F = 0$, $S_{SW} = 1$. Thereafter, in Fig. 7, if the S_{SW} signal turns off the M_1 transistor, the system charges C_{buff}, and accordingly, the V_{SC} level gradually rises. When the V_{SC} reaches V_H, both S_{START} and S_F signals become high levels. The A_2 comparator is then activated via the S_F signal. At the same time, the comparator output is zero, resulting in $S_{SW} = 0$. Therefore, the low state of the S_{SW} signal turns on the M_1 transistor, the charge inside the C_{buff} capacitor is now transferred to the MOPLC. This causes the V_{SC} to show a sharp drop and reach V_L level. When the V_{SC} falls below the V_L, the A_2 comparator output becomes 1, S_{RST} becomes 0, and eventually, the S_{SW} signal becomes 1, which disconnects the C_{buff} from the MOPLC. This sequence occurs repeatedly and adjusts the V_{SC} level within V_H and V_L. Selecting a structure suitable for both comparators requires a consideration of the operating conditions of each comparator

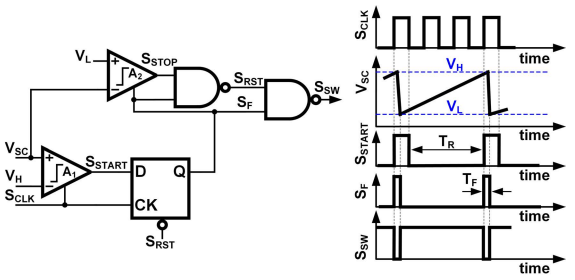


FIGURE 9. Schematic of hysteresis controller.

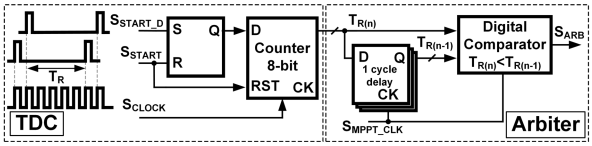
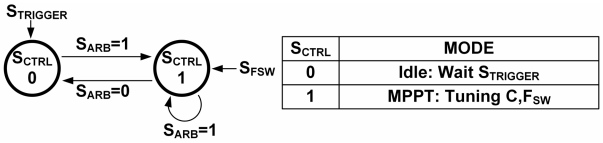


FIGURE 10. Schematic of TDC and arbiter.



S_{CTRL}	MODE
0	Idle: Wait $S_{TRIGGER}$
1	MPPT: Tuning C,F_{SW}

FIGURE 11. Finite state machine.

during charging and discharging period. During the charging time, the V_{SC} is slowly charged. Therefore, the dynamic comparator structure can be used in A_1 to reduce power consumption. The V_{SC}, on the other hand, discharges very quickly during the discharge time. This suggests that continuous high-speed comparators are better for comparator A_2 to detect such a fast transition. Continuous high-speed comparators typically consume large amounts of power, but in our design, they are turned on for a short period of discharge (T_F), resulting in low average power consumption. It should be noted here that by measuring the distance between two consecutive S_{START} pulses, the charging time (T_R) during the operation of the Hysteresis Controller can be estimated. As discussed in the previous section, the timing information of the T_R will be transmitted to the MPPT circuit as power information of the PV cells.

C. TIME-DIGITAL CONVERTER(TDC) AND ARBITER

The Time-Digital Converter (TDC) and Arbiter units receive an output signal S_{START} from the Hysteresis Controller and check the time duration between adjacent S_{START} signals as the time delay between the signals indicates the current power level emitted from the PV cells. A schematic diagram of the TDC and Arbiter of the proposed EHS is shown in Fig. 10. As shown in the figure, all subunits are composed of digital logic gates, contributing to the high PCE of the system. With respect to the individual operation of the TDC and the Arbiter, the TDC initially receives the S_{START} pulse and generates one cycle delayed signal S_{START_D}. Two signals are used as a reset signal and set signals for SR-latch, respectively.

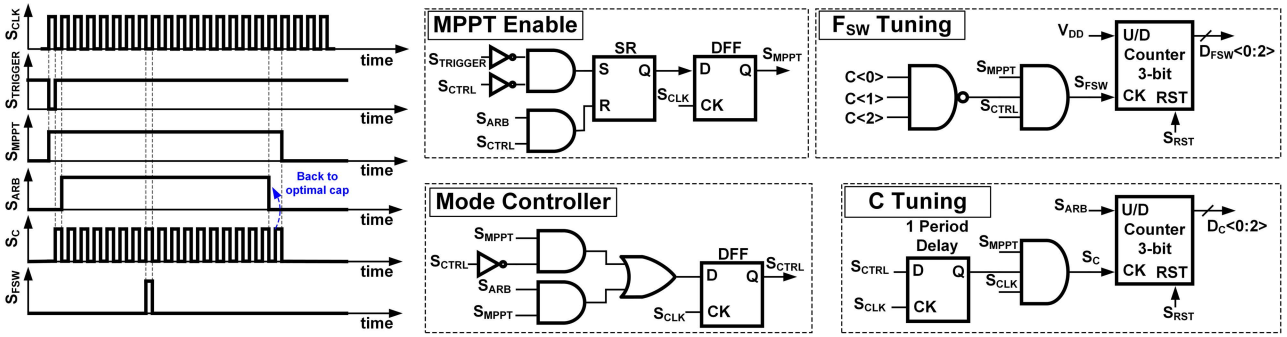


FIGURE 12. Schematic of FSM.

The output from the SR-latch then becomes a pulse with a width proportional to the delay between two consecutive S_{START} pulses (actually, one clock cycle delay less than the ideal). Note that, here the pulse width represents the power information of the EHS. The generated pulse is presented as a counter enable signal at the next 8-bit counter and the input pulse width is converted to digital code ($T_{R(n)}$) accordingly. This digital code is sent to Arbiter. In Arbiter, the digital code is stored and evaluated using DFF and Digital Comparator, respectively. Because the first digital codes do not represent the power information of PV cells correctly due to the transient response of V_{PV} after changing tracking point. Therefore, the 4-time lower frequency (S_{MPPT_CLK}) is used in Arbiter to guarantee that the V_{PV} is stable before evaluating the power information. The digital code ($T_{R(n)}$) containing the current power information is now compared to the previous power information stored in the DFF ($T_{R(n-1)}$). Based on the comparison results, the Arbiter activates the S_{ARB} signal when the system moves in the correct direction, such that the power from the PV cells increases or the current time delay decreases. This means that if the system detects an MPP, the S_{ARB} signal will be lowered due to the longer time delay in subsequent operations. Lastly, the time resolution of the digital counter is a function of the throughput power of the EHS and the magnitude of the C_{buff} capacitor. The proposed design shows that an 8-bit digital counter is sufficient based on the system clock (S_{CLOCK}) used.

D. FINITE STATE MACHINE (FSM)

The operation of the proposed EHS is controlled by a 1-bit finite-state machine (FSM). The state diagram and important signals of the 1-bit FSM are shown in Fig. 11. As shown in the figure, the two modes are idle ($S_{CTRL} = 0$) and MPPT ($S_{CTRL} = 1$), and the mode transition depends on the logic level of the S_{ARB} signal transmitted from the arbiter unit. The system is initialized to idle mode with $S_{CTRL} = 0$. When the $S_{TRIGGER}$ signal is transmitted from MCU to the EHS, the FSM switches $S_{CTRL} = 1$ to change the operation of the system to MPPT mode. Then, the MPP tracking operation occurs through the Regulation Loop and MPPT Loop, as described in Fig. 7(a). The MPP search continues with

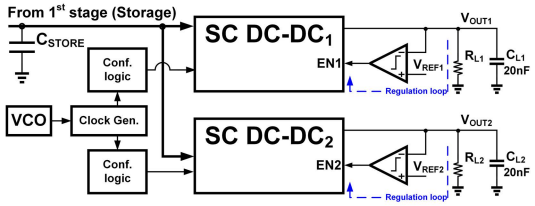


FIGURE 13. Schematic of MOPLC.

$S_{ARB} = 1$, and the proposed system adjusts the capacitance value or switching frequency until the monitored power of the Arbiter decreases. If this happens, it means that MPP has been found. Accordingly, the FSM switches the operating mode back to idle mode with $S_{CTRL} = 0$ and completes the MPPT procedure. A detailed implementation and timing diagram of the FSM is shown in Fig. 12. The FSM block consists of four sub-units: MPPT Enable, Mode Controller, F_{SW} Tuning, and C Tuning. As the unit's name suggests, the MPPT enable unit generates S_{MPPT} signal when the $S_{TRIGGER}$ signal is presented from the external. The S_{MPPT} signal then drives the Mode Controller, making the S_{CTRL} signal high, and the system starts MPP tracking operation. The system now uses two independent loops in the EHS to find MPP while the S_{ARB} signal is high by controlling the Capacitor Bank via D_C <0:2> or by controlling the switching frequency via D_{FSW} <0:2>. Tracking is maintained until the system finds the MPP. When the system reaches the MPP, the TDC and Arbiter switch the S_{ARB} signal to a low level, and eventually $S_{CTRL} = 0$ on the Mode Controller. The F_{SW} and C Tuning blocks then stop the FF update. In addition, when MPP is found, the FSM is turned off to save power consumption.

E. MULTIPLE OUTPUT POINT OF LOAD CONVERSION (MOPLC)

MOPLC is an essential unit to provide a stable regulated DC output voltage for each load block including ADC, sensor, or DSP in the IoT system as mentioned previously. The MOPLC unit can provide two different output voltages using two separate sc dc-dc converters as shown in Fig. 13. The upper (lower) sc dc-dc converter provides an output voltage of 3V (1.5V) using a fixed conversion ratio of 1(0.5).

To obtain sufficient PCE, the regulation loop uses a hysteresis control method. The operation of the regulation loop and the description of each block can be expressed as follow. First, VCO generates a signal at the switching frequency, where the frequency is determined by the optimization method [35] for minimizing the loss factors of the sc dc-dc converter. The Clock Gen. block then receives this signal and generates a non-overlapping clock. This clock signal is used as a control signal for each power switch of the sc dc-dc converter. The switching pattern of the power switch is defined by the Conf. Logic unit that provides the desired CR from the converter. The sc dc-dc converter compares the output voltages $V_{OUT1,2}$ with the reference voltages $V_{REF1,2}$ in the comparator and controls the output voltage in the regulation loop. This voltage regulation process can cause a large output voltage ripple in the comparator. Therefore, the 20nF load capacitor is used to improve the output voltage ripple.

IV. MEASUREMENT RESULTS

The proposed MPPT circuit is fabricated with a commercial 180nm CMOS process. Fig. 14 illustrates a chip micrograph. The MPPT circuit occupies an active area of 0.42 mm^2. Note that, much of the area is consumed by the dual-layer high-density metal-insulator-metal (MIM) on-chip capacitor in the capacitor module of sc dc-dc converter. Fig. 15 shows the measurement settings for MPPT circuit and a photo of the PV cells with a light sensor. The halogen lamp is used as an adjustable light source. The commercial PV cell (KXOB25-12 $\times$ 1F, 22mm $\times$ 7mm, 0.69V-46.7mA) is used to demonstrate the performance of the MPPT circuit. To startup the system, the C_S needs to be pre-charged above 2.5V which can be done using an auxiliary charge pump. The energy of C_S is used as a power source for control circuit. This startup circuit operates only once at the beginning of normal harvesting. In this work, the design is focused on exploring the relationship between MPPT and tuning variables. Thus, the auxiliary charge pump is not implemented. Once the control circuit is powered, the system operates based on the MCU's trigger signal. If MCU detects a change of the light intensity (greater than 100 lux) by monitoring analog output of the light sensor, a trigger signal ($S_{TRIGGER}$) is sent to MPPT circuit. Then, MPPT circuit starts finding MPP of the system. It is noted that the light sensor should be placed nearby the PV cells to guarantee that they receive the same light intensity as shown in Fig. 15(b). The output signals are captured by the oscilloscope to monitor the behavior of the output voltage regulation and MPP tracking performance. Based on the measurement settings, the transient response of the circuit is monitored at two different light intensities (150 lux and 600 lux), where two internal voltages (V_{SC} and V_{PV}) and two control signals ($S_{TRIGGER}$ and $MPPT_{EN}$) are shown in Fig. 16(a). As can be seen, once the MPPT circuit detects the $S_{TRIGGER}$ signal, the $MPPT_{EN}$ is set to high level to enable MPP tracking. When MPPT operation is initiated, two operation loops (Regulation loop and MPPT loop in Fig. 7) collaborate to seek MPP, in which the V_{SC}

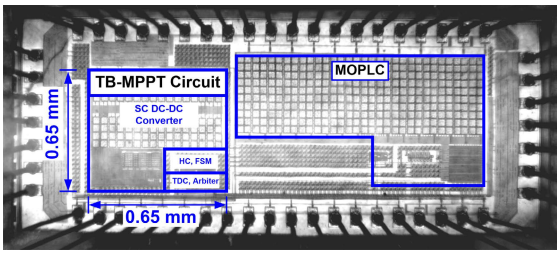


FIGURE 14. Die micrograph of proposed MPPT circuit and MOPLC.

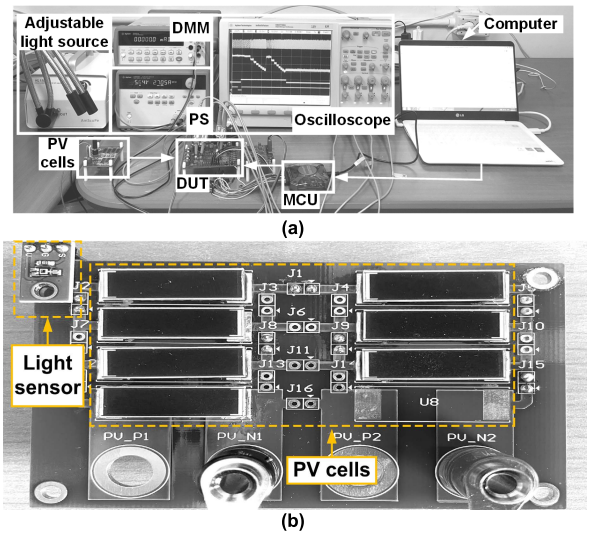


FIGURE 15. (a) Measurement setup, (b) PV cells with a light sensor.

level (regulated voltage within V_H and V_L) and the V_{PV} level (PV cell output voltage) are changed. If the applied luminosity is 150 lux, the MPPT circuit finds the MPP only with a seven-step change in Capacitor Bank (A_0 to A_6) without increasing the switching frequency step. At the beginning of the MPPT lock period, the capacitance is changed from A_6 to A_5, indicating that the MPPT point is close to A_5, so the system returns to the previous step and suspends MPPT operation. The V_{SC} level is also well regulated within the upper and lower bounding voltages with a voltage ripple of $\sim$220 mV. It is important to note that the system maintains the minimum switching frequency ($F_0 = 70$ kHz) from the start of MPPT operation, so that the system consumes the minimum power. The right measurement results of Fig. 16(a) show a situation in which the light intensity applied to the PV cells is changed to 600 lux. Because of the increased intensity of light, the system could not find MPP at the minimum switching frequency, and when the Capacitor Bank reaches its maximum value at the current switching frequency setting, the Power Tracking unit increases the switching frequency by one step. Eventually, the system tests four different switching frequencies from F_0 (70 kHz) to F_3 (151 kHz) before reaching the MPP. In addition to monitoring the overall tracking procedure, the regulated voltage level (V_{SC}) of the sc dc-dc converter and the output voltage of the PV cells (V_{PV})

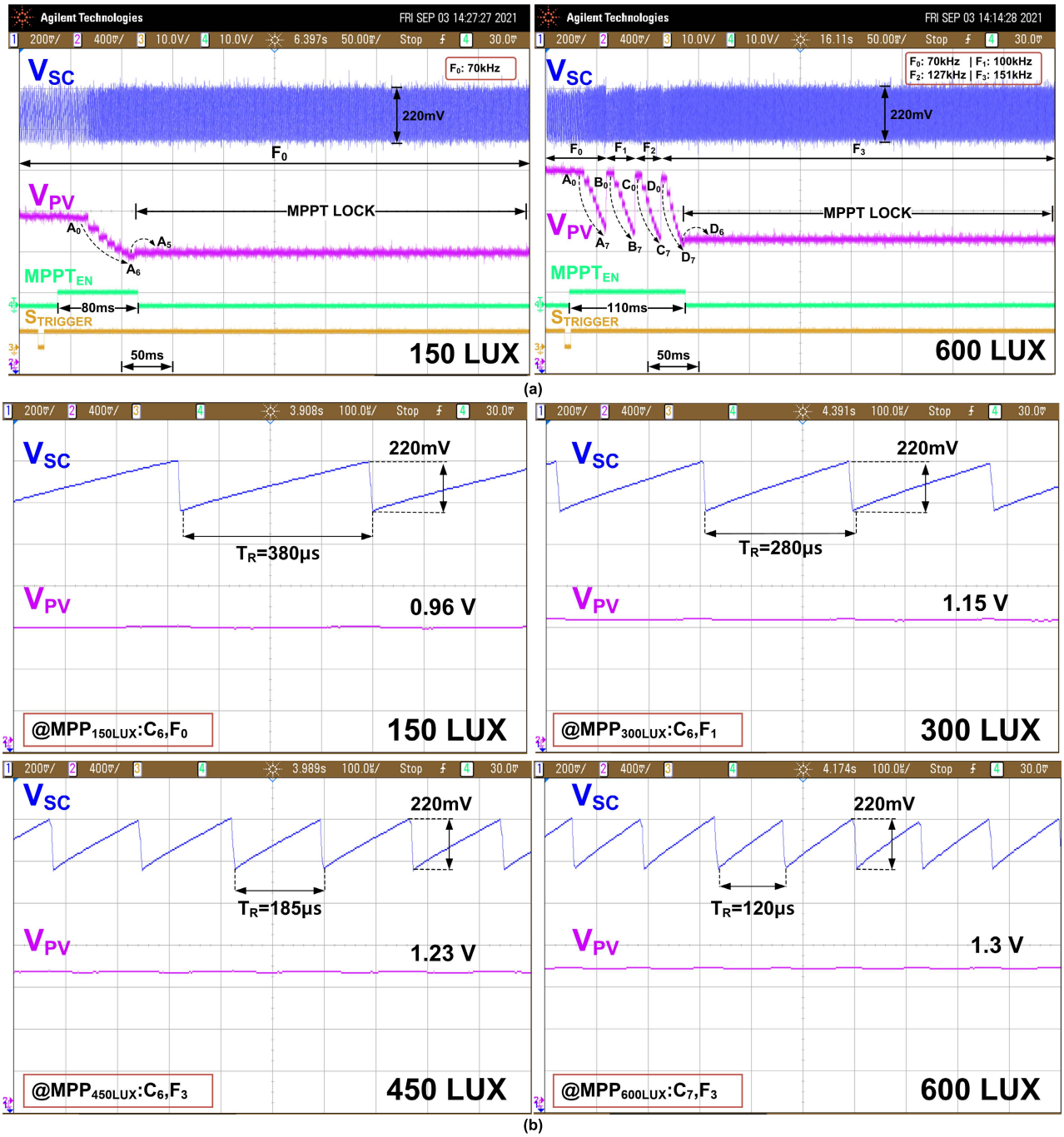


FIGURE 16. **(a) The tracking waveforms of proposed MPPT circuit when light intensities of 150 lux and 600 lux are applied, (b) collected MPPs at four different light intensities.**

are checked at four different light intensities after the MPP is found. Here, the charging time (T_R) at MPP locked state indirectly represents the current power level drained from the PV cells, which is affected by the intensity of the light. Obviously, T_R gets shorter (longer) as the light intensity increases (decreases). Fig. 16(b) shows that the optimal charging time at MPP (T_{R_MPP}) is measured to be 380 μs, 280 μs, 185 μs and 120 μs at different light intensities of 150 lux, 300 lux, 450 lux, and 600 lux, respectively. In addition, the output voltage of PV cells at MPPs with different light intensities are 0.96 V, 1.15V, 1.23V, and 1.3V, respectively. It is noteworthy here that the shorter period of one cycle V_{SC} signal at high light intensity confirms that the proposed MPPT circuit adjusts the switching frequency to find the MPP located far from the initial point.

To verify the dynamic tracking performance of the proposed MPPT circuit, the light source is adjusted to change the light intensity. The MCU then sends the trigger signal to the system by detecting the change of light intensity through a light sensor to invoke the MPPT operation. The two different

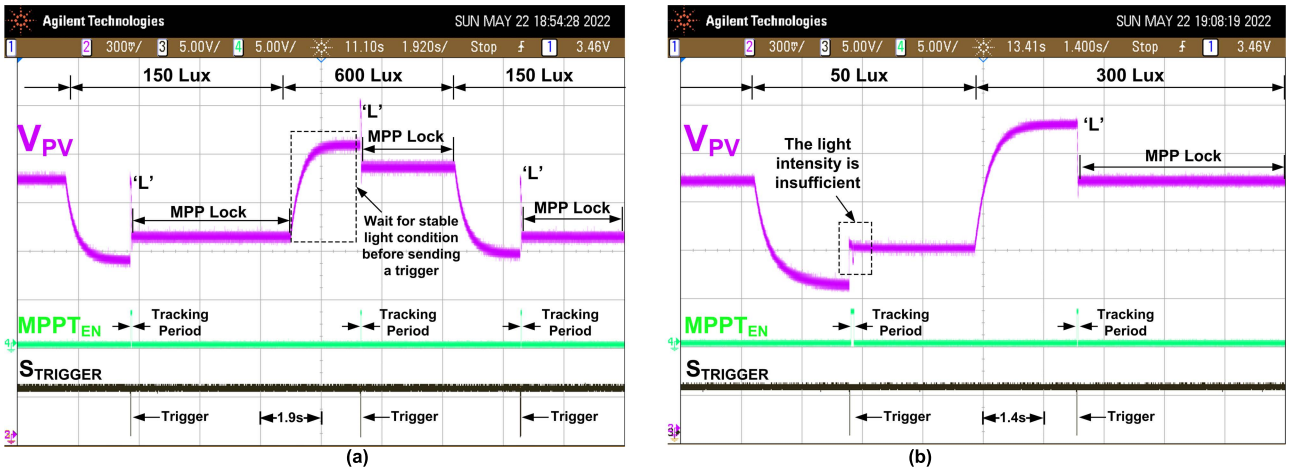


FIGURE 17. Dynamic tracking performance of proposed MPPT circuit under normal light condition (a) and (b) low light condition.

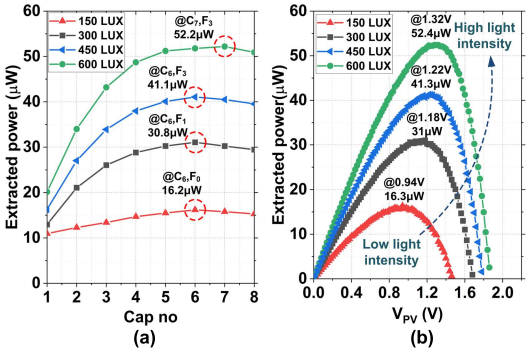


FIGURE 18. (a) Extracted power with different capacitance and switching frequency values under different light intensities, (b) power characteristic of PV cells under different light intensities.

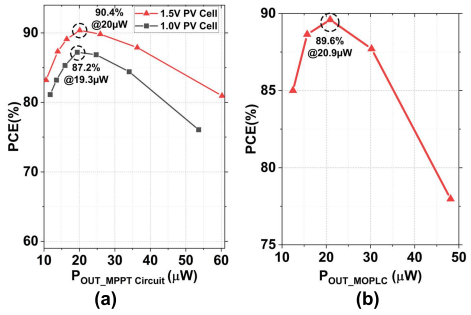


FIGURE 19. (a) Power conversion efficiency of proposed MPPT circuit with different PV cells configuration, (b) power conversion efficiency of MOPLC.

lighting conditions were checked: 1) 150 lux to 600 lux and 2) 50 lux to 300 lux. Fig. 17 shows the corresponding voltage waveforms (V_{PV}, $MPPT_{EN}$, $S_{TRIGGER}$). As shown in the Fig. 17(a), the proposed circuit attempts to track the change in light intensity when the $S_{TRIGGER}$ signal is received. Whenever the change of light intensity is detected, the system finds and locks the MPP successfully. Fig. 17(b) shows a situation where a low light intensity is applied to the system. Unlike the successful MPP tracking operation in Fig. 17(a), a system with insufficient light intensity (50 lux in the test) failed to find MPP. For proper operation in this situation, the TDC unit requires more storage cells because one cycle period of the V_{SC} signal (T_R) must be much longer than the system can provide. When the illumination changes to 300 lux, the system normally tracks the MPP point and displays the MPPT lock after the 'L' point. Note that, C_{buff}'s capacitance is set to 2nF in this work, which is sufficient to operate with real-life light intensity ranging from 150 lux to 600 lux.

The tracking accuracy of the MPPT circuit is evaluated under the different light intensities from 150 lux to 600 lux and can be described as follow: First, the Power Tracking unit is turned off and the capacitance and switching frequency are swept through the MCU. The extracted power versus the number of used capacitors and the switching frequency are recorded and shown in Fig. 18(a). The information of the two variables (capacitance step and switching frequency step) and the extracted power at the MPP are also annotated with a red circle in the figure. As can be seen, these two variables are consistent with the measured transient results in Fig. 16(b). The results verify that the proposed MPPT circuit is successfully converged at the actual MPP. Then, by comparing the actual MPP with the theoretical MPP of PV cells, the tracking accuracy can be obtained. The theoretical MPPs are measured by sweeping the V_{PV} voltage of PV cells under the different light intensities as shown in Fig. 18(b). These theoretical MPPs can now be compared with the actual MPPs which is obtained from the measured extracted power in Fig. 18(a), and the peak tracking accuracy of the proposed system is found to be 99.6% at the light intensity of 600 lux.

Fig. 19 shows the PCE of the proposed MPPT circuit and MOPLC. The proposed circuit improves PCE over a wide range of PV cells input voltages using a reconfigurable sc dc-dc converter. With three CRs (2x, 3x, and 4x) and the target output voltage of 3V, the proposed MPPT circuit can cover the input voltage range of 0.8V∼1.5V. Typically, a high PCE of the MPPT circuit can be obtained by selecting a low (high)

TABLE 1. Performance comparison of energy harvesting system.

Parameters	[4] TCAS' 19	[8] JSSC' 16	[5] TCAS' 18	[14] JSSC' 15	[7] VLSI' 15	[13] JSSC' 18	[36] TCAS' 2022	This work
Technology (nm)	65	180	180	180	180	65	28	180
Converter Topology	SC	SC	SC	SC	SC	SC	SC	SC
Conversion Ratio	Reconf.	Reconf.	Reconf.	1:3	1:3	Reconf.	Reconf.	Reconf.
MPPT turning	2-D CR-FRE	2-D CR-FRE	2-D CR-FRE	1-D CAP	1-D CAP	3-D CR-FRE-SW	2-D CR-FRE	**Enhanced 3-D CR-FRE-CAP**
Switching Frequency (kHz)	500-2300	27~1000	20-1000	250 (Fixed)	150 (Fixed)	-	54-3400	**70-600 (Optimized selection)**
MPPT algorithm	Voltage-based	Voltage-based	Time-based	Time-based	V-I Sensors	V-I Sensors	Voltage-based	Time-based
Input range (V)	0.55-1.6	0.45-3V	0.5-1.8	1.1-1.5	1-1.5	0.35-1	0.65-1.5	0.8-1.5
Output range (V)	1.8-2.5	3.3V	1.2-1.8	3.3	3-3.5	1	<2	3
Output ripple (mV)	18	>100	-	50	207	20	-	220
Throughput power (μW)	35-70	<50	<35.1	20	29	300	60-2800	52
PCE (%)	74.6	89 w/o controller 81 w/ controller	72	86.4	88.7	83 @0.5V 88 @0.85V	88.9	**90.37 @20 μW (Highest)**
Tracking efficiency (%)	-	-	95.6	99	-	-	97	**99.6 (Highest)**
Area (mm^2)	0.47	4	0.552	2.25	2.25	0.54	4.8	**0.42 (Smallest)**

CR for high (low) PV cells input voltage level. Accordingly, the 3V regulated output is achieved by adaptively using the 1V and 1.5V PV cells inputs at the 2x, 3x, and 4x CRs. The peak PCEs according to the two PV cells inputs, 1V and 1.5V, are 87.2% and 90.4%, respectively (Fig. 19(a)). With output power from 10 μW to 52 μW, the PCE of the proposed MPPT circuit is always maintained to be higher than 75%. The PCE of the MOPLC is also monitored to be high enough, where the peak PCE was proven to be 89.6% at 20.9 μW as shown in Fig. 19(b). The detailed power breakdown of the proposed MPPT circuit is shown in Fig. 20. The time-based MPPT approach significantly reduces the power consumption compared to analog-based MPPT. Furthermore, the proposed MPPT circuit allows the system to use the minimum switching frequency to find MPP that significantly improves power consumption. At the minimum switching frequency, the overall power consumption is 1.41μW whereas the losses of sc dc-dc converter are 1μW, accounting for 70.6% of the total MPPT circuit. The Hysteresis Controller consumes 0.3 μW, which is mainly used by comparators. The TDC and FSM & Digital Comparator consume 0.11μW and 0.004μW,

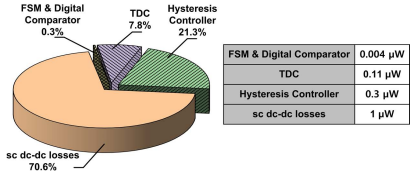


FIGURE 20. Detail power breakdown of the proposed MPPT circuit.

respectively. Note that, the TDC and FSM & Digital Comparator do not always operate and are turned off during the idle mode of the MPPT procedure. Because these blocks are active for a short period of time, power consumption is negligible. The detailed power breakdown and other performance metrics of MOPLC are not the main goal of this paper and will not be mentioned.

Table 1 compares the performance of the proposed work with the other state-of-the-art MPPT circuits. The proposed MPPT circuit uses a 3-D MPPT tuning algorithm to improve the throughput power, which turns out to be 52μW. Compared to a system with a similar capacitance in the sc dc-dc converter of [14], the throughput power of the proposed circuit

is more than twice as large. It is worth noting here that the proposed circuit finds an optimal combination of capacitance and switching frequency to achieve MPP, and in particular, the minimum switching frequency is selected in a given situation. This results in low dynamic power loss and the proposed MPPT circuit achieves 90.4% which is the highest PCE among previous state-of-the-art works. Furthermore, the proposed MPPT circuit is able to track the optimal power extraction with fine granularity based on the 7.2 pF unit capacitor of the sc dc-dc converter and the 8-bit resolution of the TDC register, leading to the best performance of 99.6% power tracking efficiency compared to other competitors. In addition to performance figures in terms of conversion efficiency and tracking efficiency, the proposed circuit provides reconfigurable CRs. Compared to previous studies using a single CR in [7], [14], the three CRs in the proposed system improve the overall PCE with a wide input voltage range (0.8V∼1.5V). Although the output voltage ripple of the regulated voltage V_{SC} exceeds 200mV, the ripple decreases four times at the output node of the MPPT circuit (V_{OUT}) due to the supercapacitor connected for energy storage.

V. CONCLUSION

This paper presents a highly efficient TB-MPPT circuit with an enhanced 3-D tuning method. In the proposed circuit, reconfigurable sc dc-dc converter with three CRs is used to extend power range. Due to the CRL of the sc topology, CR is first selected based on the output level of PV cells. Then, the proposed algorithm can find the MPP with the minimum tuning switching frequency and capacitance control knob. This work is fabricated in the 180 nm CMOS process and tested with commercial PV cells. The measurement shows that the proposed circuit can obtain maximum throughput power of 50 μW while achieving a power conversion efficiency of 90.4% and a power tracking efficiency of 99.6%.

REFERENCES

[1] S. Abdelwahab, B. Hamdaoui, M. Guizani, and A. Rayes, "Enabling smart cloud services through remote sensing: An internet of everything enabler," *IEEE Internet Things J.*, vol. 1, no. 3, pp. 276–288, Jun. 2014.

[2] R. Yao, W. Wang, M. Farrokh-Baroughi, H. Wang, and Y. Qian, "Quality-driven energy-neutralized power and relay selection for smart grid wireless multimedia sensor based IoTs," *IEEE Sensors J.*, vol. 13, no. 10, pp. 3637–3644, Oct. 2013.

[3] W. Jung, S. Oh, S. Bang, Y. Lee, Z. Foo, G. Kim, Y. Zhang, D. Sylvester, and D. Blaauw, "An ultra-low power fully integrated energy harvester based on self-oscillating switched-capacitor voltage doubler," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2800–2811, Dec. 2014.

[4] A. Devaraj, M. Megahed, Y. Liu, A. Ramachandran, and T. Anand, "A switched capacitor multiple input single output energy harvester (solar + piezo) achieving 74.6% efficiency with simultaneous MPPT," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 12, pp. 4876–4887, Dec. 2019.

[5] X. Liu, K. Ravichandran, and E. Sánchez-Sinencio, "A switched capacitor energy harvester based on a single-cycle criterion for MPPT to eliminate storage capacitor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 2, pp. 793–803, Feb. 2018.

[6] K. Rawy, F. Kalathiparambil, D. Maurath, and T. T.-H. Kim, "A self-adaptive time-based MPPT with 96.2% tracking efficiency and a wide tracking range of 10 μ a to 1 mA for IoT applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 9, pp. 2334–2345, Sep. 2017.

[7] X. Liu and E. Sánchez-Sinencio, "A highly efficient ultralow photovoltaic power harvesting system with MPPT for Internet of Things smart nodes," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 12, pp. 3065–3075, Dec. 2015.

[8] X. Liu, L. Huang, K. Ravichandran, and E. Sánchez-Sinencio, "A highly efficient reconfigurable charge pump energy harvester with wide harvesting range and two-dimensional MPPT for Internet of Things," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1302–1312, May 2016.

[9] A. K. Abdelsalam, A. M. Massoud, S. Ahmed, and P. N. Enjeti, "High-performance adaptive perturb and observe MPPT technique for photovoltaic-based microgrids," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1010–1021, Apr. 2011.

[10] H. Kim, S. Kim, C.-K. Kwon, Y.-J. Min, C. Kim, and S.-W. Kim, "An energy-efficient fast maximum power point tracking circuit in an 800-μW photovoltaic energy harvester," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2927–2935, Jun. 2013.

[11] Y. Jiang, J. A. A. Qahouq, and T. A. Haskew, "Adaptive step size with adaptive-perturbation-frequency digital MPPT controller for a single-sensor photovoltaic solar system," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3195–3205, Jul. 2013.

[12] V.-T. Dang, M.-G. Yang, Y. Shim, W. Lee, and K.-H. Baek, "An accurate time-based MPPT circuit with two-period tracking algorithm and convergence range averaging technique for IoT applications," *IEEE Access*, vol. 9, pp. 31401–31410, 2021.

[13] K. Rawy, T. Yoo, and T. T. H. Kim, "An 88% efficiency 0.1–300 μW energy harvesting system with 3-D MPPT using switch width modulation for IoT smart nodes," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2751–2762, Oct. 2018.

[14] X. Liu and E. Sanchez-Sinencio, "An 86% efficiency 12 μW self-sustaining PV energy harvesting system with hysteresis regulation and time-domain MPPT for IoT smart nodes," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1424–1437, Jun. 2015.

[15] S. Uprety and H. Lee, "A 0.4W-to-21W fast-transient global-search-algorithm based integrated photovoltaic energy harvester with 99% GMPPT efficiency and 94% power efficiency," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2153–2167, Sep. 2016.

[16] Y. Nakase, S. Hirose, H. Onoda, Y. Ido, Y. Shimizu, T. Oishi, T. Kumamoto, and T. Shimizu, "0.5 V start-up 87% efficiency 0.75 mm^2 on-chip feed-forward single-inductor dual-output (SIDO) boost DC-DC converter for battery and solar cell operation sensor network micro-computer integration," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1933–1942, Aug. 2013.

[17] O. Lopez-Lapena, M. T. Penella, and M. Gasulla, "A closed-loop maximum power point tracker for subwatt photovoltaic panels," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1588–1596, Mar. 2012.

[18] X. Liu and E. Sanchez-Sinencio, "21.1 A single-cycle MPPT charge-pump energy harvester using a thyristor-based VCO without storage capacitor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, p. 364.

[19] W. Jung, S. Oh, S. Bang, Y. Lee, D. Sylvester, and D. Blaauw, "23.3 A 3nW fully integrated energy harvester based on self-oscillating switched-capacitor DC–DC converter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, p. 398.

[20] X. Liu and E. Sanchez-Sinencio, "20.7 A 0.45-to-3 V reconfigurable charge-pump energy harvester with two-dimensional MPPT for Internet of Things," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, p. 370.

[21] S. Bandyopadhyay and A. P. Chandrakasan, "Platform architecture for solar, thermal, and vibration energy combining with MPPT and single inductor," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2199–2215, Sep. 2012.

[22] S. S. Amin and P. P. Mercier, "MISIMO: A multi-input single-inductor multi-output energy harvester employing event-driven MPPT control to achieve 89% peak efficiency and a 60,000x dynamic range in 28nm FDSOI," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, p. 144.

[23] Q. Wan, Y.-K. Teh, Y. Gao, and P. K. T. Mok, "Analysis and design of a thermoelectric energy harvesting system with reconfigurable array of thermoelectric generators for IoT applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 9, pp. 2346–2358, Sep. 2017.

[24] J. Kim and C. Kim, "A DC–DC boost converter with variation-tolerant MPPT technique and efficient ZCS circuit for thermoelectric energy harvesting applications," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3827–3833, Aug. 2013.

[25] J. Jeong, M. Shim, J. Maeng, I. Park, and C. Kim, "A high-efficiency charger with adaptive input ripple MPPT for low-power thermoelectric energy harvesting achieving 21% efficiency improvement," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 347–358, Jan. 2020.
[26] J. Goeppert and Y. Manoli, "Fully integrated startup at 70 mV of boost converters for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1716–1726, Jul. 2016.
[27] P. H. Chen and P. M. Y. Fan, "An 83.4% peak efficiency single-inductor multiple-output based adaptive gate biasing DC–DC converter for thermoelectric energy harvesting," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 2, pp. 405–412, Feb. 2015.
[28] E. J. Carlson, K. Strunz, and B. P. Otis, "A 20 mV input boost converter with efficient digital control for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 741–750, Apr. 2010.
[29] Y. K. Ramadass and A. P. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 189–204, Jan. 2010.
[30] P. Gasnier, J. Willemin, S. Boisseau, G. Despesse, C. Condemine, G. Gouvernet, and J. J. Chaillout, "An autonomous piezoelectric energy harvesting IC based on a synchronous multi-shot technique," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1561–1570, Jul. 2014.
[31] G. Papotto, F. Carrara, and G. Palmisano, "A 90-nm CMOS threshold-compensated RF energy harvester," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1985–1997, Sep. 2011.
[32] T.-C. Huang, C.-Y. Hsieh, Y.-Y. Yang, Y.-H. Lee, Y.-C. Kang, K.-H. Chen, C.-C. Huang, Y.-H. Lin, and M.-W. Lee, "A battery-free 217 nW static control power buck converter for wireless RF energy harvesting with α-calibrated dynamic on/off time and adaptive phase lead control," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 852–862, Apr. 2012.
[33] J. Rabaey, F. Burghardt, D. Steingart, M. Seeman, and P. Wright, "Energy harvesting—A systems perspective," in *IEDM Tech. Dig.*, Dec. 2007, pp. 363–366.
[34] Z. Hua and H. Lee, "A reconfigurable dual-output switched-capacitor DC–DC regulator with sub-harmonic adaptive-on-time control for low-power applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 724–736, Mar. 2015.
[35] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.
[36] Y. Yoon, H. Gi, J. Lee, M. Cho, C. Im, Y. Lee, C. Bae, S. J. Kim, and Y. Lee, "A continuously-scalable-conversion-ratio step-up/down SC energy-harvesting interface with MPPT enabled by real-time power monitoring with frequency-mapped capacitor DAC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 4, pp. 1820–1831, Apr. 2022.

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