IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received May 22, 2022, accepted June 11, 2022, date of publication June 14, 2022, date of current version June 17, 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3183028

A Low-Noise Fast-Transient-Response Delta-Sigma-Modulation Buck Converter With Hysteresis-Voltage-Controlled Techniques

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This work was supported by the Ministry of Science and Technology (MOST), Taiwan under Grant MOST 110-2221-E-027-126-MY3.

ABSTRACT A low-noise fast-transient-response second-order delta-sigma-modulation buck converter with hysteresis-voltage-controlled techniques is proposed. With the proposed control approach, the transient time can be accelerated by roughly 60%. The rail-to-rail OTA generates a current I_{Sense}, which replicates the inductor current I_L with K times. As ISense flows through the capacitor C_{Sense}, it will be converted into VSense. Then, the hysteresis-voltage-controlled (HVC) circuit compares the two terminal voltages of hysteresis comparator to detect the overshoot and undershoot of V_{Sense}. Once V_{Sense} is detected, the output signal of HVC circuits becomes opposite to the previous state to conduct M_P and M_N previously. Besides, the 2nd-order delta-sigma-modulation (DSM) circuit plays a vital role of mitigating noise-interference and elevating noise in whole circuits. The proposed converter has been fabricated in TSMC 0.18μm 1P6M CMOS processes with an active area of 1.19 × 1.09mm^2. The measured results show the transient time are 3.5μs and 3.2μs, respectively, when the load current changes between 500mA and 100mA. On the basic of the measured results of fast-fourier-transform (FFT), the value of output-to-noise ratio (ONR) is 76.6dB at the sampling frequency of 10MHz. The peak conversion efficiency is 92.1% while the load current is 300mA.

INDEX TERMS Buck converter, fast-transient-response, delta-sigma-modulator (DSM), hysteresis-voltage-controlled (HVC), rail-to-rail OTA.

I. INTRODUCTION

In our daily life, smart phones, aerospace industry, medical care, and e-commerce build up the chip industry chain. For the purpose of satisfying the demand from all walks of life, the integration of systems-on-chip (SoCs) seems extremely important. In recent years, the Delta-Sigma-Modulation (DSM) architecture have been applied to the field of power electronics owing to the superiority of low electromagnetic interference (EMI) and high efficiency over a wide load range. To overcome the spurious switching noise and enhance the transient response, the scheme we proposed utilizes the noise-shaping theorem and hysteresis-voltage-controlled techniques. In the field of power management integrated circuits (PMICs), the architecture of DSM is adopted to alleviate the impact on the noise-sensitive circuits [1]–[5]. On the other hand, the drawback of DSM is inevitable.

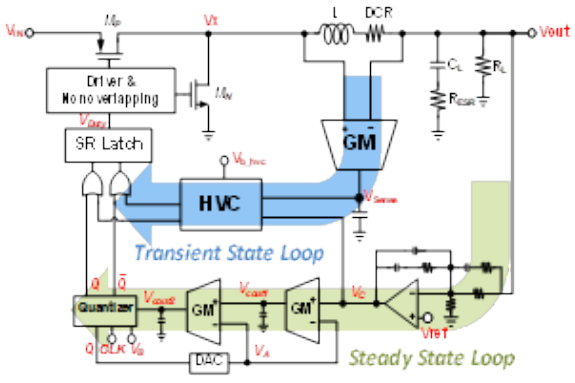


FIGURE 1. The proposed buck converter.

The associate editor coordinating the review of this manuscript and approving it for publication was Harikrishnan Ramiah.

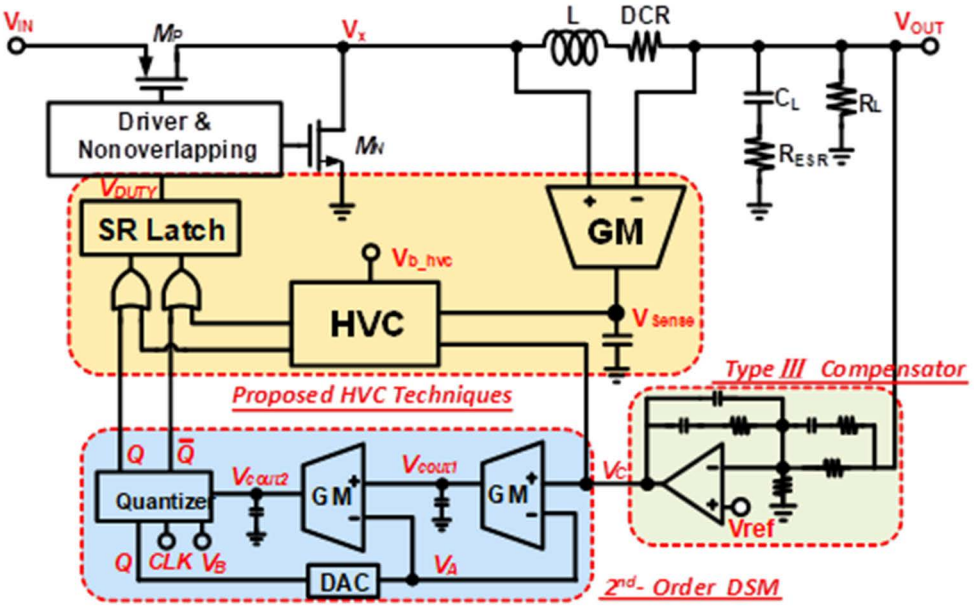


FIGURE 2. Block diagram of a fast-transient-response second-order delta-sigma-modulator buck converter with hysteresis-voltage-controlled techniques.

Namely, the characteristic of transient response is relatively poor compared with other architectures. Hence, a current-sensing path that can ameliorate the recovery time is needed.

Figs. 1 and 2 illustrates the simplified architecture of the proposed buck converter, which is categorized as two loops, voltage and current loops. Power stage, LC filter, compensator, DSM, driver and nonoverlapping circuits constitute the voltage loop, namely the steady-state loop of proposed buck converter, and the other loop comprises the HVC circuits and rail-to-rail current-sensor. The blue line shadowed block is regarded as transient-state loop, which is designed to rapidly detect the overshoot and undershoot of the output voltage of rail-to-rail current-sensor voltage V_{Sense}. Once V_{Sense} is detected by the HVC circuits, the output voltage of SR Latch V_{Duty} will change the state immediately. And this movement makes the switches conduct in advance so that the recovery time of output voltage improves greatly. Moreover, the current-sensing-feedback loop can move the inductor pole to high frequency and increase the phase margin of loop gain. To verify the large-signal stability of the proposed converter, we have used HSPICE to simulate the converter and obtained stable results.

The work is organized as follows. In Section II, the proposed architecture and the operation mechanism are introduced successively. We will examine circuit implementations in more detail later in Section III. Section IV shows the experimental results and comparison chart of the proposed converter. Finally, the conclusion is presented in Section V.

II. THEORY AND OPERATION MECHANISM OF THE PROPOSED CONVERTER

In this section, features related to over-sampling theorem, Nyquist-sampling theorem, noise-shaping and the quantization error will be discussed as followed. Characteristics mentioned above will also be applied to first-order as well as second-order CT-DSM architecture. And the pros and cons between two structures are listed in the comparison chart.

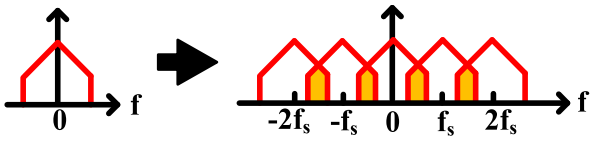


FIGURE 3. Phenomenon of aliasing signals.

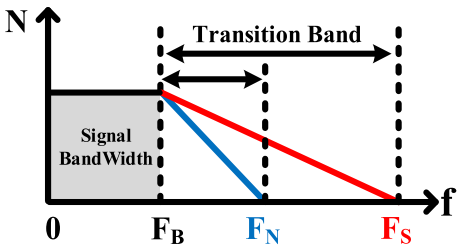


FIGURE 4. Spectrum of Nyquist s and over sampling frequency.

A. OVERSAMPLING THEOREM

Generally, the conversion of analog signals in nature into digital signals requires anti-aliasing to prevent the sampling signals from distortion. The sampling circuit will separate the analog signal to form a discontinuous signal and send it to the next circuit. The discontinuous signal after sampling is converted into the nearest segmented analog signal through the quantization circuit. A number of digital signals will form a voltage or current signal level, and this step determines

the resolution of the entire converter. The digital signal is then converted into usable digital signal through the digital decoding. The more sampling points the converters sample, the higher resolution of the converter has.

The Nyquist sampling theorem defines that the sampling frequency (F_S) must be at least twice the signal bandwidth (F_B) as formula (1) expressed. If the sampling frequency F_S is less than twice the signal bandwidth F_B, the sampled signal will overlap, which means that the signal aliases. In order to overcome the difficulty of the sampling, the design of anti-aliasing filter is essential.

The oversampling theorem is defined as the sampling frequency is much greater than twice the signal bandwidth of the sampling frequency (F_B). Moreover, the oversampling ratio (OSR) can be defined by the Oversampling frequency and the Nyquist-sampling frequency as formula (2) expressed. If the sampling frequency defined by the Nyquist theorem is selected, the signal transition band on the spectrum is narrower than the sampling frequency defined by the Oversampling theorem. It makes the design of the anti-aliasing filter easier.

$$F_S \geq 2F_B \tag{1}$$

$$\text{Oversampling Ratio (OSR)} = \frac{F_S}{2F_B} \tag{2}$$

B. QUANTIZATION ERROR

The quantization process of Nyquist sampling frequency is that the sampled analog discontinuous signals converter into multi-segment digital signals. Ideally, analog signals will be accurately sliced into the over-sampling frequency spectrums of several discontinuous signals. And the level of each analog signal corresponds to the value of a digital signal one by one. The situation that different analog signal levels are converted into the same digital signal won't occur. However, there will be an error in signal conversion due to external factors in the circuit, which is called quantization error as shown in Fig. 5.

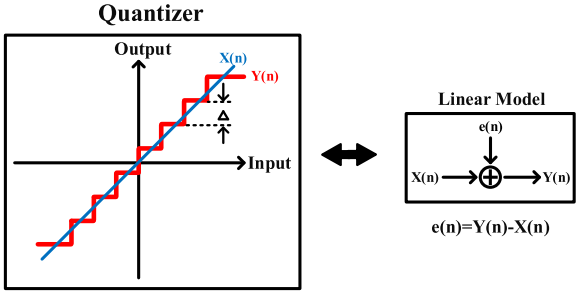


FIGURE 5. Quantization error and the linear model of quantizer.

The quantization error signal is defined as the difference between the output signal Y(n) of the quantizer minus the input signal X(n) as shown in Fig.6. The symbol Δ represents the difference between the levels at which each analog signal is converted into a digital signal. The smaller the Δ, the better the quantization effect. The input signal of the quantizer must still be within a certain input range, so that the variation of the quantization error is limited to the range of $-\Delta/2 \sim +\Delta/2$, otherwise the quantizer will be overloaded and the quantization error will be boundless.

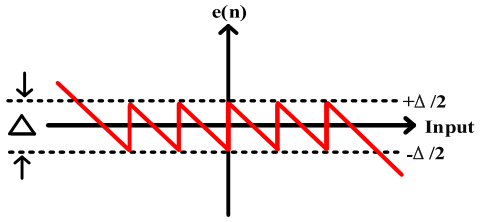


FIGURE 6. Relationship of quantizer input signal and quantization error.

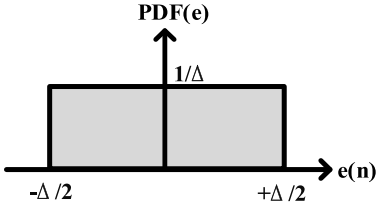


FIGURE 7. Quantization error probability density function.

We can assume that the quantization error is an independent signal that is not affected by the input signal, meaning a white noise signal, as shown in Fig. 7, which is the probability density function (PDF) of the quantization error e(n). It can be seen from Fig. 7 that the quantization error range will be evenly distributed between $\pm\Delta/2$, and the probability density function of the quantization error e(n) and the quantization error product are 1, so we infer that the total noise power P_{Noise} is the probability density function and quantization. The area enclosed by the error can be expressed as formula (3).

$$P_{Noise} = \int_{-\infty}^{\infty} e^2 \times pdf\,(e)\,de = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12} \tag{3}$$

Assuming that the input signal is a sine wave signal $A\sin(\omega t)$, the power P_S of the output signal can be expressed as equation (4). By using formula (4), we can derive the Signal-to-Noise Ratio (SNR) expressed as formula (5). As shown in formula (5), it can be seen that the SNR can be improved by 6.02 dB when the quantizer increases by one quantization bit.

$$P_S = 2^{2N} \times \frac{\Delta^2}{8} \tag{4}$$

$$SNR = 10\log\frac{P_S}{P_{Noise}} = 6.02N + 1.76\,(dB) \tag{5}$$

Fig. 8 shows the quantization error power spectral density (PSD) graph, and the height H_E of the power spectral density is shown in equations (6). As long as the value of the sampling frequency F_S is increased, the height of the power spectral density will be reduced, and the distribution become

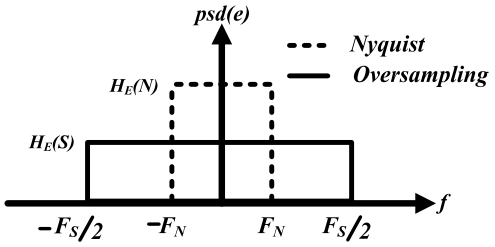


FIGURE 8. Quantization error power spectral density.

evenly. At this time, the power spectral density boundary will expand from $\pm F_N$ to $\pm F_S/2$, and the overall power sum is still consistent with the power sum of the Nyquist sampling frequency.

$$H_E(N) = \frac{\Delta}{\sqrt{12F_N}}, \quad H_E(S) = \frac{\Delta}{\sqrt{12MF_N}} \tag{6}$$

$$\begin{aligned} SNR &= 10\log\left(\frac{3}{2}\times 2^{2N}\times OSR\right) \\ &= 6.02N + 1.76 + 10\log(OSR)\,(dB) \end{aligned} \tag{7}$$

PSD can not only break apart the noise distribution within the bandwidth significantly, but also makes SNR a noticeable increase. As shown in formula (7), it can be derived from the results that the SNR can be improved by 3dB for every doubling of OSR. Compared to blindly increasing the number of quantization bits to ameliorate the SNR, adjusting the sampling frequency is more effective.

C. NOISE SHAPING

In the previous paragraph, it is mentioned that the over-sampling technology can be used to spread the noise distribution evenly and reduce the amount of noise in the signal bandwidth. However, there is still an upper limit for increasing the sampling frequency, which cannot be solved by simply increasing the sampling frequency. Therefore, the concept of noise shaping was introduced.

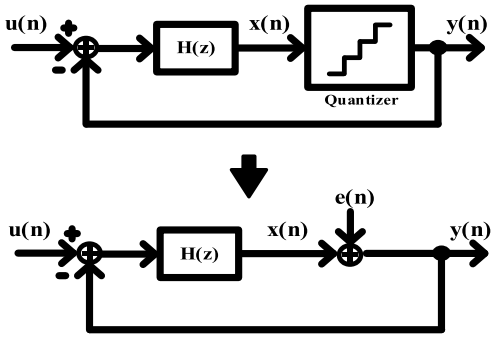


FIGURE 9. Linear model of first-order delta-sigma-modulator.

The purpose of noise shaping is to change the energy distribution of the quantization noise and move the noise to a higher frequency spectrum. This can not only obtain a high-resolution signal, but also reduce the multiple of the oversampling frequency. Fig. 9 shows the interpolative architecture and linear model of the first-order delta-sigma modulator, u(n) and y(n) are the input and output signals, e(n) is the quantization error, and H(z) It is a loop filter. This architecture is similar to the concept of operational amplifier feedback, using high-gain operational amplifiers with the concept of feedback to reduce the impact of noise at the low frequency.

In the light of the superposition theorem and Mason's Gain Formula (MGF), the relationship between the input and output signal of this first-order system can be derived, as shown in formula (8).

$$Y(z) = \frac{H(z)}{1+H(z)}\cdot X(z) + \frac{1}{1+H(z)}\cdot e(z) \tag{8}$$

H(z) is the loop filter, and it can be expressed as formula (9) after Laplace Z conversion. With formula (8), assuming that e(z) and X(z) are zero respectively, the signal transfer function (STF) and noise transfer function (NTF) can be defined separately as formula (10) and (11). Based on the results, Z^{-1} can be regarded as a delay time $T = 1/RC$, and $(1 - Z^{-1})$ can be viewed as a high-pass filter. The high-frequency signal will be filtered.

$$H(z) = \frac{Z^{-1}}{1-Z^{-1}} \tag{9}$$

$$\begin{aligned} STF(z) &= \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \\ &= Z^{-1} by\ setting\ e(z) = 0 \end{aligned} \tag{10}$$

$$\begin{aligned} NTF(z) &= \frac{Y(z)}{e(z)} = \frac{1}{1+H(z)} \\ &= 1 - Z^{-1} by\ setting\ X(z) = 0 \end{aligned} \tag{11}$$

It can be found from equation (10) that the larger the gain of H(z) is designed, the more similar the output signal's frequency spectrum can be to the input signal. In order to calculate the resolution of the delta-sigma modulator, $z = e^{j\omega t} = e^{j2\pi f/Fs}$ can be substituted into equation (10) and (11). And by taking the square, STF(z) and NTF(z) can be calculated, as shown in formulas (12) and (13).

$$|STF(z)|^2 = 1 \tag{12}$$

$$|NTF(z)|^2 = \left[2\sin\frac{\pi f}{F_S}\right]^2 \tag{13}$$

As shown in Fig.10, the signal transfer function (STF) is not affected by the frequency and is a constant. The noise transfer function (STF) can be quantized to push the noise to the high frequency, and then use a low-pass filter to filter out high-frequency noise. In order to obtain the performance of the first-order delta-sigma modulator, the noise power within the bandwidth can be calculated, as shown in equation (14).

$$\begin{aligned} P_{Noise} &= \int_{-F_B}^{F_B} N(f)^2\cdot|NTF(z)|^2\,df \\ &= \int_{-F_B}^{F_B} \frac{\Delta^2}{12\times F_S}\cdot\left[2\cdot\sin\frac{\pi f}{F_S}\right]^2 df \end{aligned} \tag{14}$$

Under the condition of oversampling, $F_S \gg F_B$, it can be seen that $\sin(\pi f/F_S) \approx \pi f/F_S$, so the noise power can be

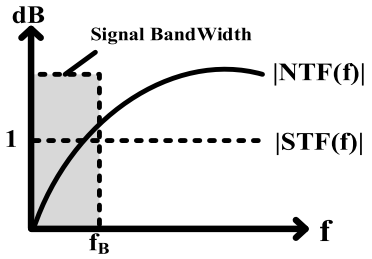


FIGURE 10. Linear model of first-order delta-sigma-modulator.

rewritten as equation (15). Equation (16) is the signal-to-noise ratio (SNR).

$$P_{Noise} = \frac{\Delta^2}{12 \times F_S} \int_{-F_B}^{F_B} \left[2 \cdot \frac{\pi f}{F_S}\right]^2 df = \frac{\Delta^2}{12} \times \frac{\pi^2}{3} \times \left(\frac{2F_B}{F_S}\right)^3 \quad (15)$$

$$\mathrm{SNR} = 10\log\left(\frac{P_S}{P_{Noise}}\right) = 10\log\frac{\frac{2^{2N}\times\Delta^2}{8}}{\frac{\Delta^2}{12} \times \frac{\pi^2}{3} \times \left(\frac{2F_B}{F_S}\right)^3} = 6.02N + 1.76 + 30\log(OSR) - 5.17\,(dB) \quad (16)$$

From equation (16), it can be obtained that for every doubling of the OSR, the SNR can be improved by about 9 dB, which means that the resolution is increased by 1.5 bits.

D. SECOND-ORDER DSM

The second-order delta-sigma-modulator is composed of two integrators (Integrator, Z^{-1}) and a quantizer, and this architecture is interpolative.

The transfer function of the second-order delta-sigma modulator is set to $z = e^{j\omega t} = e^{j2\pi f/Fs}$, which can be expressed as equation (17). After squaring both sides of the equal sign of equation (17), the signal transfer function STF(z) and the noise transfer function NTF(z) can be obtained, as shown in equations (18) and (19).

$$Y(z) = \mathrm{STF}(z) \cdot X(z) + \mathrm{NTF}(z) \cdot e(z) = z^{-2} \cdot X(z) + (1 - z^{-1})^2 \cdot e(z) \quad (17)$$

$$|\mathrm{STF}(z)|^2 = \left|z^{-2}\right|^2 = 1 \quad (18)$$

$$|\mathrm{NTF}(z)|^2 = \left[2\sin\frac{\pi f}{F_S}\right]^4 \quad (19)$$

From the above conclusions, the noise power and SNR within the bandwidth can be expressed as equations (20) and (21).

$$P_{Noise} = \int_{-F_B}^{F_B} N(f)^2 \cdot |NTF(z)|^2\, df = \int_{-F_B}^{F_B} \frac{\Delta^2}{12 \times F_S} \cdot \left[2 \cdot \sin\frac{\pi f}{F_S}\right]^4 df = \frac{\Delta^2\pi^4}{60} \times \left(\frac{1}{OSR}\right)^5 \quad (20)$$

$$SNR = 6.02N + 50\log(OSR) - 11.4\,(dB) \quad (21)$$

TABLE 1. Comparison of DSM.

Architecture	Advantage	Disadvantage
First-Order	Simpler design	Lower OSR
Second-Order	Higher OSR	Complex design

From equation (21), it can be seen that for every doubling of the OSR, the SNR improves by about 15 dB, which means that the resolution increases by 2.5 bits. In contrast, the second-order architecture has better noise immunity than the first-order. So far, the chapter has focused on the theory adopted by the designer. The following section will discuss the circuit implementations. The comparison of DSM is shown in Table 1.

III. CIRCUIT IMPLEMENTATIONS

The power stage, the type-III compensator, 2nd-order DSM, and the circuit with proposed HVC techniques make up the proposed continuous-time-delta-sigma-modulation (CT-DSM) buck converter as shown in Fig. 2. Before proceeding to examine the proposed buck converter, it will be necessary to elaborate the operation mechanism about the whole circuit. When this circuit works in steady state, the voltage V_{Sense} sensed by the inductor will fall between the upper and lower limits (V_{BH}, V_{BL}) of the hysteresis voltage band. This result will let the output of the comparator in the HVC architecture set to zero. In this moment, it doesn't affect the input value of SR Latch in the original circuit. Nonetheless, when the output load current is switched between the light and heavy load, the change of load current will make the signal V_{Sense} to switch at once. As the V_{Sense} is greater than the upper limit or less than the lower limit, the output V_{DUTY} of the SR latch will change accordingly. Hence, only this situation will the transient loop be activated. In conclusion, the transient and steady-state loops won't affect each other. The detailed structure and functions of the buck converter will be indicated in the forthcoming parts.

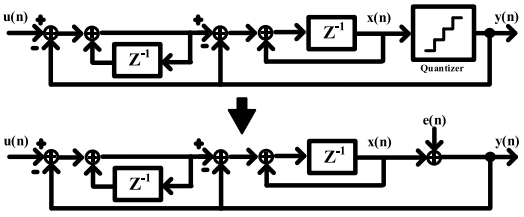


FIGURE 11. Linear model of second-order delta-sigma-modulator.

A. OTA-C CURRENT-SENSING CIRCUITS (GM)

The OTA-C current sensing circuit is shown in Fig. 13. Thanks to the advantage of wide input voltage range, large bandwidth, and simple architecture, we adopted rail-to-rail OTA as *GM* of the current sensing circuit. The current flowing from the output terminal V_{Sense} of the Rail-to-Rail

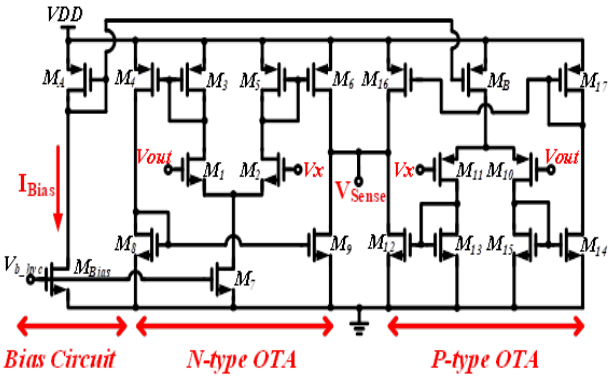


FIGURE 12. Rail-to-Rail OTA.

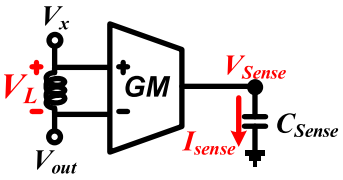


FIGURE 13. The OTA-C current-sensing circuit.

transconductance amplifier is the sensing current I_{Sense}. A capacitor C_{Sense} is added to the output terminal, and then the current is converted into the voltage signal V_{Sense}, which is used as the transient acceleration detection. The relationship between the transconductance of rail-to-rail transconductance amplifier and the sensing voltage V_{Sense} is expressed as equations (22), (23), (24).

$$G_m = gm_2 \times \frac{gm_6}{gm_5} + gm_{10} \times \frac{gm_{12}}{gm_{13}} \tag{22}$$

$$I_{Sense} = G_m \times (V_x - V_{out}) \tag{23}$$

$$\therefore V_{Sense} = \frac{1}{C_{Sense}} \int G_m (V_x - V_{out})\, dt \tag{24}$$

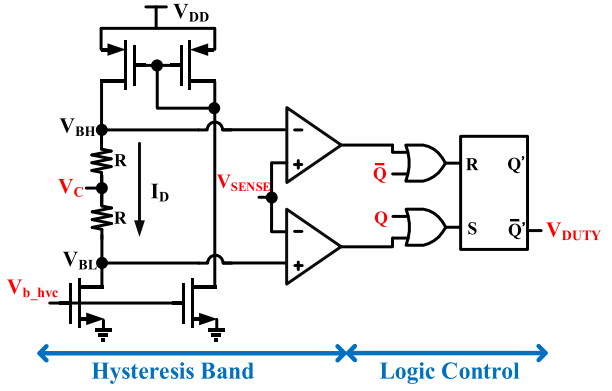


FIGURE 14. HVC circuits.

B. HYSTERESIS-VOLTAGE-CONTROLLED (HVC) CIRCUITS

The hysteresis voltage circuit is shown in the Fig.14. The purpose is to provide the level of the current sensing voltage

TABLE 2. Truth table of HVC circuits.

Condition	A	B	V_{DUTY}	Mode	Operation
$V_{BL}<V_{BH}<V_{Sense}$	1	0	0	H→L	PMOS ON
$V_{BL}<$ $V_{Sense}<V_{BH}$	0	0	1	Hold	NMOS ON
$V_{Sense}<$ $V_{BL}<V_{BH}$	0	1	0	L →H	PMOS ON

V_{Sense} and generate the upper and lower limits (V_{BH}, V_{BL}) of the hysteresis voltage band. At the same time, the circuit detects the change of load current, and transfers a digital signal V_{DUTY} to the following circuit. When V_{SENSE} is between V_{BH} and V_{BL}, the circuit works in a steady state, as shown in the attached table 2. Both points A and B, which are the output terminals of upper and lower comparators respectively, are low, so the original input of SR Latch won't be changed. At this moment, the transient acceleration circuit will not start, but when V_{Sense} is greater than V_{BH} and V_{BL}, points A and B are high and low, respectively. On the contrary, when V_{Sense} is less than V_{BH} and V_{BL}, points A and B are low and high. This result will make SR Latch input reset, so that the SR Latch output V_{DUTY} transition, that is, the V_{DUTY} signal is switched from high to low. Finally, the consequence turns off the conducted NMOS previously and turn on the PMOS in advance. The method we utilize is that making the pair of power MOS switches earlier to ramp up the transient response of the entire circuit.

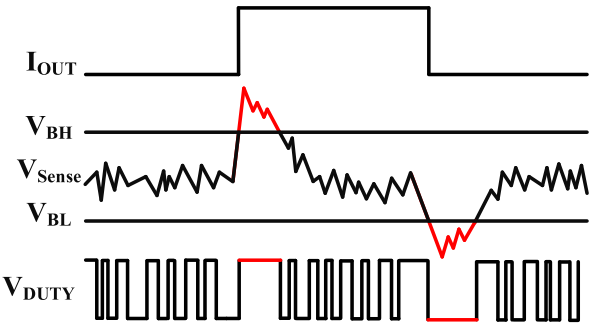


FIGURE 15. State diagram of HVC circuits.

C. QUANTIZER

As shown in Fig. 16, it consists of two parts: the dynamic comparator and RS Latch. By adjusting the frequency of the clock signal V_{CLK}, the state of the signal can trigger two working modes of the quantizer, namely the hold mode and the compare mode. Furthermore, we pull out the V_{DUTY} signal and use it as the output voltage of the quantizer. Finally, we can control the digital-to-analog converter (DAC) with the high and low voltage signals of different potentials.

D. TYPE III COMPENSATOR

Fig. 17 shows the type III compensator circuit, which is usually used in voltage mode as a compensation circuit

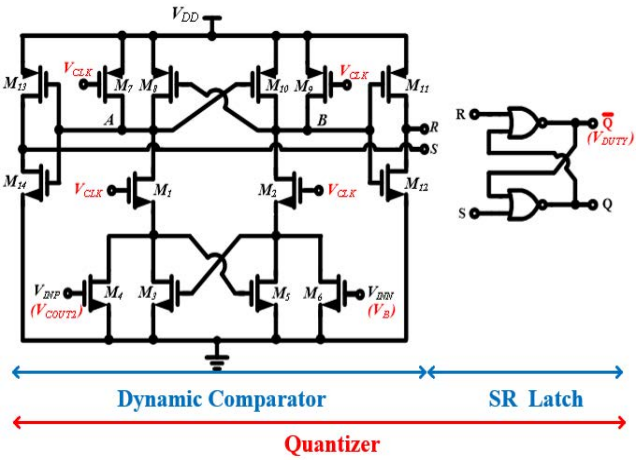


FIGURE 16. Quantizer.

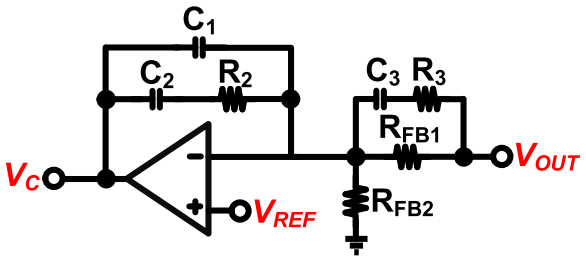


FIGURE 17. The Type III compensator.

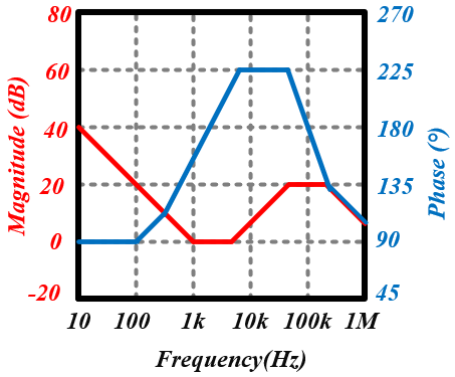


FIGURE 18. Bode plot of Type III compensator.

to make the circuit stable. Compared with the type II compensator, it provides additional high-frequency pole and zero. Therefore, it totally contains three poles and two zeros. The type III compensator can increase both the bandwidth and phase margin of a closed-loop system. Equations (25)-(28) are the simplification results of the type III compensator transfer function.

$$\frac{V_C(s)}{V_{OUT}(s)} = -\frac{A_V \cdot \omega_{z0}}{s} \frac{(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \tag{25}$$

$$A_V \approx \frac{R_1}{R_3} \tag{26}$$

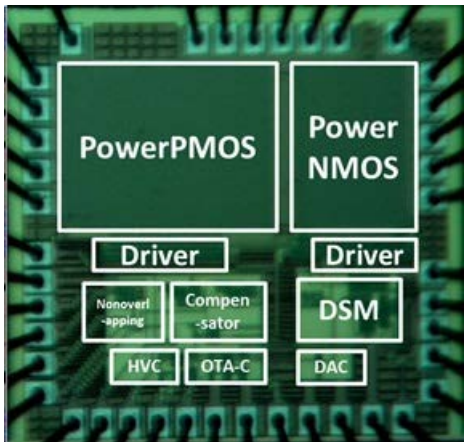
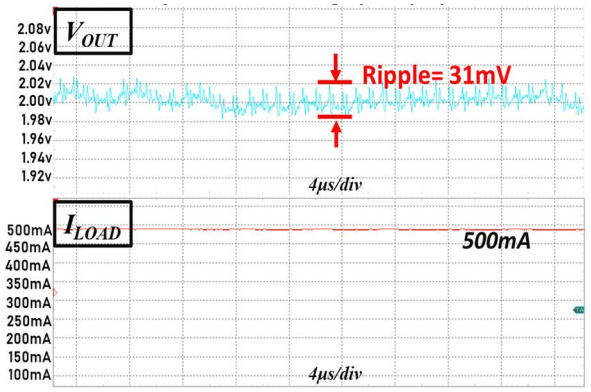
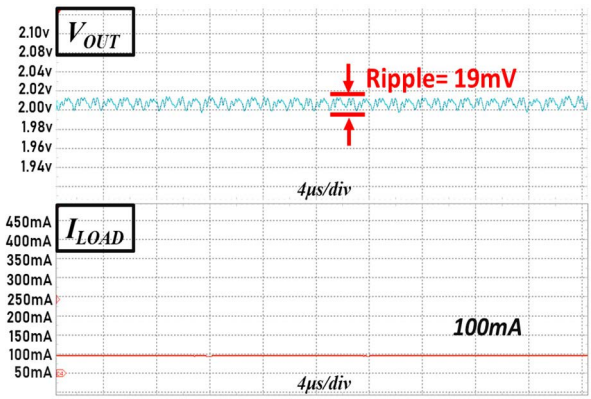


FIGURE 19. The layout and the micrograph of proposed converter.



(a)



(b)

FIGURE 20. Measured results of I_{LOAD}, at V_{IN} = 3.3 V, V_{OUT} = 2V, (a) I_{LOAD} = 500 mA and (b) I_{LOAD} = 100 mA.

$$\omega_{Z1} = \frac{1}{R_1 C_1}; \quad \omega_{Z2} \approx \frac{1}{R_3 C_2} \tag{27}$$

$$\omega_{P0} = 0; \quad \omega_{P1} = \frac{1}{R_2 C_2}; \quad \omega_{P2} \approx \frac{1}{R_1 C_3} \tag{28}$$

IV. EXPERIMENTAL RESULTS

The proposed converter has been implemented in TSMC 0.18μm Mixed-Signal/RF 1P6M processes with an active

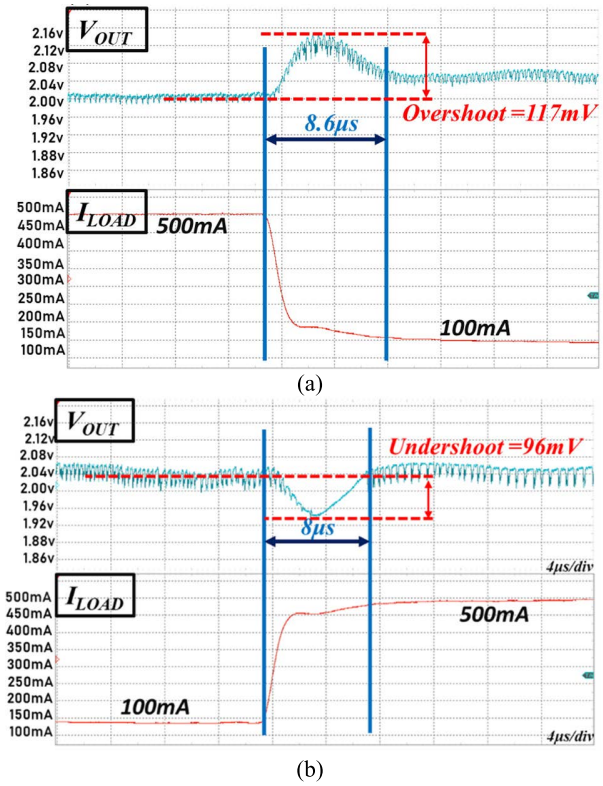


FIGURE 21. Measured results of transient response without the proposed accelerated scheme (a) 500 mA-100 mA (b) 100 mA −500 mA.

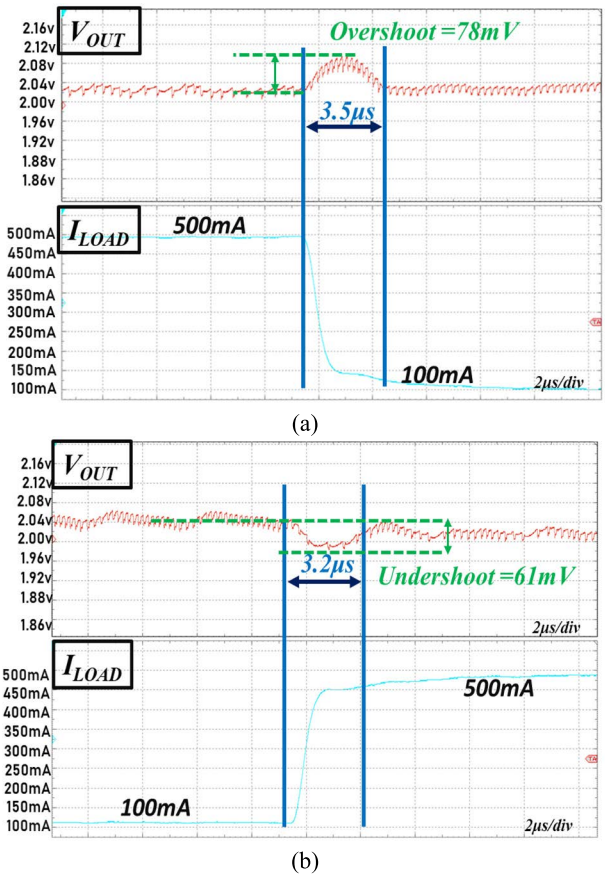


FIGURE 22. Measured results of transient response with the proposed accelerated scheme (a) 500 mA-100 mA (b) 100 mA −500 mA.

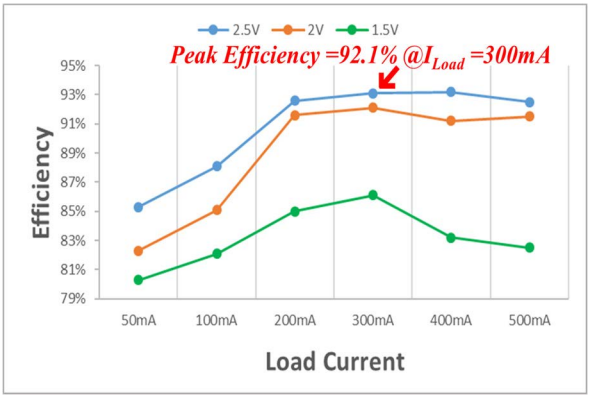


FIGURE 23. Measured efficiency of the proposed buck converter.

area of 1.26mm^2. And the layout and micrograph of the whole chip are shown in Fig. 19. Fig. 20 is the steady state waveform for the input voltage 3.3V and the output voltage 2V. Fig. 21 shows the experimental results of transient response of the buck converter without the proposed accelerated scheme. Additionally, Fig. 22 shows the experimental results of transient response of the buck converter with the proposed accelerated scheme. As the output load current varies from 500mA to 100mA and 100mA to 500mA, the transient response time are shortened to roughly 3.5μs and 3.2μs, which means that the transient time are improved by 60% respectively. With the objective of reducing the switching noise as well as enhancing the transient time and transient voltage, this paper proposes a fast-transient-response approach with hysteresis-voltage-controlled techniques applying to the second order delta-sigma-modulator buck converter. On the basic of the measured results of Fast-Fourier-Transform (FFT), the value of Output-to-Noise Ratio (ONR) is 76.6dB at the sampling frequency of 10MHz. As a result, it can be found that the transient time improves beyond 4μs when the load current varies with 400mA. Namely, it accelerates approximately 60% after transient-enhancement. As shown in Fig. 23, the peak conversion efficiency is 92.1% as the load current is 300mA. A comparison sheet is attached in Table 3, which compares the specification and performance of the proposed buck converter to others. The prominent point this work presented are listed as described below.

(1) With utilizing the proposed HVC techniques, we can ramp up the recovery time nearly 5μs.

(2) The second-order delta-sigma-modulator circuits and compensation circuits, which constitute the steady loop, overcome EMI problems as well as the switching noise to reduce the output harmonic tones.

TABLE 3. Comparisons to delta-sigma-modulator buck converters.

References		2020 [15]	2018 [20]	2018 [21]	2016 [22]	This Work
Technology		0.18μm	0.18μm	0.35μm	0.35μm	0.18μm
Topology		R-DSM	R-DSM	CT-DSM	DT-DSM	CT-DSM
Input Voltage (V)		2.5-5.0	2.5-5.5	3.3-3.6	3.6-5	3-3.3
Output Voltage (V)		2.0-4.6	1.0-2.4	1.0-2.5	1-3	1.0-2.5
Inductor (μH)		3	4.7	4.7	4.7	2.2
Capacitor (μF)		20	4.7	10	4.7	10
Sampling Frequency (Hz)		14 / 7M	3.75-15M	5 M	5.12M	10M
Max. Load Current (mA)		500	1000	600	500	500
Load Current Step (mA)		410	590	550	270	400
Transient Response(μs)	Light→Heavy	**65**	**20**	**16**	**10**	**3.2**
	Heavy →Light	**75**	**25**	**6**	**10**	**3.5**
Transient Voltage(mV)	Undershoot	**42**	**100**	****150**	**150**	**61**
	Overshoot	**43**	**110**	****160**	**150**	**78**
*ONR(Output-to-Noise-Ratio) (dB)		76	81	67.5	64	76.6
Peak Efficiency (%)		94.8	95.4	91.6	88.5	92.1
FOM		**0.09**	**0.23**	**0.35**	**0.1**	**1.3**

* ONR = Output-to-Noise Ratio ** Extracted from graph

$$FOM = \frac{Load\ Current\ Step\ (mA) \times Peak\ Efficiency\ (\%) \times ONR\ (dB)}{Maximum\ Transient\ Response(\mu s) \times Maximum\ Transient\ Voltage\ (mV)} \times 10^{-4} \quad [21]$$

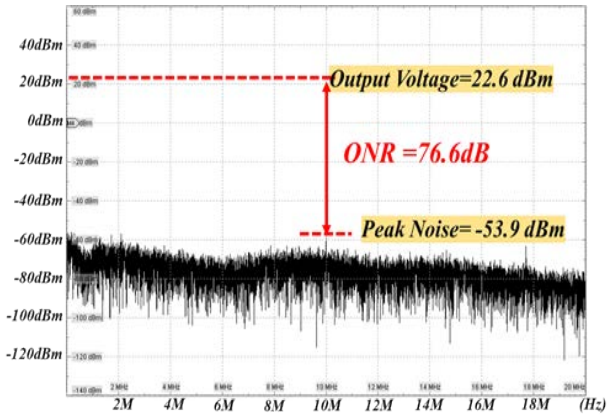


FIGURE 24. Measured spectrum of output voltage V_{OUT}.

(3) As seen Table 3, this work has a better FOM with the sampling frequency equal to 10MHz.

V. CONCLUSION

A low-noise fast-transient-response second-order delta-sigma-modulation buck converter with hysteresis-voltage-controlled techniques is proposed. With the proposed control approach, the transient time can be accelerated by roughly 60%. Besides, 2nd-Order delta-sigma-modulation plays a vital role of mitigating noise-interference and elevating SNR in whole circuits. The proposed converter has been fabricated in TSMC 0.18μm 1P6M CMOS processes with an active area of $1.19 \times 1.09\text{mm}^2$. The measured results show the transient time are 3.5μs and 3.2μs, respectively, when the load current changes between 500mA and 100mA. On the basic of the measured results of fast-fourier-transform (FFT), the value of output-to-noise ratio (ONR) is 76.6dB at the sampling frequency of 10MHz. The peak conversion efficiency is 92.1% while the load current is 300mA.

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