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Open Loop Synchronization Techniques Benchmarking for Distributed Energy Sources Connection

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ABSTRACT Synchronization is a crucial process in the operation of grid-connected distributed energy sources. Synchronization techniques are classified in closed-loop (CLS) and open-loop synchronization (OLS) techniques. Unlike the CLS technique, OLS techniques are recent and less known. This paper discusses a comparative analysis of the three prominent state-of-the-art OLS techniques. Accordingly, a benchmark model is proposed to systematically evaluate the performance of the OLS techniques under grid voltage disturbances such as harmonic distortions, voltage unbalance, DC offset, and low voltage ride through operation. Given the hardware resource utilization, the computational complexity and the execution time are also presented to judge the efficacy of the proposed model. Thus, engineers/or researchers can better understand the choice of hardware resources and the preferred dynamic performance of a synchronization scheme applied to control and protect a grid-tied power converter. Simulation and experimental results are presented and discussed to demonstrate the purpose of the proposed model.

INDEX TERMS Open-loop synchronization, benchmark, delayed-signal cancellation, reduced-order generalized integrator, renewable energy sources, grid side converters.

I. INTRODUCTION

In a modern power grid, distributed energy sources (DESs), mainly based on renewable energy, have an increasing share of the overall generation. To connect a power converter to a grid, one needs to provide it with information on the voltage phase and frequency. A synchronization algorithm is used to provide the power converter controller with such information. Traditionally, the synchronous reference frame phase-locked loop (SRF-PLL) is used for synchronization. The conventional SRF-PLL has a wide- bandwidth; thus, it can track fast and accurately the sudden phase or frequency jump. However, the presence of harmonics, voltage unbalance, and DC offset will seriously degrade its output. Filtering out these adversaries requires a narrow-bandwidth. For a long time, SRF-PLL provided a sufficient synchronization technique where the rapidity and accuracy were the main concern in the traditional power grid. However, the move from the centralized large power plant to the distributed renewable energy sources compromised the grid stability and deteriorated the quality of the voltage. Hence, the modern power grid is subjected to new standards and requirements that are developed in response to the increased penetration of DES and to enhance the stability and reliability of the grid [1]. Meeting these requirements involves providing the connected power converter with fast and accurate information about the grid voltage phase angle. The large penetration of power electronics in the modern power grid requires a synchronization technique that is simultaneously fast and robust; thus, conventional methods are no longer viable. In the last decade, many advanced synchronization techniques have been proposed in the literature [1]–[9]. The main effort of researchers is to

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develop a fast synchronization technique with high disturbance rejection capability and low computation burden [4], [6], [10]–[12].

By design, a PLL is susceptible to harmonics; hence, an in-loop or pre-loop filter is used. Introducing an in-loop filter will affect the dynamic of the PLL. Using a pre-loop filter will complicate the algorithm of the PLL since these filters are implemented in the stationary frame [10], [13], [14]. A frequency-locked loop (FLL) has been proposed to replace the PLL in power systems and power electronics applications [4], [8], [15], [16]. An FLL is a PLL implemented in a stationary frame [3]; hence, it inherited its drawbacks: enhancing its disturbances capability will affect the response time and complicate the design. The closed-loop synchronization technique, namely PLLs and FLLs, has a struggle between the stability margin, bandwidth, and filtering.

Frequency and phase locked loops are now in competition with another advanced technique as open-loop synchronization (OLS). An OLS employs a certain filtering technique to extract the fundamental component of the grid voltage directly without phase and frequency feedback loops. The filter includes discrete Fourier transform [17], [18], least squares estimation [19], [20], low-pass notch filters [21], Kalman filter [7], [22]–[24], cascaded delayed signal cancellation (CDSC) operator [25]–[27], and moving average filter (MAF) [28], [29].

In general, an OLS scheme is unconditionally stable and immune to disturbances [25], [30]. However, to be satisfactorily efficient, an OLS needs to be fast with low computational complexity. Three OLS techniques, including enhanced open-loop synchronization (ETOLS) [25], pseudo-open-loop synchronization (POLS) [31], and reduced-order generalized integrator (ROGI) based technique [32], are within the scope of these requirements. Unlike the previously reported OLS techniques, these techniques omit sine or cosine calculations to make their implementation in a low-cost microcontroller easier. Other advantages of these three techniques are the overall simplicity of the algorithm and easy tuning.

While the PLL and the FLL had their share of reviews [2], [4], [6], [10], [11], the OLS technique is relatively new, and as the knowledge of authors, no benchmarking is made to evaluate these techniques. While each technique was submitted to a certain test to confirm its performance, these tests differ from one paper to another.

To fill the gap in the state of the art of OLS, this paper proposes a benchmarking model that will allow distinguishing the performance of each technique. The benchmarking includes the main events that may occur in a power grid. To meet the standard and recommendation applied to the connection of a DES to the grid [33]–[37], the severity of the perturbation is elevated without exaggeration. For a better assessment, a systematic procedure that implies, not only the typical visual evaluation used in most publications, but also, a quantitative evaluation to give more insight into the performances of the synchronization method. Authors seek to provide a simple benchmark to the non-synchronization experts to evaluate several synchronization techniques to choose a proper method for their application.

The rest of the paper is organized as follows. Section II presents the mathematical model and the block diagram of methods. A benchmark is presented in Section III and applied to the methods as shown in Section IV. In Section V, a real-time implementation of the selected OLS techniques is presented. Finally, in Section VI, a discussion followed by a conclusion that summarizes the findings of the paper is presented.

II. OPEN-LOOP SYNCHRONIZATION TECHNIQUES

The quest of developing benchmarking models begins by revisiting three well-known pre-filtering techniques, i.e., the delayed signal cancellation operators directed towards the development of enhanced open-loop synchronization technique [25] and intermediate $\alpha\beta$-axes signal cross-coupling based synchronization techniques [31], [32]. It is important to stress that the organization of the fundamental phase detector unit in the respective schemes is of the same interest and avoided due to the wide acceptance. Further, the fundamental in-phase and quadrature signal extraction is an essential task achieved by a fast-responding pre-filtering stage. Consequently, the estimated phase angle information required for the generation of clean reference and optimal control of a grid-tied power converter is always dependent on the strong disturbance rejection ability of a synchronization scheme. With this interest, the mathematical model of the respective approaches, along with the merits and demerits, are discussed in this section.

A. ENHANCED OPEN-LOOP SYNCHRONIZATION (ETOLS)

In [25], the authors proposed a new open-loop synchronization technique named True Open-Loop Synchronization (TOLS). This method is based on multiple delayed signal cancellation (DSC). The DSCs are implemented in the $\alpha\beta$ frame; thus, authors refer to it as $\alpha\beta CDSC$ ($\alpha\beta$).

1) THE DELAYED SIGNAL CANCELLATION OPERATOR

In a three-phase system, the Clarke transformation is given by

$$\boldsymbol{v}_{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{(3)}}{2} & -\frac{\sqrt{(3)}}{2} \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{1}$$

If the voltage is contaminated with harmonics, the $\boldsymbol{v}_{\alpha\beta}$ is the sum of all harmonics given by:

$$\boldsymbol{v}_{\alpha\beta} = \sum_h \boldsymbol{v}^h_{\alpha\beta} \tag{2}$$

where $\boldsymbol{v}^h_{\alpha\beta} = V_h e^{h\omega t+\varphi_h}$ V_h is the magnitude. ω: Fundamental angular frequency. φ: The phase angle. h: is the harmonic order h = 1, 2 . . .

The signal $\boldsymbol{v}_{\alpha\beta}$ can be viewed as a group of space vectors, each of which is rotating at a speed of $h\omega$ and having its magnitude and phase. Positive sequence harmonics (7,13,19) rotate counterclockwise —in the same direction as the fundamental– generating heat by the Joule effect. Negative sequence harmonics (5,11,17) rotates clockwise causing motor torque problems [38]. Lets $\boldsymbol{v}^h_{\alpha\beta}$ a harmonic vector. Adding T/n (where T is the fundamental cycle and n is a delay factor) will delay the vector by (T/n) second or by a θ_n rad. $\theta_n = h\omega T/n = 2\pi h/n$. Multiplying the new delayed vector by a rotation angle θ_r will result in a new rotated vector [39]. The DSC operator is given by:

$$\begin{aligned} DSC_n\left[\boldsymbol{v}^h_{\alpha\beta}\right] &= \frac{1}{2}\left[\boldsymbol{v}^h_{\alpha\beta} + e^{-i\theta_r}\boldsymbol{v}^h_{\alpha\beta}\left(t-\frac{T}{n}\right)\right] \\ &= \frac{1}{2}\left[\boldsymbol{v}^h_{\alpha\beta} + e^{-i\theta_r}e^{-i\theta_n}\boldsymbol{v}^h_{\alpha\beta}\right] \\ &= \frac{\left(1+e^{-i\,(\theta_r+\theta_n)}\right)}{2}\,\boldsymbol{v}^h_{\alpha\beta} \\ &= \boldsymbol{G}\cdot\boldsymbol{v}^h_{\alpha\beta} \end{aligned} \tag{3}$$

The gain $\boldsymbol{G}$ is a harmonic specific gain given by:

$$\boldsymbol{G} = \frac{1+e^{-i(\theta_r+\theta_n)}}{2} = G\cdot e^{i\varphi} \tag{4}$$

with $G = |\cos(\theta_r+\theta_n)/2|$ and $\varphi = -(\theta_r+\theta_n)/2$ are the modulus and phase angle respectively.

In (3), the degree of attenuation of harmonic h is related to G. For a $\theta_r = -\theta_n$ G is equal to one; the DSC will pass the harmonic with a unity gain and zero-phase shift. For a $\theta_r = \pi - \theta_n$ G is zero; the DSC will eliminate the harmonic h. For real-time implementation, the vector form of the DSC given in (3) is rewritten in the time domain as:

$$DSC_n[\boldsymbol{v}_{\alpha\beta}(t)] = \frac{1}{2}[\boldsymbol{v}_{\alpha\beta}(t) + \boldsymbol{R}(\theta_r)\cdot\boldsymbol{v}_{\alpha\beta}(t-\frac{T}{n})] \tag{5}$$

where $\boldsymbol{R}$ is the rotation matrix given by

$$\boldsymbol{R}(\theta_r) = \begin{bmatrix} \cos(\theta_r) & \sin(\theta_r) \\ -\sin(\theta_r) & \cos(\theta_r) \end{bmatrix} \tag{6}$$

and θ_r is the rotation angle

$$\theta_r = -2\pi\frac{h^*}{n} \tag{7}$$

The block diagram of a DSC with $h = +1$ and n delay is illustrated in Fig. 1.

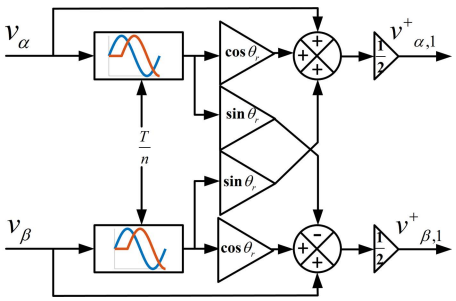

FIGURE 1. Block diagram of the DSC_n^{+1}.

2) EFFECT OF THE DSC ON $\boldsymbol{v_{\alpha\beta}}$

Applying the DSC operator on $\boldsymbol{v}_{\alpha\beta}$ signal will delay each harmonic by an angle $\theta_n = 2\pi h/n$ during an interval of T/n. Conversely, the rotation angle θ_r will have a uniform effect on all harmonics. Choosing $\theta_r = -2\pi h^*/n$ will yield to a unity gain and zero-phase shift of the harmonic $h = h*$ and zero gain for harmonics $h = h^* - \left(k+\frac{1}{2}\right)n,\ k = 0, \pm1, \pm2\ldots$. Other harmonics will be attenuated but not eliminated [39]. Hence, by selecting $h*$ and n, the DSC can be designed to pass, attenuate or eliminate a chosen harmonic. $DSC_n^{\pm h}$is the convention used by [40]. A $\pm$ indicates whether the harmonic is a positive or negative sequence. h: order of harmonic and n is the number of delays as delay factor.

It is worth mentioning that a single DSC operator cannot perfectly blocks all harmonics. Thus, Multiple DSCs are used in cascade —CDSC (Cascade DSC)— with each DSC designed to block a range of harmonics as more details are in [40]). In [25], the authors propose the CDSC as a building block for the TOLS. In the TOLS $h* = +1$, meaning the CDSC will have a unity gain and zero-phase shift for the fundamental positive component. To eliminate all major harmonics contained in $v_{\alpha\beta}$ the TOLS uses the $CDSC^{+1}_{4,8,16,32}$ (in [25] authors dropped the $+1$ notation).

To enhance the performances of the TOLS, authors in [25] used the cascade of two $CDSC_{4,8,16,32}$ and a compensation unit. The compensation unit is a countermeasure for the phase shift and magnitude scaling caused by the $CDSC_{4,8,16,32}$ operator. its transfer function is given by [25]:

$$G_c(s) = 1 + T_d(s - j\omega_n) \tag{8}$$

where $T_d = 15T/64$.

The enhanced TOLS (ETOLS) is given in Fig. 2. In [25] authors proposed other modifications to address certain issues such as the presence of DC offset or the presence of a highly unbalance voltage. Both modifications are named CTOLS1 and CTOLS2 respectively. For the sake of clarity and brevity, only the ETOLS is considered in this paper. For more detail about the two modifications, the reader may refer to [25].

B. PSEUDO OPEN-LOOP SYNCHRONIZATION

The POLS introduced in, [31], is based on the Positive Fundamental Component Estimator (PFCE) shown in Fig. 3 which is introduced first in [41].

The park transformation of a three-phase voltage is given by:

$$\boldsymbol{v}_{dq} = \frac{2}{3}\begin{bmatrix} \cos(\omega_n t) & \cos(\omega_n t - \frac{2\pi}{3}) & \cos(\omega_n t - \frac{4\pi}{3}) \\ \sin(\omega_n t) & \sin(\omega_n t - \frac{2\pi}{3}) & \sin(\omega_n t - \frac{4\pi}{3}) \end{bmatrix} \times \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{9}$$

where ω_n is the fundamental angular frequency.

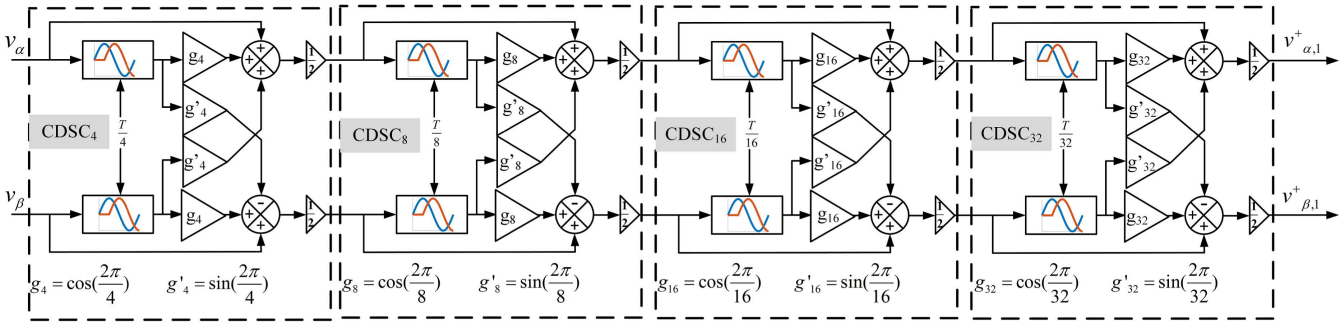

FIGURE 2. The block diagram of the Cascade DSC.

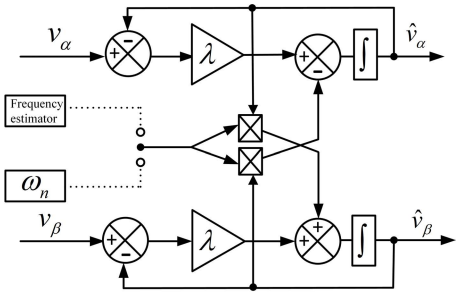

FIGURE 3. The block diagram of PFCE.

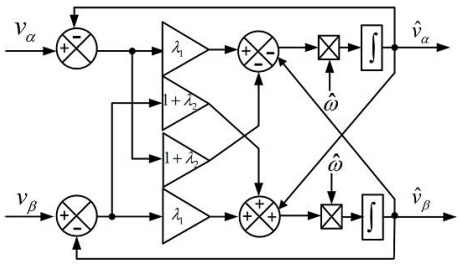

FIGURE 4. The block diagram of ROGI.

In the stationary frame, $\boldsymbol{v}_{\alpha\beta}$ is given by

$$\boldsymbol{v}_{\alpha\beta} = e^{\boldsymbol{J}\omega_n t}\boldsymbol{v}_{dq} \tag{10}$$

where $e^{\boldsymbol{J}\omega_n t}$ and $\boldsymbol{J}$ are given by:

$$lll e^{\boldsymbol{J}\omega_n t} = \begin{bmatrix} \cos(\omega_n t) & \sin(\omega_n t) \\ -\sin(\omega_n t) & \cos(\omega_n t) \end{bmatrix}$$
$$\boldsymbol{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \tag{11}$$

Deriving $\boldsymbol{v_{\alpha\beta}}$ yields:

$$\dot{\boldsymbol{v}}_{\alpha\beta} = \omega_n \boldsymbol{J}\boldsymbol{v}_{\alpha\beta} \tag{12}$$

Thus, the PFCE is given by

$$\hat{\boldsymbol{v}}_{\alpha\beta} = \omega_n \boldsymbol{J}\hat{\boldsymbol{v}}_{\alpha\beta} + \lambda\tilde{\boldsymbol{v}}_{\alpha\beta} \tag{13}$$

where λ is a damping factor and $\tilde{\boldsymbol{v}}_{\alpha\beta} = \boldsymbol{v}_{\alpha\beta} - \hat{\boldsymbol{v}}_{\alpha\beta}$.

The performance of the POLS depends on two parameters: the frequency estimator and λ. Using a constant frequency of 50 Hz will enhance the dynamic of the POLS at the expense of the frequency adaptability. Likewise, selecting a high value for λ will enhance the dynamics but compromise the POLS's immunity to voltage perturbation [31].

C. THE REDUCED-ORDER GENERALIZED INTEGRATOR

Another pseudo-open loop synchronization technique is presented in [32]. The authors used a reduced-order generalized integrator (ROGI) [42]. The transfer function of the estimator is given by [32]:

$$\frac{\hat{v}_\alpha(s) + j\hat{v}_\beta(s)}{v_\alpha(s) + jv_\beta(s)} = G_{\alpha\beta}(s) = \frac{\lambda}{s - j\hat{\omega} + \lambda} \tag{14}$$

where $\hat{\omega}$ is the estimated angular frequency; $-\lambda \pm j\hat{\omega}$ is the eigenvalue as making the ROGI only tunable by its real part. In [32], the authors proposed an enhancement to the ROGI as shown in Fig. 4 making it tunable by both the real and imaginary parts.

$$\begin{cases} \dot{v}_\alpha = -\hat{v}_\beta\hat{\omega} + \lambda_1(v_\alpha - \hat{v}_\alpha)\hat{\omega} - (1+\lambda_2)(v_\beta - \hat{v}_\beta)\hat{\omega} \\ \dot{v}_\beta = \hat{v}_\alpha\hat{\omega} + (1+\lambda_2)(v_\alpha - \hat{v}_\alpha)\hat{\omega} - \lambda_1(v_\beta - \hat{v}_\beta)\hat{\omega} \end{cases} \tag{15}$$

The transfer function of the new ROGI —refereed afterward simply as ROGI— is given by:

$$\frac{\hat{v}_\alpha(s) + j\hat{v}_\beta(s)}{v_\alpha(s) + jv_\beta(s)} = G_{\alpha\beta}(s) = \frac{\lambda_1 + j\lambda_2}{s - j\hat{\omega} + \lambda_1 + j\lambda_2} \tag{16}$$

Eigenvalues of ROGI are $\hat{\omega}(\lambda_1 \pm j\lambda_2)$, making the ROGI tunable in both real and imaginary parts. Thus, the user has more control over the dynamic performances of ROGI.

III. PROPOSED BENCHMARK MODEL

To be connected to the power grid, a DER must satisfy the technical requirement of the country grid code. A distribution system operator (DSO) and/or transmission system operator (TSO) will require specific measures to be satisfied in case of a power quality issue. A synchronizer unit must provide the fundamental components of the grid voltage event under adverse power quality to allow the DER to remain synchronized during a disturbance event.

The proposed benchmark model addresses two parts that reflect real-world problems in a power grid. The first part deals with the dynamic events, shown in cases A to D, with a limited time lap. The main trigger of such events is the sudden connection/disconnection of a load or a source and line fault. The goal of these tests is to check the capability of

the synchronizer to deliver the voltage phase after a sudden change in voltage parameters, including magnitude, phase, or frequency. The second part deals with steady-state events, as shown in Cases E-G. These are power quality problems that may occur in a grid and take a long time as several periods. They are caused by the nature of the loads/source due to an ill-designed control and an uneven distribution of single-phase loads or the nonlinear nature of the loads are the cause of the most power quality problems. The goal of such tests is to check the performance of the synchronizer in accurately tracking the phase of the fundamental component of the voltage under a non-ideal main voltage.

The benchmark is designed to take into consideration the most important events that may face a grid-connected inverter. Table 1 shows the values derived from international standards and recommendations that deal with the connection of the DER to the grid. The European norm (ENTSO [34], [35]), the IEEE standard (519-2014 [37] and 1547-2018 [36]), and the NEMA standard [43] are used in this work.

TABLE 1. The benchmark parameters.

Case	Component	Value
	150 Hz	10%
	250 Hz	9%
	350 Hz	8%
Harmonic	550 Hz	7%
	160 Hz	7 %
	20 Hz	7 %
Unbalance	Negative sequence	27%
ROCOF		5 Hz/s
Phase Jump		40°
DC offset		0.5

The benchmark covering seven cases is detailed as follow:

A. FREQUENCY STEP JUMP

The goal of this benchmark is to test the capability of the synchronizer to provide an accurate estimation under a frequency change. IEEE 1547 defines Frequency ride-through requirements between 62 Hz and 57 Hz (5 % High-frequency ride-through and 3.3% for Low-frequency ride-through) [36]. European countries limit the values between 52 Hz and 47 Hz [35].

B. PHASE JUMP

Most grid codes do not include a phase jump requirement [44]. However, in the future, a phase jump could be included. Under the South Africa grid code, a DER must remain connected over a phase jump of 40° [33].

C. RATE OF CHANGE OF FREQUENCY (ROCOF)

Between the minimum and maximum allowed frequency as $47 - 52$ Hz, a DES must maintain operation under a shift in frequency that has rates specified by the operator. According to generation capacity, the frequency change rate is limited between 0.5 Hz/s and 3 Hz/s by IEEE 1547 [36] and 0.5 and 2.5 Hz/s adopted by ENTSO-E in Europe [34], [45].

D. LVRT

Low voltage ride through is a specification at which a DER shall maintain synchronism with the EPS area despite the disturbances in the mains voltage [34], [36]. The synchronization algorithm is required to provide the grid-tied inverter with the voltage information through the LVRT fault. The profile of the voltage differs from countries. In this benchmark, the German profile is used [46].

E. HARMONIC DISTORTION

IEEE 519-2014 limits the voltage total harmonic distortion to 8% for low voltage systems and 1.5% for high voltage systems as well as 5% to 1% for individual harmonics. The inter harmonic is harmonic with a frequency that is not an integer multiple of the fundamental frequency (as opposed to characteristic harmonic) [37]. IEEE $519 - 2014$ limits the inter-harmonics to 5% for individual harmonics [37].

F. UNBALANCED VOLTAGE

A voltage unbalance occurs mainly due to the non-uniform distribution of the single-phase loads over the three-phase grid. This kind of behavior is observed in low and medium-voltage grids. A voltage unbalance negatively affects rotating machines. ANSI $C84.1 - 220$ [43] limits the maximum voltage unbalance to 3.0% under no-load conditions.

G. DC OFFSET

Although DC current injection is limited below 1% in most legislation [47], Voltage DC component may appear in the microgrid due to grid faults, measurement devices, DC injection from DES,etc [48]. A good synchronizer will remove the DC offset from the fundamental.

H. EVALUATION METHOD

In the literature, a visual evaluation is widely used to determine the performance of a synchronization technique. Authors usually plot the response of multiple methods and then evaluate them based on the look of the graph. This method, even if it is effective in some instances, is not the best suited especially when comparing methods with similar performances or comparing several methods.

A quantitative-based comparison is the best approach to evaluate several methods accurately. Hence, in this paper, an evaluation based on the Root Mean Square Error (RMSE), which is a statistical method that allows the evaluation of deviation of the estimated measurement from the real one using a single number, is suggested. The RMSE is given as:

$$RMSE = \sqrt{\frac{\sum_{i=1}^{N} (x_i - \hat{x}_i)^2}{N}} \tag{17}$$

where $(x_i - \hat{x}_i)$ is the error between the estimated and the actual value. In this benchmark, the visual evaluation is based on the following plots:

1) The waveform of the estimated voltage: The fundamental component of the mains is plotted alongside

TABLE 2. Normalized root mean square error.

	Frequency jump		Harmonics		Unbalance		DC offset	
	Phase	Magnitude	Phase	Magnitude	Phase	Magnitude	Phase	Magnitude
Before norm	0.0022	0.0029	0.1	0.11	0.026	0.003	0.5	0.51
ETOLS	1	1	1	1	1	1	1	1
POLS	0.57	0.57	0.23	0.03	0.33	0.01	0.03	0.04
ROGI	0.32	0.32	0.84	1.68	518.75	120.44	0.56	0.69

the estimated fundamental part of each method. This presentation allows us to visually assess the accuracy of the estimation for each method.

2) The magnitude error: By subtracting the fundamental component of the mains to the generated waveform, we can represent the deviation of the estimation from the reference.
3) The phase error: The phase of each generated voltage is extracted and then subtracted from the mains phase.

The quantitative evaluation is based on the RMSE as described in Fig. 5, where the number of samples N can be selected independently of the length of a period. However, choosing an N big enough to cover several periods will provide more accuracy. Table 2 presents a normalized RMSE for the three methods —values are normalized to the ETOLS method- raw data are available in a data repository [49].

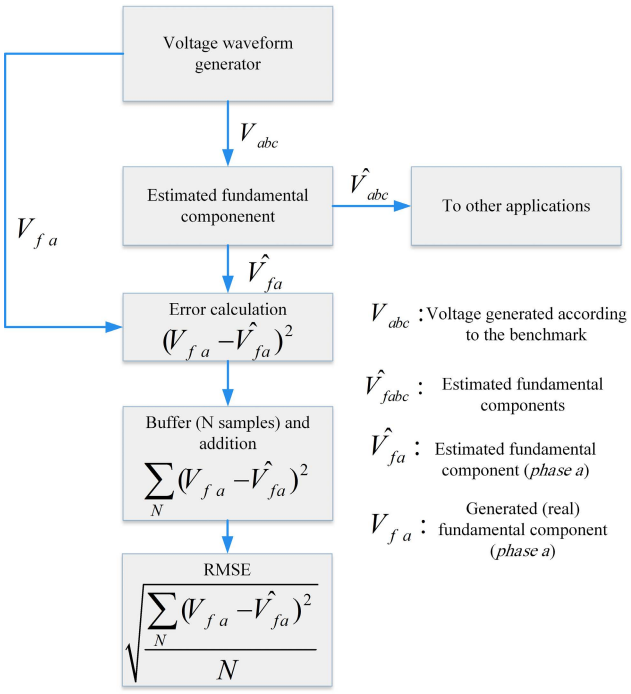

FIGURE 5. Flowchart of RMSE calculation.

To choose a synchronization or to design a new one, it can follow the steps illustrated in Fig. 5:

1) Develop the waveform generator block based on the benchmark shown in Table 1.
2) The synchronizer takes as input the waveform generated. The outputs are the estimated fundamental components, the estimated frequency, and the phase.
3) The error between the fundamental and its estimation is then calculated and buffered. For better accuracy, the buffer size must correspond to at least the number of samples during a period of the fundamental 0.02 s for 50 Hz. Finally, the RMSE is calculated by (17).

It is preferable that the designer tests all cases; however, cases with no interest can be omitted. Since the choice is based on several cases, a visualization of the obtained RMSE is recommended to draw the big picture. To draw a picture, the performance comparison of the methods is studied to draw a rough idea of the strength and weakness of each compared method and the proper application. The radar chart is a good way to summarize the performances in one graph. It is recommended to use one synchronization method as a base to normalize all other data. Since visually the bigger is better, it needs to inverse the values; thus, the lowest RMSE will be visually attractive.

IV. TEST RESULTS AND DISCUSSION

In this section, the proposed benchmarking model is applied to the three-synchronization methods to evaluate their performances. The methods are evaluated using four criteria previously mentioned. For a fair comparison, the three algorithms are tuned according to their respective articles. For the ETOLS [25] there is no parameter to tune, however, authors proposed four variants: TOLS, ETOLS, CTOLS2, CTOLS3 but focused on the ETOLS. For the ROGI based POLS, we take the same parameters as the paper, $\lambda_1 = \lambda_2 = 1/\sqrt{2}$ [32]. Finally, for the POLS we took $\lambda = 50$ [31].

A. FREQUENCY STEP JUMP

In this step, a sudden frequency jump of 3 Hz is introduced. The main frequency jumped from 50 Hz to 53 Hz as shown in Fig. 6(a). For the frequency estimation, the 5% settling time of 53± 0.15 Hz of the ETOLS and ROGI was 30 ms, while the POLS had a settling time of 323 ms. Fig. 6(b) shows the fundamental and generated waveform of phase of the three algorithms. The three algorithms generated a pure sinusoidal waveform. To get more insight, the magnitude and phase error between the fundamental and its estimation is displayed in Figs. 6(c) and 6(d). The three algorithms presented a faint magnitude and phase error. Table 2 shows a quantitative presentation of the magnitude and phase error. In this test, the POLS had the largest settling time, but it had a lower

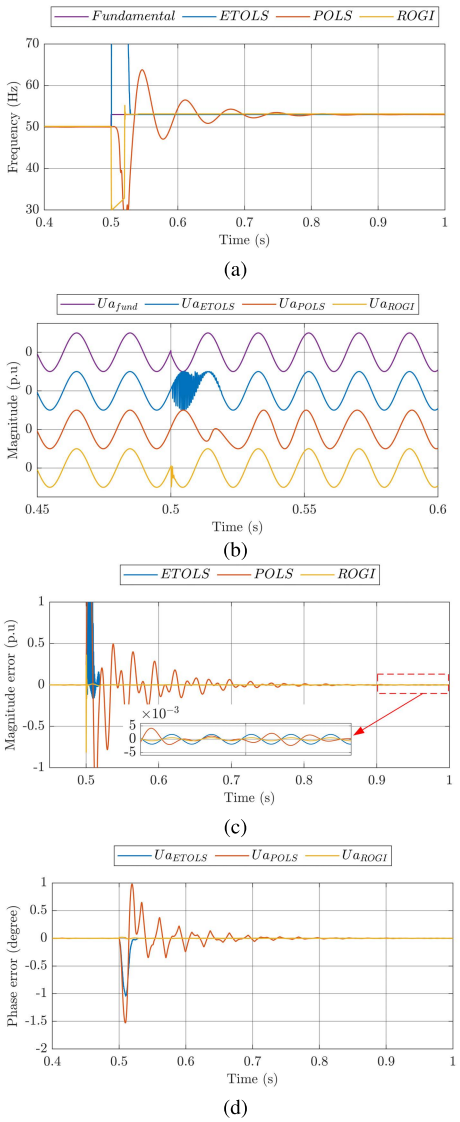

FIGURE 6. Synchronization algorithm response to a frequency jump. (a) Estimated frequency, (b) the output unitary waveform, (c) magnitude error, (d) phase error.

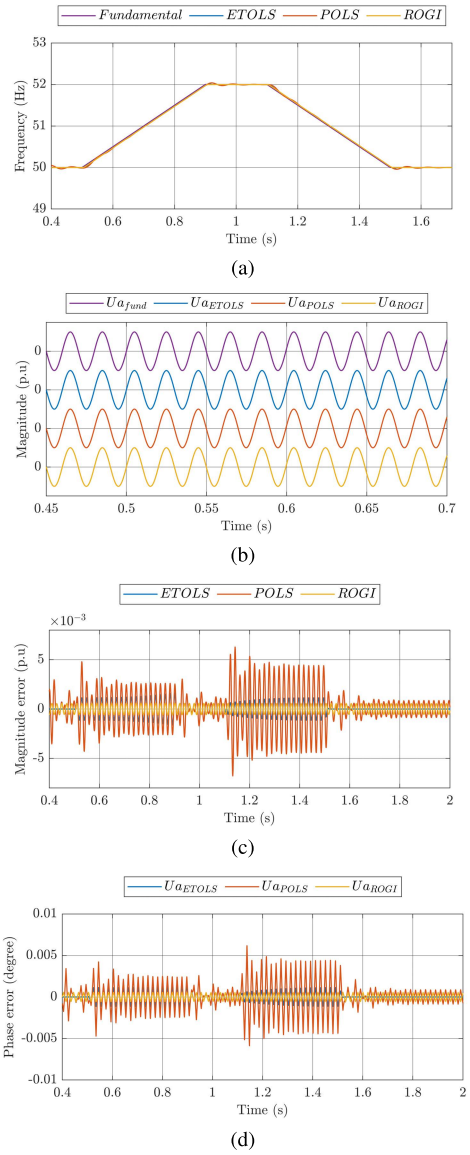

FIGURE 7. Synchronization algorithm response to a frequency ramp. (a) Grid voltage, (b) The output unitary waveform, (c) Magnitude error, (d) Phase error.

error than the ETOLS. It is worth mentioning that a 3 Hz step-change differs drastically from a 2 Hz step change.

After a dynamic response, the three-algorithms settled with a magnitude RMSE of 13×10^{-4}, 12×10^{-4}, and 0.4×10^{-4} for the ETOLS, POLS, and ROGI respectively. This faint error demonstrates the frequency adaptivity of the three algorithms.

B. RATE OF CHANGE OF FREQUENCY

The rate of change of frequency (ROFOC) has been set to 5 Hz as shown in Fig. 7(a). Under this frequency change, all the algorithms showed a good tracking performance with a minor error as shown in Figs. 7(b)-(d).

C. PHASE JUMP

In this scenario, a sudden phase jump is introduced in the three phases at 0.5 s in Fig. 8(a). The generated waveform, magnitude error and phase error in Figs. 8(b)-(d), respectively, show that the ROGI had the fastest response. The ETOLS had some chattering during a half period. The POLS had the longest dynamic response.

D. HARMONIC DISTORTION

The voltage is contaminated with harmonics, sub-harmonics, and inter-harmonics as shown in Table 1 and Fig. 9(a). Under this severe perturbation, the ETOLS and POLS generated a pure sine wave in Fig. 9(b), with the POLS having the smallest magnitude and phase error as shown in Figs. 9(c) and 9(d). The ROGI had relatively the worst performances where the generated output is visibly not a pure sine wave. Table 2 shows the advantage of the POLS over the ETOLS

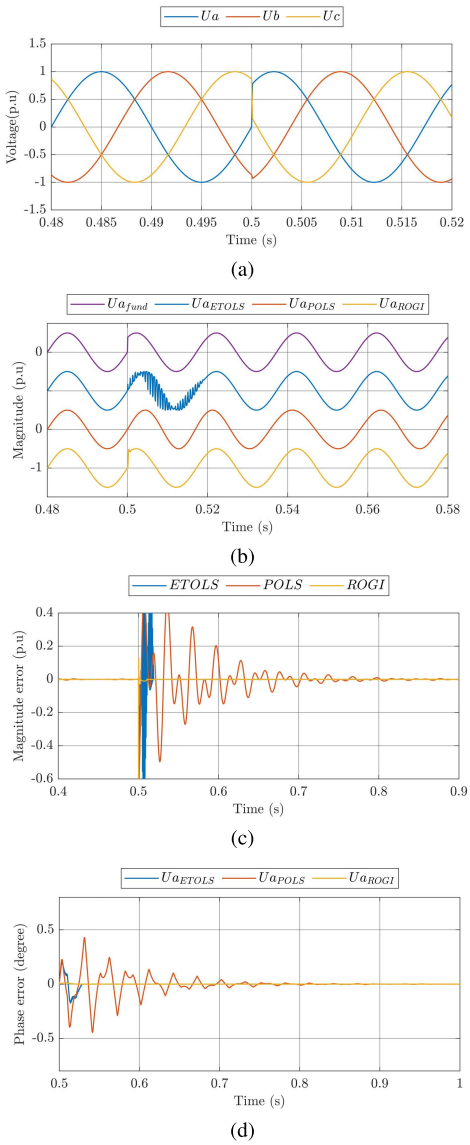

FIGURE 8. Synchronization algorithm response to a phase jump. (a) Grid voltage, (b) The output unitary waveform, (c) Magnitude error, (d) Phase error.

and ROGI in terms of harmonic rejection, where the RMSE error of the POLS is 0.03 times lower than the ETOLS.

E. UNBALANCED VOLTAGE

In this case, a negative sequence of 21% is injected into the mains; thus, an unbalance in the three-phase voltage is created as shown in Fig. 10(a). Under this condition, unlike ROGI, the ETOLS and POLS managed to generate a pure sine wave in Fig. 10(b). The magnitude in Fig. 10(c) and phase error in Fig. 10(d) of the ROGI demonstrated its inefficiency to perform under severe unbalanced conditions. The POLS, on the other hand, had the best performances.

F. LVRT

The LVRT is the most severe test. One of the challenges of LVRT is the ability to resynchronize after a total loss of

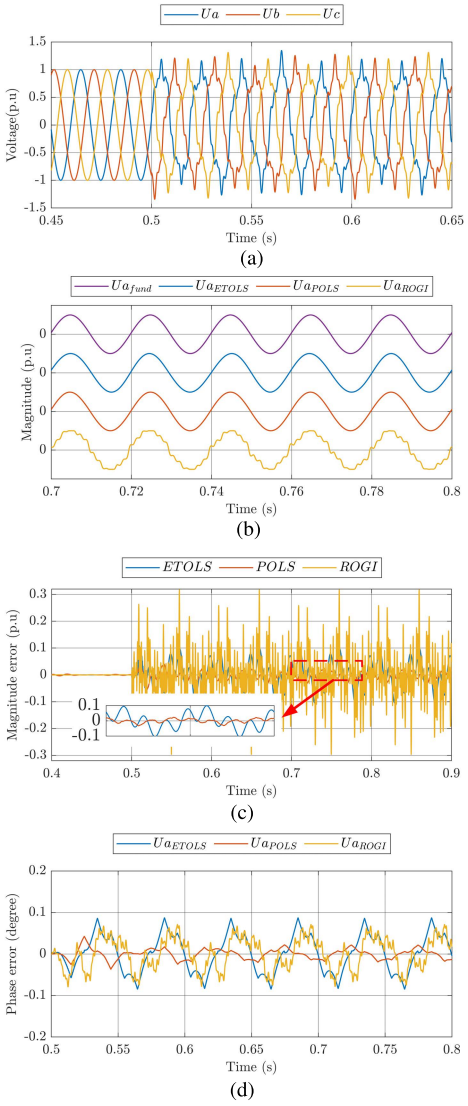

FIGURE 9. Synchronization algorithm response to a harmonic contaminated voltage. (a) Grid voltage, (b) the output unitary waveform, (c) magnitude error, (d) phase error.

the voltage. In our case, the voltage is lost at 0.5 s and starts recovering at 0.65 s [46]. Fig. 11 shows the simulation result of the LVRT test. ETOLS and ROGI had a very fast dynamic. POLS, on the other hand, needed 5 cycles to enter the 10 % error band.

G. DC COMPONENTS

In this test, a DC component is added to phase b in Fig. 12(a). ETOLS and ROGI generated a non-sinusoidal waveform, with the ROGI having the largest magnitude and phase error. On the other hand, the POLS generated a pure sine waveform with a faint magnitude and phase error as shown in Figs. 12(b)-(d), respectively.

H. PERFORMANCE COMPARISON AND SELECTION GUIDELINES

By analyzing the simulation results shown in Figs. 6 to 12 and the data in Table 2, the following points are derived:

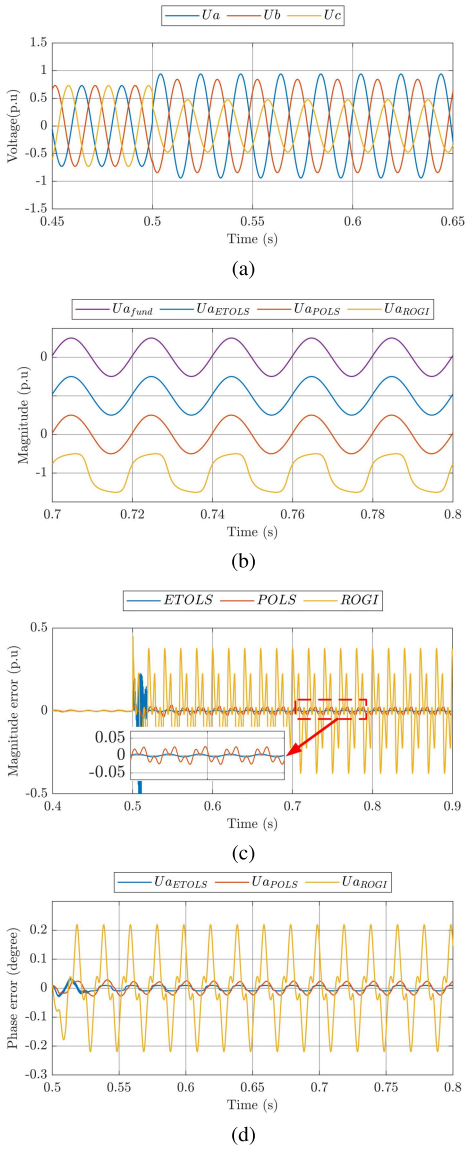

FIGURE 10. Synchronization algorithm response to an unbalanced voltage. (a) Grid voltage, (b) the output unitary waveform, (c) magnitude error, (d) phase error.

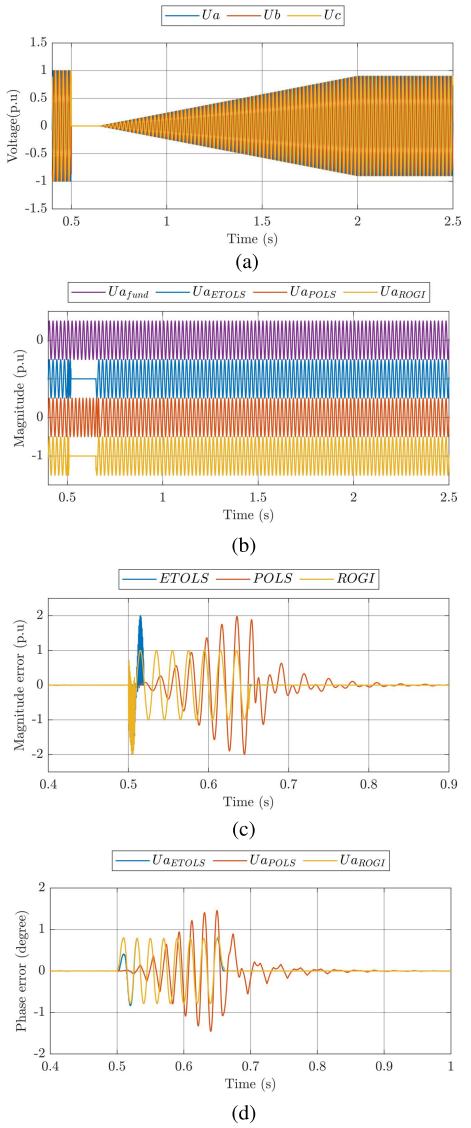

FIGURE 11. Synchronization algorithm response to an LVRT situation. (a) Grid voltage, (b) The output unitary waveform, (c) Magnitude error, (d) Phase error.

- The ROGI had the best dynamic performances with settling time lower than the other two algorithms. However, its performance decreased drastically under off-nominal voltage conditions.
- The POLS had the best performances under heavy power quality issues: Harmonic contamination, unbalance, and DC offset. But it has a slow dynamic response.

Under ideal conditions, the ETOLS had no estimation error. However, it had the largest RMSE after a frequency change. It had a better dynamic response than the POLS and a better filtering capability than the ROGI.

Based on these remarques, one can draw a picture of the best synchronization algorithm that better fits the application. For example, in the case of a weak grid with a power quality problem, the best choice is the POLS. In the case of a grid with an unset frequency (for example, islanded microgrid), the ROGI will perform the best. For a compromise between dynamic and filtering capability, the ETOLS is the right choice.

Another alternative is to tune a synchronization algorithm so that it covers more area in the charts. For example, tuning the POLS needs only one parameter. A low λ means a more accurate estimation of the PFCE but a slower settling time. To address the issue of the settling time, one can use a higher λ. ROGI, on the other hand, uses two parameters (λ_1 and λ_2) for the tuning. The ETOLS has no parameter to tune, but to customize the estimation accuracy or the settling time, one needs to add/delete CSDC as the case with CTOLSI and CTOLSII [25]. Hence, to customize the ETOLS, one needs to change its structure.

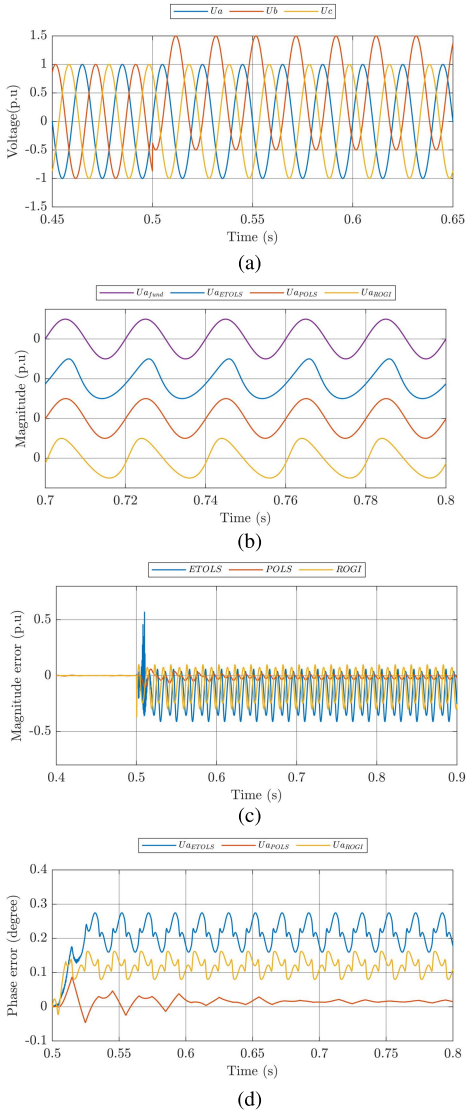

FIGURE 12. Synchronization algorithm response to a DC offset. (a) Grid voltage, (b)The output unitary waveform, (c) Magnitude error, (d) Phase error.

The radar chart shown in Fig. 13 visually illustrates the finding of the benchmark. In addition to the simulated model, it includes the tuning difficulty and the execution time. The execution time in Table 3 is measured using the RTI library in a dSPACE 1104 [50]. The more area an algorithm covers, the more polyvalent it is.

TABLE 3. Execution time.

Method	Execution time
ETOLS	$40\mu s$
POLS	$3\mu s$
ROGI	$40\mu s$

I. EXPERIMENTAL RESULTS

The benchmark is validated experimentally using the same simulation steps. For rapid prototyping, the authors propose

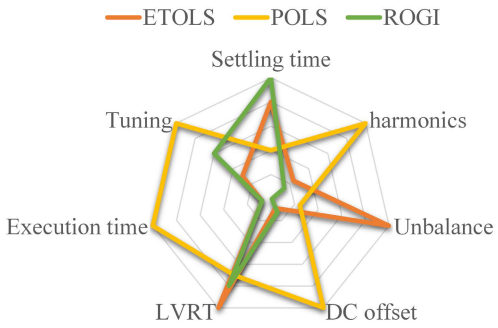

FIGURE 13. Performances of synchronization methods.

to follow the method used in [31]. The signal generator is implemented in a real-time digital platform of the dSPACE 1104, but instead of feeding the generated signal directly to the synchronization algorithm, a Digital to Analog Converter (DAC) is used to send the signal out of the card. Then, an Analog to Digital Converter (ADC) is used to read the generated analog signal and feed it to the synchronization algorithm. This method allows the emulation of reading a signal from a physical sensor. Thus, the benchmark is simplified by eliminating the need for a programmable voltage source that may not be available for the researcher. In this paper, we used two dSPACE 1104 platforms as shown in Fig. 14, the first implements the benchmark model, and the second hosts these three tested synchronization methods. The execution time is measured using the RTIlib library [50]. Fig. 15 shows the experimental results of the benchmark model. One obvious remark is the similarity between the simulation and the experimental results. This is logical since the same benchmark model (signal generator) is used.

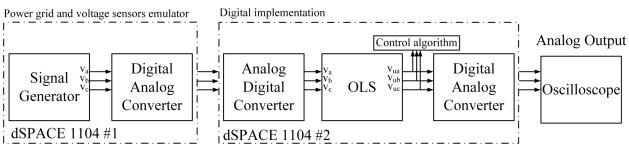

FIGURE 14. The experimental setup.

The dynamic behavior of the three algorithms under a frequency step jump and frequency ramp are presented in Figs. 15(a) and 15(b). The similarity between these figures and Figs. 6(a) and 7(a) is observed where the POLS had the largest response time. Under a phase jump, the three algorithms had a clean sinusoidal output as shown in Fig. 15(c). In Fig. 15(d), the harmonic contamination in the grid voltage is considered as per the simulation environment scenario as shown in Fig. 9. Note that all the schemes are able to generate clean unit template signals. In even to voltage imbalance shown in Fig. 15(e), it can be observed that the ROGI scheme yields non-linear behavior in the unit template generation despite using a good pre-filtering approach. Note that POLS and ETOLS scheme are more suitable choices for grid voltage unbalance. Further, the grid voltage undergoes nearly a zero

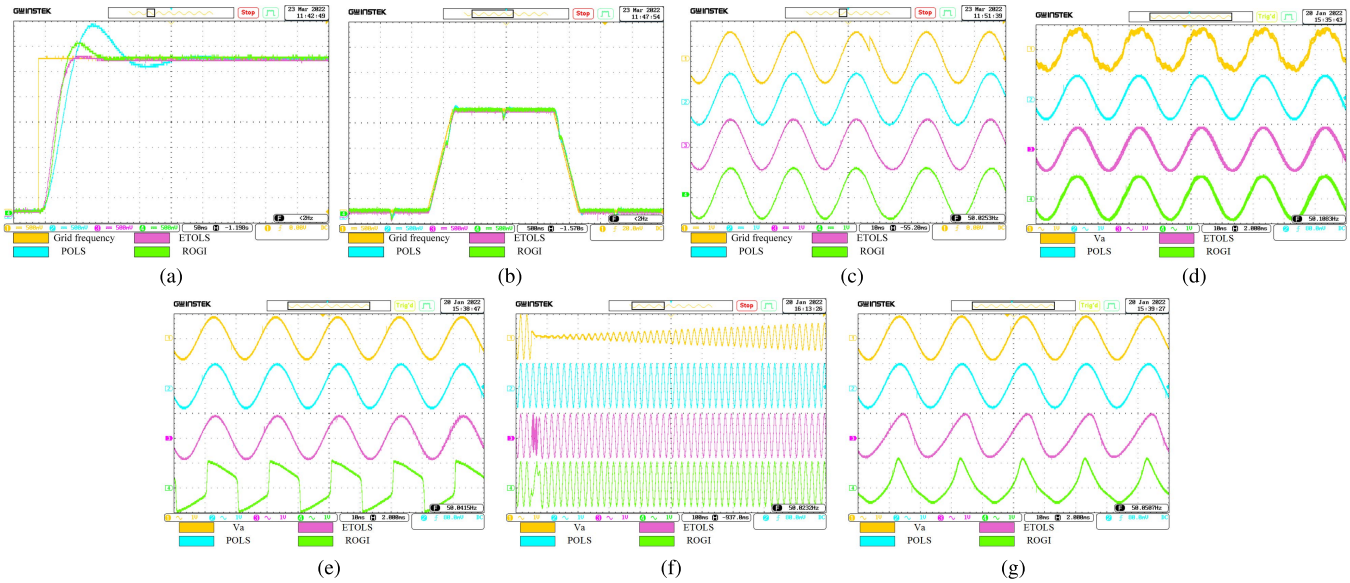

FIGURE 15. Experimental validation of the benchmark model. (a) Frequency jump, (b) Rate of change of frequency (ROCOF), (c) Phase Jump, (d) Harmonic contamination, (e) Voltage unbalance, (f) LVRT, (g) DC offset.

voltage drop along with a slow variation in the voltage signal as shown in Fig. 15(f) indicating the dynamic performance evaluation of the schemes for an LVRT event. Note that the POLS has better potential capability to generate the clean reference signal and can help maintain a better phase synchronization with the utility grid. Nevertheless, ETOLS and ROGI will suffer from an abrupt loss of synchronous operation and may consequently lead to grid-tied inverter failure. Finally, when the grid voltage is contaminated with 0.5 pu DC-offset as shown in Fig. 15(g), it is clear that the POLS has a superior performance in generating clean reference signals when compared to the ETOLS and the ROGI schemes.

Testing the synchronization algorithm in a real-time platform will allow engineers to assess the feasibility of running on a digital platform and check the execution time in a real-time application.

V. CONCLUSION

A benchmark for open-loop synchronization techniques is developed in this paper. The benchmark model aims to evaluate the behavior of the synchronization techniques in case of power grid adverse such as frequency step jump; frequency ramp; harmonic pollution; voltage unbalance; LVRT situation; the presence of a DC offset. Three open-loop synchronization techniques are presented and evaluated using this benchmark: the ETOLS, POLS, and ROGI. The performance of each method is analyzed and evaluated. The strength and weaknesses of each technique regarding each case have been highlighted. Then, a recommendation on choosing the proper synchronization technique is presented. Finally, an experimental protocol has been proposed to validate the synchronization method in a real-time digital platform and measure the execution time. Experimental results are in perfect match with the simulation tests.

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