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Switched LC Network-Based Multistage Ultra Gain DC-DC Converter

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ABSTRACT A multi-stage active switched inductor-capacitor network (SLCN)-based high gain DC-DC converter structure with a single switch is proposed in this paper. The idea of utilizing multiple number of SLCN networks to achieve an ultra-voltage gain is proposed. The achievement of ultra-gain helps to operate the converter at lower duty ratio. Hence, a reduction of conduction loss, improvement in efficiency and elimination of core saturation are attained in the proposed bi-quadratic converter compared to the conventional converters. The performance of a biquadratic boost converter which is formulated from the n-stage SLCN converter for $n = 2$, is analyzed. To reduce the effect of parasitic elements of the semiconductor devices, the SiC-based devices are selected. The small-signal model of the biquadratic converter is derived, and a PI controller is designed to regulate the output voltage. The designed controller is implemented using XSG platform. Experimental waveforms for 650 V output voltage, 500 W output power and 50 kHz switching frequency are presented. The performance of the proposed converter with similar recently reported topologies is compared. Simulation results of the bi-quadratic converter interfaced solar PV panel with P&O algorithm are presented to assess the feasibility of the proposed converter in solar PV application.

INDEX TERMS DC-DC converter, high voltage gain, switched LC network, wide bandgap devices.

I. INTRODUCTION

More than three decades, the high and medium voltage DC systems have been utilized successfully to transmit the power collected from the renewable energy sources (RESs). But, the output voltage produced by these RESs like solar PV module and fuel cell is lower. The modules are used to connect in series to enhance the solar PV panel voltage. Whereas, the output power produced by the panel is affected due to hot spot, partial shading, etc. Hence, a parallel connected PV panel gives better performance compared to the series connected PV panel. In conventional approach as shown in Fig. 1(a), a step-up transformer is used along with the boost converter to integrate this low voltage RES to improve the voltage level of the load. However, this step-up transformer gives poor performance in the PWM power topologies, and also it is bulk in size and more in weight. To overcome the demerits of using transformer in the RES integration application, DC-DC converters with a high DC-voltage gain are proposed as an alternative approach in Fig. 1(b). A complete removal of the transformer [1]–[2] is achieved in this approach, so the overall system size is reduced. Apart from the aforementioned RES integration, these converters are used in the applications such as medical X-ray, electrostatic precipitation, high-energy physics, [3] telecommunication

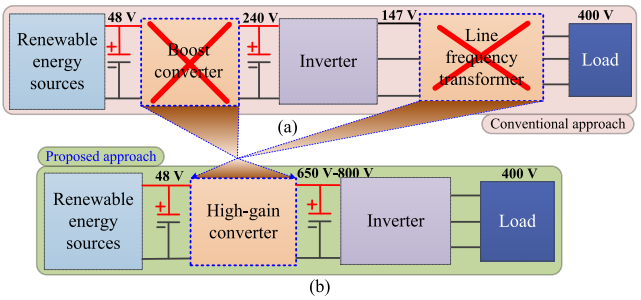

FIGURE 1. Application (a) Conventional approach, (b) Proposed approach.

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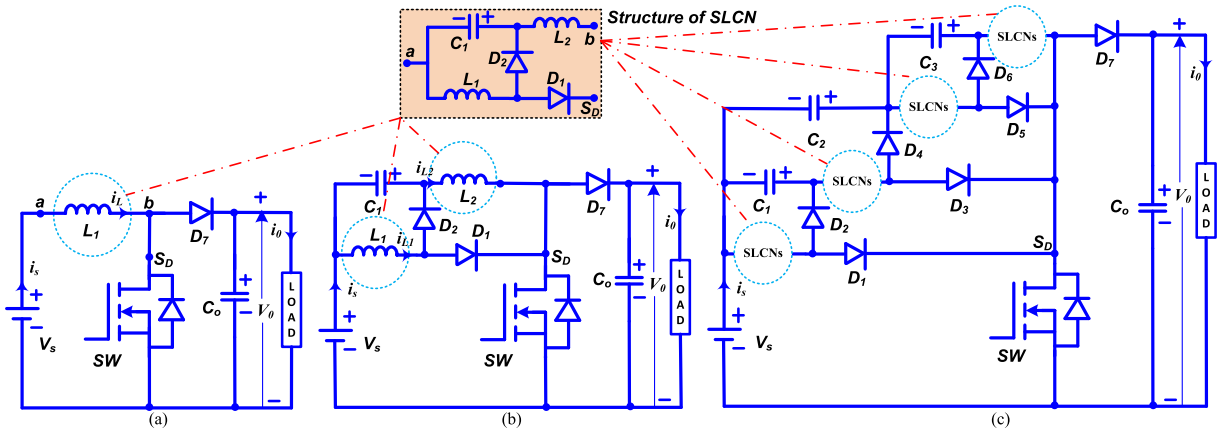

FIGURE 2. (a) Boost converter (b) Quadratic boost converter for n = 1 (c) Proposed n-stage SLCN-based DC-DC converter.

equipment, etc. In addition, these converters are employed in the offshore wind farms to convert low voltage DC to medium voltage DC [4], [5]. The classical boost converter is widely used in some of the applications to enhance the output voltage. But, it has a voltage gain of $1/(1-D)$. To increase the voltage gain, the concepts based on switched inductors and switched capacitors are introduced [6], [7]. A wide voltage range DC-DC converter using a switched capacitor (SC) is presented with a gain of $2/(1-D)$ in [8]. A modified SEPIC converter with a gain of $(1+3D)/(1-D)$ is reported in [9]. The converter utilizes ten components, and produces the maximum gain of seventeen. By combining the switched inductor (SL) and SC, active switched LC network-based high gain DC-DC converters are reported in [10], [11]. But, these converters produce the maximum voltage gain $G < 30$.

A high gain converter is presented by incorporating the charge pump concept, self-lift circuit and voltage multiplier (VM) cells [12]–[15]. Using a capacitor clamped submodule, a high gain converter is presented for the HVDC application [16]. The converter achieves a gain of $n/(1-D)$. An n-stage high gain converter using SL concept is presented in [17]. The converter achieves a gain of $[(1+(2n+3))/(1-D)]$. Few more n-stage high gain DC-DC converters [18]–[19], [25] and single stage [21]–[24] are reported in the literature. As the number of stages increases, the components count also increases. Some of these converters utilize more components when the converter extended to next stage, that increases the converter losses, bulkiness of the converter, etc. Some of the high gain DC-DC converters are reported in [27]–[30]. These converters use 2 switches in the topological structure; moreover, the converter [28] has a limitation in the operating when duty ratio $D > 0.5$ (ideally). As shown in Fig. 1, the high gain non-isolated DC-DC converters are proposed to replace the transformer. The transformer is used to step-up the voltage and to provide the galvanic isolation. For the applications where the galvanic isolation is not mandatory like stand-alone solar PV, portable devices, high voltage test equipment, etc, the voltage gain provided by the transformer is met by the non-isolated DC-DC converter. The suppression of the leakage current is facilitated by the inverter unit which is coupled with the dc-dc converter [32].

A novel n-stage high gain DC-DC converter structure, which is basically derived from the boost converter, is presented in this paper. Fig. 2(a) shows the structure of the boost converter [26]. By replacing the inductor L (across terminal a-b) by an active switched inductor-capacitor network (SLCN), a high gain DC-DC converter [Fig. 2(b)] is reported with a voltage gain of $1/(1-D)^2$ [20]. The active SLCN has two inductors, a capacitor and two diodes, and it has three terminals such as a, b and S_D. Here, S_D represents the drain terminal of the MOSFET. By replacing the inductors L_1 and L_2 by dedicated active SLCNs, a biquadratic high gain DC-DC converter which is shown in Fig. 2, is proposed with a voltage gain of $1/(1-D)^4$ in this paper. The converter can be extended to any number of stages by replacing the inductors by dedicated SLCNs as an n-stage converter to achieve a voltage gain of $1/(1-D)^{2n}$, as shown in Fig. 2(c). The n-stage converter requires $(4n-1)$ diodes, $2n$ inductors, $2n$ capacitors and a single semiconductor switch. One of the key features of the proposed n-stage SLCN-based DC-DC converter is the utilization of single switch irrespective of the number of stages of the converter. Compared to the aforementioned converters, the proposed bi-quadratic converter produces higher dc-voltage gain. Typically, it produces the voltage gain of 625 at $D = 80\%$.

II. PROPOSED BIQUADRATIC DC-DC CONVERTER

The circuit diagram of the proposed biquadratic high gain DC-DC converter is derived from Fig. 2(c) when $n = 2$. It consists of a switch SW, four inductors L_1, L_2, L_3 and L_4, four capacitors C_1, C_2, C_3 and C_0 and seven diodes. The energy present in the inductor L_1 is recycled in the capacitor C_1. The energy present in C_1 and L_2 is recycled in the capacitor C_2. Further, the energy present in L_3 is recycled in the capacitor C_3. Such a cascaded recycling process helps the proposed biquadratic DC-DC converter to achieve a high

DC-voltage gain. The operation of the biquadratic high gain DC-DC converter in continuous conduction mode (CCM) is discussed in the below section.

Mode 1: In this mode, the semiconductor switch SW is turned on at the instant t_0, and all the inductors are in the charging state. The inductor L_1 charges from the source voltage V_S. At the same time, L_2 charges with the source voltage V_S along with the capacitor voltage V_{C1}, where the input source and the capacitor C_1 are connected in series. This series connection causes a voltage of $V_S + V_{C1}$ across the inductor L_2. The inductor L_3 charges from the source voltage V_S and the capacitor voltage V_{C2}, i.e., $V_S + V_{C2}$. The inductor L_4 charges with a voltage of $V_S + V_{C2} + V_{C3}$. Here, the diodes D_1, D_3 and D_5 are in forward biased condition, and the remaining diodes are in reverse biased condition. The operation of the converter in mode 1 is depicted in Fig. 3. The current of the inductors increases with a positive slope, as shown in the analytical waveform Fig. 5. The voltage across the inductors are expressed as,

$$V_{L1} = V_S; \quad V_{L2} = V_S + V_{C1} \tag{1}$$
$$V_{L3} = V_S + V_{C2}; \quad V_{L4} = V_S + V_{C2} + V_{C3} \tag{2}$$

Mode 2: In this mode, the semiconductor switch SW is turned on from t_1 to T_s. The capacitor C_1 starts charging from stored energy of the inductor L_1 through the diode D_2. Similarly, the other capacitors C_2 and C_3 also start charging, as shown in Fig. 4. Along with the charging of these capacitors, the inductors L_1, L_2, L_3 and L_4 form a series path with the input source V_S, as shown in Fig. 4, and discharge power into the load side. Here, the diodes D_2, D_4, D_6 and D_7 are in forward biased condition, and the remaining diodes are in reverse biased condition. The current of the inductors decreases to a finite value with a negative slope, as shown in Fig. 5. The voltage across the inductors during this mode is:

$$V_{L1} = -V_{C1}; \quad V_{L2} = V_{C1} - V_{C2} \tag{3}$$
$$V_{L3} = -V_{C3}; \quad V_{L4} = V_S + V_{C2} + V_{C3} - V_0 \tag{4}$$

From (3-4), the voltage of the capacitors and the voltage gain during CCM mode are obtained as given in (5) and (6).

$$V_{C1} = \frac{V_S D}{1-D}; V_{C2} = \frac{V_S D\,(2-D)}{(1-D)^2}; V_{C3} = \frac{V_S D}{(1-D)^3} \tag{5}$$

$$G_{CCM} = \frac{V_0}{V_S} = \frac{1}{(1-D)^4} \tag{6}$$

By substituting $D = 80\%$ duty ratio in (6), the voltage gain is obtained as 625. Achieving such a high voltage gain using 16 components, including a single semiconductor switch is one of the merits of the proposed biquadratic converter.

III. DESIGN AND COMPONENTS SELECTION

The output power of 500 W is considered for the design, and the value of other parameters are given in Table 1.

i) Inductors selection: Using the expression of the current ripple Δi_L of the inductors, the inductance values and the

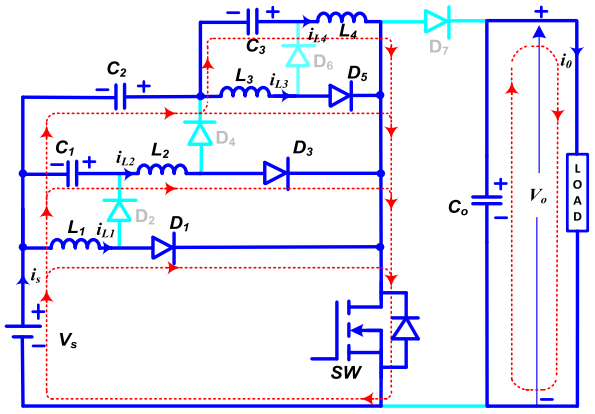

FIGURE 3. Operation of biquadratic converter in CCM mode 1.

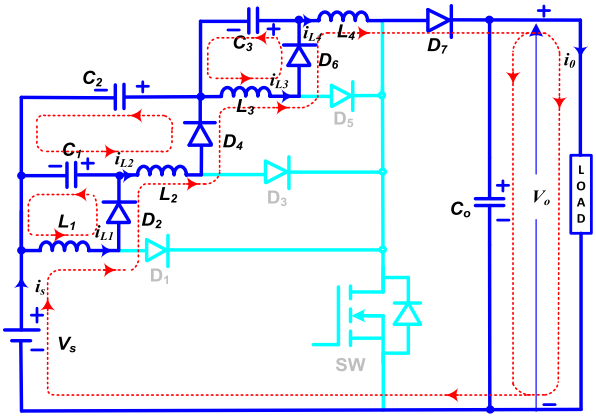

FIGURE 4. Operation of biquadratic converter in CCM mode 2.

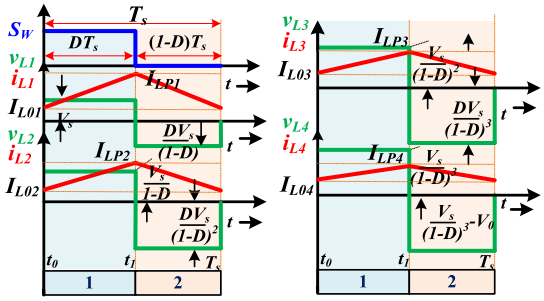

FIGURE 5. Analytical waveforms of biquadratic converter in CCM.

average current of the inductors are derived as,

$$L_1 \geq \frac{V_S D}{f_s \Delta i_{L1}} \; ; \; L_2 \geq \frac{V_S D}{f_s \Delta i_{L2}(1-D)} \tag{7}$$
$$L_3 \geq \frac{V_S D}{f_s \Delta i_{L3}(1-D)^2} \; ; \; L_4 \geq \frac{V_S D}{f_s \Delta i_{L4}(1-D)^3} \tag{8}$$

The average current through each inductor is expressed as,

$$I_{L1} = \frac{I_0}{(1-D)^4} \; ; I_{L2} = \frac{I_0}{(1-D)^3}; I_{L3} = \frac{I_0}{(1-D)^2};$$
$$I_{L4} = \frac{I_0}{1-D} \tag{9}$$

TABLE 1. Parameters of biquadratic converter.

Parameters	Value
Output power	500 W
Voltage V_S & V_0	48 V and 650 V
Swiching frequency f_S	50 kHz
Capacitors C_1, C_2, C_3 & C_0	100 µF, 47 µF, 22 µF & 22 µF,
Inductors L_1, L_2, L_3 & L_4	1 mH, 2 mH, 3 mH & 5 mH
Switch SW	C2M0040120D
Diodes D_1-D_6 & D_7	FFSH4065A & FFSH30120A

ii) Capacitors selection: The capacitors are charged in mode 2. Using the expression of energy stored in the capacitors, the final expressions of the capacitors are derived as,

$$\begin{cases} C_1 \geq \frac{V_0 D}{(1-D)^3 R_0 f_s \Delta V_{C1}}; C_2 \geq \frac{V_0 D}{(1-D)^3 R_0 f_s \Delta V_{C2}} \\ C_3 \geq \frac{V_0 D}{(1-D) R_0 f_s \Delta V_{C3}}; C_0 \geq \frac{V_0 D}{R_0 f_s \Delta V_{C0}} \end{cases} \tag{10}$$

where ΔV_C is the ripple voltage across the capacitor.

iii) Power switch and diodes selection: The appropriate switch and diodes are selected based on the converter specifications given in Table 1. The voltage and the current stresses of the switch and the diodes are given as,

$$\frac{V_{SW}}{V_S} = \frac{1}{(1-D)^4}; I_{SW} = \frac{\sqrt{D}\, I_0}{(1-D)^4}; \tag{11}$$

$$\frac{V_{D1}}{V_S} = \frac{-D}{(1-D)^2}; I_{D1} = \frac{\sqrt{D} I_0}{(1-D)^4}$$

$$\frac{V_{D2}}{V_S} = \frac{-1}{1-D}; I_{D2} = \frac{\sqrt{1-D} I_0}{(1-D)^4}; \tag{12}$$

$$\frac{V_{D3}}{V_S} = \frac{D(D-2)}{(1-D)^4}; I_{D3} = \frac{\sqrt{D} I_0}{(1-D)^3}$$

$$\frac{V_{D4}}{V_S} = \frac{-1}{(1-D)^2}; I_{D4} = \frac{\sqrt{1-D} I_0}{(1-D)^3}; \tag{13}$$

$$\frac{V_{D5}}{V_S} = \frac{-D}{(1-D)^4}; I_{D5} = \frac{\sqrt{D} I_0}{(1-D)^2}$$

$$\frac{V_{D6}}{V_S} = \frac{-1}{(1-D)^3}; I_{D6} = \frac{\sqrt{1-D} I_0}{(1-D)^2}; \tag{14}$$

$$\frac{V_{D7}}{V_S} = \frac{-1}{(1-D)^4}; I_{D7} = \frac{\sqrt{1-D} I_0}{1-D}$$

IV. EFFECT OF PARASITIC ELEMENTS ON CONVERTER PERFORMANCE

A detailed investigation is conducted to study the effect of the parasitic elements on the output voltage of the converter. The winding resistance of the inductor is denoted by R_L. The series equivalent resistance of the capacitor is denoted by R_C. The forward voltage drop and the internal resistance of the diode are expressed as V_{FD} and R_D, respectively. The input source resistance is expressed as R_S, and the on-state resistance of the switch is represented as R_{SW}. When the switch SW is turned on, the expressions of the voltage across the inductors are given in (15)-(18).

$$V_{L1} = V_S - i_{S,avg}R_S - i_{L1,avg}R_L - i_{D1,avg}R_D - V_{FD} - i_{SW,avg}R_{SW} \tag{15}$$

$$V_{L2} = V_S - i_{S,avg}R_S + V_{C1} - i_{L2,avg}R_L - V_{FD} - i_{D3,avg}R_D - i_{SW,avg}R_{SW} \tag{16}$$

$$V_{L3} = V_S - i_{S,avg}R_S + V_{C2} - i_{L3,avg}R_L - i_{D5,avg}R_D - V_{FD} - i_{SW,avg}R_{SW} \tag{17}$$

$$V_{L4} = V_S - i_{S,avg}R_S + V_{C2} + V_{C3} - i_{L4,avg}R_L - i_{SW,avg}R_{SW} \tag{18}$$

When the switch SW is turned off, the expressions of the voltage across the inductors are given in (19)-(22).

$$V_{L1} = -i_{L1,avg}R_L - i_{D2,avg}R_D - V_{FD} - V_{C1} \tag{19}$$

$$V_{L2} = V_{C1} - V_{C2} - V_{FD} - i_{L2,avg}R_L - i_{D4,avg}R_D \tag{20}$$

$$V_{L3} = -i_{L3,avg}R_L - i_{D6,avg}R_D - V_{FD} - V_{C3} \tag{21}$$

$$V_{L4} = V_S - i_{S,avg}R_S + V_{C2} + V_{C3} - i_{L4,avg}R_L - i_{D7,avg}R_D - V_{FD} - V_0 \tag{22}$$

By solving (15) – (22), the final expression of the output voltage with the parasitic elements is derived as,

$$V_0 = \frac{V_S + V_{FD}\left(-D^4 + 5D^3 - 9D^2 + 7D - 3\right)}{(1-D)^4 + a\frac{R_S}{R_0} + b\frac{R_D}{R_0} + c\frac{R_L}{R_0} + d\frac{R_{SW}}{R_0}} \tag{23}$$

where, a, b, c, and d, as shown at the bottom of the next page. Using (23), the variation of the output voltage with respect to the duty ratio D is drawn, as shown in Fig. 6 for (i) ideal (ii) $R_0 = 845\ \Omega$ and (iii) $R_0 = 2000\ \Omega$. Fig. 6 shows the output voltage of the biquadratic converter and the converters reported in [20], [25]. The output voltage is significantly affected by the parasitic elements. To reduce the effect of parasitic elements, the SiC-based semiconductor devices are used.

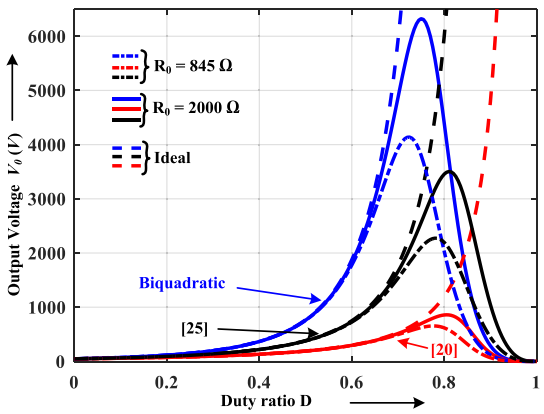

FIGURE 6. Output voltage with parasitic elements.

The total ohmic loss of the inductors, capacitors, diodes and switch is derived, respectively as given in (24).

$$P_L = \left[\sum_{i=1}^{4} I_{Li,RMS}^2\right] R_L P_C = \left[\sum_{i=0}^{3} I_{Ci,RMS}^2\right] R_C$$

$$P_{D,C} = \left[\sum_{i=1}^{7} I_{Di,RMS}^2 R_{Di}\right]$$
$$P_{SW,C} = I_{SW,RMS}^2 R_{SW} \tag{24}$$

The switching loss of the switches is expressed as,

$$P_{SW,SWI} = \frac{1}{2} V_{SW} I_{SW,avg} (t_{on} + t_{off}) f_s \tag{25}$$

where V_{SW} - the maximum voltage across the switch, I_{SW} - the maximum current flowing through the switch, t_{on} - the summation of rising time and turn-on delay time, and t_{off} - the summation of fall time and turn-off delay time. The diode conduction loss associated with the diodes is derived as in (26).

$$P_{D,VF} = \left[\sum_{i=1}^{7} I_{Di,avg} V_{FDi}\right] \tag{26}$$

Hence, the total power loss of the biquadratic converter is,

$$P_{loss} = P_L + P_C + P_{SW,C} + P_{SW,SWI} + P_{D,C} + P_{D,VF} \tag{27}$$

Using (24) to (27), the various losses of the biquadratic converter using i) SiC-based semiconductor devices and ii) Si-based semiconductor devices are calculated for the operating point of $V_0 = 650$ V, $V_s = 48$ V, $P_0 = 500$ W. Fig. 7 shows the losses of the biquadratic converter and the quadratic boost converter. The comparison shows that, the losses associated with the MOSFET and diodes are reduced approximately by more than two times in the case of SiC compared to the case of Si. The proposed bi-quadratic converter has seven diodes, and these diodes are realized using the SiC Schottky diodes of FFSH4065A & FFSH30120A. These seven diodes cause the loss of 8.7 W (conduction loss $P_{D,C}$ and loss due to forward voltage drop $P_{D,VF}$), as shown in Fig. 7. The losses of the diodes D_1 and D_2 are 2.56 W and 2.79 W, respectively and these losses are more compared to other diodes. Hence, the diodes D_1 and D_2 affect the efficiency compared to the other diodes. Compared to the quadratic converter which operates at $D = 73\%$, the operation of the biquadratic converter at $D = 48\%$, i.e., operation at lower duty ratio for $V_0 = 650$ V and $V_S = 48$ V reduces the switch loss significantly.

Fig. 8 shows the analytical and the experimental efficiency profiles of the biquadratic converter and the quadratic converter. The biquadratic converter produces the analytical efficiency of 95.48% at 500 W for $V_0 = 650$ V, $V_S = 48$ V. The analytical efficiency profiles of the biquadratic and the quadratic converters at $V_0 = 1000$ V and $V_S = 48$ V are also

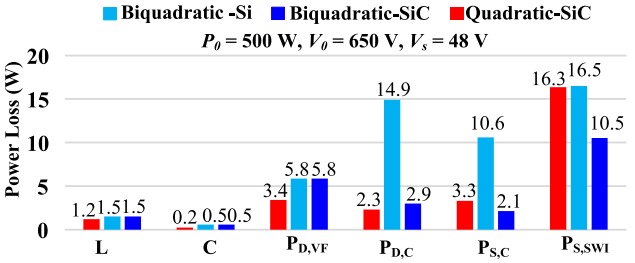

FIGURE 7. Loss breakdown analysis.

marked in Fig. 8. At this operating point, the quadratic boost converter produces significantly lower efficiency compared to the biquadratic converter.

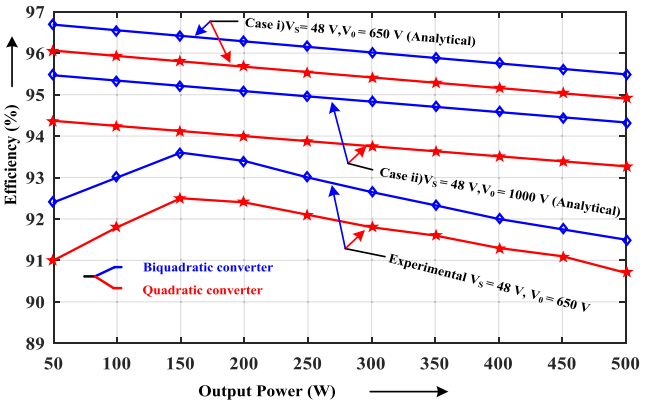

FIGURE 8. Output power versus efficiency.

V. SMALL-SIGNAL MODEL

Using the state-space averaging, the small-signal model of the biquadratic converter is developed. The on-state resistance and the forward voltage drop of semiconductor devices and the parasitic resistance of reactive elements are not considered in the circuit to reduce the calculation complexity. Instead, a loop resistance of r which exist in every loop is considered. The voltage across the inductors and the current through the capacitors for mode 1 are:

$$\begin{cases} v_{L1} = v_S - i_{L1} r;\ v_{L4} = v_S + v_{C2} + v_{C3} - i_{L4} r \\ v_{L2} = v_S + v_{C1} - i_{L2} r;\ v_{L3} = v_S + v_{C2} - i_{L3} r \\ i_{C1} = -i_{L2};\ i_{C2} = -i_{L3} - i_{L4};\ i_{C3} = -i_{L4};\ i_{C0} = -i_0 \end{cases} \tag{28}$$

Similarly, necessary equations for mode 2 are derived. Using those equations, the state-space average model is:

$$\dot{x} = A_{av} x + B_{av} u;\ y = C_{av} x \tag{29}$$

$$a = \frac{1}{(1-D)^4};\ d = \frac{-D^3 + 4D^2 - 5D + 3}{(1-D)^4};\quad c = \frac{(1-D)^6 + D^4 - 4D^3 + 7D^2 - 6D + 3}{(1-D)^4};$$
$$b = \frac{(1-D)^4 D^2 + (1-D)^2 (1 - D + D^2) - D(1-D)^4 + D^3 (1-D)^2 + D^3 - D^2 + D}{(1-D)^4}$$

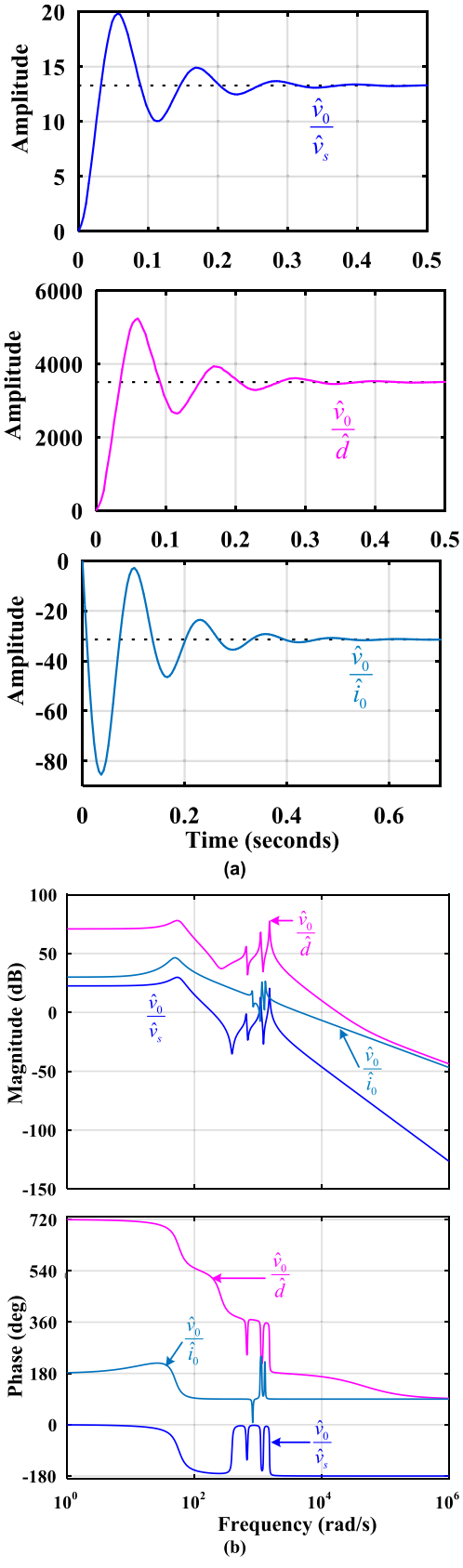

FIGURE 9. Dynamic response (a) step response (b) Bode plot.

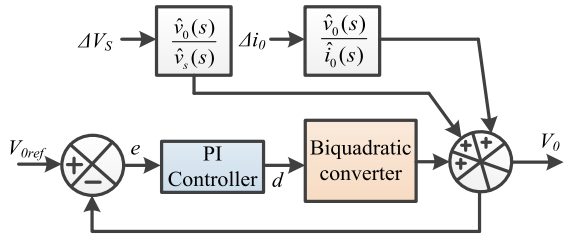

FIGURE 10. Closed loop system of biquadratic converter.

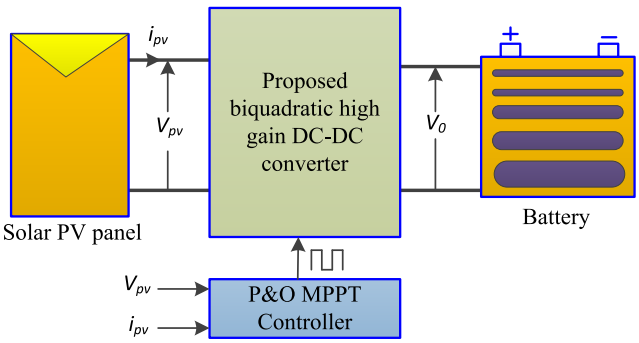

FIGURE 11. Biquadratic converter interfaced solar PV panel.

where $x = [i_{L1} i_{L2} i_{L3} i_{L4} v_{C1} v_{C2} v_{C3}\ v_{C0}]^T$, $u = [v_s i_0]$, $y = [v_0]$. By applying the AC perturbations on the above state-space average model, the final small-signal model of the biquadratic converter is obtained, as expressed in (30)-(31), as shown at the bottom of the page 8. Using the small-signal model, the transfer functions are derived as expressed in (32)-(34), as shown at the bottom of the page 8, for the specifications given in Table 1. The eight poles of the transfer function are located in the left-hand side of the s-plane. Hence, the proposed biquadratic converter is stable. The Bode plot and the step response of the transfer function are shown in Fig. 9. The step response of the biquadratic converter shows that response settle down with a finite gain.

The schematic diagram of the closed-loop system of the proposed biquadratic is shown in Fig. 10. A PI controller is designed to regulate the output voltage when there is a disturbance in the source side and load side. The proportional gain K_P and integral gain K_i are designed using Ziegler-Nichols method. The obtained values are $K_P = 0.015$ and $K_i = 1.42$. The designed controller has been successfully implemented in Xilinx System Generator (XSG). The implemented program is realised in the real time by using Zynq 7000 FPGA® module which operates at the 40 MHz clock period. Based on the feed-back output voltage, a protection scheme is developed to disable the control signal when the output voltage exceeds 750 V.

VI. BIQUADRATIC CONVERTER INTERFACED SOLAR PV PANEL

To assess the feasibility of the biquadratic converter in solar PV application, a simulation study has been conducted on the

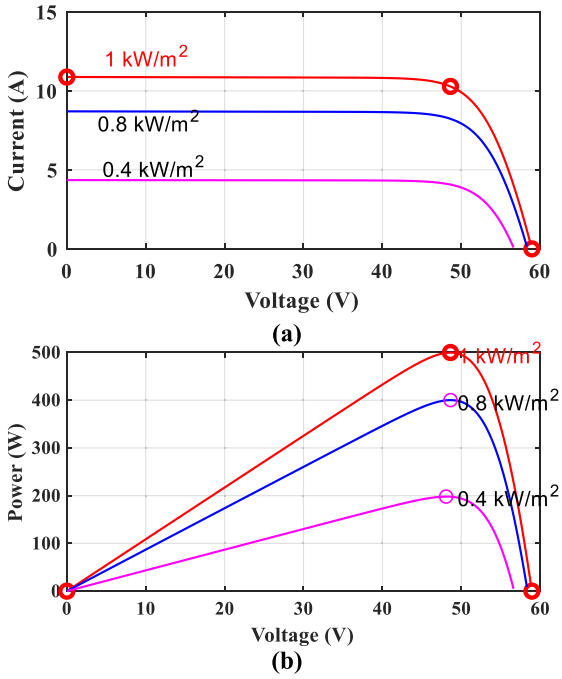

FIGURE 12. Characteristics of the solar panel (a) current versus voltage (b) power versus voltage.

biquadratic converter interfaced solar PV panel. The Perturb & Observe (P&O) algorithm [30] is used for tracking the maximum power from the solar PV panel. The block diagram of the biquadratic converter interfaced solar PV panel with MPPT controller is shown in Fig. 11.

The current *versus* voltage and power *versus* voltage characteristics of the solar panel of GSM 500-96 is shown in Fig. 12. The considered solar panel has the maximum power of 500 W with the open circuit voltage of 58.95 V and the short circuit current of 10.87 A. The panel produces the output voltage of closely 48.63 V at the maximum power point (MPP), as shown in Fig. 18(b). The simulation of the biquadratic converter interfaced solar PV panel has been conducted, and the simulation waveforms are shown in Fig. 19. The input solar radiation is varied from 1000 W/m^2 to various levels as given in Fig. 13(a). The V_{PV} and I_{PV} of the solar panel are sensed and given to the P&O algorithm. The control duty ratio given by the algorithm is given to the PWM unit, and the control pulse for the switch SW of the biquadratic converter is generated. The V_{PV} and I_{PV} of the solar panel observed from the simulation are shown in Fig. 19(b-c). When the input solar radiation is changed from 1000 W/m^2 to 800 W/m^2 at 0.5 sec, as shown in Fig. 13(a), the power produced by the solar PV is changed from 500 W to 400 W. The MPP corresponding to 800 W/m^2 solar radiation is shown in Fig. 12(b). The output power shown in Fig. 13(d) witnesses that the biquadratic converter tracks the MPP from the solar panel with help of the P&O algorithm for the variation in the solar radiation.

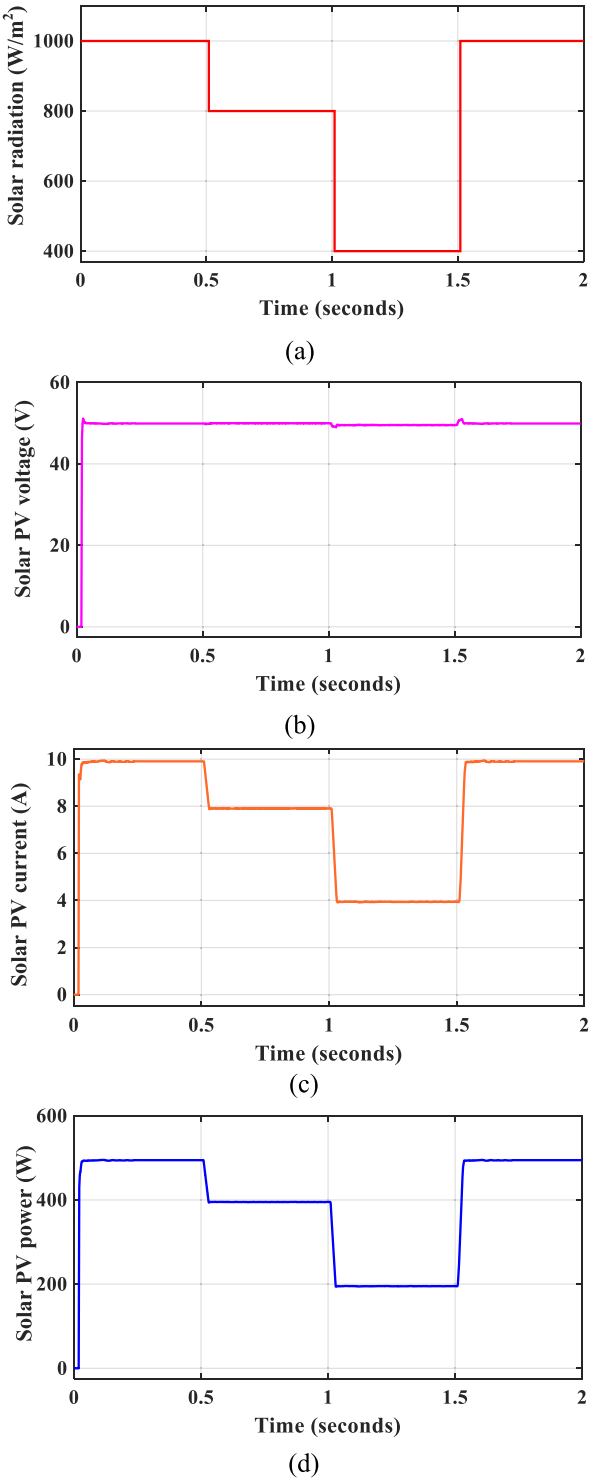

FIGURE 13. Simulation results of biquadratic converter with solar PV panel (a) Solar radiations (b) Solar PV panel voltage (c) Solar PV panel current (d) Solar PV panel power.

VII. EXPERIMENT RESULTS AND DISCUSSIONS

A 500 W laboratory prototype of the biquadratic converter is fabricated, as shown in Fig. 14. The components are selected

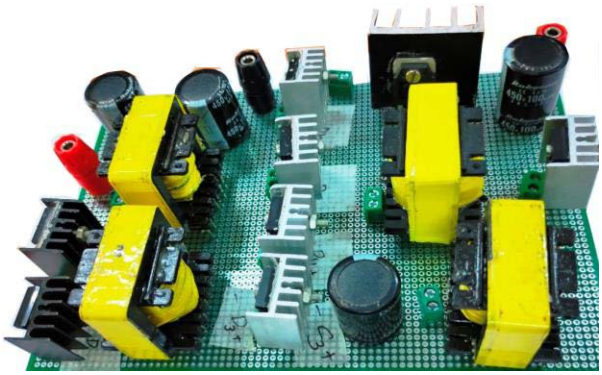

FIGURE 14. Experiment prototype of biquadratic converter.

according to the proper design as explained in section III. For the experimental validation, the switching frequency of 50 kHz is considered. The input voltage source is realized using a programmable voltage source of GWINSTEK, and it is set to 48 V. To generate the switching pulse of 48% duty ratio for the switch SW, Tektronix TPS 2024B pulse generator is used. Using Digital Storage Oscilloscope (DSO), the hardware results are captured under the steady-state in CCM, as shown in Fig. 15. Fig. 15(a) shows that the inductor L_1 is charged with a voltage V_S of 48 V, and it is discharged with a voltage of V_{C1} of 44 V. Fig. 15(b) shows the voltage and current waveforms of the L_2. The L_2 charges with a voltage ($V_{C1}+V_S$) of 92 V, and it discharges with a voltage (V_{C2}-V_{C1}) of 82 V. The voltage values of both the capacitors C_2 and C_3 become 126 V and 160 V, respectively. Fig. 15(c) shows the voltage and current waveforms of the L_3. The experimental waveforms of each inductor closely match with the analytical waveforms, which are shown in Fig. 5. Fig. 15(d) shows the voltage waveforms captured from the inductor L_4 and the capacitor C_3. The waveforms confirm that the inductor L_4 charges with a voltage of 340 V, and it discharges with 291 V. The capacitor C_3 holds energy with a voltage of 160 V. Fig. 15(e) presents the voltage and current waveforms of the input source and the load. Although the input current has higher ripple content, the ripple can be reduced by changing the connection of the negative terminal of the capacitor C_1 to the source negative terminal. However, the voltage stress of the capacitors C_1, C_2 and C_3 will be increased. The experiment on the biquadratic converter has been done in the closed-

$$\hat{v}_0 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} & \hat{i}_{L2} & \hat{i}_{L3} & \hat{i}_{L4} & \hat{v}_{C1} & \hat{v}_{C2} & \hat{v}_{C3} & \hat{v}_{C0} \end{bmatrix}^T \tag{30}$$

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{i}_{L3} \\ \dot{i}_{L4} \\ \dot{v}_{C1} \\ \dot{v}_{C2} \\ \dot{v}_{C3} \\ \dot{v}_{C0} \end{bmatrix} = \begin{bmatrix} -\frac{r}{L_1} & 0 & 0 & 0 & \frac{D-1}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{r}{L_2} & 0 & 0 & \frac{1}{L_2} & \frac{D-1}{L_2} & 0 & 0 \\ 0 & 0 & -\frac{r}{L_3} & 0 & 0 & \frac{D}{L_3} & \frac{D-1}{L_3} & 0 \\ 0 & 0 & 0 & -\frac{r}{L_4} & 0 & \frac{1}{L_4} & \frac{1}{L_4} & \frac{D-1}{L_4} \\ \frac{1-D}{C} & -\frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1-D}{C} & -\frac{D}{C} & -\frac{1}{C} & 0 & 0 & 0 \\ 0 & 0 & \frac{1-D}{C} & -\frac{1}{C} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1-D}{C} & 0 & 0 & 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{L3} \\ \hat{i}_{L4} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \\ \hat{v}_{C3} \\ \hat{v}_{C0} \end{bmatrix} + \begin{bmatrix} \frac{D}{L_1} \\ \frac{D}{L_2} \\ \frac{D}{L_3} \\ \frac{1}{L_4} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_s$$
$$+ \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_3} & \frac{1}{L_3} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_4} \\ -\frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C} & -\frac{1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ I_{L4} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C0} \end{bmatrix} \hat{d} \tag{31}$$

$$\frac{\hat{v}_0}{\hat{v}_s} = \frac{4.7 \times 10^5 (s^2 + 20s + 1.5 \times 10^5)(s^2 + 20s + 4.73 \times 10^5)(s^2 + 20s + 1.5 \times 10^6)}{(s^2 + 24.6s + 3213)(s^2 + 20s + 4.2 \times 10^5)(s^2 + 20.2s + 1.2 \times 10^6)(s^2 + 20.5s + 2.3 \times 10^6)} \tag{32}$$

$$\frac{\hat{v}_0}{\hat{i}_0} = \frac{-4545.5(s + 20)(s^2 + 20s + 6.9 \times 10^5)(s^2 + 20s + 1.1 \times 10^6)(s^2 + 20s + 1.6 \times 10^6)}{((s^2 + 24.6s + 3213)(s^2 + 20s + 4.2 \times 10^5)(s^2 + 20.2s + 1.2 \times 10^6)(s^2 + 20.5s + 2.3 \times 10^6)} \tag{33}$$

$$\frac{\hat{v}_0}{\hat{d}} = \frac{-6466.3(s - 4.65 \times 10^4)(s^2 - 98.4s + 6.5 \times 10^4)(s^2 + 14.1s + 4.7 \times 10^5)(s^2 + 30.8s + 1.4 \times 10^6)}{(s^2 + 24.6s + 3213)(s^2 + 20s + 4.2 \times 10^5)(s^2 + 20.2s + 1.2 \times 10^6)(s^2 + 20.5s + 2.3 \times 10^6)} \tag{34}$$

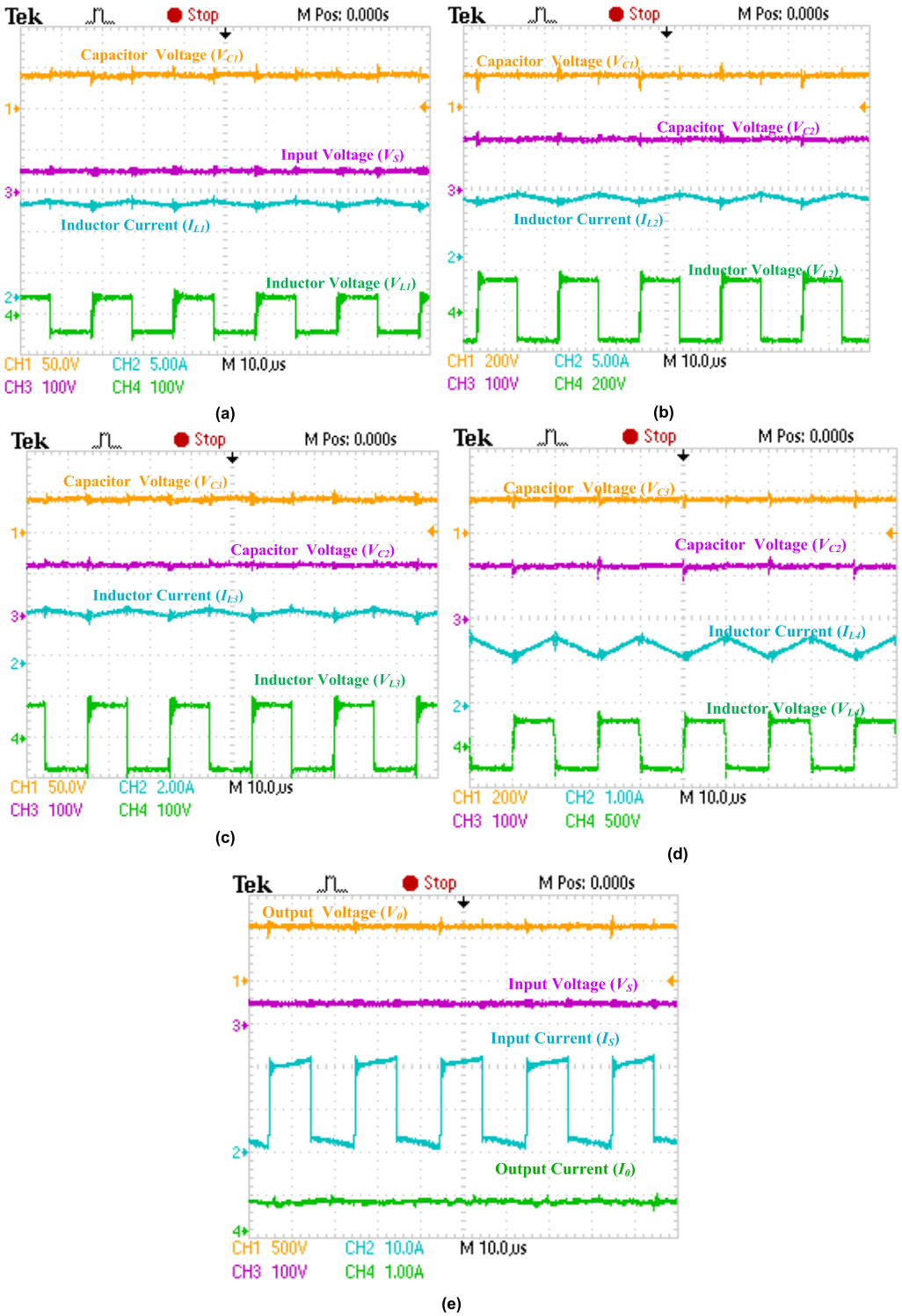

FIGURE 15. Experimental results (a) V_S, I_{L1}, V_{L1}, V_{C1} (b) V_{C2}, I_{L2}, V_{L2}, V_{C1} (c) V_{C2}, I_{L3}, V_{L3}, V_{C3} (d) V_{C2}, I_{L4}, V_{L4}, V_{C3} (e) V_S, I_S, V_0, I_0.

loop condition. The output voltage across the load is fed into the Zynq controller, and the control signal derived from the controller is given to the gate driver. The dynamic response of the biquadratic converter for the step-change in the input voltage and the output load is observed, and the experimental results are presented in Fig. 16. Fig. 16(a) shows the response of the converter when load current is changed from 0.15 A to 0.46 A by keeping the V_S constant. The output waveforms

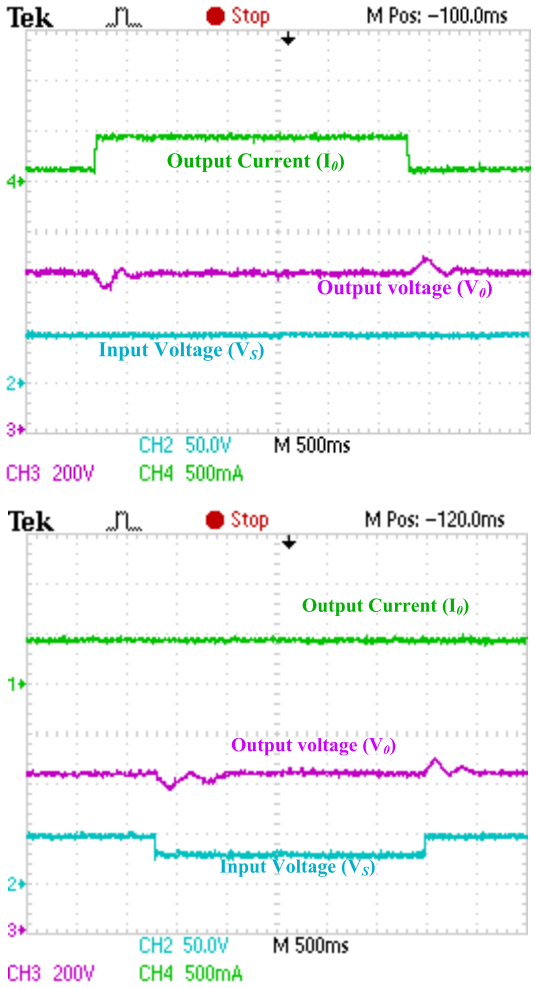

FIGURE 16. Closed loop results (a) load change (b) input voltage change.

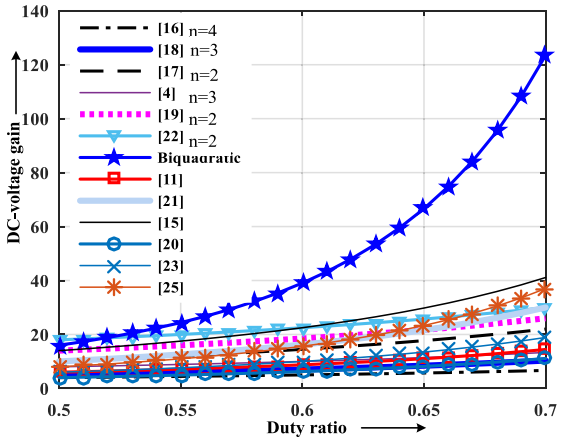

FIGURE 17. Voltage gain comparison of biquadratic converter.

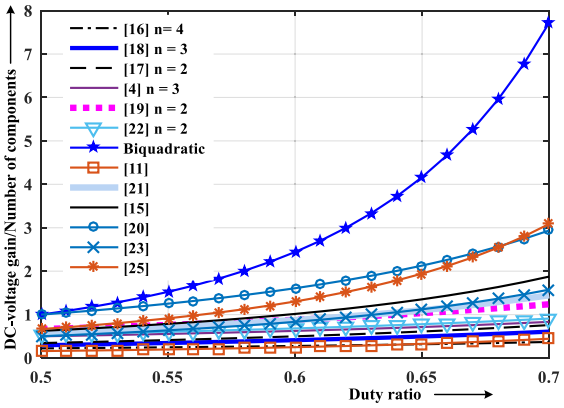

FIGURE 18. Comparison in terms of voltage gain/number of components.

confirm that the controller regulates the V_0 at 650 V. Similarly, the response of the converter for the step change in source is also shown in Fig. 16(b). Here, the input voltage is changed from 48 V to 30 V.

VIII. PERFORMANCE COMPARISON

The performance of the proposed biquadratic converter is compared with the similar recent reported topologies, as given in Table 2. The comparison of dc-voltage gain in terms of duty ratio for the biquadratic converter with the conventional converters (given in Table 2) is shown in Fig. 17. This plot shows that the proposed biquadratic converter produces more dc-voltage gain compared to other dc-dc converters. Although [22] with $n = 2$ produces slightly better dc-voltage gain, as shown in Fig. 14 for D $\leq$ 0.52, it uses 33 components including 4 semiconductor switches. Compared to some of the existing converters [4], [15]–[18], [21] and [22], the proposed SLCN-based converter requires only one semiconductor switch. Also, the comparison of the biquadratic converter in terms of dc-voltage gain/number of components is shown in Fig.18. As given in Table 2, though the number of components of [4] with $n = 3$, [15], [16] with $n = 4$, [18] with $n = 3$, [21] and biquadratic converter is close to each other, the biquadratic converter has more voltage gain/number of components, as shown in Fig. 18.

The maximum potential of the proposed biquadratic converter shall be extracted when the converter is operated at a higher output voltage. The proposed bi-quadratic converter achieves the output voltage 1000 V from 48 V at $D = 53.2\%$ with help of a single semiconductor switch. Whereas, the other converters achieve the same output voltage at the higher duty ratio, as given in Table 2. However, [22] achieves this output voltage at $D = 47.2\%$. But, it uses 33 components. The comparison of switch stress for various converters is given in Table 2. Fig. 19(a) shows the comparison of switch voltage and current stress of the high gain converters which use a single switch. Although the switches present in [11] with $n = 2$ and [23] have lower voltage stress of 806 V and 612 V respectively, to produce $V_0 = 1000$ V; they have more current stress of 10.26 A and 14.07 A, respectively. When the biquadratic converter is operated at lower duty ratio, i.e., at $D = 53.2\%$, the current stress is significantly reduced (i.e., 5.54 A) compared to the other converters. Accordingly, the switching loss is also reduced, and the volume of the

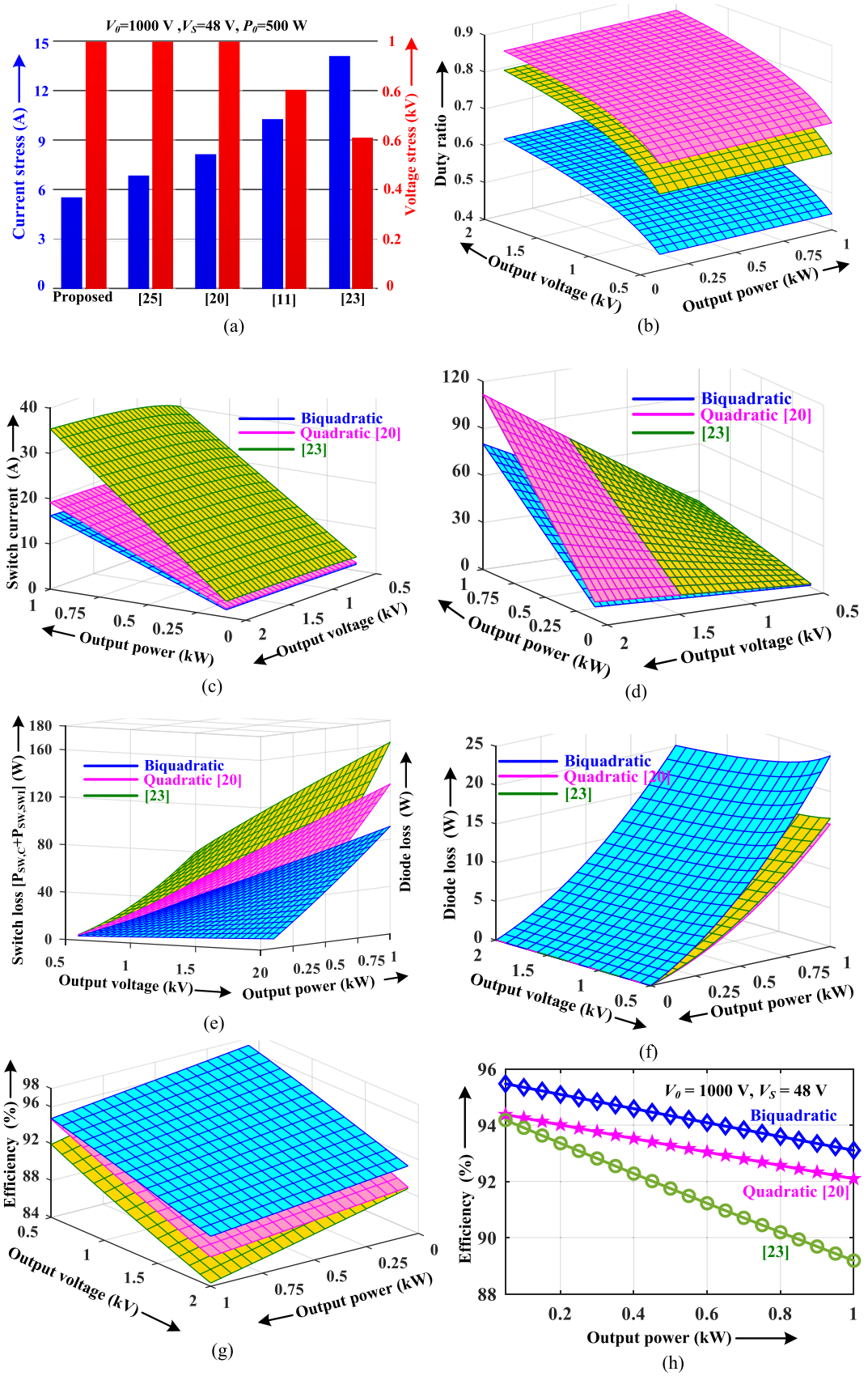

FIGURE 19. Performance comparison (a) switch stress (b) duty ratio *Versus* P_0 and V_0 (c) Switch current *Versus* P_0 and V_0 (d) Switching loss *Versus* P_0 and V_0 (e) Switch loss *Versus* P_0 and V_0 (f) Diode loss *Versus* P_0 and V_0 (g) %η *Versus* P_0 and V_0 (h) %η *Versus* P_0 at V_0 = 1000 V and V_S = 48 V.

TABLE 2. Performance comparison.

Topology	Switch	Diode	Capacitor	Inductor	Total count	Voltage gain	%D for V_0=1000V V_S=48 V	Source current	V_{SW}/V_0	I_{SW}/I_0	V_{Dmax}/V_0
[16]	n+2m	n	n+m+1	2	3(n+m+1)	$\frac{n}{1-D}$	80.8	Cont.	$\frac{1}{n}$	$\frac{2n}{1-D}$	$\frac{1}{n}$
[18]	n+2	2n	1	n+2	4n+5	$\frac{1+(n+1)D}{1-D}$	80	Cont.	$\frac{2+n}{(n+1)D+1}$	$\frac{2+(n+1)2D}{1-D}$	$\frac{2+nD}{(n+1)D+1}$
[17]	n+2	5n+6	1	2n+4	8n+13	$\frac{1+(2n+3)D}{1-D}$	71.4	Cont.	$\frac{1+D}{(2n+3)D+1}$	$\frac{4}{1-D}$	$\frac{2+2D(1+n)}{(n+1)D+1}$
[4]	m	mn	mn	m	2m(1+n)	$\frac{mn}{1-D}$	71.2	Cont.	$\frac{1}{mn}$	$\frac{n}{1-D}$	$\frac{2}{mn}$
[19]	1	4+2(m+n)	n+2m+2	n+2	9+4(m+n)	$(n(D+m+1)+2D+m)/(1-D)$	63.8	Discont.	$\frac{3}{5+4D}$	$D[n(D+m+1)+2D+m]/(1-D)$	$\frac{n}{5+4D}$
[22]	4	4n+4	4n+5	4	8n+17	$\frac{4n+3}{1-D}$	47.2	Cont.	$\frac{2}{4n+3}$	$\frac{2n}{1-D}$	$\frac{4}{4n+3}$
SLCN *n*-stage	**1**	**4*n*-1**	**2*n***	**2*n***	**8*n***	$\frac{1}{(1-D)^{2n}}$	**53.2**	**Cont.**	**1**	$\frac{D}{(1-D)^{2n}}$	**1**
Biqua		**7**	**4**	**4**	**16**	$\frac{1}{(1-D)^4}$				$\frac{D}{(1-D)^4}$	
[20]	1	3	2	2	8	$\frac{1}{(1-D)^2}$	78.1	Cont.	1	$\frac{D}{(1-D)^2}$	1
[23]	1	4	4	3	12	$\frac{1+D}{(1-D)^2}$	71.4	Cont.	$\frac{1}{1+D}$	$(2D+D^2+D^3)/(1-D)^2$	$\frac{1}{1+D}$
[25]	1	5	3	3	12	$\frac{1}{(1-D)^3}$	63.7	Cont.	1	$\frac{D}{(1-D)^3}$	1
[14]	2	4	4	2	12	$\frac{3-2D}{(1-D)^2}$	73	Cont.	$\frac{1}{3-2D}$	$\frac{1+2D-2D^2}{(1-D)^2}$	$\frac{2-D}{3-2D}$
[11]	1	4	3	2	10	$\frac{2-D}{(1-D)^2}$	75.6	Cont.	$\frac{1}{2-D}$	$\frac{1+D-D^2}{(1-D)^2}$	$\frac{1}{2-D}$
[21]	2	5	6	3	16	$\frac{2+D}{(1-D)^2}$	64.4	Cont.	$\frac{1}{2+D}$	$\frac{2-D-D^2}{(1-D)^2}$	$\frac{1}{2+D}$
[15]	2	5	5	2	14	$\frac{3+D}{(1-D)^2}$	58.6	Cont.	$\frac{1+D}{3+D}$	$(1+3D-D^2-D^3)/D(1-D)^2$	$\frac{2}{3+D}$
[27]	2	5	4	3	14	$\frac{5+D}{1-D}$	72.5	Cont.	$\frac{2}{5+D}$	$\frac{3+D}{1-D}$	$\frac{3}{5+D}$
[28]	2	4	5	3	14	$\frac{3-3D-2D^2}{(1-D)(1-2D)}$	44.5	Cont.	$\frac{1-D}{3-3D-2D^2}$	$\frac{1+D}{1-4D}$	$\frac{3D-2}{3-3D-2D^2}$
[29]	2	5	3	4	14	$\frac{3+D}{1-D}$	82	Cont.	$\frac{2}{3+D}$	$\frac{1+D}{1-D}$	$\frac{1}{3+D}$

heat sink for the switch can be minimized. Compared to the biquadratic converter, the converters [17] with $n = 2$, [19] with $n = 2$ and [22] with $n = 2$ use more diodes, i.e., 16, 10 and 12, respectively. Whereas, the other converters use six or lesser number of diodes. The voltage stress of the diodes D_1-D_3 of the quadratic converter [20] is exactly equal to the voltage stress expressions of D_3-D_5 of [25]. Similarly, the voltage stress expressions of D_3-D_7 of the biquadratic converter is exactly equal to D_1-D_5 of [25]. However, the voltage stress of D_1 and D_2 of the biquadratic converter and [25] is lesser compared to their respective diode D_3, as given in Table 2. An extensive analysis has been conducted to assess the performance for the biquadratic converter with respect to the output voltage and load power for the region 0.5 kV $\leq V_0 \leq$ 2 kV and $0 \leq P_0 \leq$ 1 kW. Fig. 19(b) indicates that thebiquadratic converter is operated at the lower duty ratio region in the considered output voltage and power regions compared to [20] and [23]. Hence, the switch current of the biquadratic converter is lesser compared to [20] and [23], as shown in Fig. 19(c). Although [23] has lesser voltage stress, the switching loss of the biquadratic converter is lower because of the lower current stress, as shown in Fig. 19(d). The switch loss comparison shown in Fig. 19(e) indicates that the switch loss is very low for the biquadratic converter. The 7 diodes of the biquadratic converter lead higher diode loss compared to [20] and [23], as shown in Fig. 19(f). The *%η Versus* P_0 and V_0 shown in Fig. 19(g) indicates that the biquadratic converter gives better efficiency in the high voltage region compared to [20] and [23]. The analytical efficiency profiles of the above three converters at $V_0 = 1000$ V and $V_S = 48$ V are shown in Fig. 16(h). The extensive analysis proves that the biquadratic converter gives

a better performance in the high voltage region compared to the conventional converters. The operation of the converter at lower duty ratio, lower current stress, continuous source current, improved efficiency, the requirement of a single control signal and a single driver circuit are the attractional features of the proposed biquadratic converter.

IX. CONCLUSION

The structure formulation of an active SLCN-based high gain DC-DC converter with n-stage was proposed. From the n-stage structure, the biquadratic converter was derived for $n = 2$, and its operation was discussed in the CCM. The design of various components of the biquadratic converter was carried out. The effect of parasitic elements of the components of the biquadratic converter was investigated, and an attempt was made to reduce the parasitic effect using SiC-based semiconductor devices. The utilization of the SiC devices enhances the overall efficiency of the converter to 95.48% at 500 W output power. The experimental waveforms of the laboratory prototype of the converter for $P_0 = 500$ W, $f_s = 50$ kHz and $V_S = 48$ V were observed by considering $V_0 = 650$ V. The small-signal model of the biquadratic converter was developed, and the transfer functions were derived. A PI controller was designed, and the designed controller was implemented in XSG. The dynamic response of the converter was observed for the closed loop system. Simulation results of the bi-quadratic converter interfaced solar PV panel with P&O algorithm were presented to assess the feasibility of the proposed converter in solar PV application. The performance comparison of the proposed n-stage SLCN-based converter with the similar recently reported topologies shows that the operation of the converter at lower duty ratio, lower current stress, improved efficiency, the requirement of a single control signal and a single driver circuit are the attractional features of the proposed bi-quadratic converter. Hence, the biquadratic converter is a suitable candidature for the applications such as integration of solar PV and fuel cell, high voltage test equipment, medical X-ray, electrostatic precipitation, high-energy physics, telecommunication equipment, medium/high voltage wind farms, etc.

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