IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received May 18, 2022, accepted June 8, 2022, date of publication June 13, 2022, date of current version June 22, 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3182695

Performance Analysis of Resonant-Fin Transistors and Their Application in RF-Circuit Design

RICHARD HUDECZEK[1,2], EHRENTRAUD HAGER[3,4], (Graduate Student Member, IEEE), PETER BAUMGARTNER[2], (Member, IEEE), AND HARALD PRETL[4], (Senior Member, IEEE)

[1]Department of Electrical Engineering and Information Technology, Technical University of Munich, 80333 Munich, Germany
[2]Intel, 85579 Neubiberg, Germany
[3]Christian Doppler Laboratory for Digitally Assisted RF Transceivers for Future Mobile Communications, Johannes Kepler University (JKU) Linz, 4040 Linz, Austria
[4]Institute for Integrated Circuits, Johannes Kepler University (JKU) Linz, 4040 Linz, Austria

Corresponding authors: Richard Hudeczek (richard.hudeczek@intel.com) and Ehrentraud Hager (ehrentraud.hager@jku.at)

This work was supported in part by the Austrian Federal Ministry for Digital and Economic Affairs; in part by the National Foundation for Research, Technology and Development; and in part by the Christian Doppler Research Association.

ABSTRACT Emerging new communication standards like 5G or 6G aggravate the circuit design of radio-frequency generation systems as they constantly increase demand on high bandwidths, low latency, and high spectral purity. The utilization of high-Q oscillators, however, provides a possibility of optimisation of radio-frequency oscillators regarding their phase-noise performance in the overall system. This paper analyses one of the most promising electromechanical resonator devices, the resonant fin transistor with respect to its performance and application in oscillator circuit design. Several investigations regarding its working principle, design trade-offs and limits are carried out in this work. An oscillator circuit design is given for two variants of the resonant fin transistor device together with an outlook on its performance compared to other state-of-the-art radio-frequency oscillator designs. Following the performance analyses conducted throughout this work, the fundamental limit for the Q-factor of this resonator is investigated, challenging the validity of functionality of the resonant fin transistor and its potential for circuit applications.

INDEX TERMS Circuit simulation, finite element analysis, FinFET, oscillator, resonator, high$Q$-factor, resonant-fin oscillator, RFO, resonant-fin transistor, RFT.

I. INTRODUCTION

With the emerging market of 6G, radar, applications for car-to-car communication, internet of things and industry 4.0 the need for higher spectral purity signal generation is rising [1]–[3]. Stable Radio Frequency (RF)-signals with the lowest phase-noise possible are key to these new communication standards to enable high-order modulation schemes and thus high data transfer rates. The most important circuit component in these RF systems with regard to its phase-noise performance is the oscillator. As a frequency generation building block, the oscillator directly impacts and shapes the phase-noise of the complete RF system. One possibility to optimize the oscillator circuit with respect to the lowest phase-noise is the utilization of high quality-factor (Q-factor) resonators [4]. However, those high Q-factors can hardly be attained by current complementary metal-oxide-semiconductor (CMOS) process compatible devices, like conventional LC-based structures, which suffer from severe cross-coupling and large device footprints. To fill in the gap, modern micro-electro-mechanical-systems (MEMS) devices like surface-acoustic-wave (SAW)- and bulk-acoustic-wave (BAW)-resonators offer large Q-factors at high frequencies [5]–[10]. Nevertheless, integration of these devices often requires extensive pre- or post-processing, which forces the devices to be fabricated externally on a stand-alone die, increasing cost and limiting performance [11]. One recent device, the so-called resonant fin transistor (RFT)—schematically depict in Fig. 1—gathered much attention as it can be fabricated monolithically in the Front-End-of-Line (FEOL) of the CMOS stack with no additional post-processing required [12]. This is especially beneficial in mobile communication scenarios, where device power and area consumption matter. Moreover, the device promises excellent performance, with a Q-factor of 49 000 while resonating at 32 GHz.

The associate editor coordinating the review of this manuscript and approving it for publication was Teerachot Siriburanon.

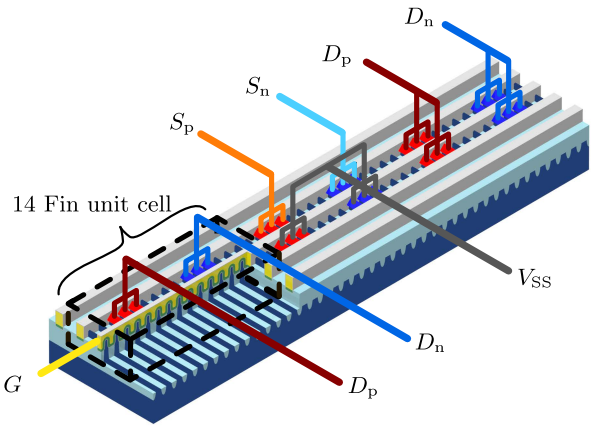


FIGURE 1. RFT device for an exemplary configuration of two differential drive cells–formed by a 14-fin unit cell–with positive and negative electrical drive connections D_p and D_n and one differential sense cell with the positive and negative electrical connections S_p and S_n as well as a ground connection V_{SS}. The gate is electrically connected via port G.

It utilizes the periodic arrangement of hundreds of adjoining fin field-effect transistorss (FinFETs) connected as metal-oxide-semiconductor (MOS) capacitors to create a mechanical wave inside a common gate via electromechanical coupling. The wave is picked up in the centre of the cavity as the change in FinFET current, which is caused by a modulation of the carrier mobility through the resonant mode. Several research efforts have been reported in order to take advantage of the performance of this device in an oscillatory circuit [13], [14]. This paper will carry out a more detailed theoretical evaluation of the working principle, performance and its limitations. Thus, we will give an estimate on the device's significance in RF circuit design for mobile communications and alike.

At first, the working principle of the RFT is outlined in Section II. It is followed by the geometrical explanation of the Finite-Element-Method (FEM) setups for the simulations in Section III. The mechanical anisotropy of the silicon wafer in CMOS technologies is discussed in Section IV, along with the investigated wafer orientations. After the mechanical prerequisites, the electromechanical simulation of the drive is explained in Section V. Afterwards, starting with the stress tensor and the derived pressure inside the sense FinFETs the sensing mechanism is explained in Section VI. Lastly, the FEM setups are calibrated with respect to their CMOS capacitance to measured quantities in Section VII and the Q-factor for the FEM simulation is introduced in Section VIII. Section IX presents simulation results of the conducted FEM simulation. Several impacts on the RFT performance by geometry, biasing, temperature and doping are investigated, resulting in a three orders of magnitude lower transconductance than initially reported. Despite these discrepancies, in Section X of the paper, a study on oscillator circuit design, utilizing the RFT device for frequency generation, is carried out. Furthermore, a comparison in performance to state-of-the-art oscillator designs is given to evaluate the significance of the resonator for high-performance RF circuit design. Finally, the paper concludes with caveats and possible improvements of the FEOL resonator in Section XI. Following from insufficient performance of the resonant fin transistor found in this work, and the fundamental Q-factor limit, imposed by the Achiever effect and Landau-Roomer regime, the validity of the functionality in prior literature of the resonant fin transistor is challenged.

II. FinFET RFT MEMS WORKING PRINCIPLE

To verify the performance of the RFT and its possible application in circuits, for example as resonant fin oscillator (RFO), three-dimensional FEM simulations were carried out with a commercially available simulator[1]. The working principle of the RFT is based on MOS capacitor actuation, which couples to a mechanical eigenmode inside a FinFET gate with hundreds of adjacent fins [12]. The best electromechanical coupling can be achieved by driving neighbouring fins with opposite phases, thus directly coupling to the differential eigenmode of the RFT. However, common foundry design rules prevent separated contacts to adjoining fins, therefore a higher spatial harmonic of the mode is driven. This is achieved by connecting groups of three neighbouring FinFET MOS capacitors, while four intermediate fins between the electrical phases are unconnected, thereby forming a 14-fin unit cells (UC). The mode is sensed in the centre of the cavity by a differentially wired FinFET pair, biased at a constant voltage. The mechanical deformation of the FinFETs causes a modulation of the carrier mobility and consequently a modulation of the drain current in the sense transistor pair at the frequency of the eigenmode [12], [14].

III. MECHANICAL SIMULATION SETUPS

To study the feasibility of the RFT concept, three different simulation setups are considered. The first, shown in Fig. 2b, models the smallest differential UC, with two adjacent fins. The structure is assumed infinite along the channel direction (X-axis) by utilizing symmetric boundary conditions. This creates a device with an infinite number of parallel fingers. However, this simplification suppresses out-of-plane movements of the gate. Nevertheless, it is still valid, even in the presence of anisotropic materials, as the impact of this assumption on the mechanical performance is negligible, which is studied in more detail in Section IX-A. Floquet-Bloch boundary conditions are deployed along the gate direction (Y-axis), which creates an infinite periodic cavity. The vertical directions (Z-axis) are terminated by perfectly matched layers in order to mimic a thick wafer without reflections in the far distance. As noted before, this configuration cannot be manufactured due to common design rule constraints. They prevent different electric contacts to adjacent fins without shorting. Thus, a larger 14-fin UC is required to be compliant with the design rule constraints, as depicted in Fig. 2c [12]. Fin packs of three, made from fins 3–5 or 10–12,

[1]COMSOL Multiphysics® v. 5.5. www.comsol.com

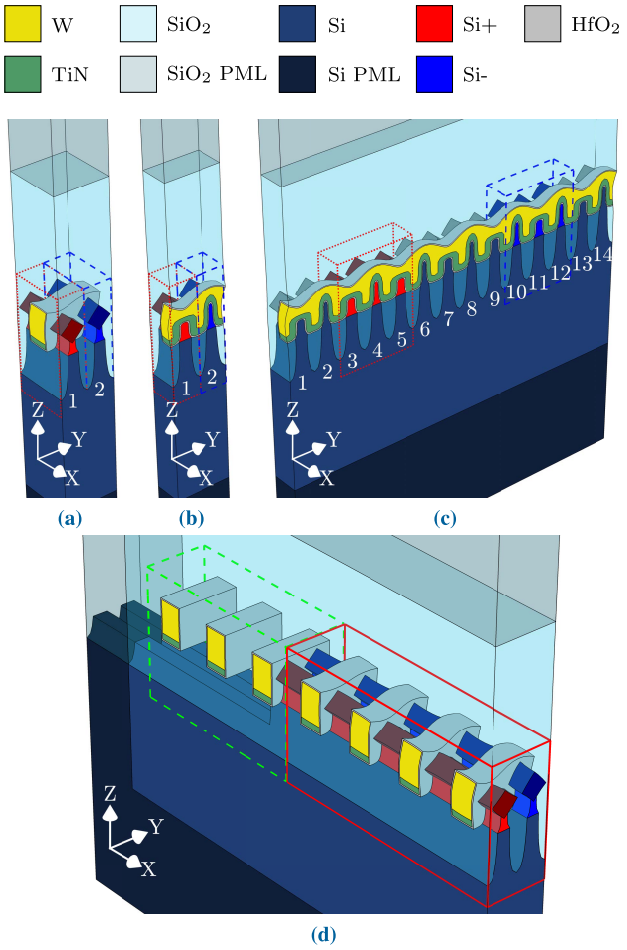


FIGURE 2. Finite Element Method Unit Cells (a) to (d). Electrically active fins are coloured in red and blue. Dummy and real fingers in (d) are marked by a dashed green and a solid red box. The deformation indicates the displacement in resonance and is not to scale.

are jointly connected to the same electric potential with both phases separated by four electrically floating fins.

The two electric phases are indicated by the red coloured fins and dotted box and the blue coloured ones with a dashed box, as depicted in Fig. 2b and Fig. 2c, respectively. To also quantify the impact of a finite amount of fingers and dummy fingers, a third simulation setup, shown in Fig. 2d, is used. The UC is based on the smallest 2-fin UC, however, it is now finite along the channel direction. Therefore, a certain number of active and dummy fingers can be modelled. The latter are required to control the electrical performance by creating an even surrounding for the active gates. The impact of a finite cavity on the final result is not studied in this work. The performance is expected to degrade with a shorter cavity length and badly matched termination, but further investigation is required to prove these expectations. Typical modern Back-End-of-Line (BEOL) stacks for integrated circuits (ICs) consist of a low-κ dielectric such as SiCO:H, with copper for wiring. Copper, which is a highly anisotropic material, strongly affects the acoustic band gap formation in the phononic crystal (PC) as the compliance changes for different

TABLE 1. Anisotropy factor A, elastic constants c_{11}, c_{12} and c_{44} and density ρ for some CMOS materials.

Material		A	c_{11} GPa	c_{12} GPa	c_{44} GPa	ρ kg m^{-3}
Cu	[19]	3.2	168.0	121.0	75.0	8960
Si	[18], [22]	1.6	165.7	63.9	79.6	2330
SiCO:H	[23]	1.0	6.6	2.5	2.1	1100
SiO_2	[24], [25]	1.0	78.5	16.0	31.2	2200
W	[19], [26]	1.0	501.0	198.0	151.0	19 280
HfO_2	[23], [25]	1.0	278.0	156.9	61.0	9800
TiN	[23]	1.0	227.5	97.5	65.0	4300

crystallographic orientations [15], [16]. To reduce complexity the BEOL is neglected in this study as it may vary strongly between different foundries and technology nodes. Thus, the BEOL is replaced by an SiO_2 slab in all simulations. Both the silicon wafer as well as the SiO_2 slab are able to confine the resonant mode due to index guiding for frequencies well in excess of the resonant mode's frequency [12], [17]. The higher porosity SiCO:H cannot be used for confinement as the index guiding properties are not sufficient. Hence, for modern SiCO:H based BEOL stacks a PC mirror is obligatory, but further investigation is required.

IV. WAFER ORIENTATIONS

The FEOL was modelled to reasonable 16 nm technology node dimensions and assumed identical for n-channel metal-oxide-semiconductor (NMOS) and p-channel metal-oxide-semiconductor (PMOS) devices. Several of the involved cubic materials exhibit anisotropic mechanical effects which alter the response of the MEMS [15], [18]–[21]. The mechanical properties of all materials used in this work are listed in Table 1. Consequently, as a result of the mechanical anisotropy of silicon, four common wafer orientations, depicted in Fig. 3, are investigated. For the first wafer (001) orientation, with the wafer normal pointing along [001] as shown in Fig. 3a, the crystal axes align with the spatial axes. The second configuration (001)[45], depicted in Fig. 3b, is rotated clockwise around the wafer normal by 45°, which is the typical orientation used in foundry processes due to its beneficial electrical response to uni-axial strain along the channel direction [110] [27]–[31]. The third wafer orientation (011) was added for completeness and does not exhibit known electrical or mechanical benefits over the other orientations. The wafer normal for the last orientation, shown in Fig. 3d, is pointing along [111]. This orientation is often times deemed beneficial for MEMS designs as Young's modulus, Poisson's ratio and shear modulus are isotropic in the {111} planes [18], [20], [21].

V. ELECTROMECHANICAL SIMULATION SETUP

All depicted setups are initially simulated in an electromechanical fashion for the different wafer orientations discussed in Section IV. The drive MOS capacitors and gates are biased at a constant direct current (dc) voltage $V_{\text{drive}} = 40$ mV

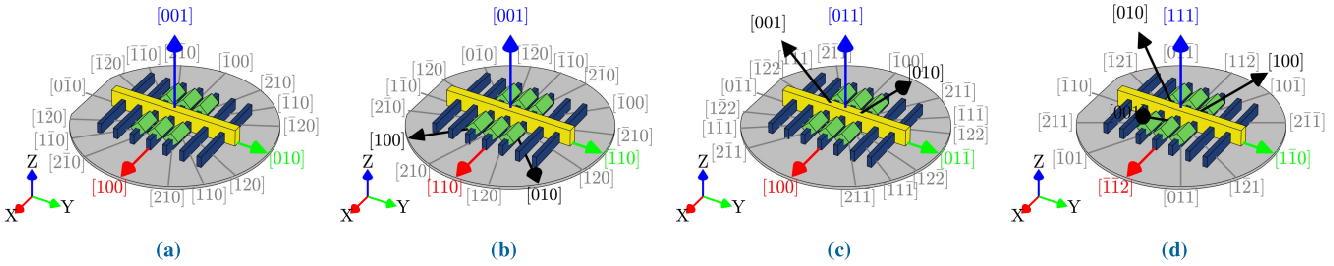


FIGURE 3. Simulated wafer orientations (a) (001), (b) (001)[45], (c) (011) and (d) (111). The channel and wafer normal direction are denoted by the red and blue arrows along the X and Z axis, respectively. The principal axes of the silicon crystal are indicated by black arrows.

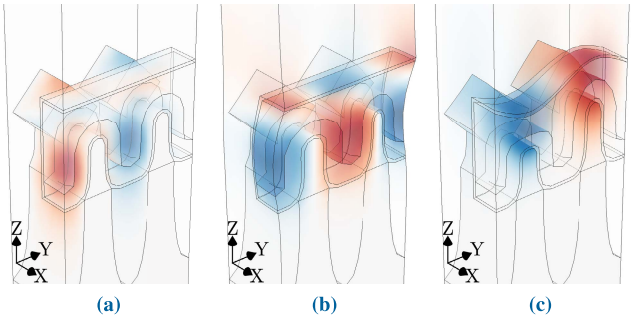


FIGURE 4. Deformation of the resonant mode for (a) *x*, (b) *y* and (c) *z* displacement only. Red and blue colours denote positive and negative displacement with regard to the displayed direction.

and $V_{\text{gate}} = 800\,\text{mV}$ for the NMOS and $V_{\text{drive}} = 760\,\text{mV}$ and $V_{\text{gate}} = 0\,\text{V}$ for the PMOS, respectively, as proposed in [12]. The initial stress inside the FEOL, introduced by the dc bias, is simulated with a stationary electromechanical simulation. For this pre-stressed structure, the possible mechanical eigenmodes are computed. All simulation setups support multiple resonant modes, however, not all can be coupled electro-mechanically for symmetry reasons. Depending on the exact configuration of the setups, a strong differential eigenmode, with regard to adjacent fins, can be found between 30–35 GHz. It is exemplarily depicted in Fig. 4 for the ideal 2-fin UC, separated in the displacements along the three principal axes. In resonance, adjacent fins expand and compress periodically around the channel. The mode causes only little deformation along the channel direction (X-axis) as shown in Fig. 4a. Along the gate direction (Y-axis), however, shown in Fig. 4b, the fins are alternately contracted and expanded. The same also applies to the vertical direction (Z-axis) illustrated in Fig. 4c. Those deformations lead to a breathing motion of adjacent fins and result in opposite stress, orthogonal to the channel direction, in neighbouring FinFETs. The overall displacement is also indicated in all three setups shown in Fig. 2.

It should be noted, that the larger the size of the UC is assumed, the more spurious modes can coexist, which in turn further degrades the performance of the device. In this work, all spurious modes are filtered out. Only the dominant mechanical eigenmode, referred to as RFT mode, depicted in Fig. 4, is investigated. The RFT mode is then used in an electro-mechanical frequency domain eigenmode simulation, considering the pre-stressed state, with an alternating current (ac) drive voltage amplitude of $v_{\text{drive}} = 30\,\text{mV}$ [12]. The Q-factor of the mode is limited to $Q = 1000$ via Rayleigh damping, to offer greater numerical stability.

VI. STRESS TENSOR

The mode exerts not only stress on the drive MOS capacitor FinFET channels, but—in resonance—will also deform the sense FinFETs. Therefore, the volume-averaged stress tensor is extracted from each frequency-domain simulation:

$$\sigma = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{bmatrix}. \tag{1}$$

It is fitted component-wise with a Fano function [32]:

$$S(f) = a + b\frac{2(f - f_{\text{R}}) - qf_{\text{R,BW}}}{2(f - f_{\text{R}}) - jf_{\text{R,BW}}}, \tag{2}$$

with a and b being complex-valued pre-factors, f_{R} denoting the resonant frequency, $f_{\text{R,BW}}$ the bandwidth of the resonance and q, the Fano parameter, describing the overall symmetry of the Fano resonance. The Q-factor of the resonance can be retrieved from $Q_{\text{R}} = f_{\text{R}}/f_{\text{R,BW}}$, which is identical to the value derived from the Rayleigh damping. In Fig. 5, the stress tensor of an exemplary 2-fin infinite UC, fitted with (2), is shown.

The stress tensor is expressed in the spatial coordinate frame with the X, Y and Z directions pointing along the channel, gate direction as well as the wafer normal direction, respectively. Fitting the stress tensor allows to reduce the frequency resolution of each simulation and thereby significantly speed up the analysis [14]. For a generalized representation of the data the pressure inside the channels [19]:

$$p = -\frac{1}{3}\sigma_{ii} \quad i = 1, 2, 3 \tag{3}$$

can be defined as the mean of the diagonal components of the stress tensor.

Exemplarily, the pressure spectrum calculated with (3) from the data displayed in Fig. 5 is shown in Fig. 6. It exhibits a distinct peak at the frequency f_{R} of the mechanical eigenmode. In addition to the main resonance, an antiresonance f_{A} is observed. Together, they define an electromechanical

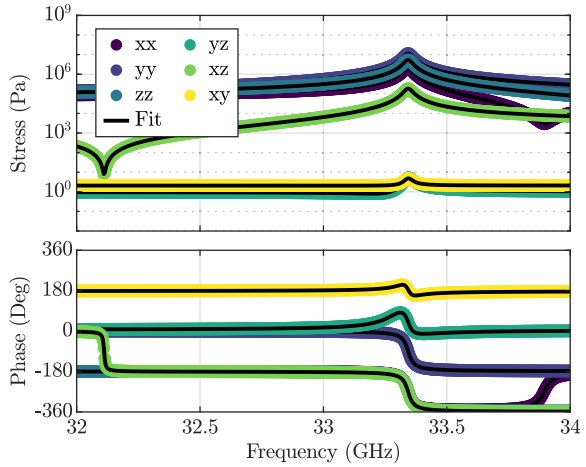


FIGURE 5. Fit of the individual stress tensor components with a Fano function for a (001)[45] oriented wafer and a 24 nm gate length at $Q = 1000$.

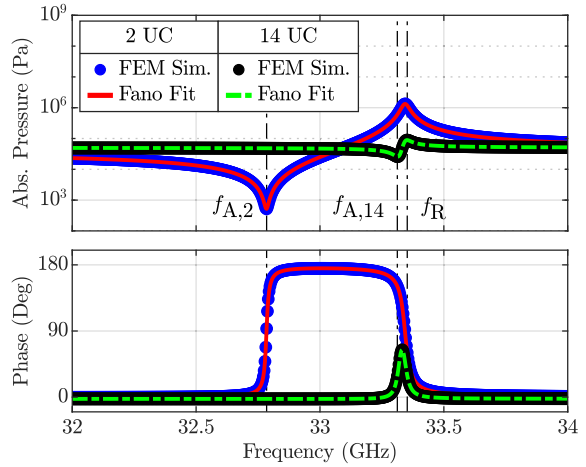


FIGURE 6. Fit of the overall pressure response for a 2-fin UC and 14-fin UC with a Fano function for a (001)[45] oriented wafer and a 24 nm gate length at $Q = 1000$.

coupling factor [33]:

$$k_{\text{eff}}^2 = \frac{\pi^2}{4}\left(\frac{f_R - f_A}{f_R}\right), \tag{4}$$

which describes the conversion efficiency from electrical to mechanical energy and vice versa. The coupling coefficient mainly relies on the static FinFET capacitance. It decreases for larger capacities, which leads to a strongly reduced coupling for the 14-fin UC compared to the ideal 2-fin case [14], [33], [34]. Moreover the absolute pressure in the 14-fin UC is greatly reduced compared to the ideal case, which is explained in more detail in Section IX-E6.

VII. CALIBRATION OF SIMULATION

The drive MOS capacitor simulations are calibrated to the measured capacitance of typical NMOS and PMOS gate lengths. As a result of the simplified gate stack, the fin to gate capacitance is overestimated in our simulations. Thus the

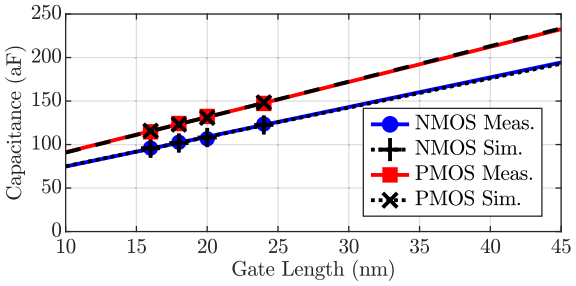


FIGURE 7. Calibration of the FEM capacitance to measurements. The data is fitted by linear regression.

dielectric constant $\epsilon_r = 25$ of the high-κ HfO_2 is scaled to the effective dielectric constant required to match simulation and measurement [23], [25]. The factors are calculated to $\epsilon_{r,nmos} = \epsilon_r/4.05$ and $\epsilon_{r,pmos} = \epsilon_r/3.2$. The measured and simulated capacitance of the structure is shown in Fig. 7 for some chosen gate lengths. The single fin capacitances are obtained from de-embedded RF measurements between 25–40 GHz from a larger device with four parallel gates and 30 fins, resulting in capacitances in the pF range. The gate length values correspond to the drawn gate length, however, a constant technology dependant offset for the gate length is considered in the simulations. After calibration, the capacitance of the NMOS and PMOS FinFETs are in excellent agreement with the measured data. Both measurement and simulation are fitted by linear regression as a guide to the eye. As the electromechanical force in a capacitor, formed between gate and fin, changes linearly with the capacitance, the fin pressure p also scales linearly with the relative permittivity of the high-κ layer as shown in Fig. 8. The changed relative permittivity does not affect the frequency of the resonance. Solely the anti-resonance is affected as electromechanical coupling changes with the static capacitance of the MEMS [14], [33], [34]. With an increasing static capacitance, the coupling coefficient is reduced. Therefore, the 14 UC should perform worse as the capacitance of the drive is threefold of the 2-fin counterparts. However, this effect is neglected in the following as the geometric variation and dependence on the Q-factor are assumed more important for the performance.

VIII. QUALITY FACTOR DEPENDENCY

The working principle of the RFT MEMS strongly relies on the reported Q-factor of almost 50 000. The Q-factor is reached with the aid of a PC mirror in the BEOL [12]. The large acoustic impedance mismatch of the different metal, liner and oxide layers can lead to the formation of a mechanical band gap. Through careful optimisation of the layer thicknesses and horizontal slotting, a wide band gap—matching the resonant frequency of the RFT MEMS—can possibly be created [15], [17], [35], [36]. A well-matched BEOL mirror can reduce losses and thereby increase the Q-factor. However, the copper metal layers are neither isotropic nor mono crystalline, which makes the modelling challenging [15], [16].

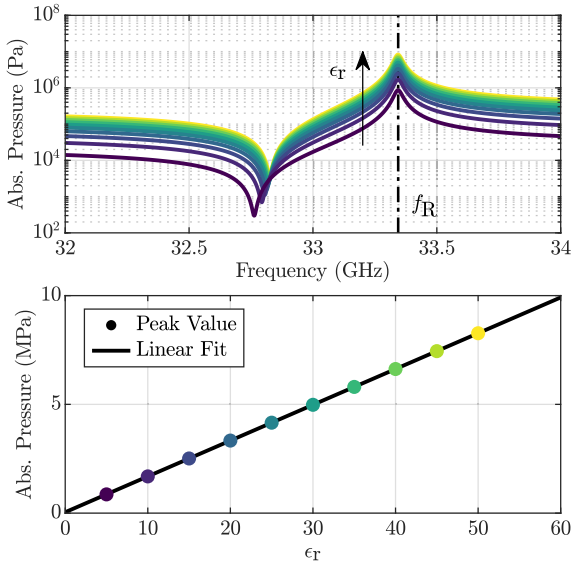


FIGURE 8. Dependence of the absolute pressure for the resonant mode on ϵ_r for a $(001)^{45}$ oriented wafer and a 24 nm gate length at $Q = 1000$.

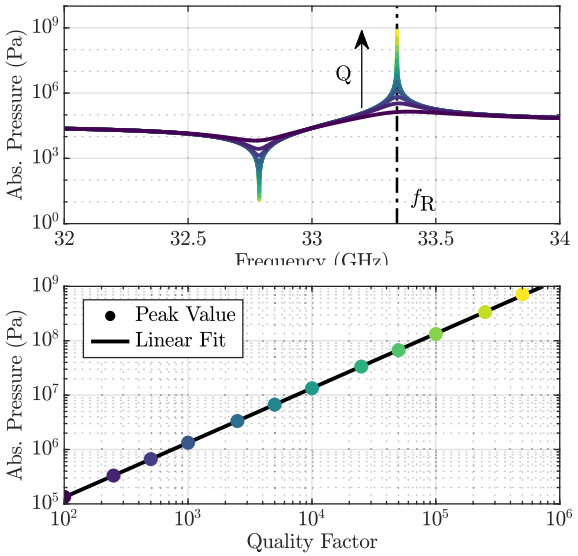


FIGURE 9. Dependence of the absolute pressure for the resonant mode on the Q-factor for a $(001)^{45}$ oriented wafer and a 24 nm gate length.

During fabrication, copper is crystallizing into grains with distinct orientations [16]. This effect further complicates the band gap formation as all metal layers would therefore exhibit varying mechanical properties based on the grain size and orientation. In the worst case the BEOL would not be able to form a PC and thus provide no shielding for the RFT. Moreover, current CMOS BEOL stacks are optimized for the electrical performance of existing devices, making adaptions for the needs of a singular device challenging. However, further investigations and in-depth analysis are required. Other SAW and BAW devices achieve Q-factors in the 100–10 000 range, although at much lower frequencies. They typically fall into the mega- to low gigahertz regime, with a few notable exemptions surpassing 100 000 [5]–[9].

Many of those designs, however, are partially released structures, which suffer mainly from anchor losses. Monolithic integration, on the other hand, requires extensive shielding in all directions. Therefore, more research is required to substantiate the—considering the results from prior art, surprisingly high—reported Q-factor of 49 000 [12]. Due to the increased complexity and the variance of the BEOL for each foundry and process node it was removed from the simulations and the Q-factor is added only via Rayleigh damping, which in turn enables the usage of arbitrary values. The RFT is thus modelled at a much lower Q-factor of 1000 for greater numerical stability, convergence and speed in the FEM simulations. Furthermore, it provides a worst-case approximation, in the case of a lower Q-factor than reported, for the circuit simulation in Section X.

The impact of a changing Q-factor on the pressure in resonance is shown in Fig. 9. It was varied between 100–500 000, however, the change in pressure at f_R scales linearly over multiple orders of magnitude as a result of the employed Rayleigh damping formalism. Thus, all simulations are carried out at a Q-factor of 1000, and can be scaled with:

$$p_{\text{new}} = p_{1000}\frac{Q_{\text{new}}}{1000} \tag{5}$$

to the desired Q-factor Q_{new}. This is only true for the resonance frequency and can not be used to scale the full spectrum to a new Q-factor. Note that (5) is only valid under the assumption of a linear mechanical response, however, the fins displacements are small, and thus justifying this assumption.

IX. SIMULATION RESULTS

The simulations were performed on the infinite 2-fin and 14-fin UC for typical CMOS FinFET gate lengths, ranging from 16–150 nm on four different silicon wafer orientations. Each simulation was repeated for both NMOS and PMOS FinFETs. The resonant frequency was extracted from the fitted data with (2), as explained in Section VI and is shown in Fig. 10. The resonant frequency shifts from 34.35–30.71 GHz with increasing gate lengths. Both UC configurations yield the same resonant frequency, which is to be expected as only the number of repetitions of the UC is changed. Furthermore, the different mechanical properties of each wafer result in separate resonant frequencies at the same gate length. As shown previously in Fig. 8, the choice of NMOS or PMOS devices does not influence the resonant frequency in those simulations.

Choosing a different gate length also enables MEMS with individual resonant frequencies, which can coexist on the same wafer. While this is a beneficial factor for circuit applications it is a challenge to design a mechanical BEOL band gap for a wider frequency range [15].

A. SYMMETRY SIMPLIFICATION OF FEM SIMULATIONS

In order to speed up the large scale simulations, depicted in Fig. 2c and Fig. 2d, the impact of a symmetric boundary

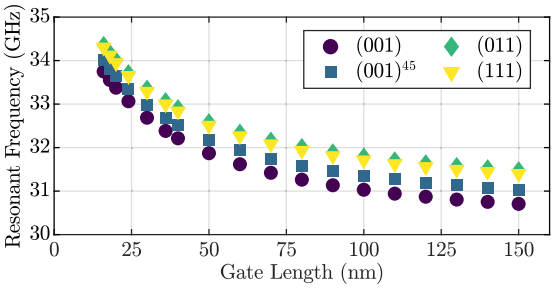


FIGURE 10. Resonant frequency f_R with wafer orientation and gate length.

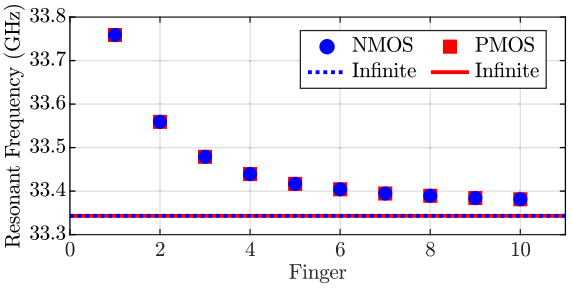


FIGURE 12. Resonant frequency f_R with number of fingers for a gate length of 24 nm and $(001)^{45}$ oriented wafer.

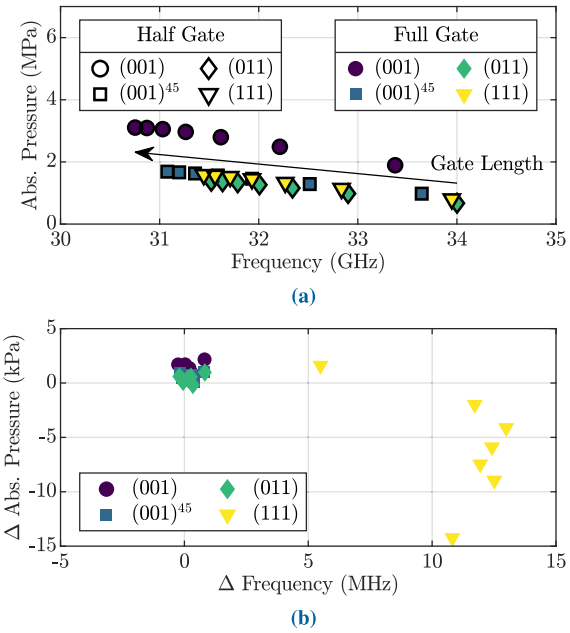


FIGURE 11. (a) Comparison of a simplified (black markers) and not simplified (coloured markers) 2-fin UC for different gate lengths and wafer orientations. (b) Difference between the simplified and not simplified simulation setup.

condition on the resonance was investigated. The simulations for the 2-fin UC were compared for a simplified geometry, with only half of a gate modelled (compare Fig. 2b), and a structure with a full gate and periodic boundary conditions in all lateral directions (compare Fig. 2a). The results of the half gate UC are unfolded at the symmetric boundary, and the resonant frequencies and absolute peak pressures are compared in Fig. 11a for several selected gate lengths for an NMOS device, to the full gate UC. For all orientations, the absolute pressure increases with longer gate lengths, as shown in Fig. 11a, whereas the resonant frequency decreases at the same time. The deviation between the modelled full gate and half gate is small for the orientations (001), $(001)^{45}$ and (011) as shown in Fig. 11b. For these orientations, the symmetry plane of the simplification aligns with one of the cubic symmetry planes of the anisotropic silicon. In those instances, both simulations yield almost identical results. However, if the simplification plane of the simulation UC does not align with one of the material symmetries—as is the case for (111)—the results will deviate from each other. In the case of misalignment, the gate experiences additional lateral bending motions along the X-axis, which are caused by an antisymmetric poisons ratio, resulting in a more pronounced shift. Moreover, the structure can also support additional modes, for example with displacements normal to the X-plane, which were suppressed by the symmetric boundary condition. However, all deviations are minor for the investigated wafer directions with the largest deviation in pressure being 14 kPa and in frequency 13 MHz, which justifies the usage of the simplified geometry regardless of the wafer orientation.

B. INFLUENCE OF A FINITE FINGER COUNT

The previous simulations assume an infinite number of parallel fingers due to the symmetric boundary conditions. A real device, however, has a finite number of fingers which are supported by a variable amount of dummy fingers on both sides. Dummy fingers serve only for structural uniformity as the fins are etched away in the region indicated by the dashed green box in Fig. 2d. The UC depicted in Fig. 2d is finite along the X-axis with a perfectly matched layer after the dummy fingers and a symmetric boundary condition on the opposite side in the centre of the RFT cavity. The depicted UC has eight true fingers which are protected by three dummy fingers on each side. The simulations were repeated for a $(001)^{45}$ wafer orientation and a gate length of 24 nm. The number of fingers and dummy fingers was swept from 1–10 and 1–3 , respectively. The resulting resonant frequencies for NMOS and PMOS devices are shown in Fig. 12. For a single finger, the resonant frequency is higher when compared to the infinite case (compare Fig. 10). However, for an increasing number of fingers, the resonant frequency assimilates to the infinite case. The number of dummy fingers on the other hand does not influence the resonant frequency. The same behaviour is to be expected in the case of a semi-infinite UC with 14 fins.

C. FINITE CAVITY LENGTH

The impact of the cavity length, i.e. the number of consecutive fins also impacts the performance. All simulations were carried out for an infinite number of fins, however, for a finite

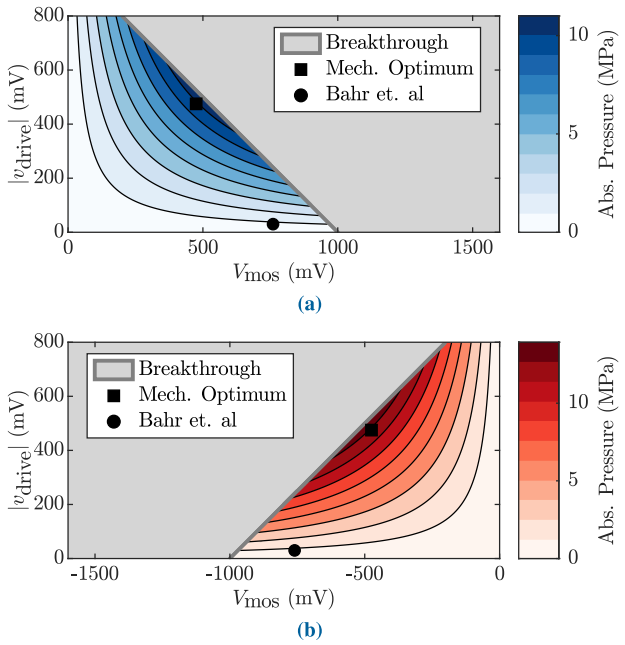


FIGURE 13. Absolute pressure with dc bias and ac amplitude for a 2-fin UC with a *Q*-factor of 1000 and 24 nm gate length for (a) NMOS with $V_{\text{gate}} = 0.8\,\text{V}$ and (b) PMOS with $V_{\text{gate}} = 0\,\text{V}$.

cavity length, the performance of the device should degrade as cavity termination plays a more important role. A termination similar to the BEOL reflector could be used, however, many different variations are possible and all should perform worse than the infinite assumption of the cavity. Therefore the infinity cavity assumption, very likely, overestimates the final result.

D. DC-BIASING AND AC-EXCITATION

For all simulations, the common gate is biased at a constant voltage $V_{\text{gate}} = 0.8\,\text{V}$ for NMOS and $V_{\text{gate}} = 0\,\text{V}$ for PMOS devices. The bias conditions for the drive and sense are discussed in the following sections.

1) DRIVE MOS CAPACITOR BIAS

All previous simulations were carried out for the voltages used by [12]. However, the absolute pressure inside the fin can be improved by optimizing the dc bias and ac amplitude. The results are shown in Fig. 13, for varying dc voltages $V_{\text{mos}} = V_{\text{gate}} - V_{\text{drive}}$ over the MOS capacitor and ac drive amplitude. With an increasing dc voltage $|V_{\text{mos}}|$ and an increasing ac voltage, the pressure inside the channel is rising. The larger the voltage difference between the channel of the MOS capacitor and gate, the higher the electro-mechanical force. This trend is limited by the breakthrough voltage of the gate oxide as well as the forward bias condition of the well-diodes. However, for both NMOS and PMOS devices the gate oxide is the limiting factor. The grey region highlights all bias combinations for $V_{\text{gate}} - (V_{\text{drive}} + |v_{\text{drive}}|)| > 1\,\text{V}$, which could potentially damage the MOS capacitors. The difference in pressures for the NMOS and PMOS devices is a factor of 1.266 which is caused by the different dielectric permittivity used for the gate oxide. When considering the gate oxide reliability, with a reduction of 50 mV for safety reasons, the optimum bias point for the highest mechanical pressure can be found. A mechanical improvement factor of approximately ten, over the values used by [12], can be achieved by moving the dc bias point to $V_{\text{drive}} = 325\,\text{mV}$ for the NMOS and $V_{\text{drive}} = 575\,\text{mV}$ for the PMOS with an ac amplitude for both to $v_{\text{drive}} = 475\,\text{mV}$. This bias point produces the largest deformation and is therefore the optimum from a mechanical perspective. For comparability, all the following simulations are carried out at $V_{\text{drive}} = 40\,\text{mV}$ and $v_{\text{drive}} = 30\,\text{mV}$. The optimized condition is used in Section X for the design of an oscillator circuit.

2) SENSE TRANSISTOR BIAS

The differentially wired sense transistor pair is biased in the linear regime at 200 mV which ensures the opening of a conductive channel. Furthermore, in this regime, the transistor behaves like a voltage-controlled resistor with the source-drain current being linearly dependent on the carrier mobility inside the channel which is explained in the following section.

E. PIEZORESISTIVE EFFECT

For stressed silicon, the energy band structure and thereby the electronic transport properties of the carriers are altered [31], [37]–[40]. The main contribution to the change in mobility—induced by a resistivity change—is known as the piezoresistance effect [37], [38]. This effect has revolutionized modern CMOS technology as strain engineering opened the path for better-performing transistors with enhanced channel mobility [30], [31]. Early investigations only focused on uniaxial deformation and subsequent mobility enhancements, whereas later the impact of inhomogeneous stress on mobility was studied in a generalized approach [37]–[39]. The anisotropic piezoresistance effect can be described analogously to the anisotropic mechanical properties with a 4^{th}-rank piezoresistance tensor or a 6×6 matrix using the Voigt's notation as [37]–[39]:

$$\Pi = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44}. \end{bmatrix}, \quad (6)$$

Its components π_{11}, π_{12} and π_{44} were originally obtained through measurements and are given in Table 2 for n-Si and p-Si.

1) DEPENDENCE ON TEMPERATURE AND DOPING CONCENTRATION

The components in Table 2 were originally measured at 300 K, however, they depend on the channel doping

TABLE 2. Piezoresistance components of n- and p-doped silicon at 300 K [37]–[39].

	π_{11} (Pa^{-1})	π_{12} (Pa^{-1})	π_{44} (Pa^{-1})
n-Si	-102.2×10^{-11}	53.4×10^{-11}	-13.6×10^{-11}
p-Si	6.6×10^{-11}	-1.1×10^{-11}	138.1×10^{-11}

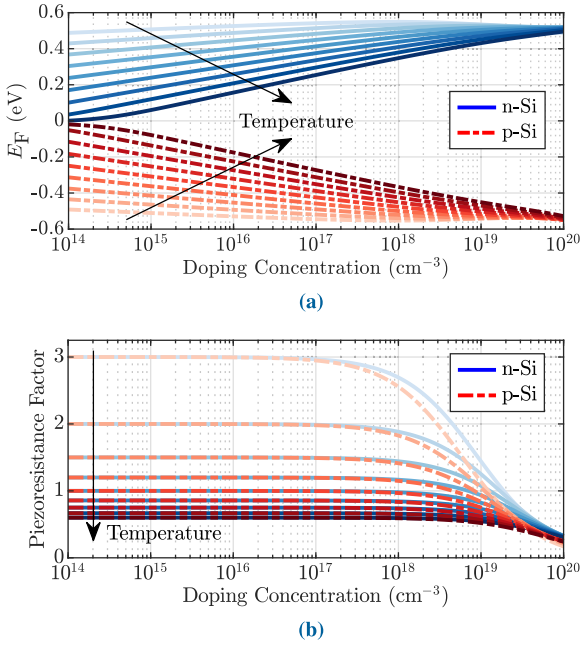


FIGURE 14. (a) Fermi level for n-Si and p-Si. (b) Piezoresistance factor for n-Si and p-Si. The temperature is increased from 100 – 500 K in steps of 50 K.

concentration N and temperature T [39]:

$$\Pi(N, T) = P(N, T)\Pi(300\,\mathrm{K}), \tag{7}$$

where P is the piezoresistance factor. It is given by:

$$P(N, T) = \frac{300}{T} \frac{F'_{s+(1/2)}(E_F/k_b T)}{F_{s+(1/2)}(E_F/k_b T)}, \tag{8}$$

with the Fermi integral F_s and its derivative F'_s as a function of the temperature and doping dependent Fermi energy E_F, the Boltzmann constant k_b, and temperature T [39], [41]–[43]. The doping concentration and temperature dependant Fermi energy for n-Si and p-Si is shown in Fig. 14a. At low channel doping densities around $1 \times 10^{15}\,\mathrm{cm}^{-3}$, which are typical for modern FinFET processes, the piezoresistive effect is enhanced with temperature for both n-Si and p-Si [44]. With larger doping densities, scattering processes increase and the overall mobility decreases [45], [46]. The absolute enhancement, however, is moderate in both cases, with an increase of only 50 % at 200 K for n-Si and p-Si. As such temperatures are difficult to maintain in a real-world application, all following considerations are carried out at room temperature.

Modern CMOS devices are initially strained along the channel direction during fabrication. By adding germanium to the epitaxial source- drain contacts the channel is compressed, effectively enhancing the mobility for PMOS devices. NMOS devices can be improved by adding a stress layer to the device, effectively putting the channel under tension and thereby increasing mobility [31]. This pre-existing strain is not considered in our simulations as only the harmonic response of the system is considered. This is possible due to the linearity of the piezoelectric model where the static part does not contribute to the final result. Using a method like $\mathbf{k} \cdot \mathbf{p}$ which is not linear at large strain the result might be different, however further analysis is required [29], [47], [48].

2) FinFET CHANNEL MOBILITY

In order to derive the mobility change in the sense transistor unit—caused by the deformation of the resonant mode—the piezoresistance tensor is transformed into the spatial coordinate frame for each wafer orientation with [39], [49], [50]:

$$\Pi_{ijkl} = A_{im}A_{jn}A_{kp}A_{lq}\Pi'_{mnpq} \quad (i, j, k, l, m, n, p, q = 1, 2, 3). \tag{9}$$

Here $A_{ij} = \mathbf{e}_i \cdot \mathbf{e}'_j$ are the direction cosines between the orthonormal bases of the crystal (primed) and the spatial (unprimed) basis with the orthonormal basis vectors $\mathbf{e}_i$ and $\mathbf{e}'_j$ with i, j run over 1, 2, 3. The absolute direction-dependent mobility variation inside the fins in spatial coordinates can then be determined by [37], [39]:

$$\frac{\Delta\mu_{ij}}{\mu_0} = -\Pi_{ijkl}\sigma_{kl} \quad (i, j, k, l = 1, 2, 3). \tag{10}$$

Hence the FinFET channel mobility change from source to drain, using Voigt's notation, is given by $\Delta\mu_{xx}$ in the spatial frame with the unstrained carrier mobility μ_0 [18], [37], [39]. The mobility along the channel is thus influenced by the longitudinal, transversal and shear stresses acting on the FinFET channel, which are accounted for by (10). Herein the change in channel conductance $\Delta\mu_{xx}$ is referred to as $\Delta\mu$ for the rest of this work, as all other directional enhancements are not of interest.

3) VALIDITY OF THE MODEL

For cubic semiconductors, the mobility change is linear for small stress up to 200 MPa [37]–[39], [47], [51]. For larger stress the mobility change is non-linear and the piezoresistance model is no longer valid. Since all simulations are carried out at $Q = 1000$ and the pressure scales linearly with the Q-factor (compare Fig. 9), the highest Q-factor for which the piezoresistance model should still yield sufficiently accurate results can be calculated. The maximum Q-factors, for an upper pressure-limit of 150 MPa, which is well below the confidence region of 200 MPa, are shown in Table 3. Therefore all simulations, regardless of the device type, wafer orientation, UC and gate length, should offer good accuracy at the reported Q-factor of almost 50 000 [12]. For Q-factors exceeding those values, the stress inside the FinFET channels surpasses 150 MPa and the piezoresistance model starts to overestimate the mobility change.

TABLE 3. Valid *Q*-factor range of the piezoresistance model for the infinite UCs with peak pressure at f_R scaled to 150 MPa.

MOS type	UC Fins	GL nm	*Q*-factor (in millions) (001)	$(001)^{45}$	(011)	(111)
NMOS	2	16	0.09	0.17	0.26	0.21
		24	0.07	0.14	0.20	0.17
		150	0.05	0.09	0.11	0.09
	14	16	1.68	2.67	3.17	2.93
		24	1.46	2.42	2.87	2.63
		150	1.00	1.75	2.04	1.80
PMOS	2	16	0.07	0.14	0.21	0.17
		24	0.06	0.11	0.16	0.13
		150	0.04	0.07	0.09	0.07
	14	16	1.34	2.14	2.58	2.39
		24	1.16	1.93	2.33	2.12
		150	0.80	1.40	1.63	1.45

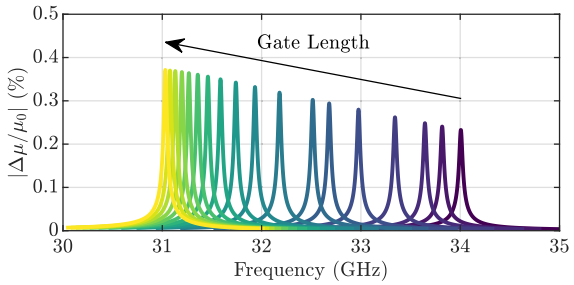


FIGURE 15. NMOS mobility variation for a $(100)^{45}$ oriented wafer and 2-fin UC (compare Fig. 2b).

4) MOBILITY CHANGE FOR A 2-FIN UC

Although the ideal 2-fin UC is not compliant with the foundry design rules it provides a best-case approximation, if all fins could be connected individually. From the fitted stress tensor (1) the mobility variation (10) in each fin can be calculated, as depicted in Fig. 15 for an infinite 2-fin NMOS UC on $(100)^{45}$ silicon. For this wafer orientation $|\Delta\mu/\mu_0|$ increases steadily with increasing gate length. However, this differs for each transistor type and wafer orientation. In the following the peak values at f_R are extracted and plotted for both transistor types and wafer orientations in Fig. 16. For n-Si, depicted in Fig. 16a, the mobility change at $Q = 1000$ is similar for all four orientations. At small gate lengths, the (001) wafer slightly outperforms all other wafers, with $(001)^{45}$ yielding a larger change at longer gate lengths. The absolute enhancement, however, is similar, regardless of the wafer orientations. For p-Si, shown in Fig. 16b, the spread is much larger, with the $(001)^{45}$ orientation being the strongest contender and outperforming all other orientations regardless of the gate length. The mobility changes between 1.6–2.4 % from short to long gate lengths. All other orientations are well below 0.5 % with (001) and (011) offering virtually no enhancement. Hence the focus is on the $(001)^{45}$ orientation for the remainder of this work, as it offers the best mobility enhancement independent of the type and gate length.

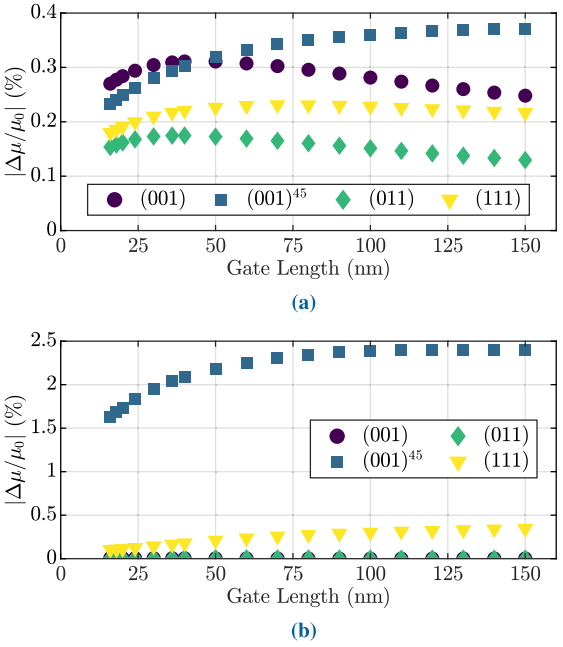


FIGURE 16. Mobility variation for the 2-fin UC at $Q = 1000$ for (a) NMOS and (b) PMOS devices.

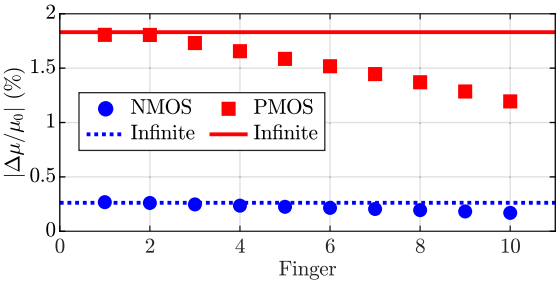


FIGURE 17. Mobility variation against the number of fingers.

Moreover, due to its beneficial electrical properties, this orientation is most commonly used in standard foundry IC design [27]–[31].

5) MOBILITY CHANGE WITH FINITE NUMBER OF FINGERS

The simulation was repeated for the semi-infinite setup (compare Fig. 2d), with a gate length of 24 nm and for the best orientation of $(001)^{45}$. The number of fingers and dummy fingers was varied and the results are shown in Fig. 17. Interestingly the mobility change for a single finger is the same as for the infinite case, albeit at a different frequency, as shown in Fig. 12. With an increasing number of parallel fingers the mobility enhancement decreases. This can be explained as the displacement decreases with a larger number of fingers. As all neighbouring gates expand and contract at the same time they impede each others movement which reduces the overall displacement. The decrease in displacement with added fingers can also be observed in Fig. 2d, with the gates closer to the dummy gates showing less deformation in comparison to the centre gates. The number of dummy

gates was swept from 1 to 3, which does not impact the result. The optimal mode shape would be differential between neighbouring fins and also between adjoining gates. In this constellation, they would contract and expand in a chequerboard pattern and not obstruct each other. However, there is no possibility to connect the RFT in a foundry design rule compliant fashion to be able to couple to this mode electromechanically.

6) MOBILITY CHANGE FOR A 14-FIN UC

For the ideal configuration, each fin is connected to a different electric potential, however, for the real 14-fin UC, groups of three fins are jointly connected to the same potential, as shown in Fig. 2c. The overall mobility change in each three fin package is calculated from the sum of the individual fins:

$$\Delta\mu = \Delta\mu_3 + \Delta\mu_4 + \Delta\mu_5 \approx \Delta\mu_3, \tag{11}$$

With the subscript denoting the fin number indicated in Fig. 2c. For the second group, the mobility change can be calculated from fins 10 to 12, respectively although the absolute mobility change in both groups should be identical with opposite signs, as a result of the linearity of the piezoresistance model. For each fin, a separate stress tensor is extracted and used for the calculation. In resonance, all fins are deformed equally with a phase shift of 180° between neighbouring fins. Therefore the total mobility change in (11) is equal to the change inside a single fin as two fins in each group cancel. Using a more accurate model like the $\mathbf{k}\cdot\mathbf{p}$ perturbation method, the mobility change is not linear and saturates at different levels for opposing signs of stress which would prevent a perfect cancellation in each group [29], [47], [48]. However, the pressures are in the low MPa range and saturation is not reached. The mobility change for the 14-fin UC is shown in Fig. 18. The trends are almost identical compared to the 2-fin configuration with the $(001)^{45}$ PMOS device, shown in Fig. 18b, again outperforming all other orientations. However, the absolute mobility enhancement is reduced by a factor of approximately seven compared to the 2-fin UC. This can be explained as only two fins out of the 14-fin UC are actively contributing to the driving and sensing of the resonant mode due to the previously described cancellation. Minor deviations between the 14-fin and 2-fin UC can be discerned, which may be attributed to minor differences in the actual mode shape during a frequency domain simulation in the larger UC.

In order to achieve the largest mobility enhancement inside the sense transistor units, the PMOS is the preferred choice over NMOS devices. Furthermore, the $(001)^{45}$ wafer is on a similar level as the other orientations when it comes to the NMOS, but outperforms all of them for the PMOS devices. To achieve the best mobility enhancement and thus the biggest ac current, the least amount of parallel fingers is preferential. Not only due to the overall reduced mobility with each added finger, but also the increasing dc current, which increases the power consumption of the device.

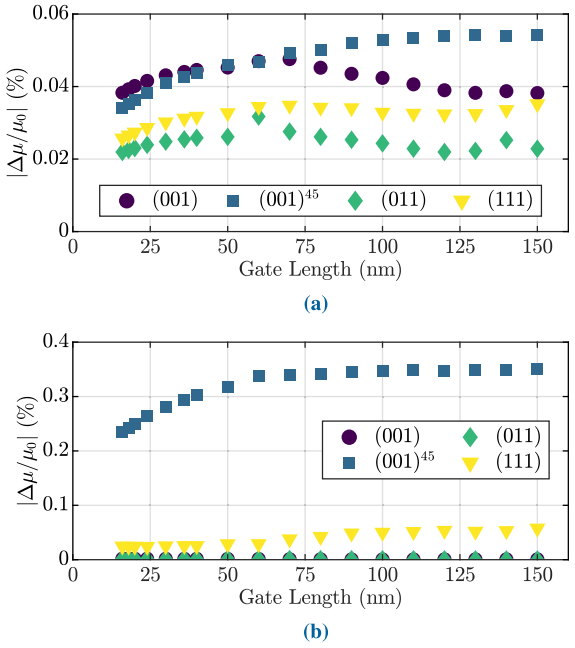


FIGURE 18. Mobility variation for the 14-fin UC at $Q = 1000$ for (a) NMOS and (b) PMOS devices.

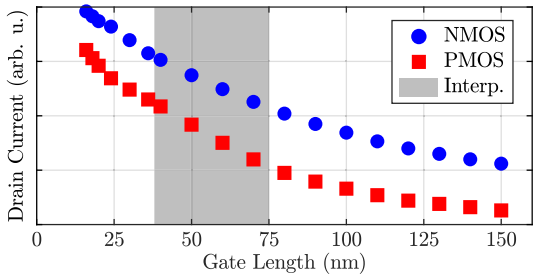


FIGURE 19. Drain current scaling of a one fin transistor with a single gate with gate length. The values in the grey region are interpolated with an Akima spline.

F. SENSE FINFET CURRENTS

The resonant mode causes a carrier mobility change in the sense transistors channels. It modulates the current under a constant sense dc bias of $V_{\text{sense}} = 200\,\text{mV}$, which is shown for a single fin and finger FinFET in both types and at various gate lengths in Fig. 19 [12]. The dc current degrades with longer gate lengths as channel resistance increases. Also, the NMOS FinFET offers a higher absolute current at the same gate length compared to a PMOS device. The scaling with number of parallel fingers for a single fin transistor is shown in Fig. 20. It scales linearly for both types with the number of fingers. From the dc current, with the mobility change calculated from the piezoresistance model in Section IX-E, the ac current running through the sense transistor pair of the 2-fin UC can be calculated to:

$$i_{\text{sense}} = I_{\text{sense}} \frac{\Delta\mu_1}{\mu_0}, \tag{12}$$

with the dc current I_{sense} of a single fin FinFET. For the 14-fin UC the ac current is analogously derived from the sum of the

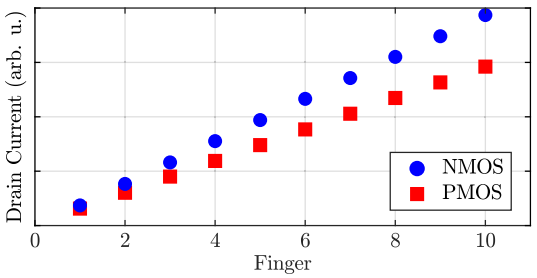


FIGURE 20. Drain current scaling for a one fin transistor with a 24 nm long gate.

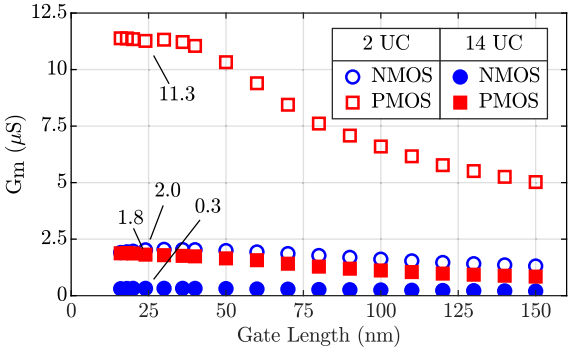


FIGURE 21. Mechanical transconductance of NMOS and PMOS for the two and 14 UC at a *Q*-factor of 1000.

individual fins in each group with:

$$i_{\text{sense}} = I_{\text{sense}}\frac{\Delta\mu_3}{\mu_0} + I_{\text{sense}}\frac{\Delta\mu_4}{\mu_0} + I_{\text{sense}}\frac{\Delta\mu_5}{\mu_0} \approx I_{\text{sense}}\frac{\Delta\mu_3}{\mu_0}, \tag{13}$$

with the single fin current I_{dc} and the mobility variation from the individual fins. Again, two fins cancel as a result of the linearity at small pressures. Therefore the absolute ac current is accounted for by just one fin out of each group in the UC. From the ac voltage at the drive MOS capacitors and the ac current at the sense transistors the mechanical transconductance [12]:

$$G_{\text{m}} = \left|\frac{i_{\text{sense}}}{v_{\text{drive}}}\right| \tag{14}$$

is calculated. Note that effects such as the stress induced shift of the silicon band gap and subsequent threshold voltage shift in the sense transistors as well as velocity saturation have not been considered in this model [52], [53]. Their impact is expected to be negligible as the simulated stress levels are small. Possible modelling approaches have been shown in [54].

It is shown for both FinFET types on the optimal wafer orientation $(001)^{45}$ for the infinite two and 14-fin UCs in Fig. 21. The transconductance is almost plateauing for gate lengths up to 40 nm. In this region the increase in mobility and the decrease in current compensate each other, however, for longer gates, the transconductance starts to decrease

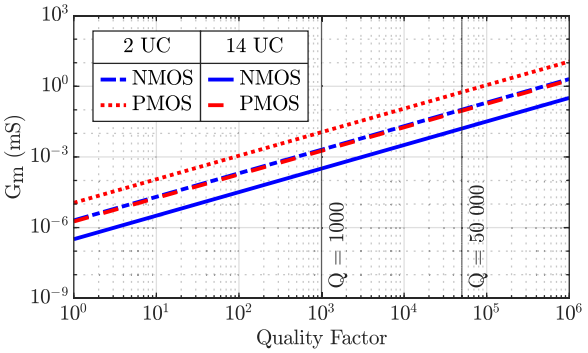


FIGURE 22. Mechanical transconductance of NMOS and PMOS for the two and 14 UC at with a gate length of 24 nm on a $(001)^{45}$ silicon wafer.

as the mobility enhancement cannot counteract the current decrease. Again the 2-fin configuration outperforms the 14-fin UC by a factor of approximately seven. Considering all displayed configurations a 24 nm gate length is the best over all variants. Those results are scaled to $Q = 50\,000$ with (5) and shown in Fig. 22. At a Q-factor of 50 000 the 14-fin UC achieves a mechanical transconductance in the low µS regime. The G_{m} can be improved by utilizing more parallel fingers, as the dc current and hereby ac current would increase. However, an important figure of merit to consider is the transconductance per dc current as it is the main contribution to the power consumption of the device. The best configuration possible, without major adjustments to the CMOS process, is the 2-fin configuration with $Q = 50\,000$, where each fin is actively driven without sparse fins in-between, achieves 100 µS for the NMOS and 565 µS for the PMOS, respectively.

Analogously to Section IX-D the optimal bias condition for the largest transconductance at a sense bias of 200 mV can be found as shown in Fig. 23. The transconductance for the previously optimized bias point is worse than the original bias condition, albeit the increased mobility enhancement. As the drive voltage increases so does the pressure and further the ac sense current, however the latter increases at a slower rate which worsens the transconductance. From a circuit perspective, the best bias condition must be chosen, in accordance with the circuit requirements like signal amplitude and phase-noise. It is in-between the points for the optimal transconductance and the best mechanical performance. A feasibility study for an RFO circuit with the new results at the best mechanical bias point is carried out in the next section.

A discrepancy of two orders of magnitude was found between our simulated mechanical transconductance in comparison to the reported values of 14 mS by Bahr et al., for an unknown device MOS-type and gate length [12]. Our analysis yields only 0.1 mS for the NMOS and 0.565 mS for the PMOS RFT with a Q-factor of 50 000. Furthermore, a G_{m} of 14 mS with a drive voltage of $v_{\text{drive}} = 30$ mV would require an ac output at the sense transistor of $i_{\text{sense}} = 420$ µA. Given the reported dc currents of the sense transistor at $I_{\text{sense}} = 120$ µA a mobility enhancement of 350 % is required [12].

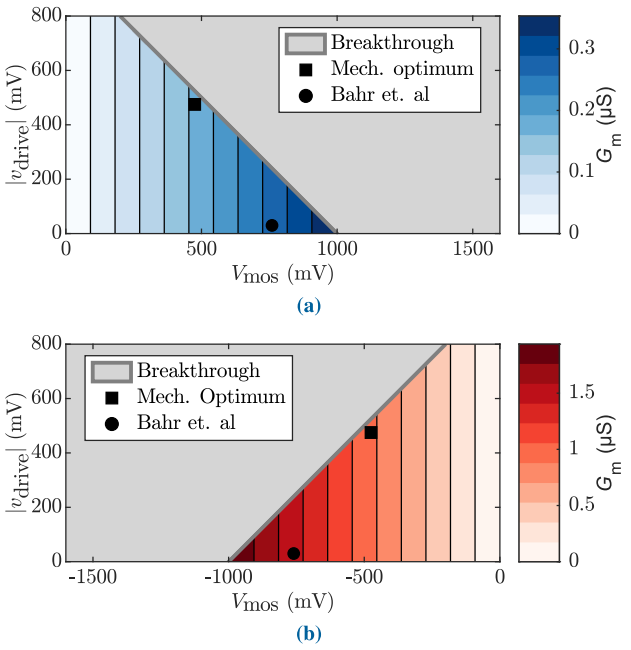


FIGURE 23. Mechanical transconductance with dc bias and ac amplitude for a 2-fin UC with a *Q*-factor of 1000 and 24 nm gate length for (a) NMOS with $V_{gate} = 0.8$ V and (b) PMOS with $V_{gate} = 0$ V.

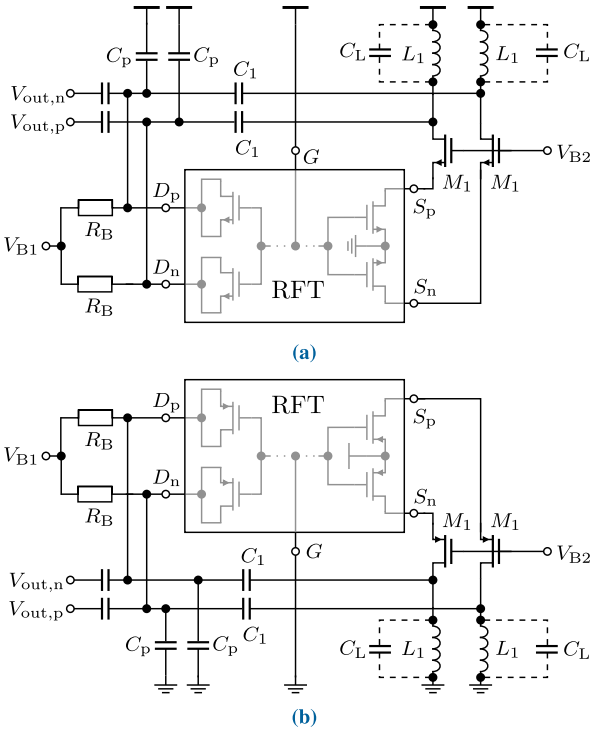


FIGURE 24. Schematic of exemplary RFO implementation, (a) for the NMOS-RFT and (b) for the PMOS-RFT.

An enhancement of this magnitude is not reported in literature for silicon. The largest enhancements possible according to prior art, require stress in the low gigapascal range for a change up to approximately 60 % [29], [31], [47], [55]–[58]. However, for all possible CMOS compatible voltage combinations (compare Fig. 13) only low megapascal pressures inside the RFT FinFETs were found. Even with an increased *Q*-factor of 50 000, the pressure does not surpass 700 MPa for the PMOS and therefore will suffice only for a µS transconductance. Low megapascal values for the RFT were also reported in literature, further substantiating the lower G_m [13]. Thus, considering our simulations results and the material properties reported in literature, high values for G_m above 1 mS seem impossible to reach by the RFT device.

X. CIRCUIT DESIGN

As already discussed in Sec. I an important application for the RFT resonator can be found in the field of RF circuit design. Therefore, in this section, despite the decreased performance as described in Sec. IX, an exemplary oscillator design is shown, using the RFT as resonator in the oscillator circuit in order to asses the significance of this device for RF circuit design. Thus, performance estimations with respect to phase-noise (PN) and power are discussed in the following sections.

A. OSCILLATOR CIRCUIT DESIGN

Due to the active 4-port nature of the RFT, common RF LC-oscillator solutions like crossed coupled CMOS cores–shown e.g. in [59] and implemented e.g. in [60]–can not be instantly used as oscillator core for this type of resonator. The oscillator topology has to serve four main purposes in order to achieve a stable oscillation: 1) biasing of the RFT sense transistors, 2) transformation of the sense current into a voltage signal, 3) amplification of the sense signal to an appropriate drive voltage for the RFT input, and 4) phase correction of the fed-back sense signal. The two requirements 3) and 4) can be formulated by the well known Barkhausen's criteria [59]:

$$|H(j\omega_0)| \stackrel{!}{=} 1 \tag{15}$$

$$\angle H(j\omega_0) \stackrel{!}{=} 180°, \tag{16}$$

with $H(j\omega)$ as open-loop transfer function of the oscillator structure at a finite frequency ω_0. Fig. 24 shows the schematic of an oscillator variant in (a) NMOS-implementation and (b) PMOS implementation using a cascode amplifier in the feedback loop to fulfil all requirements. The biasing is mainly set by the transistors M_1, while the gain of the feedback loop is achieved by the equivalent parallel resistance R_p of the inductors L_1. The feedback capacitor C_1 is dimensioned to resonate the inductance L_1 at the resonance frequency of the RFT to ensure the correct phase of the drive signal is fed back from the sense output. The dc bias of the drive-side is set via the resistors R_B. For a first dimensioning of the oscillator, the configuration of the RFT shown in Table 4 is used in accordance with the results presented in Sec. IX. Fig. 25 shows the equivalent circuit diagram of the RFT with its external circuitry corresponding to the parameters shown in Table 4. The oscillator is designed for both MOS-types.

TABLE 4. Selected RFT configuration for RFO dimensioning.

Parameter	MOS-type	Value
UC configuration		14-fin
Resonance frequency f_R	both	33.342 GHz
Q-factor Q_R		1000
Cell configuration[1]	both	10 drive cells 1 sense cell
dc current I_{sense}	PMOS NMOS	124 µA 150 µA
Mobility variation $\Delta\mu$	PMOS NMOS	2.6172 % 0.3802 %
Gate voltage V_{gate}	PMOS NMOS	0 V 800 mV
Drive ac voltage v_{drive}	both	475 mV 475 mV
Drive bias voltage V_{drive}	PMOS NMOS	575 mV 325 mV

[1] differential UC

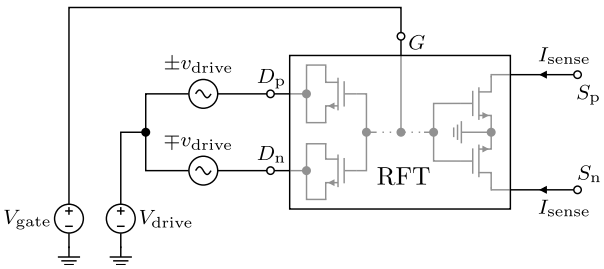


FIGURE 25. Equivalent circuit diagram of the RFT and its input voltages and current in accordance with Table 4.

1) DIMENSIONING

The transistors M_1 are dimensioned to set the drain-source-voltage of the RFT sense transistors to 200 mV to ensure a fully developed conducting channel as discussed in Section IX-D. The gate voltage V_{B2} is set to operate the M_1-transistors in saturation with $V_{B2} = 520$ mV for the NMOS-RFO (NRFO) and $V_{B2} = 270$ mV for the PMOS-RFO (PRFO). The gain of the feedback is determined by the inductor L_1, more precisely by its equivalent parallel resistance R_p. With the parameters for the dc-current and the mobility variation from Table 4, an ac-sense current in the range of nA is to be expected at the output of the RFT device. Thus the gain in the feedback loop has to be quite high in order to provide 475 mV at the drive input. Therefore, the parallel resistance R_p, given by [59]:

$$R_p = Q \cdot 2\pi f_R \cdot L_1, \tag{17}$$

with Q as Q-factor of the metal inductor, L_1 the inductance and f_R the fixed resonance frequency of the RFT should be maximized. With the frequency parameter fixed, the geometric properties of the inductor should be chosen in order to achieve the highest product $Q{\cdot}L_1$ possible within a reasonable on-chip area of 100 µm x 100 µm. This area constraint is chosen to keep the area consumption of the RFO circuit within the range of common state-of-the-art RF-digitally controlled oscillator (DCO) implementations cf. [61], [62]. For the exemplary dimensioning of the RFO, a symmetrically shaped metal inductor with dummy metals and guard-ring as depicted in Fig. 26 was chosen. The geometric parameters for L_1 as well as its electrical properties are given in Table 5 for an implementation of L_1 on thick top-metals of an RF-metal-stack.

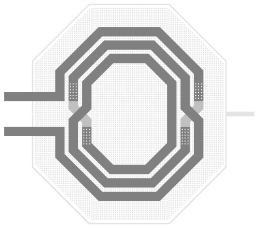


FIGURE 26. Layout of head inductor L_1.

TABLE 5. Properties of RFO-inductance L_1.

Parameter	Value
Turns	3
Track width	4 µm
Track spacing	2 µm
Inner diameter	17 µm
Q-factor Q_L	5.28
Inductance L_1	1.26 nH
Area (with guard-ring)	90 µm x 100 µm

The series capacitance in the feedback loop combines two functionalities: 1) decoupling of feedback voltage from dc potential, and 2) phase correction for feedback voltage according to (16). In order to correct the phase of the output voltage of the RFO, the capacitor C_1 has to resonate the head inductor L_1 at the resonance frequency f_R of the RFT. For the dimensioning of C_1, also the drive input capacitance given by C_{moscap} as well as the parasitic capacitance C_L of the head inductor itself have to be taken into account. Therefore the complete capacitance contributing to the resonating tank is given by:

$$C_{res} = \frac{C_{moscap} \cdot C_1}{C_{moscap} + C_1} + C_L. \tag{18}$$

For the given RFT configuration of Table 4, the drive input capacitance for one drive port (D_p or D_n) accumulates to values of $C_{moscap} = 3.55$ fF for the NRFO and $C_{moscap} = 3.47$ fF for the PRFO, which are extracted by simulation and proven by measurement of the transistor devices, respectively. The needed tank capacitance for the given inductance to hit the resonance frequency f_R can be calculated to:

$$C_{res,goal} = \left(\frac{1}{2\pi f_R}\right)^2 \cdot \frac{1}{L} = 18.037\,\text{fF}. \tag{19}$$

The parasitic capacitance of the inductor can be extracted from a circuit simulation to $C_L = 610.0$ aF. In order to

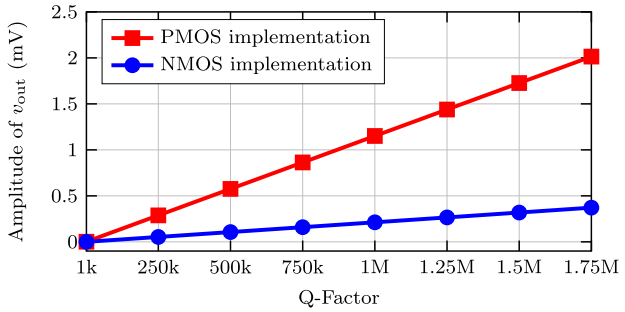


FIGURE 27. Amplitude of drive voltage v_{out} against the Q-factor sweep of the RFT for pure NMOS and pure PMOS implementation of the RFO simulated open-loop for a drive-input amplitude of 475 mV.

achieve the needed $C_{res,goal}$ and therefore fulfil (18), a capacitance C_p is placed in parallel to the drive input capacitance C_{moscap} to enlarge the series circuit formed by C_{moscap} and C_1. The tank capacitance C'_{res} then calculates to:

$$C'_{res} = \frac{(C_{moscap} + C_p) \cdot C_1}{C_{moscap} + C_p + C_1} + C_L. \tag{20}$$

C_p and C_1 are dimensioned in consideration of the ratio of the capacitive voltage divider formed by C_{moscap}, C_p and C_1:

$$k_{cdiv} = \frac{C_1}{C_1 + C_{moscap} + C_p}, \tag{21}$$

as the loop-gain is degraded by k_{cdiv}. According to this design trade-offs C_p and C_1 are chosen to $C_p = 13.91$ fF and $C_1 = 321.122$ fF for the NRFO and $C_p = 13.71$ fF and $C_1 = 321.122$ fF for the PRFO. The value of C_p is additionally optimized to account for leakage currents through the sense transistor determined by ac-simulation of the oscillator circuit.

2) OPEN-LOOP SIMULATION

The loop gain of the RFO-implementation is determined by an open-loop ac-simulation of the oscillator circuit depicted in Fig. 24 with the feedback loop opened at the node between the drive input of the RFT and the feedback capacitor C_1. With the given RFO circuit, the gain-condition for oscillation in (15) can be rewritten to:

$$k_{Gain} = g_{m,RFT} \cdot R_p \cdot k_{cdiv} \stackrel{!}{=} 1 \tag{22}$$

In Fig. 27 the simulation results for the amplitude of the fed-back drive voltage v_{drive} are shown for different Q-factors of the RFT resonator. For the exemplary NMOS-RFT configuration from Table 4 and the oscillator dimensioning done in Section X-A1, the loop-gain can be determined to $k_{Gain} = 0.477 \cdot 10^{-3}$. Thus an additional amplifier with a gain of approximately 67 dB is needed in the feedback loop in order to meet the criteria in (15). For a rough worst-case noise- and power estimation a simple inverter-based buffer chain is implemented with a total gain of $k_{Amp} = 5938 \equiv 75.5$ dB. The buffer chain has a length of nine stages with ac-coupling and dc-biasing in-between each stage as depicted in Fig. 28. The stages are scaled

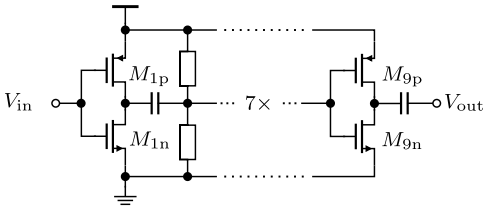


FIGURE 28. Schematic of a simple inverter-based amplifier.

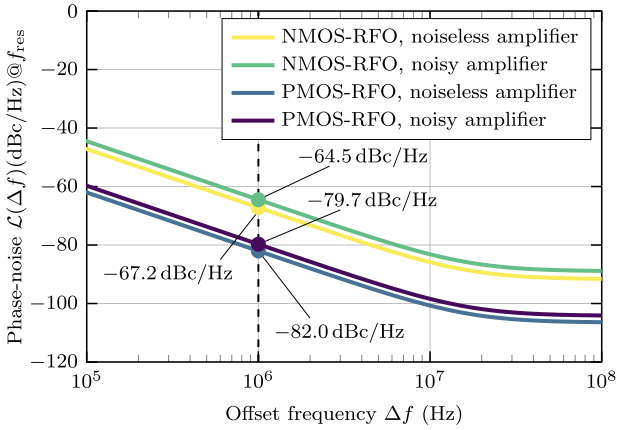


FIGURE 29. Phase-noise performance of RFO with ideal and noisy amplifier in the feedback loop.

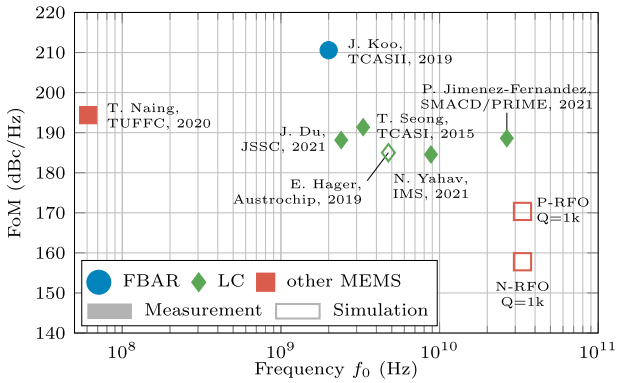


FIGURE 30. Comparison of the simulated NRFO and PRFO implementations with ideal noiseless feedback amplifier to state-of-the-art oscillator implementations regarding their FoM.

in their size, starting at minimal transistor dimensioning at the first stage up to a multiplication factor of four at later stages, respectively. For the subsequent circuit analysis and simulation, the additional phase shift induced by the feedback amplifier is neglected. For a complete RFO implementation, a phase compensation has to be integrated. The noise estimation is done by calculating the input-referred noise at each stage of the amplifier using its small-signal equivalent circuit diagram [63]:

$$\overline{V^2_{in,n}} = \frac{4k_b T\gamma}{g_{m,PMOS,n} + g_{m,NMOS,n}}, \tag{23}$$

with n being the stage number ranging from 1 to 9, $g_{m,*,n}$ representing the transconductance of the NMOS- and PMOS-transistors in the buffer, k_b as Boltzmann constant, T as absolute temperature in K and γ as noise coefficient.

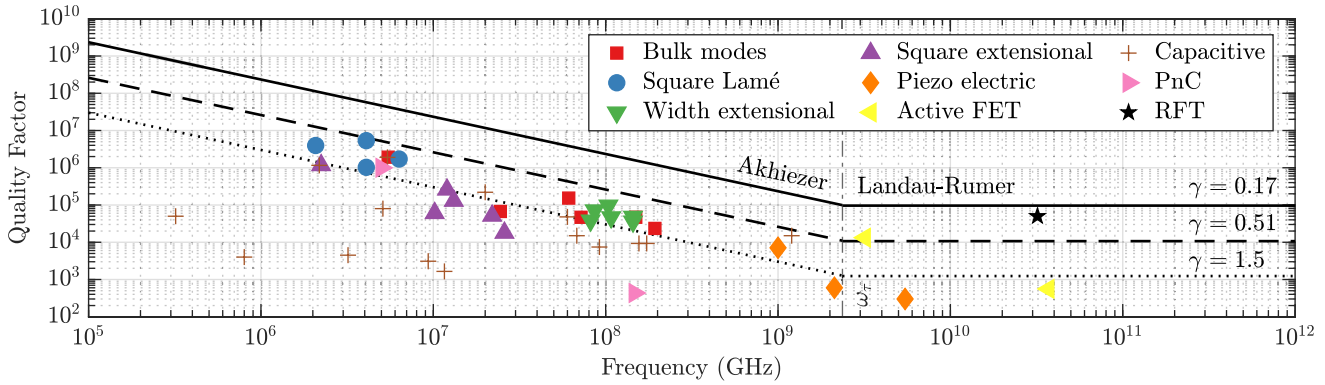


FIGURE 31. Upper, average and lower AKE and LR $Q \cdot f$ limit for silicon MEMS. Values collected from [6], [12], [67], [68].

The individual noise contributions are summarized using Friis' formula [64]:

$$\overline{V^2_{\text{out,tot}}} = \sum_{i=1}^{n} \left(\overline{V^2_{\text{in,i}}} \cdot \prod_{k=i}^{n} G_k^2 \right). \tag{24}$$

For the exemplary amplifier implementation of $n = 9$ stages, the total noise contribution of the amplifier at the output can be calculated to $\overline{V^2_{\text{out,tot}}} = 0.734\,\text{nV}^2/\text{Hz}$ at the resonance frequency f_R of the RFT. This noise voltage is taken as flat noise contribution over the complete frequency span of interest (1 Hz – 100 GHz) for further circuit simulations, in order to get a worst-case estimation for the phase-noise contribution of the amplifier to the overall RFO phase-noise. Effects of flicker-noise in the amplifier are not taken into account by the used flat noise characteristic. For the PRFO the loop-gain can be determined to $k_{\text{Gain}} = 2.423 \cdot 10^{-3}$, which enables a decreased gain-target for the feedback amplifier. For the oscillator implementation, the same amplifier is used as for the NRFO circuit. The number of stages is reduced to $n = 7$ resulting in a total gain of $k_{\text{Amp}} = 806 \equiv 58.1\,\text{dB}$ and a flat noise contribution of $\overline{V^2_{\text{out,tot}}} = 0.013\,\text{nV}^2/\text{Hz}$. The selection of this amplifier topology is solely motivated by its simplicity and expected small on-chip area of the layout. However, the wide noise bandwidth of this amplifier type is not optimal for the narrow-band RFT signal as it introduces superfluous noise in the output signal. Thus a tuned amplifier with reduced bandwidth would be more suitable for the feedback amplifier. This topology uses tuned LC-tanks to achieve a narrow bandwidth. The biggest drawback of these architectures is their larger layout-area because of the tank inductors. Furthermore, to ensure the needed feedback-gain of over 50 dB, multiple amplifier stages are needed. It should be also noted, that, no matter which amplifier architecture is chosen, each additional amplifier stage in the feedback loop of the RFO increases the chip-area of the oscillator device and, due to the low Q-factor of the amplifier-tank, impacts the phase-noise of the complete circuit. Therefore, both main advantages of the RFT as resonant device in the oscillator, namely small size and excellent phase-noise due to the high Q-factor, are negatively impacted by the need of additional amplifier stages in the feedback. Nevertheless, the simulations in the following section, conducted using the inverter-based feedback amplifier give a good basic estimation of the achievable performance of an RFO-implementation. Furthermore, the simulations are also carried out for an ideal noiseless amplifier in the feedback loop, to determine the fundamental limit in phase-noise of the oscillator structure.

3) CIRCUIT SIMULATION

With the additional amplifier in the feedback loop a safety factor of 2.65 is achieved for closed loop operation of the RFO. In the closed loop circuit, the amplifier is implemented as ideal gain with its noise contribution added through a noise source. For correct operation of the resonator an automatic gain control (AGC) has to be employed between amplifier-output and RFT-input, as the RFT circuit model used for the simulations does not include any limiting mechanism. The AGC is implemented as a limiter, following a tanh-shape with the upper and lower limits set according to the RFT configuration for the ac-drive voltage reported in Table 4. The RFO phase-noise is simulated with a periodic-steady-state (PSS) simulation followed by a phase-noise simulation. Fig. 29 depicts the simulation results for the phase-noise simulation of the RFO at its fixed resonance frequency f_R in closed loop operation with and without the impact of the amplifier-noise. The phase-noise data for lower offset-frequencies Δf is approximated by a Lorentzian spectrum as presented in [65]. For the ideal implementation–without the amplifier noise–at an offset frequency of $\Delta f = 1\,\text{MHz}$ from the carrier-frequency the RFO achieves a phase-noise of $-67.2\,\text{dBc/Hz}$ and $-82.0\,\text{dBc/Hz}$, respectively for the NRFO and PRFO.

With a corresponding power consumption of 1.62 mW and 1.24 mW, respectively, the FoM of the RFO for an ideal amplifier implementation calculated by [66]:

$$\text{FoM} = -\mathcal{L}(\Delta f) + 20 \cdot \log\left(\frac{f_0}{\Delta f}\right) - 10 \cdot \log\left(\frac{P_{\text{DC}}}{1\,\text{mW}}\right), \tag{25}$$

can be determined to 157 dBc/Hz for the NRFO and to 170 dBc/Hz for the PRFO. Fig. 30 shows the FoM of the RFT in comparison with other state-of-the-art oscillator implementations in the field of mobile communication. This comparison illustrates the big gap in performance between the RFO and common oscillator implementations due to the limited performance of the RFT itself. In the recent publication [13] the RFT has already been shown in combination with a CMOS circuitry in order to form a mmW-oscillator with high spectral purity. However, the pursued modelling approach is incorrect as it assumes a capacitive sensing mechanism. Following from the original publication by Bahr et al. active FinFET sensing is vital. Consequently, the modified Butterworth-Van-Dyke model may not be deployed in the classical sense, as a conversion from voltage domain at the drive to the current domain at the sense is necessary, as highlighted in this publication [14]. Since the authors of the original [12] and the erroneous modelling publication [13] are affiliated, the controversy of the reported values in both publications may not be disregarded.

XI. CONCLUSION

Our study confirmed the basic working principle proposed by [12]. It was investigated with FEM simulations, which brought insights into the best device configuration from a mechanical perspective. The RFT performs best on a $(001)^{45}$ oriented silicon wafer with a gate length of 24 nm. Here the carrier mobility variation inside the sense unit is the largest, in both NMOS and PMOS type devices. Considering a multi-finger device the optimum is found to be at a singular gate as mechanical displacement and hereby mobility modulation degrade with an increasing number of fingers. Considering a 14 UC with a Q-factor of 50 000 at the default bias values the device could achieve a theoretical mechanical transconductance of 15 µS for NMOS and 90 µS for PMOS devices, respectively. Although the basic functionality of the devices was confirmed by our simulations, a discrepancy to the reported value of 14 mS was found. Given the uncertainty of the reported Q-factor and the unreasonably high carrier mobility enhancements, the results reported in [12] could not be verified.

Nevertheless, the transconductance of the RFT can be improved by different means: Firstly by adding more parallel fingers, which increases i_{sense}. This comes at the expense of a higher power consumption as the gain per additional finger is decreasing while each finger contributes to the overall dc current of the device. Secondly, the G_{m} can be slightly improved by cooling the device to sub-ambient temperatures, which is challenging in a real-world application. Thirdly, an improvement up to a factor of seven can be achieved by enabling single fin contacts without sparse fins in the UC, effectively replicating the results of the 2-fin UC. Single fin contacts also allow for a reduction of the dc current by a factor of three, thereby reducing the power consumption. However, tighter FEOL and BEOL integration on this scale requires extensive lithography evolutions, which stand in contrast to the low reported performance of the RFO especially in the presence of better performing devices. And lastly, by switching to a different technology, incorporating either piezoelectric or ferroelectric materials, the coupling coefficient and therefore the mechanical transconductance could potentially be improved [5], [8], [9], [69], [70]. Nevertheless, a functional RFO circuit concept was designed with an optimized bias condition for both NMOS- and PMOS-variant of the RFT. It was evaluated for several Q-factors, ranging from a lower more plausible Q-factor of 1000 to the reported 50 000 from [12]. The FoM of the oscillator circuit design, which is based on a cascode-amplifier with additional ideal gain in the feedback-loop, achieves values for a Q-factor of 1000 of 153 dBc/Hz for the NRFO and 170 dBc/Hz for the PRFO, which is quite low compared to other state-of-the-art RF-designs (compare Fig. 30). This makes the RFT unattractive for competitive RF-circuit design for frequency generation. Furthermore, the authors of [12] fail to substantiate the claim of the astonishingly large $Q \cdot f$ product of 1.57×10^{15}. Considering all damping mechanisms, like the Achiever effect (AKE) and Landau-Roomer (LR) attenuation, as well as the thermoplastic dissipation (TED) and the PC, the total Q-factor of the RFT is limited by the Matthiessen's rule [67], [68], [71]–[73]

$$\frac{1}{Q_{\text{RFT}}} = \frac{1}{Q_{\text{AKE}}} + \frac{1}{Q_{\text{LR}}} + \frac{1}{Q_{\text{NC}}} + \frac{1}{Q_{\text{TED}}} + \cdots \tag{26}$$

to the smallest Q-factor of all involved loss mechanisms. For well designed high frequency devices the losses by TED are negligible [72], [74]. For frequencies $\omega_\tau \tau_{\text{l}} < 1$, where $\tau_{\text{l}} = 67.3$ ps is the relaxation time of longitudinal waves in silicon along the gate direction ⟨110⟩, the AKE is expected to be the dominant attenuation source [67]. It limits the Q-factor to the phonon-phonon attenuation limit [75], [76]. Here the $Q \cdot f$ product is given by [77], [78]

$$Q_{\text{AKE}} \cdot f = \frac{\rho c_{\text{l}}^2 c_{\text{d}}^2}{6\pi \gamma^2 k T} \tag{27}$$

where the Debye velocity [74], [75]

$$c_{\text{d}}^{-3} = \frac{2c_{\text{t}}^{-3} + c_{\text{l}}^{-3}}{3} \tag{28}$$

is calculated from the longitudinal and transversal sound wave velocities in silicon along the gate direction ⟨110⟩ with $c_{\text{l}} = 9130\,\text{m s}^{-1}$ and $c_{\text{t}} = 4672\,\text{m s}^{-1}$ [75]. The Grüneisen parameter γ varies between 0.17–1.5 with the commonly used average $\gamma_{avg} = 0.51$, however, it is challenging to assess this quantity accurately [67], [71], [72], [75]. Moreover $k = 130$–$148\,\text{W K}^{-1}\,\text{m}^{-1}$ is the thermal conductivity and $T = 300$ K the temperature [77], [78]. The AKE, as plotted in Fig. 31 for the upper and lower limit as well as the average, impose the fundamental limit of the frequency product by means of quantum mechanical phonon scattering, which solely relies on the involved materials [67], [79], [80]. High performing MEMS devices in that realm rarely exceed the average $Q \cdot f$ product as shown for selected silicon MEMS.

For resonators with frequencies in excess of $\omega_\tau \tau_l > 1$, the $Q \cdot f$ product is limited by the LR attenuation. In this region the wavelength is smaller than the mean free phonon path causing an acoustic attenuation proportional to ω as a result of three-phonon interactions [74]. Here the $Q \cdot f$ product [74], [76]

$$Q_{\mathrm{LR}} \cdot f = \frac{30 \rho c_{\mathrm{d}}^5 \hbar^3}{\pi^4 \gamma^2 k_{\mathrm{b}} T^4} f \tag{29}$$

increases linearly with frequency. Again, top performing MEMS rarely surpass the average LR attenuation. However, although the MEMS are limited by LR and may thus surpass the AKE in this frequency range, $Q \cdot f$ above the AKE are unreported [71].

Nevertheless the RFT approaches the upper limit, reporting the best performance to the current date [12]. This value however, is improbable as the performance of the BEOL PC is questionable in the presence of anisotropic copper which strongly alters the band gap formation [15]. Furthermore, the RFT is built out of several different materials, including high porosity SiCO:H in close proximity to the cavity, which should worsen the theoretical upper limit of the $Q \cdot f$ product. Regardless of the validity of the Q-factor, our simulations, including all assumptions and considered effects shown in Section IV to IX, could not confirm the reported transconductance. It is calculated to be three orders of magnitude lower than reported making the device ineffective for IC design.

ACKNOWLEDGMENT

(Richard Hudeczek and Ehrentraud Hager contributed equally to this work.)

REFERENCES

[1] G. Wikström, J. Peisa, P. Rugeland, N. Johansson, S. Parkvall, M. Girnyk, G. Mildh, and I. L. Da Silva, "Challenges and technologies for 6G," in *Proc. 2nd 6G Wireless Summit (6G SUMMIT)*, Mar. 2020, pp. 1–5, doi: 10.1109/6GSUMMIT49458.2020.9083880.

[2] L. Reichardt, C. Sturm, F. Grunhaupt, and T. Zwick, "Demonstrating the use of the IEEE 802.11 P car-to-car communication standard for automotive radar," in *Proc. 6th Eur. Conf. Antennas Propag. (EUCAP)*, Mar. 2012, pp. 1576–1580, doi: 10.1109/EuCAP.2012.6206084.

[3] A. L. Lacaita, S. Levantino, and C. Samori, *Integrated Frequency Synthesizers for Wireless Systems*. Cambridge, U.K.: Cambridge Univ. Press, 2007.

[4] E. Hager and H. Pretl, "Considerations on high-performance frequency synthesizers and high-Q oscillators," in *Proc. Austrochip Workshop Microelectron. (Austrochip)*, Oct. 2021, pp. 1–4, doi: 10.1109/Austrochip53290.2021.9576873.

[5] G. Piazza, P. J. Stephanou, and A. P. Pisano, "One and two port piezoelectric higher order contour-mode MEMS resonators for mechanical signal processing," *Solid-State Electron.*, vol. 51, nos. 11–12, pp. 1596–1608, 2007, doi: 10.1016/j.sse.2007.09.037.

[6] J. Yang, B. Hamelin, S. D. Ko, and F. Ayazi, "Ultra-high Q monocrystalline silicon carbide disk resonators anchored upon a phononic crystal," in *Proc. Solid-State Sens., Actuators Microsyst. Workshop*, Hilton Head Island, SC, USA, 2018, pp. 83–86, 2018, doi: 10.31438/trf.hh2018.22.

[7] L. Shi, W. Xuan, B. Zhang, S. Dong, H. Jin, and J. Luo, "Numerical investigation of phononic crystal based film bulk acoustic wave resonators," *Nanomaterials*, vol. 11, no. 10, p. 2547, Sep. 2021, doi: 10.3390/nano11102547.

[8] L. Shao, S. Maity, L. Zheng, L. Wu, A. Shams-Ansari, Y.-I. Sohn, E. Puma, M. N. Gadalla, M. Zhang, C. Wang, E. Hu, K. Lai, and M. Lončar, "Phononic band structure engineering for high-Q gigahertz surface acoustic wave resonators on lithium niobate," *Phys. Rev. Appl.*, vol. 12, no. 1, Jul. 2019, Art. no. 014022, doi: 10.1103/physrevapplied.12.014022.

[9] S. Gong and G. Piazza, "Monolithic multi-frequency wideband RF filters using two-port laterally vibrating lithium niobate MEMS resonators," *J. Microelectromech. Syst.*, vol. 23, no. 5, pp. 1188–1197, Oct. 2014, doi: 10.1109/JMEMS.2014.2308259.

[10] M. Ziaei-Moayyed, M. F. Su, C. M. Reinke, I. El-Kady, and R. H. Olsson, "Silicon carbide phononic crystals for high f.Q micromechanical resonators," in *Proc. IEEE Int. Ultrason. Symp.*, Oct. 2010, pp. 162–166, doi: 10.1109/ULTSYM.2010.5935682.

[11] A. C. Fischer, F. Forsberg, M. Lapisa, S. J. Bleiker, G. Stemme, N. Roxhed, and F. Niklaus, "Integrating MEMS and ICs," *Microsyst. Nanoeng.*, vol. 1, May 2015, Art. no. 15005, doi: 10.1038/micronano.2015.5.

[12] B. Bahr, Y. He, Z. Krivokapic, S. Banna, and D. Weinstein, "32 GHz resonant-fin transistors in 14 nm FinFET technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 348–350, doi: 10.1109/ISSCC.2018.8310327.

[13] A. Srivastava, B. Chatterjee, U. Rawat, Y. He, D. Weinstein, and S. Sen, "Analysis and design considerations for achieving the fundamental limits of phase noise in mmWave oscillators with on-chip MEMS resonator," *IEEE Trans. Circuits Syst. II, Expr. Briefs*, vol. 68, no. 4, pp. 1108–1112, Apr. 2021, doi: 10.1109/TCSII.2020.3030074.

[14] E. Hager, R. Hudeczek, P. Baumgartner, and H. Pretl, "Modeling and analysis of high-Q resonant-fin transistors," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 4780–4786, Sep. 2021, doi: 10.1109/TED.2021.3097302.

[15] R. Hudeczek and P. Baumgartner, "Mechanical band gap formation in anisotropic CMOS back-end-of-line stacks for monolithic high-Q MEMS resonator confinement," in *Proc. IEEE 51st Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2021, pp. 211–214, doi: 10.1109/ESSDERC53440.2021.9631769.

[16] A. Basavalingappa and J. R. Lloyd, "Effect of microstructure and anisotropy of copper on reliability in nanoscale interconnects," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 1, pp. 69–79, Mar. 2017, doi: 10.1109/TDMR.2017.2655459.

[17] A. Khelif and A. Adibi, *Phononic Crystals: Fundamentals and Applications*, A. Khelif and A. Adibi, Eds. New York, NY, USA: Springer, 2015.

[18] J. J. Wortman and R. A. Evans, "Young's modulus, shear modulus, and Poisson's ratio in silicon and germanium," *J. Appl. Phys.*, vol. 36, no. 1, pp. 153–156, Jan. 1965, doi: 10.1063/1.1713863.

[19] J. Roesler, *Mechanical Behaviour of Engineering Materials*. Berlin, Germany: Springer, 2007.

[20] J. Kim, D.-I. Cho, and R. S. Müller, "Why is (111) silicon a better mechanical material for MEMS?" in *Transducers'01 Eurosensors XV*. Berlin, Germany: Springer, 2001, pp. 662–665, doi: 10.1007/978-3-642-59497-7_157.

[21] Z. Qin, Y. Gao, J. Jia, X. Ding, L. Huang, and H. Li, "The effect of the anisotropy of single crystal silicon on the frequency split of vibrating ring gyroscopes," *Micromachines*, vol. 10, no. 2, p. 126, Feb. 2019, doi: 10.3390/mi10020126.

[22] J. P. Dismukes, L. Ekstrom, and R. J. Paff, "Lattice parameter and density in germanium-silicon alloys," *J. Phys. Chem.*, vol. 68, no. 10, pp. 3021–3027, Oct. 1964, doi: 10.1021/j100792a049.

[23] J. Zizka, S. King, A. G. Every, and R. Sooryakumar, "Mechanical properties of low- and high-k dielectric thin films: A surface Brillouin light scattering study," *J. Appl. Phys.*, vol. 119, no. 14, Apr. 2016, Art. no. 144102, doi: 10.1063/1.4945672.

[24] M. Tomar, V. Gupta, and K. Sreenivas, "Temperature coefficient of elastic constants of SiO_2 over-layer on $LiNbO_3$ for a temperature stable SAW device," *J. Phys. D, Appl. Phys.*, vol. 36, no. 15, pp. 1773–1777, Aug. 2003, doi: 10.1088/0022-3727/36/15/304.

[25] J. Robertson, "High dielectric constant gate oxides for metal oxide Si transistors," *Rep. Prog. Phys.*, vol. 69, no. 2, pp. 327–396, Dec. 2006, doi: 10.1088/0034-4885/69/2/R02.

[26] F. H. Featherston and J. R. Neighbours, "Elastic constants of tantalum, tungsten, and molybdenum," *Phys. Rev.*, vol. 130, no. 4, pp. 1324–1333, May 1963, doi: 10.1103/PhysRev.130.1324.

[27] E. Ungersboeck, V. Sverdlov, H. Kosina, and S. Selberherr, "Strain engineering for CMOS devices," in *Proc. 8th Int. Conf. Solid-State Integr. Circuit Technol.*, 2006, pp. 124–127, doi: 10.1109/ICSICT.2006.306094.

[28] B. Yang and M. Cai, "Advanced strain engineering for state-of-the-art nanoscale CMOS technology," *Sci. China Inf. Sci.*, vol. 54, no. 5, pp. 946–958, May 2011, doi: 10.1007/s11432-011-4224-9.

[29] S. Dhar, E. Ungersböck, H. Kosina, T. Grasser, and S. Selberherr, "Electron mobility model for ⟨110⟩ stressed silicon including strain-dependent mass," *IEEE Trans. Nanotechnol.*, vol. 6, no. 1, pp. 97–100, Jan. 2007, doi: 10.1109/TNANO.2006.888533.

[30] M. Saitoh, A. Kaneko, K. Okano, T. Kinoshita, S. Inaba, Y. Toyoshima, and K. Uchida, "Three-dimensional stress engineering in FinFETs for mobility/on-current enhancement and gate current reduction," in *Proc. Symp. VLSI Technol.*, Jun. 2008, pp. 18–19, doi: 10.1109/VLSIT.2008.4588547.

[31] S. E. Thompson *et al.*, "A 90-nm logic technology featuring strained-silicon," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1790–1797, Nov. 2004, doi: 10.1109/TED.2004.836648.

[32] A. M. Martínez-Argüello, M. Martínez-Mares, M. Cobián-Suárez, G. Báez, and R. A. Méndez-Sánchez, "A new Fano resonance in measurement processes," *Europhys. Lett.*, vol. 110, no. 5, p. 54003, Jun. 2015, doi: 10.1209/0295-5075/110/54003.

[33] V. Choudhary and K. Iniewski, *MEMS: Fundamental Technology and Applications*, V. Choudhary and K. Iniewski, Eds. Boca Raton, FL, USA: CRC Press, 2013.

[34] C.-H. Hong, H.-P. Kim, B.-Y. Choi, H.-S. Han, J. S. Son, C. W. Ahn, and W. Jo, "Lead-free piezoceramics—Where to move on?" *J. Materiomics*, vol. 2, no. 1, pp. 1–24, Mar. 2016, doi: 10.1016/j.jmat.2015.12.002.

[35] B. W. A. Bahr, "Monolithically integrated MEMS resonators and oscillators in standard IC technology," Ph.D. dissertation, Massachusetts Inst. Technol., Cambridge, MA, USA, 2016.

[36] R. Hudeczek and P. Baumgartner, "Polarization independent band gaps in CMOS back-end-of-line for monolithic high-*Q* MEMS resonator confinement," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4578–4581, Nov. 2020, doi: 10.1109/TED.2020.3025521.

[37] T. Manku and A. Nathan, "Electrical properties of silicon under nonuniform stress," *J. Appl. Phys.*, vol. 74, no. 3, pp. 1832–1837, Aug. 1993, doi: 10.1063/1.354790.

[38] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Phys. Rev.*, vol. 94, no. 1, pp. 42–49, Apr. 1954, doi: 10.1103/PhysRev.94.42.

[39] Y. Kanda and Y. Kanda, "A graphical representation of the piezoresistance coefficients in silicon," *IEEE Trans. Electron Devices*, vol. ED-29, no. 1, pp. 64–70, Jan. 1982, doi: 10.1109/T-ED.1982.20659.

[40] M. Bao, *Analysis and Design Principles of MEMS Devices*. Amsterdam, The Netherlands: Elsevier, 2005.

[41] Y. Kanda, "Piezoresistance effect of silicon," *Sens. Actuators A, Phys.*, vol. 28, no. 2, pp. 83–91, Jul. 1991, doi: 10.1016/0924-4247(91)85017-I.

[42] J. C. Doll and B. L. Pruitt, *Piezoresistance Fundamentals*. New York, NY, USA: Springer, 2013.

[43] B. Abdelaziz, K. Fouad, and S. Kemouche, "The effect of temperature and doping level on the characteristics of piezoresistive pressure sensor," *J. Sensor Technol.*, vol. 4, no. 2, pp. 59–65, 2014, doi: 10.4236/jst.2014.42007.

[44] H. R. Khan, D. Mamaluy, and D. Vasileska, "Quantum transport simulation of experimentally fabricated nano-FinFET," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 784–796, Apr. 2007, doi: 10.1109/TED.2007.892353.

[45] G. Masetti, M. Severi, and S. Solmi, "Modeling of carrier mobility against carrier concentration in arsenic-, phosphorus-, and boron-doped silicon," *IEEE Trans. Electron Devices*, vol. ED-30, no. 7, pp. 764–769, Jul. 1983, doi: 10.1109/T-ED.1983.21207.

[46] S. Reggiani, M. Valdinoci, L. Colalongo, M. Rudan, G. Baccarani, A. Stricker, F. Illien, N. Felber, W. Fichtner, and L. Zullino, "Electron and hole mobility in silicon at large operating temperatures. I. Bulk mobility," *IEEE Trans. Electron Devices*, vol. 49, no. 3, pp. 490–499, Mar. 2002, doi: 10.1109/16.987121.

[47] S.-E. Ungersböck, "Advanced modeling of strained CMOS technology," Ph.D. dissertation, Inst. Microelectron., Technischen Universität Wien, Vienna, Austria, 2007.

[48] J. L. Ma, Z. F. Fu, Q. Wei, and H. M. Zhang, "Uniaxial stress induced electron mobility enhancement in silicon," *Silicon*, vol. 5, no. 3, pp. 219–224, Jul. 2013, doi: 10.1007/s12633-013-9144-4.

[49] T. Ando and T. Toriyama, "Description of new piezoresistance tensor equation for cubic single crystal and its application to multiaxial stress," *Sensors Mater.*, vol. 30, no. 9, p. 2101, Sep. 2018, doi: 10.18494/SAM.2018.1959.

[50] J. Turley and G. Sines, "Anisotropic behaviour of the compliance and stiffness coefficients for cubic materials," *J. Phys. D, Appl. Phys.*, vol. 4, no. 11, pp. 1731–1736, Nov. 1971, doi: 10.1088/0022-3727/4/11/317.

[51] F. Rochette, M. Cassé, M. Mouis, A. Haziot, T. Pioger, G. Ghibaudo, and F. Boulanger, "Piezoresistance effect of strained and unstrained fully-depleted silicon-on-insulator MOSFETs integrating a HfO_2/TiN gate stack," *Solid-State Electron.*, vol. 53, no. 3, pp. 392–396, Mar. 2009, doi: 10.1016/j.sse.2009.01.017.

[52] Y. Sun, S. E. Thompson, and T. Nishida, "Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 101, no. 10, May 2007, Art. no. 104503, doi: 10.1063/1.2730561.

[53] S. K. Marella, A. R. Trivedi, S. Mukhopadhyay, and S. S. Sapatnekar, "Optimization of FinFET-based circuits using a dual gate pitch technique," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2015, pp. 758–763, doi: 10.1109/ICCAD.2015.7372646.

[54] U. Rawat, B. Bahr, and D. Weinstein, "Analysis and modeling of an 11.8 GHz fin resonant body transistor in a 14 nm FinFET CMOS process," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 69, no. 4, pp. 1399–1412, Apr. 2022, doi: 10.1109/TUFFC.2022.3147973.

[55] W. Lee, Y. Hwangbo, J.-H. Kim, and J.-H. Ahn, "Mobility enhancement of strained Si transistors by transfer printing on plastic substrates," *NPG Asia Mater.*, vol. 8, no. 3, p. e256, Mar. 2016, doi: 10.1038/am.2016.31.

[56] J.-L. Ma, H.-M. Zhang, X.-Y. Wang, Q. Wei, G.-Y. Wang, and X.-B. Xu, "Valence band structure and hole effective mass of uniaxial stressed germanium," *J. Comput. Electron.*, vol. 10, no. 4, pp. 388–393, Oct. 2011, doi: 10.1007/s10825-011-0374-7.

[57] H. Irie, K. Kita, K. Kyuno, and A. Toriumi, "In-plane mobility anisotropy and universality under uni-axial strains in NAND p-MOS inversion layers on (100), [110], and (111) Si," in *IEDM Tech. Dig.*, Dec. 2004, pp. 225–228, doi: 10.1109/IEDM.2004.1419115.

[58] C. Gallon, G. Reimbold, G. Ghibaudo, R. A. Bianchi, R. Gwoziecki, S. Orain, E. Robilliart, C. Raynaud, and H. Dansas, "Electrical analysis of mechanical stress induced by STI in short MOSFETs using externally applied stress," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1254–1261, Aug. 2004, doi: 10.1109/TED.2004.831358.

[59] B. Razavi, *Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level*. Cambridge, U.K.: Cambridge Univ. Press, 2020.

[60] D. Yang, D. Murphy, H. Darabi, A. Behzad, R. Ruby, and R. Parker, "An FBAR driven −261 dB FOM fractional-N PLL," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2021, pp. 147–150, doi: 10.1109/RFIC51843.2021.9490409.

[61] M. Mercandelli, A. Santiccioli, S. M. Dartizio, A. Shehata, F. Tesolin, S. Karman, L. Bertulessi, F. Buccoleri, L. Avallone, A. Parisi, A. L. Lacaita, M. P. Kennedy, C. Samori, and S. Levantino, "A 12.9-to-15.1 GHz digital PLL based on a bang-bang phase detector with adaptively optimized noise shaping achieving 107.6fs integrated jitter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 445–447, doi: 10.1109/ISSCC42613.2021.9365768.

[62] Y. Lim, J. Kim, Y. Jo, J. Bang, S. Yoo, H. Park, H. Yoon, and J. Choi, "A 170 MHz-lock-in-range and −253 dB-FoMjitter 12-to-14.5 GHz subsampling PLL with a 150 μW frequency-disturbance-correcting loop using a low-power unevenly spaced edge generator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 280–282, doi: 10.1109/ISSCC19947.2020.9062921.

[63] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. New York, NY, USA: McGraw-Hill, 2015.

[64] A. Van der Ziel, *Noise; Sources, Characterization, Measurement* (Information and System Sciences Series). Upper Saddle River, NJ, USA: Prentice-Hall, 1970.

[65] A. Mirzaei and A. A. Abidi, "The spectrum of a noisy free-running oscillator explained by random frequency pulling," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 3, pp. 642–653, Mar. 2010, doi: 10.1109/TCSI.2009.2024970.

[66] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 896–909, Jun. 2001, doi: 10.1109/4.924852.

[67] S. Ghaffari, S. A. Chandorkar, S. Wang, E. J. Ng, C. H. Ahn, V. Hong, Y. Yang, and T. W. Kenny, "Quantum limit of quality factor in silicon micro and nano mechanical resonators," *Sci. Rep.*, vol. 3, no. 1, pp. 1–7, Nov. 2013, doi: 10.1038/srep03244.

[68] J. Basu and T. K. Bhattacharyya, "Microelectromechanical resonators for radio frequency communication applications," *Microsyst. Technol.*, vol. 17, nos. 10–11, pp. 1557–1580, Aug. 2011, doi: 10.1007/s00542-011-1332-9.

[69] S. V. Ptashnik, A. K. Mikhailov, A. V. Yastrebov, P. K. Petrov, W. Liu, N. M. Alford, S. Hirsch, and A. B. Kozyrev, "Ferroelectric thin film acoustic devices with electrical multiband switching ability," *Sci. Rep.*, vol. 7, no. 1, pp. 1–10, Nov. 2017, doi: 10.1038/s41598-017-14895-8.

[70] Y. Liu, Y. Cai, Y. Zhang, A. Tovstopyat, S. Liu, and C. Sun, "Materials, design, and characteristics of bulk acoustic wave resonator: A review," *Micromachines*, vol. 11, no. 7, pp. 1–26, 2020, doi: 10.3390/mi11070630.

[71] O. Brand, *Resonant MEMS: Fundamentals, Implementation, and Application*. Hoboken, NJ, USA: Wiley, 2015.

[72] S. A. Chandorkar, M. Agarwal, R. Melamud, R. N. Candler, K. E. Goodson, and T. W. Kenny, "Limits of quality factor in bulk-mode micromechanical resonators," in *Proc. IEEE 21st Int. Conf. Micro Electro Mech. Syst.*, Jan. 2008, pp. 74–77, doi: 10.1109/MEMSYS.2008.4443596.

[73] S. Ghaffari, E. J. Ng, C. H. Ahn, Y. Yang, S. Wang, V. A. Hong, and T. W. Kenny, "Accurate modeling of quality factor behavior of complex silicon MEMS resonators," *J. Microelectromech. Syst.*, vol. 24, no. 2, pp. 276–288, Apr. 2015, doi: 10.1109/JMEMS.2014.2374451.

[74] R. Tabrizian, M. Rais-Zadeh, and F. Ayazi, "Effect of phonon interactions on limiting the f.*Q* product of micromechanical resonators," in *Proc. Int. Solid-State Sens., Actuators Microsyst. Conf. (TRANSDUCERS)*, Jun. 2009, doi: 10.1109/SENSOR.2009.5285627.

[75] S. D. Lambade, G. G. Sahasrabudhe, and S. Rajagopalan, "Temperature dependence of acoustic attenuation in silicon," *Phys. Rev. B, Condens. Matter*, vol. 51, no. 22, pp. 15861–15866, Jun. 1995, doi: 10.1103/PhysRevB.51.15861.

[76] A. Telichko, B. Sorokin, and G. Kvashnin, "UHF acoustic attenuation and quality parameter limits in the diamond based HBAR," in *Proc. Joint Conf. IEEE Int. Freq. Control Symp. Eur. Freq. Time Forum*, Apr. 2015, pp. 94–99, doi: 10.1109/FCS.2015.7138799.

[77] S. Stoffels, E. Autizi, R. Van Hoof, S. Severi, R. Puers, A. Witvrouw, and H. A. C. Tilmans, "Physical loss mechanisms for resonant acoustical waves in boron doped poly-SiGe deposited with hydrogen dilution," *J. Appl. Phys.*, vol. 108, no. 8, Oct. 2010, Art. no. 084517, doi: 10.1063/1.3499319.

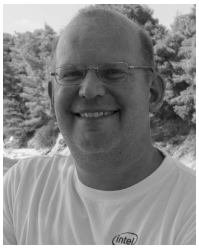
[78] D. Goettler, M. Su, Z. Leseman, Y. Soliman, R. Olsson, and I. El-Kady, "Realizing the frequency quality factor product limit in silicon via compact phononic crystal resonators," *J. Appl. Phys.*, vol. 108, no. 8, Oct. 2010, Art. no. 084505, doi: 10.1063/1.3475987.

[79] B. Hamelin, J. Yang, A. Daruwalla, H. Wen, and F. Ayazi, "Monocrystalline silicon carbide disk resonators on phononic crystals with ultra-low dissipation bulk acoustic wave modes," *Sci. Rep.*, vol. 9, no. 1, pp. 1–8, Dec. 2019, doi: 10.1038/s41598-019-54278-9.

[80] B. Andriyevsky, W. Janke, V. Y. Stadnyk, and M. O. Romanyuk, "Thermal conductivity of silicon doped by phosphorus: *Ab initio* study," *Mater. Sci.-Poland*, vol. 35, no. 4, pp. 717–724, Dec. 2017, doi: 10.1515/msp-2017-0115.

RICHARD HUDECZEK was born in Dachau, Germany, in 1994. He received the B.Sc. and M.Sc. degrees in physics from the Technical University of Munich (TUM), Germany, in 2015 and 2017, respectively, where he is currently pursuing the Ph.D. degree in physics in collaboration with Intel. His master's thesis addressed the optical design and simulation of periodic gallium-nitride nanowire arrays for photocatalytic applications at the Walter Schottky Institute. In 2018, he joined Intel. His current research interests include interdisciplinary semiconductor simulations for highly integrated MEMS devices on advanced CMOS nodes, layout optimization, and lab automation.

EHRENTRAUD HAGER (Graduate Student Member, IEEE) was born in Linz, Austria, in 1991. She received the B.Sc. and Dipl.-Ing. degrees in electronics and information technology from Johannes Kepler University (JKU) Linz, in 2015 and 2017, respectively, where she is currently pursuing the Ph.D. degree. Her master's thesis addressed sub-threshold circuit design solutions and low-power operational amplifiers. In March 2017, she joined the Institute for Integrated Circuits (IIC) and the Christian Doppler Laboratory for Digitally Assisted RF Transceivers for Future Mobile Communications, JKU. Her current research interests include low-power and high-Q circuit design for frequency generation in future transceivers for mobile communications.



PETER BAUMGARTNER (Member, IEEE) received the Dipl.-Phys. degree from the Technical University of Munich, Germany, in 1993, and the Dr.rer.nat. degree in physics from the Walter Schottky Institute, Technical University of Munich, Germany, in 1997. From 1992 to 1997, he was working on the optical and electrical characterization and fabrication of GaAs/AlGaAs nano structures, like single-electron transistors, in-plane-gate transistors, quantum point contacts, and phototransistors. In 1997, he joined the Technology Development Department, Siemens AG, and Infineon Technologies AG, Regensburg, Germany, working on CMOS transistor devices and reliability engineering for embedded flash and CMOS technologies. After different positions in technology and product management for embedded flash microcontrollers, he moved to the field of RF CMOS technologies, in 2004. He joined Intel via the wireless acquisition, where he is currently a Senior Principal Engineer, working on technology enablement for RF, mmW, and high-speed analog applications. He has authored and coauthored more than 35 publications and more than 20 patents.

HARALD PRETL (Senior Member, IEEE) received the Dipl.-Ing. degree in electrical engineering from the Graz University of Technology, Austria, in 1997, and the Dr.techn. degree from Johannes Kepler University (JKU) Linz, Austria, in 2001, for his work on first-generation direct-conversion transceivers for 3G. From 2000 to 2011, he worked as the Director and a Senior Principal Engineer at Infineon Technologies. From 2011 to 2019, he worked as a Senior Principal Engineer at Intel contributing to several generations of cellular RF transceivers and mobile communications platforms, spanning from 2G to 5G, as an Analog Circuit Designer, a Project Lead, and an RF Systems Architect. Since 2015, he has been a Full Professor at the Institute for Integrated Circuits (IIC), JKU, where he is heading the Energy-Efficient Analog Circuits and Systems Group. He has published more than 80 papers at international conferences and journals in the area of RF transceivers and analog circuits, in addition to more than 25 issued or filed patents. His current research interests include cellular transceivers, wireless sensor networks, micro-power RF SoC for medical applications, and mm-wave circuits for 6G and advanced radar. He is a member of the Austrian Electrotechnical Association (OVE) and the Technical Program Committee (TPC) of the ISSCC, from 2010 to 2012. He was a co-recipient of the first place in the 2015 MTT-S PAWR Student Paper Competition, the 2019 ReSMiQ Best Paper Award from the IEEE NEWCAS Conference, the 2019 APMC Student Prize, and the 2021 ISCAS Best Paper Award. He was also a co-recipient of the Intel Achievement Award, in 2019.