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Impact of P/E Stress on Trap Profiles in Bandgap-Engineered Tunneling Oxide of 3D NAND Flash Memory

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ABSTRACT The quantitative characteristics of traps created in the bandgap-engineered tunneling oxide (BE-TOX) layer and block layer after program/erase (P/E) stress-cycling in a 3D NAND flash memory were investigated. The trap spectroscopy by charge injection and sensing technique was used to obtain the distribution of traps in these layers. In the BE-TOX layer, significant traps were generated around 1.3 eV in the nitrogen-doped layer (N1) and increased by 48% in the fresh cell after P/E stress-cycling. The H bonds in the N1 are more likely to break during the stress-cycling and create neutral $\equiv SiO^{\bullet}$ traps. In the block layer, however, trap generation was negligible after stress-cycling.

INDEX TERMS 3D NAND flash memory, bandgap-engineered tunneling, program/erase cycling, trap profile, TSCIS.

I. INTRODUCTION

The three-dimensional (3D) NAND flash memory has various applications, including consumer electronics, autonomous vehicles, and data centers, owing to its low bit cost and high storage density [1], [2]. Thus, multilevel operation and cell scaling have been intensively developed for the 3D NAND flash memory to increase its density and reduce its manufacturing cost. These developments require a considerably tighter distribution of the cell threshold voltage (V_{TH}) and high-immune and retention characteristics. A bandgap-engineered tunneling oxide (BE-TOX) layer and block layer have been introduced to enhance the program/erase (P/E) speed and retention reliability, replacing the conventional SiO_2 layer [3], [4].

The performance of the 3D NAND flash memory is limited by the number of P/E operations that create defects in dielectric layers [5], [6]. Previous results described trap generation based on stress conditions and provided minimal information on origin of traps created in a cell [5], [6]. A detailed analysis of trap generation in dielectric layers is crucial to develop a high-efficient barrier structure and enhanced memory performance.

Herein, we characterized the traps generated in the BE-TOX layer and block layer of a 3D NAND flash memory after P/E stress-cycling with the help of technology computer-aided design (TCAD) simulation and the trap spectroscopy by charging injection and sensing (TSCIS) technique [7]–[9]. First, simulation was performed to match the measured characteristics and obtain the relevant electric field for the trap spectroscopy. Second, trap profiles were qualitatively designed in terms of energy using TSCIS. Lastly, a quantitative model was applied to correlate trap generation with the stress condition and process quality.

II. EXPERIMENTS AND SIMULATIONS

A. DATA RETENTION CHARACTERISTICS

Fig. 1(a) shows a schematic of the 3D NAND flash memory consisting of a dielectric filler, a poly-Si channel (CH), BE-TOX (O1/N1/O2) layer, charge trap layer (CTL), and block layer (BOX/H.K). Fig. 1(b) shows the retention characteristics of fresh and cycled cells at 25 °C. For the P/E stress-cycling, the program (18 V, $t_{PGM} = 50\ \mu s$) and erase (−17 V, $t_{ERS} = 1$ ms) biases were repeatedly applied to the gate

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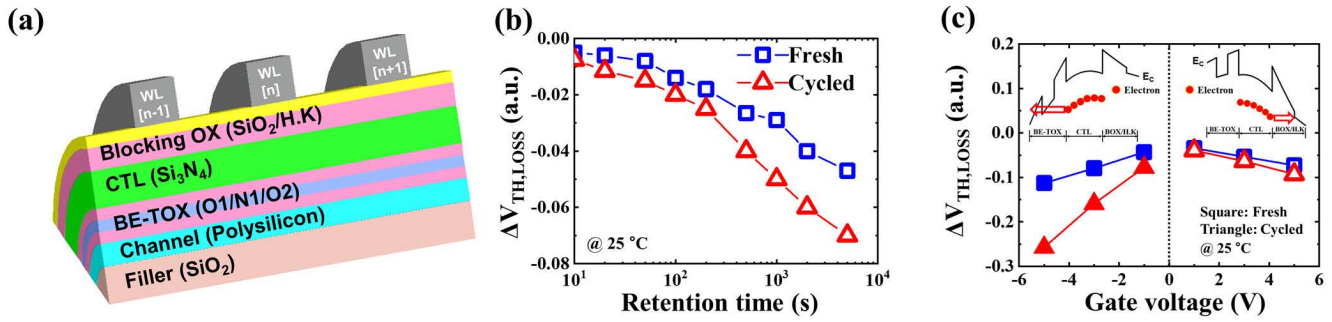

FIGURE 1. (a) Schematic of the 3D NAND flash memory and (b) $\Delta V_{TH,LOSS}$ without gate voltage at 25 °C for 5000 s. (c) Retention experiment for fresh and cycled cells with gate voltage at 25 °C for 500 s.

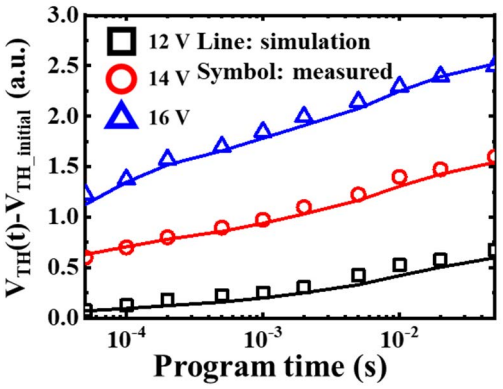

FIGURE 2. Threshold voltage measured (symbol) and simulated (line) on the 3D NAND flash memory during program operation.

electrode for 1000 cycles. The threshold voltage variation ($\Delta V_{TH,LOSS} = V_{TH,time} - V_{TH,0sec}$) was caused by the vertical and lateral charge losses. The worse retention of the cycled cell was attributed to the vertical charge loss due to trap generation in the BE-TOX layer after P/E stress-cycling [5], [10].

Fig. 1(c) shows the $\Delta V_{TH,LOSS}$ with various gate voltages in a programmed state for fresh and cycled cells. A positive gate bias preferentially accelerates the charge loss through the gate-side (GS) region, whereas a negative bias enhances the charge loss through the channel-side (CS) region. A higher $\Delta V_{TH,LOSS}$ with a negative bias indicates that the trap generation in the BE-TOX layer is more severe than that in the block layer and the trap-assisted tunneling and detrapping toward the CS region could be the dominant mechanism.

B. TSCIS MEASUREMENT AND SIMULATION

Fig. 2 shows the change of V_{TH} as a function of program time and compares it with the TCAD simulation; the density-gradient model was included to consider the quantum effect. The doping-dependent mobility model and an incomplete ionization model were used to calibrate the simulation and measurement data. In addition, the Shockley-Read-Hall generation-recombination model was employed to explain the capture and emission of carriers. The calibrated program speed data were well matched to the measured ones. The

TABLE 1. Model parameter notation.

Physical meaning	Region	Symbol	Value
Barrier height	CH/O1	ϕ_1	3.1 eV [11]
	O1/N1	ϕ_2	0.7 eV [12]
	H.K/gate	ϕ_3	3.5 eV [13]
Dielectric constant	O1	ϵ_{O1}	3.9 [14]
	N1	ϵ_{N1}	6.5 [12, 15]
	CTL	ϵ_{CTL}	7.5 [13]
	H.K	ϵ_{HK}	9.5 [11]
Effective mass	O1	m_{O1}	0.42 m_0 [15]
	N1	m_{N1}	0.42 m_0 [15]
	CTL	m_{CTL}	0.5 m_0 [16]
	H.K	$m_{H.K}$	0.22 m_0 [11]
Electron capture cross section	O1	σ_{O1}	1×10^{-15} cm^2 [17]
	N1	σ_{N1}	1×10^{-15} cm^2 [17]
	CTL	σ_{CTL}	1×10^{-14} cm^2 [18]
	H.K	σ_{HK}	5×10^{-15} cm^2 [19]

parameters used for the simulation are listed in Table 1. TCAD simulation was performed to obtain the energy band and relevant electric field, which were used to extract the trap levels in the BE-TOX layer and block layer using TSCIS.

The trap energy level and trap depth were extracted by varying charging voltage (V_{CHRG}) and charging time (t_{CHRG}). The V_{CHRG} and the t_{CHRG} determine the trap levels from the E_C of N1 and the distance from the channel interface based on Shockley-Read-Hall (SRH) statics and WKB approximation (T_{WKB}) for tunneling probability [7]–[9]. During the TSCIS charging period, the electric field in the dielectric layer was continuously changed by the electrons captured in the trap. These trapped charges also affected the tunneling probability and capture rate of the trap. Thus, the electric fields in the dielectric layers were recalculated using the numerical Poisson solver considering the captured electrons.

The TSCIS charging condition should be carefully chosen to avoid any trap generation during the charging period. Negligible differences were observed in fully discharged V_{TH} – initial state V_{TH} and the subthreshold swing values

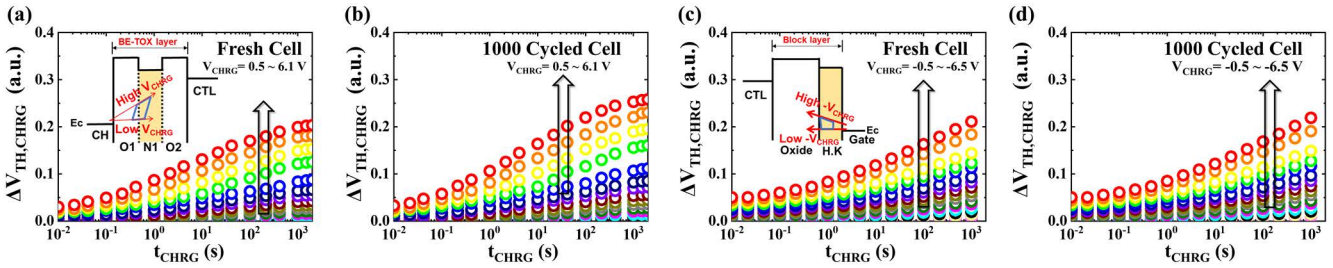

FIGURE 3. Variation of $\Delta V_{TH,CHRG}$ as a function of t_{CHRG} in (a) a fresh cell and (b) a 1000 cycled cell for CS-TSCIS, and in (c) a fresh cell and (d) a 1000 cycled cell for GS-TSCIS.

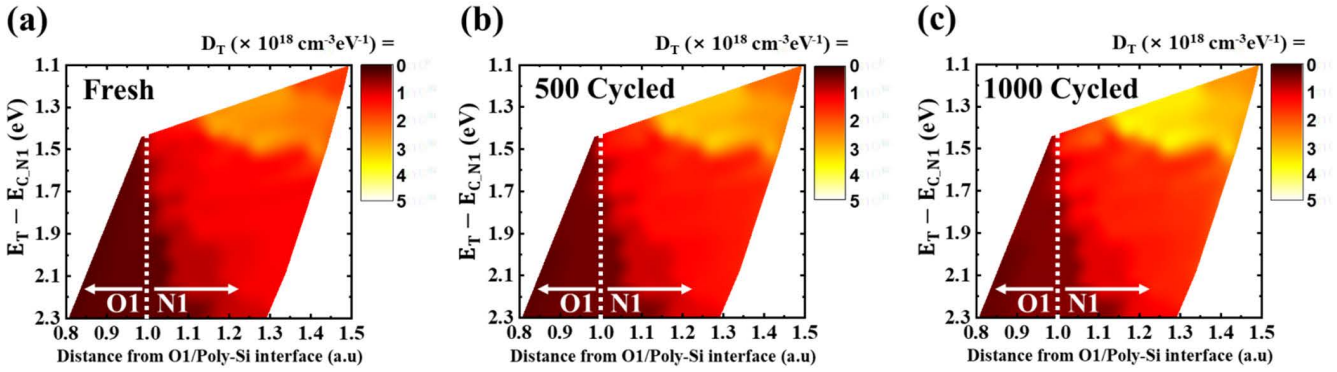

FIGURE 4. Trap spectroscopy in the BE-TOX layer of (a) a fresh, (b) a 500-cycled, and (c) a 1000-cycled cell.

with V_{CHRG} up to 6.1 V and t_{CHRG} up to 10^3 s for channel-side TSCIS (CS-TSCIS), which confirmed a negligible trap generation in the BE-TOX layer and at the O1/CH interface during the charging period [20]. Gate-side TSCIS (GS-TSCIS) also observed minimal trap generation with V_{CHRG} up to −6.5 V.

Fig. 3 shows the measured V_{TH} shifts ($\Delta V_{TH,CHRG}$) as functions of V_{CHRG} and t_{CHRG} for fresh and 1000-cycled cells, respectively. Initially, the I_D-V_G curve of the fresh cell was measured, and then V_{CHRG} was applied to the gate during 0.01 to 2000 s. At the end of a charging time, the constant V_{sense} was biased to measure the drain current, which was transferred to $\Delta V_{TH,CHRG}$ based on the initial I_D-V_G curve. Before increasing V_{CHRG}, V_G was grounded to relax electron traps. In GS-TSCIS, the same procedure was performed except that the negative V_{CHRG} was applied to the gate, as shown in Fig. 3(c) and (d). The insets in Fig. 3(a) and (c) show the profiled regions that were determined by V_{CHRG} and t_{CHRG} in TSCIS technique.

III. RESULTS AND DISCUSSION

Fig. 4 shows the trap maps obtained via the CS-TSCIS technique. The energy level of the trap was calculated from the conduction band (E_{C_N1}) of N1. The red–yellow region shows the maximum trap density for a fresh cell. Notably, as P/E stress was applied, the trap density (D_T) with the energy levels of 1.3 to 1.5 eV increased in the N1 region, and negligible trap creation in other O1/N1 regions was observed.

Fig. 5(a) shows the average trap density (D_{T_AVG}) as a function of the distance from the O1/Poly-Si interface and the energy from E_{C_N1}. The energy level was extracted by applying Gaussian fitting curves. For a fresh cell, the extracted peak value of D_{T_AVG} was obtained as 2.4×10^{18} $cm^{-3} \cdot eV^{-1}$ with a 1.34 eV energy level by applying Gaussian fitting curves. The D_{T_AVG} value was very similar to that of previous noise measurement results [21], [22]. It can be seen that the P/E stress-cycling could increase the trap density and slightly change the energy level of the peak trap density.

There are two main electron traps in a nitrogen-doped oxide (N1): $\equiv Si_2N^{\bullet}$ and $\equiv SiO^{\bullet}$ [23]. The former is a shallow trap with an energy level of less than 1.0 eV from E_{C_N1}, and the energy level of the latter is typically in the range of 1.3 to 1.9 eV from E_{C_N1} [23]–[25]. The energy level of the peak trap density is similar to that of $\equiv SiO^{\bullet}$, as shown in Fig. 5(a).

According to the following reaction, the trap generation in a stressed cell could be the break of a hydrogen (H) atom bound to $\equiv$SiOH [23], [26].

$$\equiv \mathrm{SiOH} \rightarrow \equiv \mathrm{SiO}^{\bullet} + \mathrm{H} \tag{1}$$

Fig. 5(b) shows the variation of Δ_{T_AVG}, defined as $(D_{T\_AVG,1000cycles} - D_{T\_AVG,fresh})/D_{T\_AVG,fresh}$, with P/E stress. With 1000 cycles of P/E stress, the peak Δ_{T_AVG} of 48% at 1.3 eV is obtained, which rapidly decreases as the trap level increases. The majority of the P/E stress-induced traps could be $\equiv SiO^{\bullet}$, located at approximately 1.3 eV using (1),

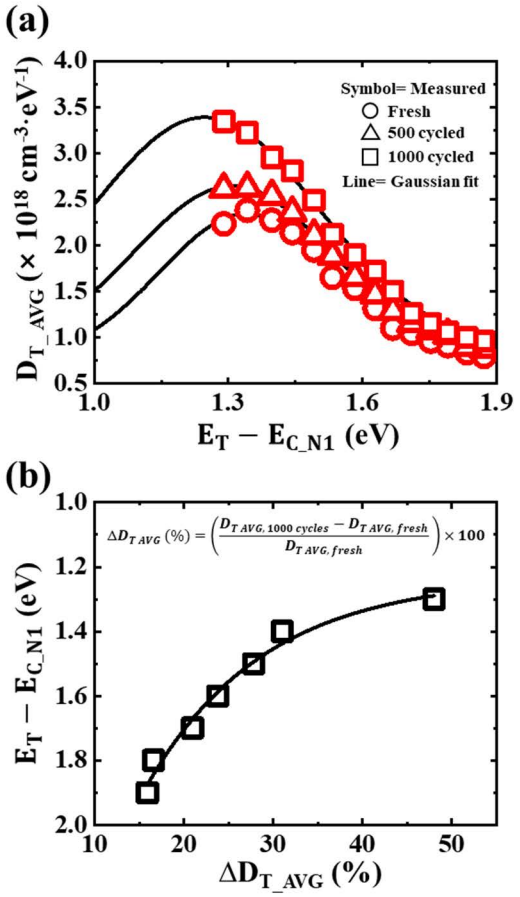

FIGURE 5. (a) Average trap density (D_{T_AVG}) as a function of the energy level from N1 band edge with different P/E cyclings. (b) The dependence of trap generation on the energy level for 1Kth P/E cycled cell.

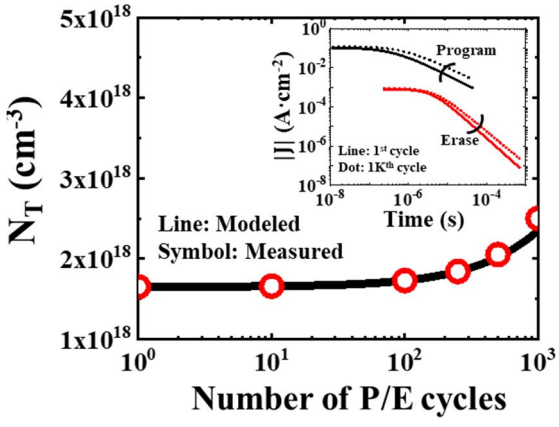

FIGURE 6. Measured and modeled N_T with the repeated P/E stress-cycling. (Inset) The program/erase tunneling current densities flowing through the BE-TOX layer for the first and 1Kth cycle using the TCAD simulation.

and a significant cause of the degradation of retention in a stressed cell.

Fig. 6 shows the variation in the accumulated total trap density ($N_{T,N}$) as a function of the number of P/E cycles. Initial N_T was obtained by integrating the Gaussian profile

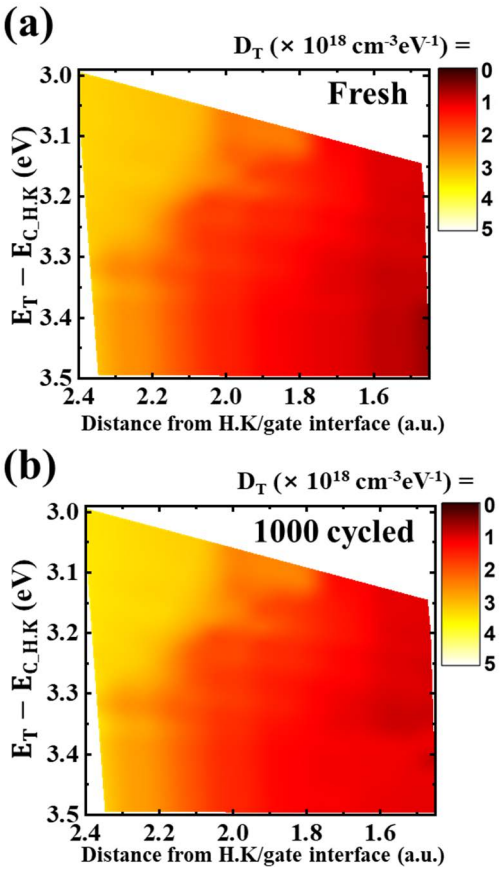

FIGURE 7. Trap spectroscopy in the H.K layer of (a) a fresh cell and (b) a 1000-cycled cell.

of D_{T_AVG}. The tunneling current density (J) during P/E stress-cycling was obtained using TCAD simulation. The P/E current densities through the BE-TOX layer became large as the P/E cycle increased, as shown in the inset of Fig. 6. Also, the J decreases continuously as time evolves in a P/E cycle.

To correlate the trap generation in the BE-TOX layer with the P/E stress-cycling, the injected charge fluence ($(Q_{inj,N}(l)$), the newly created traps ($\Delta N_{T,N}(l)$) and the $N_{T,N}$ for N^{th} P/E cycle were modeled under current stress conditions as follows [27], [28]:

$$Q_{\mathrm{inj},N}(l) = \left(\frac{N_{T,N}(l-1)}{K_{pr} \cdot J^{\beta}_{stress,N}(l)}\right)^{\frac{1}{\alpha}} + \int_{t}^{t+\Delta t} J_{stress,N}(l)\, dt \tag{2}$$

$$\Delta N_{T,N}(l) = K_{pr} \cdot J^{\beta}_{stress,N}(l) \cdot \left(Q^{\alpha}_{inj,N}(l) - \left(\frac{N_{T,N}(l-1)}{K_{pr} \cdot J^{\beta}_{stress,N}(l)}\right)\right) \tag{3}$$

$$N_{T,N} = \sum_{l=0}^{l=L} \Delta N_{T,N}(l) + N_{T,N-1}(L) \tag{4}$$

where l is a counter from $l = 0$ to $l = L = t_{PGM}/\Delta$ t in a P/E step, N is the number of P/E cycles, K_{pr} is a constant depending on the dielectric thickness and processing

conditions, $J_{stress,N}$ is the simulated tunneling current density flowing through the BE-TOX layer, α and β are the dielectric quality evaluation parameters.

For the program and erase stress, $\alpha_{pr} = 0.6$, $\beta_{pr} = 0.23$, and $K_{pr} = 1.2 \times 10^{21}$ and $\alpha_{er} = 0.50$, $\beta_{er} = 0.65$, and $K_{er} = 3.93 \times 10^{21}$ were extracted, respectively. These values were very similar to those found in previous results [27], [28].

Fig. 7 shows the trap maps with P/E stress for the high-k dielectric in the blocking layer. The D_T value of approximately 10^{18} $cm^{-3} \cdot eV^{-1}$ was obtained in a fresh cell. The extracted traps were almost uniformly distributed along the trap energy axis. As shown in Fig. 7(b), the P/E stress-cycling did not affect trap generation in the high-k blocking layer.

IV. CONCLUSION

After P/E stress-cycling, the trap generation in both the BE-TOX and block layers was characterized using the TSCIS technique, revealing that traps in the BE-TOX layer were intensively generated around 1.3 eV in N1 and increased by 48% in the fresh cell. Among several trap candidates in the nitrided layer, the neutral $\equiv SiO^{\bullet}$ trap could be a major one considering the energy from the trap profiles. The quantitative model of trap generation was also evaluated based on the stress conditions and quality of dielectric layers. In the blocking layer, negligible trap generation was characterized with the P/E stress-cycling.

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