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A 3-3.7GHz Time-Difference Controlled Digital Fractional-N PLL With a High-Gain Time Amplifier for IoT Applications

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ABSTRACT This paper presents analyses of jitter and reference spur of a digital PLL using a phase-frequency detector (PFD) and a time amplifier (TA). In the PFD-TA PLL, the TA amplifies a phase error between a reference clock and a divided feedback clock. The amplified pulse signals modulate the digitally controlled oscillator (DCO) frequency. The TA input-referred jitter limits the minimum PFD-TA PLL output jitter in case of the low DCO and reference clock jitter. However, the PFD-TA PLL achieves a lower output jitter than the BBPLL especially when the input noise is worsened by the poor DCO, which, indeed, is common in low-power and IoT applications for lower cost and power. The reference spur caused by the path mismatches of the proposed DCO modulation is analyzed by Fourier Series, and implementing the high-gain (>100) TA reduces the reference spur with the smaller DCO modulating signal distortion. To assist the narrow input dynamic range (<30ps) of the TA, a 7-bit phase interpolator (PI) is implemented to fractional frequency divider with a PI nonlinearity calibration. The theoretical predictions are compared with the behavioral simulations and verified in measurements where the chip is fabricated in a 40 nm CMOS process, and the PFD-TA PLL consumes 5 mW from a 1.1 V supply.

INDEX TERMS Time amplifier (TA), digitally controlled oscillator (DCO), digital phase-locked loop (PLL), PLL jitter analysis, reference spur, phase interpolator (PI) nonlinearity calibration.

I. INTRODUCTION

Recently, sub-1 GHz band wireless technology provides long-range network connectivity for IoT (Internet of Things) applications because the low frequencies below 1 GHz have better transmissivity than higher frequencies [1]. Especially for battery-powered IoT sensor applications [2], the power reduction, as well as cost reduction by virtue of a small die area, become essential in all RF building blocks.

Since the digital circuits have the advantage of reducing the chip area and power consumption through a low-voltage technology, all-digital PLLs with a time-to-digital converter (TDC) have been studied [3]–[11]. In the fractional-N TDC-based PLL, the high-resolution TDC with a wide dynamic range is required to cover an entire DCO cycle, which results in a large area and power. To reduce the power consumption and the design complexity, the digital-to-time converter (DTC) and bang-bang phase detector (BBPD) replace the TDC [12]–[15]. But the output of BBPD is discrete, and the quantization noise is very sensitive to the input noise that is mostly characterized by the reference clock and DCO jitter. So, the resolution of the DTC should be lower than the input noise to hold on to the random-noise regime for fractional-N operation [15].

Recent studies demonstrated sub-sampling PLLs (SSPLLs) where the phase error is linearly sampled and controls the voltage-controlled oscillator (VCO) frequency with no quantization noise [16]–[20]. The SSPLLs have achieved low in-band phase noise by using a sample-and-hold circuit and eliminating a divider from the PLL feedback path. However,

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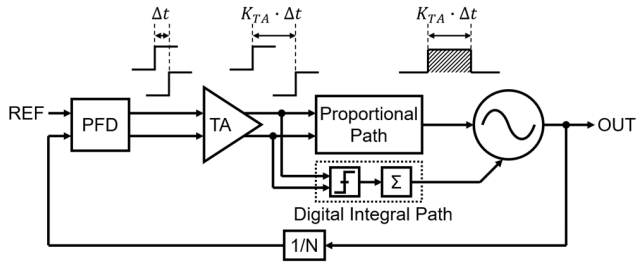


FIGURE 1. Block diagram of the time-difference controlled digital PLL with PFD-TA.

the SSPLLs alone may be a false lock to an uncertain multiple of the reference frequency due to an arbitrary phase offset, and then the SSPLL requires an additional frequency-locked loop (FLL) to avoid the false lock [18]–[20].

To utilize the advantages of both linear gain of phase-frequency detector (PFD) and digital implement, a charge pump (CP)-based hybrid PLLs have been studied [21]–[24]. The proportional path that consists of the PFD and the CP has no quantization noise by TDC or BBPD, and by virtue of the digital integral path, the hybrid PLL has a compact and scalable design. But the noise of the CP makes the PLL output noise worse, and to reduce the CP noise, a large current for the CP is needed that leads to large power consumption.

In this paper, a time amplifier (TA)-based digital PLL is proposed [25]. Conventionally, the TA is used to improve the TDC resolution of the PLL [4], [5], [9], or to reduce the CP noise with low power consumption [26]. However, in the proposed PFD-TA PLL, a phase error that is amplified by the TA modulates directly the digitally controlled oscillator (DCO) as a time-difference in the proportional path, and the integral path is implemented by digital circuit as shown in Fig. 1. By exploiting the high-gain (>100) of the TA, the reference spur by mismatches from the proposed DCO frequency control can be suppressed.

Section II describes the time-difference control structure in the proportional path and derives a linearized model of the PFD-TA PLL, and Section III analyzes the input-referred jitter and output jitter of the PLL. The jitter analysis provides the optimum TA gain, which minimizes PLL output jitter, and estimates the TA jitter that the PFD-TA PLL can achieve lower phase noise than the BBPLL. The reference spur level of the PFD-TA PLL is calculated in Section IV, and the spur analysis can estimate the reference spur level by the mismatches in the proposed proportional path. The detailed PLL structures are depicted in Section V. After all, the calculated phase noise and jitter are compared with the measurement results in Section VI. The conclusion of this work is stated in Section VII.

II. TIME-DIFFERENCE CONTROL OF THE PFD-TA PLL

In this section, the specific structure of the proportional path of the PFD-TA PLL is described to derive effective DCO period gain for the linearized model. Since the PLL blocks

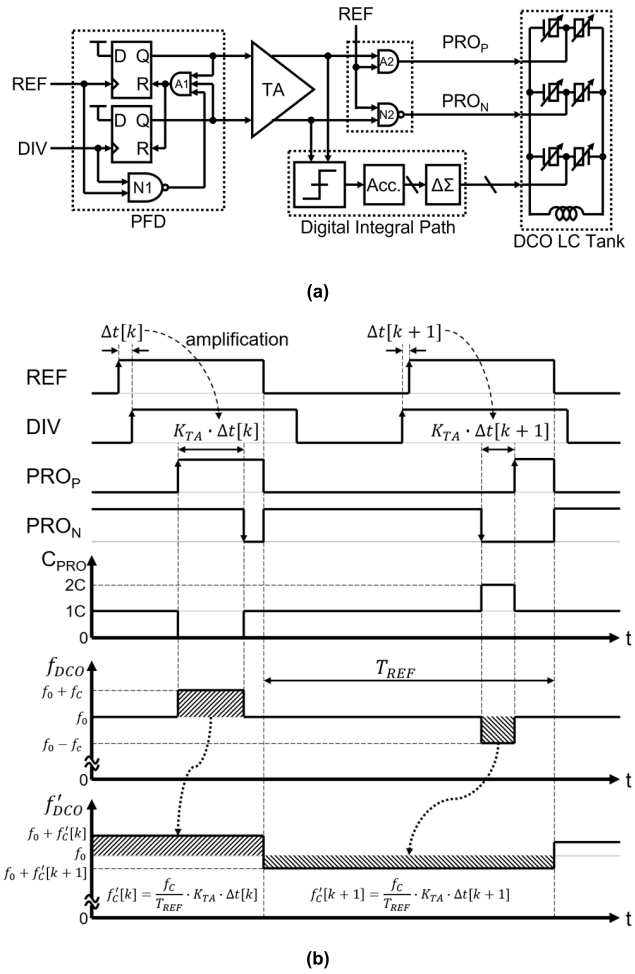


FIGURE 2. (a) Block diagrams and (b) simplified control signals of the proportional path with TA gain in time-domain.

from the feedback divider to the DCO are synchronous to the reference clock in a locked state, the time-difference DCO frequency control that has the pulse-shaped signals in the proportional path is approximated to linear frequency control.

A. PROPORTIONAL PATH WITH TA

Fig. 2 shows the DCO control path of our proposed time-difference-controlled DCO. As shown in Fig. 2(a), the PLL implements the PFD-TA-based proportional path that adjusts the capacitance of the LC tank of the DCO over the time-difference. *REF* is the reference clock pulse wave, and *DIV* is the divided DCO clock from the multi-modulus divider (MMDIV) and phase interpolator (PI) [27], [28]. Since the TA manipulates the asymmetric propagation delays of latches [29], the TA input voltage states should not be changed during the latch regeneration time to generate TA outputs. For the proper TA operation, the two input NAND (*N1*) and three-input AND (*A1*) gates stabilize the TA inputs by arranging the *Reset* timing of the flip-flop with the PFD input signals. After the TA amplifies the time difference between the rising edges of *REF* and *DIV*, the separately

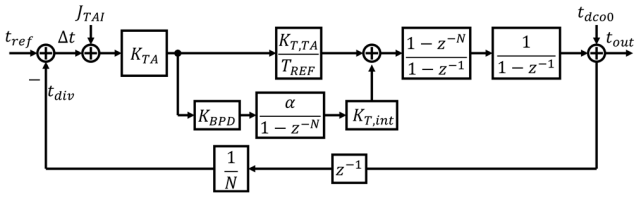


FIGURE 3. A linearized model of the PFD-TA PLL.

REF is used by two gates (*A2* and *N2*), generating PRO_P and PRO_N. For DCO frequency modulation, PRO_P keeps one TA output intact, and PRO_N inverts the other output of TA. The two signals turn ON/OFF the two capacitor tanks of the DCO, respectively [21]. The BBPD in the digital integral path receives the TA outputs that relieve the time offset between the proportional path and the integral path.

Fig. 2(b) shows how PRO_P and PRO_N in the proportional path modulate the DCO frequency. The DCO tuning capacitance, C_{PRO}, is controlled by PRO_P and PRO_N. Ideally, C_{PRO} is set to one of three values that are 0, C, and $2C$, where C is the capacitance variation for each control signal, and the DCO frequency, f_{DCO}, become $f_0 - f_C$, f_0 and $f_0 + f_C$, respectively, where f_C is the DCO frequency resolution for the capacitance C variation.

B. LINEARIZED MODEL OF THE PFD-TA PLL

The studies in BBPLL for accurate jitter estimation are based on a discrete-time domain model [30]–[34]. Similarly, we also present the discrete-time linearized model of PFD-TA as shown in Fig. 3 to figure out the noise and spur characteristics of the PFD-TA PLL.

The linearized model in Fig. 3 is synchronous to the DCO clock domain, where $z = \exp[j2\pi f/f_0]$ and f_0 is the nominal DCO frequency. Typically, the PLL operates in two clock domains of the DCO and the reference in a locked state, and the DCO output phase is down-sampled by the reference clock in the feedback path. To model the PLL in the DCO clock domain only, the down-sampling by reference is simply modeled by $1/N$ neglecting the folding effects [34] because the output is slowly varying narrow-band information. The additional delay of z^{-1} in the feedback path in Fig. 3 is needed to properly align the reference edge and the divider output edge [34], [35] so that it reflects the causality. Since the delay by one DCO cycle is short, the phase margin degradation by the additional delay is negligible by seeing only 0.1-degree degradation. The TA input-referred noise is denoted as J_{TAI} and the time amplification gain of TA is denoted as K_{TA}. t_{dco0} is the integrated noise of the DCO period noise, T_{dco0}. The integral feedforward path is obtained from the BBPLL linearized model, where K_{BPD} is BBPD gain and α is the integrator gain of the digital loop filter (DLF). The DCO code-to-period gain of the integral path is $K_{T,int}$.

The linearized models of the DCO period time gain of the BBPLL and PFD-TA PLL in the proportional path are compared in the following. From the BBPLL model in [34], a DCO period time deviation per 1 LSB is $K_{T,BB}$. Since the BBPD output is $sgn(\Delta t)$, where Δt is a time difference between *REF* and *DIV*, the DCO period variation by frequency control word (FCW) in BBPLL is:

$$\begin{aligned}\Delta T_{DCO,BB} &\approx \beta \cdot sgn(\Delta t) \cdot K_{T,BB} \\ &\approx \beta \cdot K_{T,BB} \cdot K_{BPD} \cdot \Delta t \end{aligned} \tag{1}$$

where β is the proportional digital gain of the DLF. And the period variation of the divided feedback clock in BBPLL is:

$$\begin{aligned}\Delta T_{DIV,BB} &\approx \Delta T_{DCO,BB} \cdot \frac{T_{REF}}{T_{DCO}} \\ &\approx N \cdot \beta \cdot K_{T,BB} \cdot K_{BPD} \cdot \Delta t \end{aligned} \tag{2}$$

where N is the division factor of the MMDIV and $T_{REF} = N \cdot T_{DCO}$.

While, in the PFD-TA PLL, $K_{T,TA}$ is a DCO period time gain where $K_{T,TA} = f_C/f_0^2$ from Fig. 2(b), then the DCO period variation by FCW:

$$\Delta T_{DCO,TA} \approx sgn(\Delta t) \cdot K_{T,TA} \tag{3}$$

Unlike BBPLL, where the frequency control is effective during a whole reference cycle, in the PFD-TA PLL, only the fractional time out of one reference cycle adjusts the DCO frequency according to the time difference between PRO_P and PRO_N, which is $K_{TA} \cdot \Delta t$ as shown in Fig. 2(b). The period variation of the divided feedback clock in the PFD-TA PLLs is:

$$\begin{aligned}\Delta T_{DIV,TA} &\approx \Delta T_{DCO,TA} \cdot \frac{|\Delta t| \cdot K_{TA}}{T_{DCO}} \\ &\approx \frac{N \cdot K_{TA} \cdot K_{T,TA} \cdot \Delta t}{T_{REF}} \end{aligned} \tag{4}$$

In order to make one-to-one comparison easier between (2) in BBPLL and (4) in PFD-TA PLL, the effective DCO period gain, K_T', in the PFD-TA PLL is defined by the following:

$$K_T' = \frac{K_{T,TA}}{T_{REF}} \tag{5}$$

By defining the effective DCO period gain as K_T' in the proportional path, our PFD-TA PLL model becomes similar to the BBPLL analysis in [34]. T_{ref} in the denominator in (5) finds the effective DCO period gain during one reference cycle and is more easily understood in Fig. 2(b).

III. JITTER ANALYSIS OF THE PFD-TA PLL

In this section, an analysis of the input and output jitter of the PFD-TA PLL is presented by using the linearized model in Fig. 3 that is deployed from the discrete time domain model of the BBPLL in [34]. It helps to predict the optimum loop filter parameter, such as K_{TA}, $K_{T,TA}$, K_{BPD} or α, and it affects the total output jitter accordingly.

A. INPUT REFERRED JITTER OF THE PFD-TA PLL

From Fig. 3, the input-referred jitter of the PFD-TA PLL, $\sigma_{\Delta t_{TA}}$, can be given as follows with a loop parameter $\chi = N \cdot K_{TA} \cdot K_{T,TA} \cdot f_{REF}$:

$$\sigma^2_{\Delta t_{TA}} = \frac{2}{2-\chi}\sigma^2_{t_{ref}} + \frac{\chi}{2-\chi}\sigma^2_{TAI} + \frac{N}{\chi\,(2-\chi)}\sigma^2_{T_{dco0}} \quad (6)$$

where $\sigma_{t_{ref}}$ and σ_{TAI} are absolute jitters of the reference clock and TA input-referred noise, respectively, and $N\sigma^2_{T_{dco0}}$ is N-period jitter variance of the DCO. σ_{TAI} term replaces the BBPD quantization noise term of [34].

Since the digital integral path employs BBPD, a zero frequency of the PFD-TA PLL can be estimated as follows with $\sigma_{\Delta t_{TA}}$:

$$f_z \approx \frac{1}{2\pi} \cdot \frac{K_{T,int} K_{BPD} \alpha}{K_{T,TA}} = \sqrt{\frac{1}{2\pi^3}} \cdot \frac{K_{T,int}}{K_{T,TA}} \cdot \frac{\alpha}{K_{TA}} \cdot \frac{1}{\sigma_{\Delta t_{TA}}} \quad (7)$$

where K_{BPD} is BBPD gain from [36]. f_z can be adjusted with the rate of K_{TA} and α, and (7) aids the design of the integrator in the DLF.

B. OPTIMUM PROPORTIONAL PATH GAIN

From (6), for the given noise sources, there is an optimum χ, to minimize $\sigma_{\Delta t_{TA}}$ where χ changes according to K_{TA} and $K_{T,TA}$. However, the proposed time-difference control needs large K_{TA} to reduce the reference spur, which will be explained in Section IV. And according to our simulation results, σ_{TAI} is found to be roughly proportional to $\sqrt{K_{TA}}$ in our latch-based TA due to the long regeneration time. Thus, there is a trade-off between noise and spur performance of the PFD-TA PLL. The dependence of σ_{TAI} on K_{TA} is not the limiting factor, which can be regarded as the constant when figuring out σ_{TAI} which makes the noise performance of the PFD-TA PLL lower than that of the BBPLL for the given $\sigma_{t_{ref}}$ and $\sigma_{T_{dco0}}$. Then, the optimum χ, χ_{opt}, can be derived as follows:

$$\chi_{opt} = -\gamma + \sqrt{\gamma^2 + 2\gamma} \quad (8)$$

where

$$\gamma = \frac{N\sigma^2_{T_{dco0}}}{2\left(\sigma^2_{t_{ref}} + \sigma^2_{TAI}\right)} \quad (9)$$

As shown in (8) and (9), χ_{opt} changes according to all three noises, which is contrast to the BBPLL that the optimum value of the DLF proportional path coefficient does not depend on the reference clock noise [33], [34].

C. OPTIMUM JITTER COMPARISON WITH BBPLL

Replacing the BBPD with the PFD-TA can eliminate the quantization noise in the proposed PLL proportional path, however, the noise by the high-gain TA can deteriorate the PLL output noise. To disclose the noise conditions that makes the optimum jitter of the PFD-TA PLL lower than that of the BBPLL, the PFD-TA PLL and BBPLL input-referred jitters are arranged by the reference clock and DCO noises.

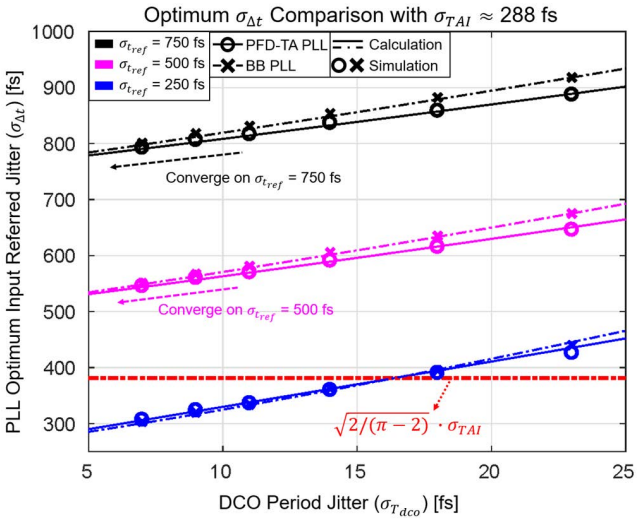


FIGURE 4. Simulated and calculated optimum input-referred jitter comparison between BBPLL and the PFD-TA PLL.

The optimum input-referred jitters of the PFD-TA PLL and the BBPLL are compared in Fig. 4 with the simulated results by the Verilog behavior model. The gaussian jitter is constructed by adding eight random number sequences to properly model the TA, the reference, and the DCO noise. The simulated optimum jitter performance for the given $\sigma_{t_{ref}}$ and $\sigma_{T_{dco0}}$ are found by sweeping the proportional path gain, such as K_{TA} in the PFD-TA PLL and β in the BBPLL, respectively. The simulation parameters are that $N = 112$, $f_{REF} = 32$ MHz, $\sigma_{TAI} \approx 288$ fs, $K_{T,TA} \approx 483$ fs and $K_{T,BB} \approx 1.25$ fs. The calculated optimum input-referred jitter of the PFD-TA PLL, $\sigma_{\Delta t_{TA}}$, can be obtained by substituting (8) to (6):

$$\sigma^2_{\Delta t_{TA}} = \left(\sqrt{\frac{N\sigma^2_{T_{dco0}}}{4}} + \sqrt{\frac{N\sigma^2_{T_{dco0}}}{4} + \sigma^2_{t_{ref}} + \sigma^2_{TAI}}\right)^2 - \sigma^2_{TAI} \quad (10)$$

And from [34], the minimum variance of the input noise of the BBPLL, $\sigma_{\Delta t_{BB}}$, can be written as follows:

$$\sigma^2_{\Delta t_{BB}} = \frac{\pi}{2} \cdot \left(\sqrt{\frac{N\sigma^2_{T_{dco0}}}{4}} + \sqrt{\frac{N\sigma^2_{T_{dco0}}}{4} + \frac{2}{\pi}\sigma^2_{t_{ref}}}\right)^2 \quad (11)$$

By subtracting (10) from (11), inequality can be induced to figure out σ_{TAI} value that $\sigma_{\Delta t_{TA}}$ is smaller than $\sigma_{\Delta t_{BB}}$:

$$\sigma_{TAI} < \frac{\sqrt{\pi\,(\pi-2)}}{2} \cdot \left(\sqrt{\frac{N\sigma^2_{T_{dco0}}}{4}} + \sqrt{\frac{N\sigma^2_{T_{dco0}}}{4} + \frac{2}{\pi}\sigma^2_{t_{ref}}}\right) \quad (12)$$

Substituting (11) into (12), the inequality reduces to

$$\sigma_{TAI} < \sqrt{\frac{\pi-2}{2}}\sigma_{\Delta t_{BB}} \approx \frac{\sigma_{\Delta t_{BB}}}{\sqrt{2}} \tag{13}$$

(13) implies that for superior performance by PFDTA PLL over BBPLL, the variance of the TA input-referred jitter should be designed to be smaller than half of the variance of the BBPLL input-referred jitter. Assuming that $\sigma_{t_{ref}} \rightarrow 0$ provides the stricter condition as:

$$\sigma_{TAI} < \frac{\sqrt{\pi\,(\pi-2)\,N}}{2}\sigma_{T_{dco0}} \approx \sqrt{N}\sigma_{T_{dco0}} \tag{14}$$

(14) indicates that the PFD-TA PLL has lower noise than the BBPLL when σ_{TAI} is lower than the N-period jitter of the DCO for any noise condition of the reference clock.

The plot shows optimum $\sigma_{\Delta t_{TA}}$ and $\sigma_{\Delta t_{BB}}$ according to $\sigma_{T_{dco0}}$ which is indicated on the horizontal axis from 5 fs to 25 fs. The solid line and the solid dotted-line represent $\sigma_{\Delta t_{TA}}$ and $\sigma_{\Delta t_{BB}}$ with (10) and (11), respectively. The O and X marks in Fig. 4 represent the simulated input-referred jitters, $\sigma_{\Delta t_{TA}}$ and $\sigma_{\Delta t_{BB}}$, for PFD-TA PLL and BBPLL respectively. In the case of $\sigma_{t_{ref}} = 750$ fs and 500 fs, both $\sigma_{\Delta t_{TA}}$ and $\sigma_{\Delta t_{BB}}$ are converged to $\sigma_{t_{ref}}$ as $\sigma_{T_{dco0}}$ becomes smaller. So, if $\sigma_{t_{ref}}$ is larger than $\sqrt{2/(\pi-2)}\cdot\sigma_{TAI}$ as shown in Fig. 4, the optimum $\sigma_{\Delta t_{TA}}$ is smaller than the optimum $\sigma_{\Delta t_{BB}}$ for the same DCO, which represents that PFD-TA PLL performs better than BBPLL in terms of jitter. Conversely if $\sigma_{t_{ref}}$ is smaller than $\sqrt{2/(\pi-2)}\cdot\sigma_{TAI}$, now $\sigma_{T_{dco0}}$ determines which architecture achieves a smaller optimum jitter. Similar to $\sigma_{t_{ref}}$, higher $\sigma_{T_{dco0}}$ leads to the advantage of PFD-TA PLL over BBPLL because optimum $\sigma_{\Delta t_{TA}}$ is smaller than the optimum $\sigma_{\Delta t_{BB}}$ as shown in Fig. 4. This comparison plot demonstrates that PFD-TA PLL is advantageous over BB PLL when $\sigma_{t_{ref}}$ and $\sigma_{T_{dco0}}$ are large, which is typical in low-power IoT applications.

D. OUTPUT JITTER DERIVATION

Assuming that the power spectral density (PSD) of the reference clock phase noise is a constant and the DCO phase noise is modeled as a random-walk noise PSD, the PLL output jitter can be obtained by integrating the PLL output phase noise. In Fig. 5, the PLL output jitter is calculated with the noise transfer functions from Fig. 3 which are expressed as follows:

$$H_{REF}(z) \approx \frac{NK_{TA}K_{T,TA}f_{ref}\left(1-z^{-N}\right)}{N\left(1-z^{-1}\right)^2+K_{TA}K_{T,TA}f_{ref}z^{-1}\left(1-z^{-N}\right)} \tag{15}$$

$$H_{DCO}(z) \approx \frac{N\left(1-z^{-1}\right)^2}{N\left(1-z^{-1}\right)^2+K_{TA}K_{T,TA}f_{ref}z^{-1}\left(1-z^{-N}\right)} \tag{16}$$

where $H_{REF}(z)$ and $H_{DCO}(z)$ represent the noise transfer functions from reference clock and DCO to the PLL output, respectively.

The simulated and calculated output jitters of PFD-TA PLL and BBPLL are compared in Fig. 5, where the PLL output phase noises are integrated from 10 kHz to 10 MHz. Since σ_{TAI} is assumed to be about 288 fs that is the same to Fig. 4, the superiority between the optimum $\sigma_{t_{out}}$ of the PFD-TA PLL and BBPLL depends on the same noise terms in Fig. 4. From the comparison in Fig. 4 and 5, the BBPLL has the lower optimum output jitter than PFD-TA PLL if both the reference and the DCO noise are small. On the other hand, for the given the reference and the DCO noise, in the PFD-TA PLL, σ_{TAI} must be reduced to have lower output jitter.

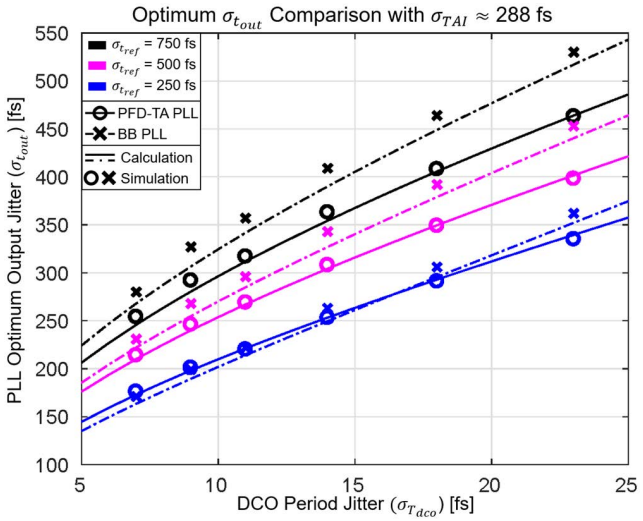


FIGURE 5. Simulated and calculated optimum output jitter comparison between BBPLL and the PFD-TA PLL.

IV. REFERENCE SPUR OF THE PFD-TA PLL

In this section, the reference spur analysis is presented to disclose the relationship between the TA gain and the spur in the PFD-TA PLL. Since χ in (6) is controlled by K_T as well as K_{TA}, this spur analysis is helpful to decide the valid K_T and K_{TA} which minimize both the PLL output jitter and reference spur.

If the PLL enters into a locked state, the random noise of the input does not influence the PLL output spurs, however, the mismatches between the PRO_P and PRO_N make unwanted DCO frequency modulation pulses which incur the reference spur. For example, the path delay and capacitor mismatch results in a periodic modulation of DCO frequency represented by $f_{DCO}(t)$ in Fig. 6. If there is an only path delay mismatch, Δt_m, between the PRO_P and PRO_N as shown in Fig. 6(a), $f_{DCO}(t)$ has two unwanted pulse signals that increase and decrease the frequency control ($+f_C$ and $-f_C$) with the interval of T_{PW} once every reference clock. Under a locked condition PRO_P and PRO_N have the similar pulse width of T_{PW} that is determined by TA latency. Longer TA latency results in smaller T_{PW}. The mismatch of capacitors driven by PRO_P and PRO_N results in frequency error of $f_P - f_N$, where f_P and f_N are the DCO frequency variations by the PRO_P and PRO_N, respectively. Such DCO modulation in every reference clock deteriorates the reference spur directly.

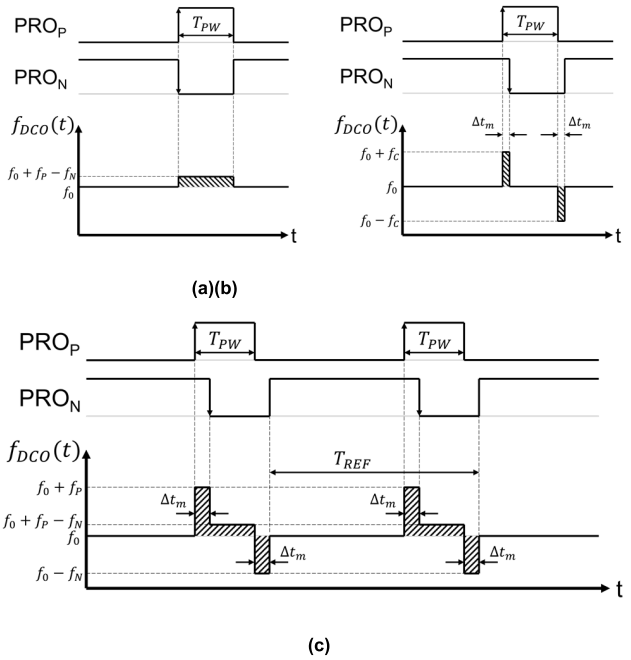


FIGURE 6. Undesired DCO frequency modulation functions by (a) path delay mismatch and (b) capacitor mismatch between PRO_P and PRO_N, and by (c) both mismatches, assuming that phase error is zero.

The total $f_{DCO}(t)$ by both the path delay and the capacitance mismatch is shown in Fig. 6(c). To calculate the reference spur by the total $f_{DCO}(t)$, assuming $f_m(t)$ is the magnitude of the variation of the periodic DCO frequency modulation function, $f_{DCO}(t)$ can be expressed as follow,

$$f_{DCO}(t) = f_0 + f_m(t) \tag{17}$$

where,

$$f_m(t) = \begin{cases} f_P, & 0 < t < \Delta t_m \\ f_P - f_N, & \Delta t_m < t < T_{PW} \\ -f_N, & T_{PW} < t < T_{PW} + \Delta t_m \\ 0, & T_{PW} + \Delta t_m < t < T_{REF} \end{cases} \tag{18}$$

And it can be represented by Fourier Series as follow,

$$f_m(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos\frac{2\pi nt}{T_{REF}} + \sum_{n=1}^{\infty} b_n \sin\frac{2\pi nt}{T_{REF}} \tag{19}$$

where,

$$a_n = \frac{2}{T_{REF}} \int_0^{T_{REF}} f_{DCO}(t) \cos\frac{2\pi nt}{T_{REF}} dt \tag{20}$$

$$b_n = \frac{2}{T_{REF}} \int_0^{T_{REF}} f_{DCO}(t) \sin\frac{2\pi nt}{T_{REF}} dt \tag{21}$$

When (19) is substituted to (17), the DC value $f_0 + a_0/2$ is corrected by the PLL feedback, however, the AC components produce dual sideband spurs with harmonics of the reference clock. To derive the reference spur level by getting the power ratio of the sideband-to-carrier, $f_m(t)$ is converted to phase as follows,

$$\theta_m(t) = \int 2\pi f_m(t)\, dt = \sum_{n=1}^{\infty} A_n \cos\omega_n t \tag{22}$$

Since $\omega_1 = 2\pi f_{ref}$ trigonometrical terms are dominant to reference spur, by substituting (19) to (22) with only a_1 and b_1 terms, the magnitude, A_1, can be obtained. After some algebra, the fundamental reference spur to carrier is as follow,

$$P = 20log\frac{T_{REF}}{2}\sqrt{f_P^2 + f_N^2 - 2f_P f_N \cos\frac{2\pi\Delta t_m}{T_{REF}}} \times \sin\frac{\pi T_{PW}}{T_{REF}} \tag{23}$$

From (23), the large DCO frequency step without the TA aggravates the spur with even a small path mismatch. For example, if there is no capacitance mismatch in the proportional path, such as $f_P = f_N = f_C$, and T_{PW} is assumed to be about 15 ns for 32 MHz reference clock. When the PLL output is 3.6 GHz and the unity gain frequency is about 1 MHz where f_C becomes about 700 MHz without the TA, then Δt_m must be less than 200 fs to lower the spur level below −70 dBc. However, if the TA provides the time gain of 100 in the proportional path, f_C can become 7 MHz from 700 MHz, maintaining the unity gain frequency of 1 MHz, and the reference spur can be about −70 dBc with Δt_m of 30 ps. So, the high-gain TA reduces the DCO frequency step and makes the reference spur less sensitive to the path delay mismatch.

On the contrary, if $\Delta t_m \rightarrow 0$, the mismatch $f_P - f_N$ becomes the dominant factor to worse the reference spur, so, reducing f_P and f_N with the high-gain TA as mentioned above is ineffective to lower the reference spur level. However, increasing the TA gain results in large latency and narrow T_{PW}, and it is effective in part to reduce the reference spur by (23). In summary, it is necessary to design the high-gain TA to achieve a low reference spur level by lessening the impact of the mismatches.

V. DETAILED STRUCTURES OF THE PFD-TA PLL

A. LOW-POWER HIGH-GAIN TA

In general, the TA utilizes the propagation delay gap of the two regeneration circuits with capacitors. For example, in [22], [37], [38], the time difference between two inputs makes an initial voltage gap between two capacitors and the discharging current ratio determines the TA gain. However, a small input time difference around zero like PLL in a locked state is difficult to generate the initial voltage gap with a high-gain because of slow turn-ON/OFF speed and dead zone characteristics. An additional gate circuit eliminates the current source dead zone [22], but the TA gain of 20 is still limited to low. From Section IV, to suppress the reference spur by the mismatches, the TA has to achieve high-gain, such as over 100. In this PFD-TA PLL, the latch-based TAs in [21], [29], [39] are exploited where the regeneration core consists of an input delay, a SR latch and an XOR, as shown in Fig. 7. In Fig. 7(a), the delay cell, T_{off}, on one input of each

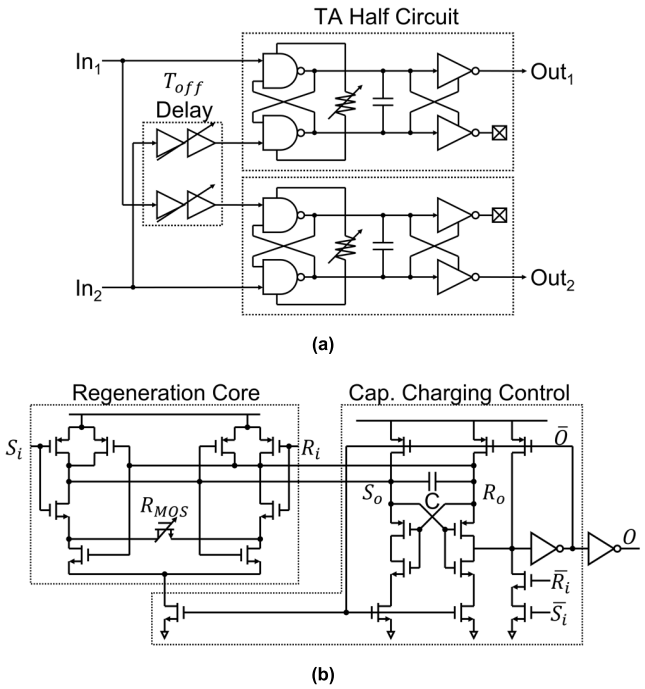


FIGURE 7. (a) TA block diagram and (b) TA half circuit.

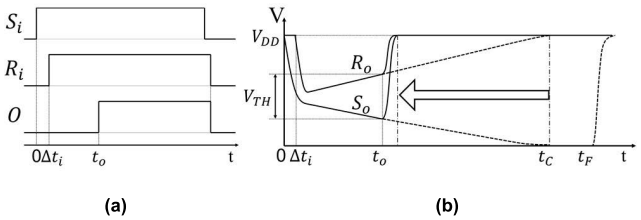


FIGURE 8. (a) Input and output signals of the TA half circuit, and (b) regeneration core outputs.

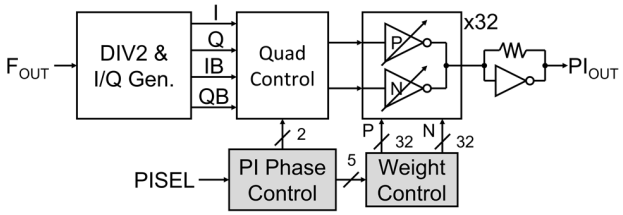


FIGURE 9. Inverter-based phase interpolator and digital control blocks.

SR latch makes the time-amplifying characteristic between $-T_{off}$ and T_{off} [39]. With R_{MOS} control in the SR latch, the TA can achieve gain over 100, but the high-gain causes the long regeneration time unavoidably, which incurs large crowbar current in the latch cores, and the core output capacitor also leads to significant power consumption from the charging and discharging cycle [29].

For lower power consumption, the XOR in the half circuit of the proposed TA is modified to the capacitor charging control circuit as described in Fig. 7 (b), which terminates the regeneration after the core output is generated. The timing graph of the TA half circuit is illustrated in Fig. 8. After t_o, $\bar{O}$ disengages pull-down paths of the core and pulls up both S_o and R_o to V_{DD}. As a result, the regeneration operation and the charging capacitor is stopped. If R_i and S_i are toggled to 0 at t_F, the core returns to the initial state.

This technique reduces the maximum voltage between the capacitor and the power consumption by a factor of 4, resulting in a consumption of 140 μW at 32 MHz. The proposed TA gain ranges from 60 to 250 with σ_{TAI} from 250 fs to 450fs, respectively. And its input dynamic range covers +/−30 ps or +/−60 ps depending on T_{off}.

B. FRACTIONAL-N DIVIDER WITH PI

The time-difference that controls DCO frequency in the proposed proportional path has limited by reference clock period, and then the high-gain of the TA over 100 that has a large latency enforces the narrow TA input dynamic range, such as 30-60 ps that is smaller than DCO one period. So, it is needed to implement PI in the fractional-N divider, like as DTC-based BBPLLs.

The PI is based on the 32 pairs of equal-strength inverters, as shown in Fig. 9, which constructs a weighted sum of quadrature phases. The four quadrature phases are generated by divide-by-2, and they are controlled by the digital circuit. 1 LSB of the PI is about 4-5 ps in a 3-4 GHz PLL, and its phase is $\Delta\Sigma$-modulated to get low in-band noise. The inverter-based PI is adopted for less current consumption as compared to the current mode PI [27], [28] that consumes the bias current and requires high supply for signal headroom.

The PI phase and weight controller splits a large PI phase jump into several smaller jumps to prevent the glitches [27], [28]. The maximum phase jump at a time is limited to $\pi/4$ rad for no glitches, which leads to a maximum of 8 phase jumps per one reference cycle. This glitch-free phase jump scheme requires at least 8 times faster digital clock than reference clock. To reduce the required digital clock frequency to half, the bi-directional PI control is proposed. The jump direction is automatically set to either counter-clockwise or clockwise depending on the magnitude of phase jump. For example, if the desired PI phase shift exceeds π rad, the clockwise direction is enabled. Concurrently, MMDIV division factor is increased by one to compensate for the one cycle slip. With the counter-clockwise PI direction, the division factor is $N = N_{int} + N_{PI}/2^7$ where N_{int} and N_{PI} are control words for MMDIV and PI, respectively. In the case of the clockwise PI rotation, the fractional division factor becomes $(1 - N_{PI}/2^7)$, and the integer division part becomes $N_{int} + 1$ to hold the overall division factor $N = (N_{int} + 1) - (1 - N_{PI}/2^7)$.

C. PI NONLINEARITY CALIBRATION

The inverter-based PI consumes less power than the current-mode phase interpolator (CMPI), however, the poor linearity

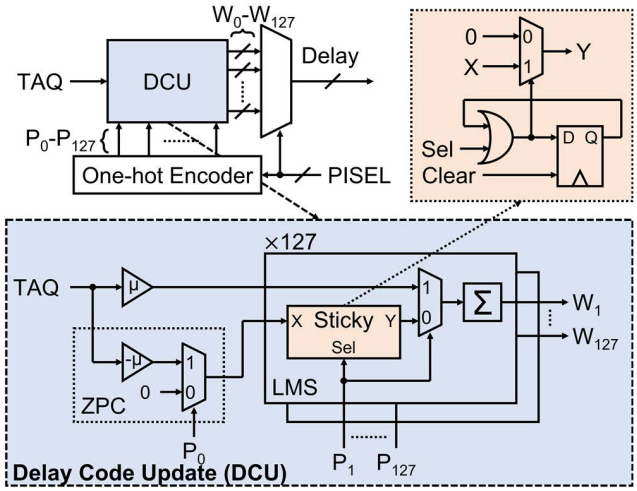


FIGURE 10. Delay control code update block diagram for PI nonlinearity calibration.

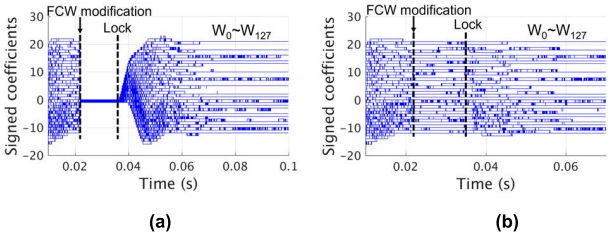


FIGURE 11. Convergence timing simulation of the delay codes for the PI nonlinearity calibration. With FCW changed by 64 MHz, the delay codes start from all zero in (a) and updates continuously from the prior frequency condition in (b).

of the 32 inverter pairs has a significant effect on the PLL fractional spur. To improve the linearity of the PI, the PI 45° phase dithering has been studied [28], but the fractional spur is still large, because the duty cycle distortion of the DIV2 can directly affects the 4 quadrants for the PI. Therefore, in this PLL, the PI nonlinearity for whole PI phases is digitally calibrated.

In this design, the PI nonlinearity is compensated by two delays in front of the PFD which of one corrects the reference clock or divided clock from the feedback path [25]. The control codes of the delays are generated by accumulating the BBPD output from the digital integral path that is called *TAQ* as shown in Fig. 10. The delay code update (DCU) block produces 127 phase control codes except zero PI phase code because the PI output for zero phase has not PI distortion. This least mean square (LMS) algorithm improves the PI nonlinearity effectively in the PLL locked state, however, if the PLL is into an acquisition state after FCW is changed, the *TAQ* that involves the PI distortion and the frequency acquisition error messes up the DCU.

To operate the DCU in background, the zero-phase canceller (ZPC) block is attached to the DCU where the ZPC cancels out the LMS update by subtracting *TAQ* when the PI zero phase is selected. Since *TAQ* at PI zero phase, which is called TAQ_0, is affected by the frequency acquisition error or Gaussian random noise from the noise sources, TAQ_0 can be used as a reference point to consider whether the PLL is locked or not. If the PLL is in the frequency acquisition, *TAQ* and TAQ_0 are likely to be the same, and then the DCU operation is canceled by subtracting the *TAQ* with TAQ_0 in the accumulator. After the PLL is locked, TAQ_0 becomes random noise and *TAQ* implies PI nonlinearity, which means that *TAQ* cannot be cancelled out by TAQ_0 and the LMS update works normally. And to prevent the unwanted subtracting according to FCW, a sticky selection block is added to LMS block. If any PI phase is selected, the corresponding sticky selection is activated, and if not, the output Y is 0. This DCU operation can be summarized as following equation:

$$W_{PI}[n] = W_{PI}[n-1] + \mu \cdot (TAQ - TAQ_0[n]) \quad (24)$$

where W_{PI} is the calibration delay code that corresponds to the PI phase state, $PI = 0, 1, \ldots, 127$, n denotes the PI phase cycle, and μ is a coefficient of the LMS update.

To verify that the DCU operates in the background, the PI nonlinearity calibration is simulated by the Verilog PLL behavior model when the DCO frequency changes from 3.5845 GHz to 3.5205 GHz. Both Fig. 11(a) and (b) show the convergence of the delay codes with the algorithm as (24). In Fig. 11(a) all W_{PI} are reset to all zeros for the FCW modification. The PLL attains the frequency lock in about 15 ms, and then and W_{PI} converge in additional about 20 ms with $\mu = 2^{-7}$. The larger μ can further reduce the convergence rate. In Fig. 11 (b), this DCU settling time reduces to a negligible number when all W_{PI} starts from the prior stored values. The overall PLL structure of the proposed PFD-TA PLL is shown in Fig. 12. The delay code for PI nonlinearity is applied to Delay P and Delay N by a polarity decoder. The positive delay code applied to Delay P and the negative delay code applied to Delay N. This separate delay control minimizes initial jitter and reduces supply sensitivity. Each delay cell covers 60 ps with a resolution of 1ps/LSB. To ensure that the fractional spur is below than −50 dBc with 4 GHz DCO output, the nonlinearity should be less than 1 ps.

VI. MEASUREMENTS

The proposed PFD-TA PLL is fabricated in a 40 nm standard CMOS process and the total power consumption is 5 mW clock. As shown in Fig. 13, the large digital block expends the most power (27%), followed by the DCO consuming 19% of the total power. The fractional-N divider with divided-by-2, PI, and MMDIV dissipates 36% of the total power. Using the inverter-based PI, the power consumption of the PI itself is 0.59 mW, less than that of the current mode PI [24], but it still dissipates considerable power in divided-by-2. The TA with the proposed low power technique has the lowest power consumption among custom cells.

Fig. 14 shows the measured and simulated phase noise plots of the PFD-TA PLL and the BBPLL, which are measured at the PLL output frequency of 3.584 GHz [25]. The

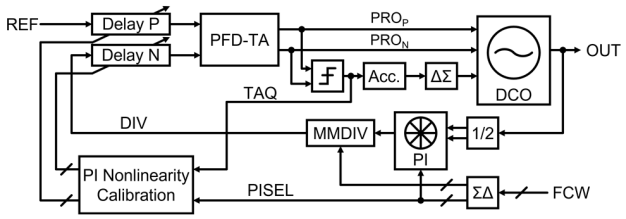
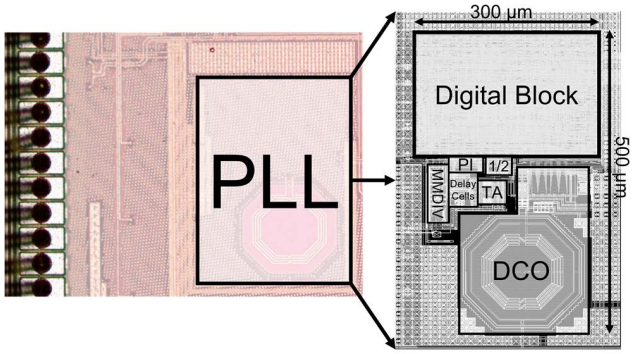
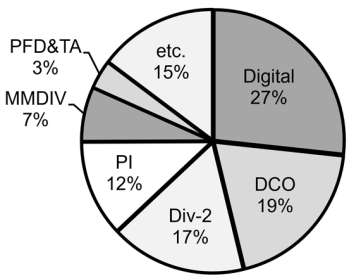


FIGURE 12. Overall structure of the proposed PFD-TA PLL with PI nonlinearity calibration.



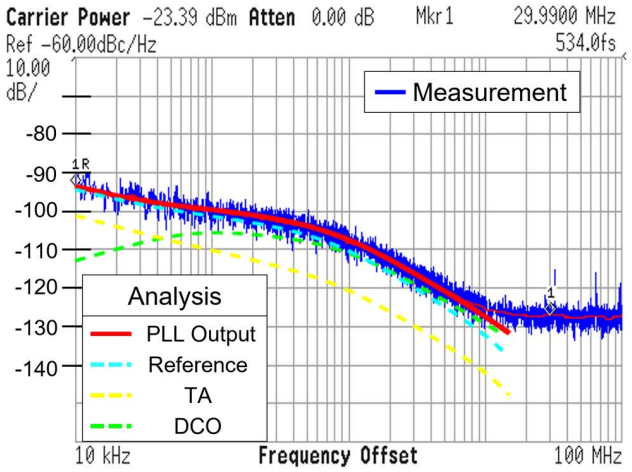
(a)



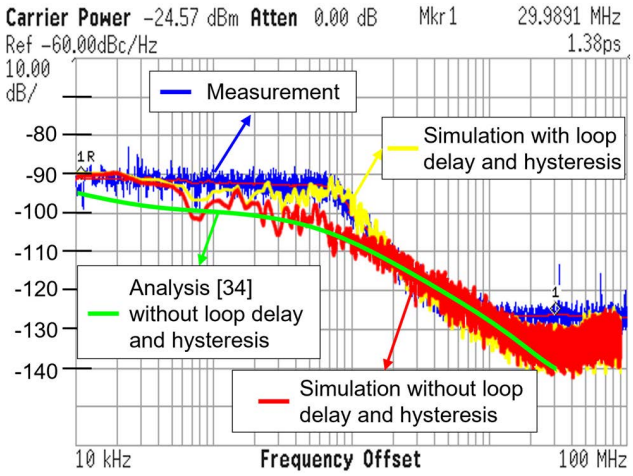
Circuit	Power (mW)
Digital	1.32
DCO	0.97
DIV-2	0.83
PI	0.59
MMDIV	0.33
PFD&TA	0.18
Etc.	0.73
Total	4.95

(b)

FIGURE 13. (a) Die photograph and layout, and (b) the detailed power breakdown of the proposed PFD-TA PLL.



(a)



(b)

FIGURE 14. Comparison plots of the measured and simulated phase noise for the PFD-TA PLL (a) and the BBPLL (b).

parameters in the measurements and simulations are that $K_{T,TA} \approx 483$ fs and $K_{TA} = 100$ for the PFD-TA PLL, and $K_{T,BB} \approx 3$ fs and $\beta = 0.5$ for the BBPLL, which achieve the optimum PLL output jitters. From the measurement results, the white phase noise level of the reference crystal is about -152 dBc/Hz that is equivalently $\sigma_{t_{ref}} \approx 700$ fs. The extracted phase noise of the DCO running at 3.584 GHz is about -110 dBc/Hz at 1 MHz offset from the carrier, where $\sigma_{t_{dco0}} \approx 14$ fs, and the σ_{TAI} is about 250 fs, when K_{TA} is about 100. And the noise sources involve the flicker noise, and the corner frequencies of the reference clock, TA, and DCO are evaluated as 1 MHz, 800 kHz, and 150 kHz, respectively.

Fig. 14(a) compares the measured output phase noise and the calculated phase noise curves of the proposed PFD-TA PLL with the theoretical noise contributions of the reference, TA, and DCO. From (8) and (9) with the estimated noise sources, the optimum K_{TA} is about 104, and the integrated output jitters of the PFD-TA PLL's measured and calculated phase noises from 10 kHz to 10 MHz are 534 fs and 515 fs, respectively.

Fig. 14(b) shows the measured and simulated output phase noises of the BBPLL for comparison. Unfortunately, the standard cell-based BBPD and the additional loop delay deteriorate the phase noise that is verified in both the measurement in blue and the behavior model simulation in yellow line in Fig.14(b) and both agree well. Without the loop delay and BBPD hysteresis, the phase noise improves as shown in red and green lines of Fig. 14(b), which are the behavioral model result and the equation in [34], respectively. In a proper design of BBPLL, the integrated output jitter from 10 kHz to10 MHz is 545 fs, which is 30 fs worse than that of the PFD-TA PLL for the same reference and DCO noise used in our design.

In Fig. 15, the fractional spurs of the PFD-TA PLL are shown before and after the PI nonlinearity calibration. The fractional spurs are measured with 3.5845 GHz PLL output frequency where the division factor of the PI-MMDIV divider

TABLE 1. Comparison with prior-art fractional-N DPLLs for IoT application.

	ISSCC'21 Qiu [40]	JSSC'18 Liu [41]	ACCESS'19 Yan [42]	TCAS-I'17 Liu [43]	JSSC'18 Pourmousavian [44]	ISSCC'17 He [45]	TCAS-I'21 Chen [46]	RFIC'18 Gong [47]	This work
Technology [nm]	65	65	55	40	28	40	65	40	40
Architecture	DAC+DTC OSPLL	TA TDC +DTC ADPLL	TDC+DTC ADPLL	Snapshot TDC SSPLL	TDC+Doubler** ADPLL	Divider-less ADPLL	Snapshot TDC+DTC ADPLL	RO-based ILPLL	PFD-TA PLL
Output Frequency [GHz]	2.0-2.8	2.0-2.8	1.5-2.05	1.7-2.7	2.05-2.55	1.8-2.5	1.9-2.6	1.8-2.7	3.0-3.7
Reference Frequency [MHz]	0.032768	26	24	32	40	N/A	32	64	32
Supply Voltage [V]	1	1	1.2	1(analog) /0.8(digital)	0.5	1(analog) /0.8(digital)	0.55	1	1.1
Power Consumption [mW]	4.97	0.98*/0.65	4	1.19	1.6	0.67	0.53	1.33	5
DCO Power Consumption [mW]	N/A	0.304*/0.285	0.84	0.62	0.4	0.263	0.2	0.61	0.97
RMS jitter [ps]	5.79 (10k-10MHz)	0.53*/1 (10k-10MHz)	1.07 (1k-10MHz)	1.7 (10k-100MHz)	0.86 (10k-10MHz)	1.98 (10k-10MHz)	0.87 (10k-10MHz)	1.6 (10k-10MHz)	0.534 (10k-30MHz)
Reference Spur [dBc]	−78	−72*/−68	−76.3	−66	−78	−62	−66	−43.6	−60
Fractional Spur [dBc]	−40	−56*/−50	−40	−37	−57	−56	−50	−45.8	−50
FoM [dB]	−217.8	−246*/−242	−233.4	−234.6	−239.2	−236	−244	−234.7	−238.4
Core Area [mm^2]	0.576	0.23	0.88	0.22	0.33	0.18	0.42	0.13	0.14

**With reference doubler*
***Switched-capacitor dc-dc doubler*

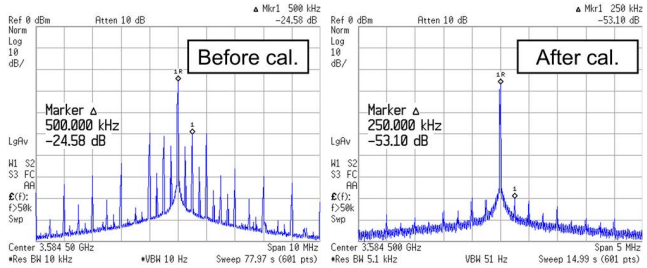


FIGURE 15. Measured fractional spurs at 3.5845 GHz of the PFD-TA PLL with and without the PI nonlinearity calibration.

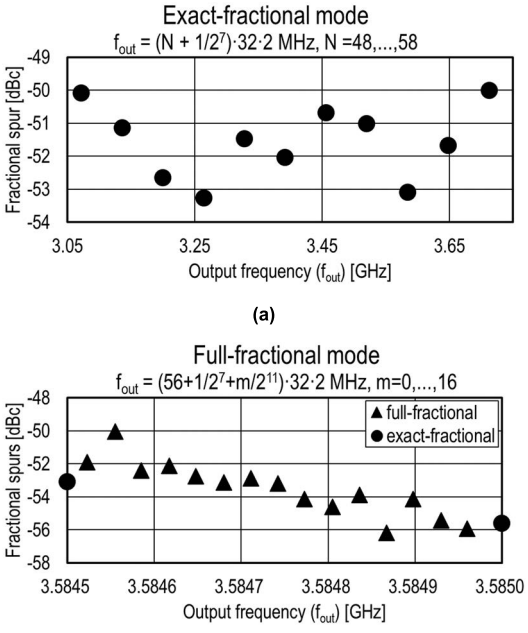


FIGURE 16. Measured fractional spurs in (a) the exact-fractional mode and (b) the full-fractional mode.

$N = 2 \cdot (56 + 1/2^7)$ that is a minimum frequency offset of the exact fractional-N [25]. With the calibration, the worst-case fractional spur is suppressed to −53 dBc. The other worst-case fractional spur levels at the exact-fractional mode are shown in Fig. 16(a). For higher fractional resolution, a second-order $\Delta\Sigma$ modulator (DSM) is used to dithering the PI that is called full-fractional mode. With the PI nonlinearity calibration, the worst-case fractional spur levels at the full-fractional mode frequencies which are between two exact-fractional mode frequencies are plotted in Fig. 16(b).

Fig. 17 shows the measured reference spur levels of the PFD-TA PLL according to TA supply voltages where the reference spur is reduced as smaller TA supply voltage. From (23), the reference spur is affected by the pulse width T_{PW} in Fig. 6 as well as the path and capacitor mismatch in the proportional path, and T_{PW} is determined by the TA latency and the period of reference clock. For the proposed TA in

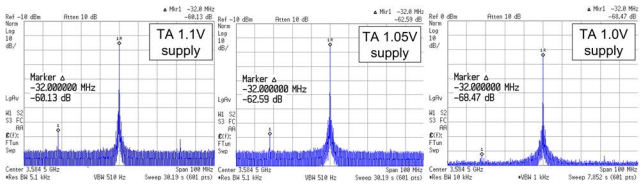


FIGURE 17. Measured reference spurs at 3.5845 GHz of the PFD-TA PLL according to TA supply voltage of (a) 1.1 V, (b) 1.05 V, and (c) 1.0 V. The reference spur is measured while the PI operates for fractional-N, and the fractional spurs occur within the PLL bandwidth.

Section V-A, the smaller TA supply voltage, the narrower T_{PW} because of the large TA latency with large TA gain, so the reference spur is reduced as shown in Fig. 17. To compute the reference spur with (23), the mismatch terms are extracted by simulation as follow: the time mismatch, Δt_m, in the proportional path of the PLL is about 30 ps, the DCO frequency step distortion, $f_P - f_N$, by the capacitor mismatch is expected to be about 300 kHz by Monte Carlo simulation, and T_{PW} is about 8 ns, 6 ns, and 2.5 ns according to TA supply voltage of 1.1 V, 1.05 V, and 1.0 V, with TA gain of 120, 145, and 200, respectively. With such parameters and (23), the estimated reference spurs are -59.3 dBc, -61.3 dBc, and -68.2 dBc depending on the supply voltages. Since (23) only considers the fundamental term of the Fourier Series, the measurement results can be better than the calculation. And the unbalanced spur levels at the frequency offset of ± 32 MHz in the measurement plot are observed, which originates from amplitude modulation by the board and substrate coupling. The reference spur would be improved by a high gain output driver or better noise isolation in the test board. Overall, if the reference clock frequency is sufficiently small, Δt_m has little effect on the spur, and the larger $f_P - f_N$, and T_{PW}, the larger the spur.

The comparison table with prior-art fractional-N DPLLs is presented in Table 1, where the DCO power consumptions are below 1 mW.

VII. CONCLUSION

This paper presents a PFD-TA PLL with a high gain TA and PI nonlinearity calibration including phase noise and reference spur analyses. The high-gain TA alleviates the reference spur caused by DCO modulation path mismatch. A background PI nonlinearity calibration suppresses the fractional spurs in fractional-N operation. Our analysis shows that if the TA jitter is lower than a certain value determined by reference clock and DCO noise, the minimum output jitter of the PFD-TA PLL is lower than that of BBPLL.

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