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Electronic Load System With Interleaved Structure Applicable to DC, Single-Phase AC, and Three-Phase AC

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ABSTRACT We propose an electronic load system with an interleaved structure applicable to DC, singlephase AC, and three-phase AC. Applying the interleaved method makes it possible to reduce voltage and current ripple, thereby reducing voltage and current stress applied to components and guaranteeing a long lifespan. The operation of the proposed electronic load is described in detail by explaining the relationship between the command value of the electronic load and the duty ratio of each switch in the interleaved structure. Adding a feedforward term to the PI controller improves the controller's response, and the simulation results of DC and single-phase AC operation are presented. The validity of the proposed electronic load is verified through the 10kW prototype test.

INDEX TERMS Aging test, burn-in test, electronic load, feed-forward control, interleaved structure, voltage ripple.

I. INTRODUCTION

As for the power supply, many products with improved performance and efficiency have been produced recently due to the development of power electronic technology, but the development of test equipment for the reliability test process that uses the most electricity in the production process is still insufficient. In particular, the equipment reliability test process is essential in producing most power supplies and converters. It includes the primary process of reducing potential defects and product quality and stability. This reliability test process is an aging and burn-in process, and a load test is performed for a prescribed time with the output power according to the rating of the produced power supply. The load is a structure that consumes most of the electrical energy as heat, and the most commonly used load is resistive. It is not easy to continuously change the load once we determine the resistance of the load for testing. An electronic load is being used to improve the disadvantages of the resistive load [1]–[4]. The electronic load uses a semiconductor switch instead of a mechanical switch to control the load current. It has operation modes such as constant current (CC), constant voltage (CV), constant power (CP), and constant resistance (CR).

An electronic recycling load can reduce power consumption by heat from the load resistance by preventing unnecessary power consumption by using the recycling load and regenerating it to the input source. Recycling load, which returns more than 80% of the power consumed as 100% heat in the conventional resistive load using a mechanical switch to the input side, does not require an air conditioner to reduce heat generation in the existing electronic load [5], [24]. Until the early 2000s, energy recycling electronic loads were mainly based on AC power sources such as uninterruptible power supplies or AC motor drivers [25], [26]. An AC electronic load for the UPS burn-in test, which consists of an input ac-to-dc converter that simulates various loads, and an output terminal of a grid-connected converter that recycles energy, was introduced in [26]. The steady-state operation characteristics are excellent since the iterative controller is applied,

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FIGURE 1. Circuit configuration of electronic load system using the interleaved method.



FIGURE 2. Equivalent resistance according to duty ratio in the parallel circuit.

but the dynamic performance is limited [28]. A single-stage configuration combining ac-to-dc and the dc-to-dc converter was introduced to obtain a fast response [27]. In this case, the response speed can be improved, but the voltage ripple of the capacitor increases as the dc-link is shared [28], [29]. These recycling electronic load systems still have problems of increasing system costs and complicated maintenance.

Since these electronic load systems generally operate with high power for an extended period, a circuit configuration with high reliability is essential. In addition, it is necessary to increase the efficiency of operation through a load configuration that can respond to DC loads, single-phase, and three-phase AC loads [6]–[12].

This paper proposes an electronic load system applicable to single-phase and three-phase AC and DC power. In particular, the proposed interleaved structure and switching method reduce voltage and current ripple to reduce stress and extend the lifespan of an electronic load system [13]–[23]. In addition, the proposed electronic load constitutes a unified system based on a single phase. However, it has the advantage of applying a three-phase AC load through parallel operation, and it is also easy to expand the load capacity. The circuit configuration and basic operating principle of the proposed electronic load system are explained in detail, and the feasibility is verified through simulation and experiments using a 10kW prototype.

II. PROPOSED 3-PHASE INTERLEAVED ELECTRIC LOAD SYSTEM

Fig. 1 shows a three-phase electronic load system to which the interleaved method is applied. A full-wave diode rectifier is located at the input stage so that both single-phase AC and DC can be used as input power sources. Therefore, the



FIGURE 3. Comparison of general switching and interleaved switching current waveforms, (a) typical switching current waveform, (b) interleaved switching current waveform, (c) total input current.



FIGURE 4. Equivalent circuit of n-phase interleaved structure.



FIGURE 5. Comparison of critical waveforms of single-phase operation and two-phase interleaved operation.

input voltage finally applied to the switch is in the form of a rectified voltage or a DC voltage.

A three-phase interleaved circuit is constructed using Q₁, Q₃, Q₅, and R₁, R₃, R₅ in a primary circuit having R₂, R₄, and R₆ resistors connected to three switches (Q₂, Q₄, Q₆). The upper arm and lower arm pair of switches are configured in the form of one module. For each resistance for six electronic load operation analyses, 10 Ω is applied to simplify the formula. For example, to generate an equivalent resistance of 20 Ω using three switches (Q₂, Q₄, Q₆), the parallel resistors connected. If the PWM signal is applied with a duty ratio *D* of approximately 1/6, each parallel circuit resistance generates a resistance of R_{p1} = R _{p2} = R_{p3} = 60 Ω by (1). Then the resistance of the circuit finally becomes 20 Ω



FIGURE 6. Relationship between the number of interleaved phases and capacitor voltage ripple.



FIGURE 7. Switching operation according to duty ratio, (a) operation using three lower switches D < 0.5, (b) operation using three upper switches, maintaining the lower switch ON state, D > 0.5.

due to the three parallel circuits by (2).

$$R_{pn} = \frac{R_n}{D} \ (n = 1, 2, 3...)$$
 (1)

$$R_{Tp} = R_{p1} ||R_{p2}|| \cdots ||R_{pn}$$
(2)

Fig. 3(a) shows the current waveform when the switching signal of the same phase is applied to the three switches without applying the interleaved operation. Fig. 3(b) shows the current waveform during interleaved operation. The waveform of the total input current synthesized in each switching method is shown in Fig. 3(c). As shown in Fig. 3(c), the difference between the peak value of the total input current



FIGURE 8. Switching operation according to duty ratio, (a) operation using three lower switches D < 0.5, (b) operation using three upper switches, maintaining the lower switch ON state, D > 0.5.

and the average current is as much as a multiple of the interleaved phase. It causes a difference in the ripple of the current flowing through the reactor. If the interleaved method is applied, the current's peak and average current values can be reduced. In addition, since the current frequency also increases by the number of interleaved phases, there is an advantage in that the weight and volume can be reduced by using a small capacity inductor.

The equivalent circuit for the proposed *n*-phase interleaved electric load system is shown in Fig. 4.

Fig. 5 shows the current flowing through the load resistor, the capacitor current, and the capacitor voltage. In Fig. 4, when the switch Q_n is turned on, the voltage across the load resistor has the same as V_c to be expressed as I_R = V_c/R. Kirchhoff's current law expresses that the current flowing through the capacitor can be expressed as I_c = I_L-I_R. Here, the change amount of charge (ΔQ) due to the current flowing through the capacitor is expressed as the area of the capacitor current, so it is the same as (3).

$$\Delta Q = DT \times \left(\frac{V_C}{R} - I_{av}\right) \tag{3}$$

From the relationship between voltage and charge in a capacitor, the capacitor voltage by the single-arm of Fig. 4 is the same as (4).

$$\Delta V_C = \frac{DT \times \left(\frac{V_C}{R} - D\frac{V_C}{R}\right)}{C}$$



FIGURE 9. Separation control of the upper switch and lower switch according to load, (a) upper switch duty control maintaining the lower switch ON, (b) equivalent circuit of interleaved electronic load system according to duty ratio.



FIGURE 10. Control block diagram of the proposed interleaved electronic load system.

$$= \frac{DT \times \frac{V_C}{R} (1-D)}{C}$$
$$= \frac{TV_{in}}{RC} D(1-D)$$
(4)

Here, *D* is the duty ratio of the switch, *T* is the period, V_{in} is the input voltage, *R* is the load resistance, and *C* is the capacitance. In the case of two-phase interleaved, the average current flowing through the load resistor is doubled, as shown in Fig. 5, and this reduces the ripple of capacitor *C* by 50% compared to single-arm.

$$\Delta V_C = kD(1 - D)$$

Here, $k = \frac{TV_{in}}{RC}, V_C = V_{in}, \omega L = 0$ (5)



FIGURE 11. CC (constant current) mode operation, (a) When changing the current command from 20A to 40A, (b) Enlarging the circled part of (a).

(5) shows the equivalent expression when there is only one switch. Here, if one interleaved circuit is added, the average current flowing through the load is doubled, and the capacitor's ripple is reduced by 50%, as shown in (6).

$$\Delta V_C = \frac{DT \times \left(\frac{V_C}{R} - 2I_{av}\right)}{C} = \frac{DT \times \left(\frac{V_C}{R} - 2D\frac{V_C}{R}\right)}{C}$$
$$= \frac{DT \times \frac{V_C}{R} (1 - 2D)}{C}$$
$$= \frac{TV_{in}}{RC} D(1 - 2D) = kD(1 - 2D) \tag{6}$$

(6) is the ripple of the capacitor voltage for the two interleaved. If it is generalized to N interleaved numbers, it is the same as (7).

$$\Delta V_C = \frac{TV_{in}}{RC}D(1 - ND) = kD(1 - ND)$$
(7)

Fig. 6 compares the capacitor voltage ripple when the number of interleaved phases increases from 1 to 6. According to the duty ratio of each phase switch, the capacitor ripple voltage is reduced by a ratio of 1/n. The proposed electronic load system



FIGURE 12. CP (constant power) mode operation, (a) When changing the power command from 5kW to 15kW, (b) The enlarged waveform of (a).

shows that the duty ratio of the interleaved phase switch can be determined by considering the capacitor voltage ripple.

The proposed 3-phase interleaved electronic load system requires switching on/off duty ratio control to operate in CR(constant resistance), CC(constant current), CV(constant voltage), and CP(constant power) mode. As shown in Fig. 7, when the duty ratio is 0.5 or less, the upper switch is turned off, and only the lower switch is controlled, and when the duty ratio is 0.5 or higher, the upper switch is controlled the on the state of the lower switch.

In CR mode, when the command of the resistive load is 2Ω , the switch operation will be described as an example. For the convenience of analysis, all load resistances are 10Ω , and when both the upper and lower switches are turned on, the current flowing in each phase is assumed to be 10A.



FIGURE 13. CR mode operation, (a) When changing the power command from 5Ω to 45Ω , (b) The enlarged waveform of (a).

A. SIMULTANEOUS CONTROL OF UPPER AND LOWER SWITCH REGARDLESS OF LOAD

Suppose the upper and lower switch are simultaneously controlled to generate a command of 2Ω . In that case, the parallel resistance of each phase can be expressed as $(R_1||R_2) = 5\Omega$, and the combined equivalent resistance at this time is about 1.66 Ω . The duty ratio *D* to make it a 2Ω command value is about 0.8. The current waveform according to the switching operation is shown in Fig. 8.

In the case of three-phase interleaved switching, when one period T is expressed in degrees, the phase difference due to the interleaved operation has a phase difference of 120 degrees by 360/n, and each switch performs ON/OFF operation according to a set duty ratio. At this time, when the duty ratio of each phase is more significant than 1/3, corresponding to 120 degrees, the current overlap and appears in the form of overlapping current like I_T.

B. SEPARATION CONTROL OF UPPER AND LOWER SWITCHES ACCORDING TO LOAD

As the switching operation applied in this paper, the duty ratio according to the control command is divided into two



FIGURE 14. Simulation results of the proposed three-phase interleaved electronic load, (a) output voltage and input current, (b) expanded waveforms of output voltage and input current ripple.

sections. When the duty ratio between the upper and lower switches is 0.5 or less, the resistance and current are the same as when the lower switch is maintained in an ON state. When the duty ratio is 0.5 or more, switching is possible, as shown in Fig. 9(a), which maintains the lower switch in the ON state and allows a constant load value through the duty control of the upper switch. By reducing the peak of the final output current, the ripple is reduced, but the rated current of the switch becomes smaller. Since the lower switch always maintains the ON state, there is an effect of improving the efficiency due to the switching loss reduction. According to the upper and lower switch's duty ratio, Fig. 9(b) shows an equivalent circuit of the proposed interleaved method.

C. CONTROLLER DESIGN

Fig. 10 shows the control block diagram of the proposed interleaved electronic load system. The operation mode of

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FIGURE 15. CR mode and CP mode when operating with DC electronic load system, (a) when resistance command is changed from 4Ω to 14Ω in CR mode, (b) Input current, resistance command 14Ω , and 3-phase interleaved switching waveform when operating with 10kW electronic load in CR mode, (c) when the control command of CP mode is changed in the order of 2kW, 10kW, and 6kW.

the electronic load is divided into a constant resistance (CR) mode, a constant current (CC) mode, a constant voltage (CV) mode, and constant power (CP) mode.

A switching signal is generated by controlling the duty ratio D for following the command using the PI controller for each mode's reference of resistance, current, voltage, and power. The command for each operation mode compensates for the command value of the duty ratio by adding the feedforward term calculated through the input voltage/current and interleaved resistance to the PI controller. It improves control speed and precision according to the resistance that varies according to the interleaved switching operation. The following formula calculates the feedforward term. When the







(c)

FIGURE 16. A photograph of a prototype of the proposed 3-phase interleaved method electronic load system, (a) front and top view, (b) side view and rear load resistor, (c) control board based on TMS320F 28055.

upper and lower switches are turned on, six load resistors R (10 Ω) are connected parallel. It is denoted by the parallel equivalent resistance R_p .

$$R_E = \frac{R}{6} = R_p \ @Q_1 \sim Q_6 = ON \tag{8}$$

When the lower switch is in the ON state, the actual resistance R_E becomes twice R_p in (8).

$$R_E = R_p \times 2 \ @Q_2 = Q_4 = Q_6 = ON \tag{9}$$

$$R_E = \frac{2R_p}{D} \tag{10}$$



FIGURE 17. The lower switch signal of the proposed 3-phase interleaved electronic load system, (a) at 30% duty ratio, (b) at 80% duty ratio.

When *D* has a control value other than 1, the actual resistance R_E is expressed by the parallel equivalent resistance R_p and the duty ratio *D*, which can be defined again as R_p^* and D^* by the command value.

$$D^* = \frac{2R_p^*}{R_F^*}$$
(11)

$$I^* = \frac{V}{R_E^*} = \frac{V}{\left(\frac{R_E}{D^*}\right)} = \frac{VD^*}{R_E}$$
(12)

If these command values are expressed in input voltage/current and the feedforward value D^* is calculated, it can be expressed as (13).

$$D^* = \frac{R_E \times I^*}{V} \tag{13}$$

III. SIMULATION AND EXPERIMENT RESULTS

We performed a PSIM simulation to verify the operation of the proposed interleaved electronic load system. It has six switches in a 3-phase interleaved configuration. Table 1 lists simulation parameters.



FIGURE 18. Load variation characteristics in the traditional electronic load system using the PI controller, (a) when the load current increases, (b) when the load current decreases.

TABLE 1	. Simu	lation	paramet	ters
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Parameter	Value	Unit
Input voltage	220	Vac
Inductor	20	μH
Inductor ESR	0.08	Ω
Capacitor	10	μF
Capacitor ESR	0.001	Ω
Load Resistor	27.5	Ω
Switching frequency	20	kHz

A. SIMULATION FOR EACH OPERATIONAL MODE WHEN WORKING AS A SINGLE-PHASE AC ELECTRONIC LOAD SYSTEM

The proposed interleaved electronic load system presents simulation results for four operation modes: CC, CP, CR, and CV mode. Fig. 11 shows that the input current waveform follows the current command well when the current command



FIGURE 19. Response when a feedforward term is added to the PI control in the proposed 3-phase interleaved method, (a) When the load current increases, (b) Waveform enlargement when load current increases, (c) When load current decreases, (d) Waveform enlargement when load current decreases.

is changed from 20A to 40A in CC mode control. From the enlarged waveform in Fig. 11(b), it can be seen that the steady-state is reached within 1ms. In order to reduce the switching loss, only the lower switch operates at the 20A command, and at the 40A command, the lower switch maintains the ON state and performs PWM control only with the upper switch.

Fig. 12 is the simulation result when the power command changes from 5kW to 20kW in CP mode control. Fig. 13 shows the response when the resistance command is changed from 5Ω to 45Ω in CR mode control. In both modes, it can be confirmed that the power control is well performed, showing a fast response to the command's change.

B. INPUT CURRENT AND OUTPUT VOLTAGE RIPPLE CHARACTERISTICS ACCORDING TO THE NUMBER OF INTERLEAVED PHASES

Fig. 14 shows the output voltage and input current of the proposed 3-phase interleaved electronic load system. We can

 TABLE 2. Ripple rates of the input current and output voltage according to the number of interleaved phases.

Parameter	1-phase configuration	2-phase interleaved	3-phase interleaved
Vc max [V]	311.61	310.39	308.86
Vc min [V]	304.63	307.28	306.94
Vc ripple [V]	6.98	3.11	1.29
$\Delta Vc=\Delta Vo [\%]$	2.26	1.0	0.62
Iin max [A]	33.90	32.79	32.38
Iin min [A]	31.13	31.44	32.15
Iin ripple [A]	2.77	1.35	0.23
ΔIin [%]	8.5	4.2	1.5

check the enlarged waveform's output voltage and input current ripple. Table 2 shows the input current and output voltage ripple rates according to the number of interleaved phases. As shown in Table 2, it can be confirmed that the output voltage ripple decreases, and the input current ripple decreases as the number of interleaved phases increases, as shown in (7).



FIGURE 20. Rated load test of the proposed three-phase interleaved electronic load, (a) when the rated current is increased from 0 to 45A when operating as an ac electronic load, (b) enlarged red box in (a), (c) When the rated current is increased by 3.5A per step when operating as a dc electronic load, (d) Enlargement of the red box in (c).

C. SIMULATION FOR EACH OPERATIONAL MODE WHEN WORKING AS DC ELECTRONIC LOAD SYSTEM

Fig. 15(a) is the simulation result when the resistance command changes from 4Ω to 14Ω when the proposed three-phase interleaved electronic load system operates in CP mode.

Fig. 15(b) is a waveform that operates as a 10kW electronic load with an input voltage of DC 750V and an average input current of 13.3A at a resistance command of 14 Ω . The waveform below shows the upper and lower switching signals operating as 3-phase interleaved. Fig. 15(c) shows the waveform in which the input current is accurately controlled according to the command while the input voltage is kept constant at 750V when the power command is changed from 2kW to 10kW back 6kW when operating in CP mode.

D. EXPERIMENTAL RESULTS

Fig. 16 shows the electronic load system of the proposed three-phase interleaved method. It was designed for 10kW,

and the controller was designed using DSP TMS320F 28055. The front part of Fig. 16(a) consists of a central control board, an operation mode selection switch, and a fan for heat dissipation of the load resistor. The lower part has an AC input stage, a rectifier, and an input LC filter and is composed of an interleaved switch module using three IGBT modules. The load resistance in Fig. 16(b) is six finned heater resistances of 27.5 Ω , and it has a maximum rated capacity of about 10kW when operating 6 in parallel.

Fig. 17 is the experimental waveform when the lower switch of the 3-phase interleaved electronic load system operates with duty ratios of 30% and 80%.

Fig. 18 shows the control response by the PI controller applied to a general electronic load system. Under the same P-gain and I-gain conditions, it can be seen that a typical PI controller applied to an existing electronic load system takes 400ms to reach a steady state when the load increases and 700ms when the load decreases. Since this corresponds to more than ten cycles of the commercial frequency, it is necessary to improve the control response. Fig. 19 shows the experimental waveform of the proposed interleaved electronic load system, which improves the control response by adding a feedforward term to the PI controller. Fig. 19(a) shows the control response when the load increases. The enlarged waveform in Fig. 19(b) shows the excellent control response that enters the steady-state in a short period. Fig. 19(c) is an experimental waveform showing the control response when the load is reduced. As can be seen from the enlarged waveform in Fig. 19(d), it shows the high-speed control response.

Fig. 20(a) shows the input voltage and input voltage waveform when the input current increases from 0A to 45A and then decreases to 0A when the proposed 3-phase interleaved method is operated as an AC electronic load system. Fig. 20(b) is an enlarged waveform of the red dotted line box in Fig. 20(a), showing fast control response characteristics with the addition of a feedforward term. Fig. 20(c) is an experimental waveform when the proposed three-phase interleaved method is operated as a DC electronic load. When the input current from 0A to 7.5kW by increasing by 3.5A per step is repeated, it shows the DC input voltage and DC input step wave current that maintains an average of 318V. Fig. 20(d) is an enlarged waveform of the red dotted line box in Fig. 20(c), and it can be seen that the fast response characteristic is shown with the addition of the feedforward term.

IV. CONCLUSION

An electronic load system with an interleaved structure is proposed as applicable to DC, single-phase AC and threephase AC. The operating principle of the interleaved method applied to the proposed electronic load is explained in detail, and its feasibility is verified through simulation and a 10kW prototype experiment. In the case of the three-phase interleaved method, the voltage ripple variation was 0.62%, which was 1.64% less than that in the case where the interleaved structure was not applied. The current ripple variation was 1.5%, which was 7% less than when the interleaved structure was not used. By adding a feedforward term to the PI controller, the response characteristics of the controller were improved, and it was confirmed through the 10kW prototype experiment that the operation of each mode as a DC and AC electronic load system according to the controller command was performed well.

REFERENCES

- C. E. Lin, M. T. Tsai, W. I. Tsai, and C. L. Huang, "Consumption power feedback unit for power electronics burn-in test," in *Proc. 21st Annu. Conf. IEEE Ind. Electron. (IECON)*, Orlando, FL, USA, Nov. 1995, pp. 6–10.
- [2] C. A. Ayres and I. Barbi, "A family of converters for UPS production burn-in energy recovery," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 615–622, Jul. 1997.
- [3] C. A. Ayres and I. Barbi, "CCM operation analysis of a family of converters for power recycling during the burn-in test of synchronized UPSs," in *Proc. 27th Annu. IEEE Power Electron. Specialists Conf.*, Baveno, Italy, Jun. 1996, pp. 23–27.
- [4] C. A. Ayres and I. Barbi, "Power recycler for DC power supplies burn-in test: Design and experimentation," in *Proc. Appl. Power Electron. Conf.* (APEC), San Jose, CA, USA, Mar. 1996, pp. 72–78.

- [5] DC/DC Burn-in Test Systems, Intepro System, Tustin, CA, USA, 2006.
- [6] K. I. Hwu and Y. T. Yau, "Active load for burn-in test of buck-type DC-DC converter with ultra-low output voltage," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, Austin, TX, USA, Feb. 2008, pp. 24–28.
- [7] K. I. Hwu and Y. H. Chen, "Design of a digitalized burn-in test plant," in *Proc. IEEE Int. Conf. Sustain. Energy Technol.*, Singapore, Nov. 2008, pp. 24–27.
- [8] G. Zulauf, W. Treichler, and J. Castelaz, "System, method, and results for the regenerative burn-in testing of high-power DC-DC converters," in *Proc. IEEE Transp. Electrific. Conf. Expo (ITEC)*, Dearborn, MI, USA, Jun. 2015, pp. 14–17.
- [9] B. O'Sullivan, R. Morrison, M. G. Egan, J. Slowey, and B. Barry, "A regenerative load system for the test of Intel VRM 9.1 compliant modules," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Anaheim, CA, USA, Feb. 2004, pp. 22–26.
- [10] D. F. B. Gomes, R. S. Vincenzi, C. Bissochi, J. B. Vieira, V. J. Farias, and L. C. Freitas, "A lossless commutated boost converter as an active load for burn-in application," in *Proc. 16th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Anaheim, CA, USA, Mar. 2001, pp. 4–8.
- [11] Y. Zhou, L. Wang, and X. Chen, "Research on digital controlled converter for AC power electronics burn-in test with energy feedback," in *Proc. Int. Conf. Elect. Mach. Syst.*, Wuhan, China, Oct. 2008, pp. 17–20.
- [12] J. Lu, M. Savaghebi, S. Golestan, J. C. Vasquez, J. M. Guerrero, and A. Marzabal, "Multimode operation for on-line uninterruptible power supply system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1181–1196, Jun. 2019.
- [13] N. A. Ahmed, B. N. Alajmi, I. Abdelsalam, and M. I. Marei, "Soft switching multiphase interleaved boost converter with high voltage gain for EV applications," *IEEE Access*, vol. 10, pp. 27698–27716, 2022.
- [14] X. Hao, I. Salhi, S. Laghrouche, Y. Ait-Amirat, and A. Djerdir, "Backstepping supertwisting control of four-phase interleaved boost converter for PEM fuel cell," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7858–7870, Jul. 2022.
- [15] R. Beiranvand and S. H. Sangani, "A family of interleaved high step-up DC-DC converters by integrating a voltage multiplier and an active clamp circuits," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8001–8014, Jul. 2022.
- [16] R. Rahimi, S. Habibi, M. Ferdowsi, and P. Shamsi, "An interleaved high step-up DC-DC converter based on integration of coupled inductor and Built-in-Transformer with switched-capacitor cells for renewable energy applications," *IEEE Access*, vol. 10, pp. 34–45, 2022.
- [17] J. Liu, Z. Liu, W. Chen, and H. Su, "Passivity-based control for interleaved double dual boost converters in DC microgrids supplying constant power loads," *IEEE Trans. Transport. Electrific.*, vol. 8, no. 2, pp. 1642–1655, Jun. 2022.
- [18] H. Dong, X. Xie, S. Xu, and H. Yu, "A novel current sharing scheme for two-phase interleaved LLC converter based on virtual controllable voltage sources," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1210–1216, Feb. 2022.
- [19] J. W. M. Soares and A. A. Badin, "An interleaved PFC boost converter with soft commutations and voltage follower characteristics," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 6732–6740, Jul. 2022.
- [20] Y.-C. Hsieh, H.-L. Cheng, E.-C. Chang, and W.-D. Huang, "A softswitching interleaved buck-boost LED driver with coupled inductor," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 577–587, Jan. 2022.
- [21] S. Y. Tseng, J. Z. Shiang, H. H. Chang, W. S. Jwoand, and C. T. Hsieh, "A novel turn-on/off snubber for interleaved boost converter," in *Proc. IEEE 38th Annu. Power Electron. Spec. Conf. (PESC)*, Jun. 2007, pp. 2718–2724.
- [22] T. Ishikawa, "Grid-connected photovoltaic power systems: Survey of inverter and related protection equipments," Int. Energy Agency, Paris, France, Tech. Rep. IEA-PVPS T5-05, Dec. 2002.
- [23] R. Hu, Z. Yan, L. Wang, M.-C. Wong, J. Zeng, J. Liu, and B. Hu, "An interleaved bidirectional coupled-inductor based DC–DC converter with high conversion ratio for energy storage system," *IEEE Trans. Ind. Electron.*, vol. 69, no. 6, pp. 5648–5659, Jun. 2022.
- [24] S. Upadhyay, S. Mishra, and A. Joshi, "A wide bandwidth electronic load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 733–739, Feb. 2012.
- [25] C. L. Chu and J. F. Chen, "Self-load bank for UPS testing by circulating current method," *IEE Proc. Electr. Power Appl.*, vol. 141, no. 4, pp. 191–196, Jul. 1994.

- [26] C. Wang, Y. Zou, K. Jia, F. Li, Y. Zhang, and X. She, "Research on the power electronic load based on repetitive controller," in *Proc.* 23rd Annu. IEEE Appl. Power Electron. Conf. Expo., Feb. 2008, pp. 1735–1740.
- [27] X. She, Y. Zou, C. Wang, L. Lin, J. Tang, and J. Chen, "Research on power electronic load: Topology, modeling, and control," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Washington, DC, USA, Feb. 2009, pp. 1661–1666.
- [28] Q. Yang, M. He, J.-H. Xu, X. Li, J. Zhu, Z. Zhang, Z. Gu, X. Ren, and Q. Chen, "Wide input voltage DC electronic load architecture with SiC MOSFETs for high efficiency energy recycling," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13053–13067, Dec. 2020.
- [29] J. Xu, Z. Zhang, M. He, J. Zhu, X. Li, Q. Yang, X. Wei, X. Ren, and Q. Chen, "Seamless transition mode control for SiC energy-recycling DC electronic loads," in *Proc. IEEE Appl. Power Electron. Conf. Expo.* (APEC), New Orleans, LA, USA, Mar. 2020, pp. 15–19.



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