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A Parallel Topology Based Power-Stage PMSM Emulator With Accurate Ripple Current Reproduced

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ABSTRACT As a power hardware-in-the-loop (PHIL) technology, the power-stage motor emulator (ME) can be employed for the port characteristics emulation of motors. Meanwhile, the ripple current reproduction is one of the key technologies for achieving the high precision emulation of the port characteristics. Commonly, the high requirement for the hardware topology and the modulation strategy with rapid response and low harmonics are the main challenges. Aiming to obtain the precision ripple current, a ME scheme with dual-branch parallel topology is proposed in this paper, of which the equivalent switching frequency can be increased greatly by mean of interleaving switch. Furthermore, a new three-level space vector modulation strategy based on the idea of virtual transformation is presented. With the proposed strategy, the dual-branch parallel topology can be equivalently transformed into a specific three-phase three-level back-to-back topology. Finally, simulation and bench experiments have been conducted to validate the effectiveness of the proposed scheme. The results indicate that the proposed topology combined with the modulation strategy has a superior performance in improving the ripple current tracking accuracy of ME. Moreover, the proposed method can provide an excellent insight into improving the emulation accuracy of motor characteristics in practical applications.

INDEX TERMS Motor emulator, three-level space vector modulation (3-level SVM), power hardware-in-the-loop.

I. INTRODUCTION

Nowadays, with the rapid development of the new energy vehicle industry, permanent magnet synchronous motor (PMSM) has been widely used due to its high efficiency, high power density, and low torque fluctuation [1]. Meanwhile, the shorter development cycle has put forward higher requirements for the testing methods of electric drive systems [2]. As a PHIL system that emulates motors, power-stage ME can provide efficient and convenient verification of electric drive systems [3]. Both ME and the motor can be regarded as a black box circuit with three ports. They are expected to have the same port characteristics, that is, when the same voltage is applied to the port, they will respond to the same current and current change rate as the motor. More importantly, reproducing the switching ripple current usually has an important influence on the actual motor characteristics emulation and drive performance verification of the motor control unit (MCU).

Commonly, the traditional PHIL system of power-stage ME employs a dual-inverter back-to-back topology [4]. In this case, the inverter capacity of ME and MCU is similar and faces the same switching performance bottleneck, so the switching frequency of ME can't be increased significantly. Therefore, only fundamental current can be reproduced with high precision and the ripple current is ignored. However, ripple current has important effects on MCU control performance, weak magnetic performance, eddy current loss, torque pulsation, noise, parameter identification and fault injection. the traditional ME that only reproduce sinusoidal fundamental current is too ideal, which is easier to control than the actual motor and cannot verify the real performance of MCU and motor. Only by improving the current tracking accuracy can the ME be closer to an actual motor and the actual performance of the MCU can be verified. To obtain the high precision ripple current, scholars have researched

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different topology schemes and modulation strategies. According to the types of power units, the power-stage ME can be divided into the linear power amplifier (LPA) and the inverter.

LPA is considered as one of the most ideal implementations in reproducing high-frequency ripple current for its excellent ability to output an arbitrary voltage and extremely fast response speed. A high-bandwidth LPA along with a high-precision finite element motor model is adopted in literature [5]–[8] to emulate the operation of different motors under specific conditions, including open-winding motors [5], PMSM [6], variable flux motors [8], and motors injected with open-circuit fault injection [7]. Usually, the current change rate at the commutation instant of brushless DC motor (BLDC) is quite high, leading to higher requirements in dynamic performances of ME. To improve the emulation accuracy of the BLDC commutation process, a solution based on LPA is proposed to reproduce the harmonic current of BLDC precisely [9]. However, it cannot be ignored that LPA is not very competitive in terms of energy conversion efficiency (the peak efficiency can reach 78.5% theoretically). In high-power motor emulations, LPA will generate a huge amount of heat, leading to a bulky heat dissipation structure for thermal damage protection [10]. Compared with LPA, the inverter based on pulse width modulation has a significant advantage in achieving efficient conversion, which has more attractive for academics aiming to optimize the ME scheme.

Currently, research on the optimization of inverter-based ME is carried out through several methodologies, including increasing the number of levels, improving the switching frequency, and optimizing the modulation strategy.

A COMPISO digital amplifier (CDA) based on a multiphase interleaved inverter is proposed in [11] to replace the LPA. Six bridges achieve an equivalent frequency of 125kHz through interleaving switches and then output a continuous voltage through coupled inductors and filters. Compared with linear amplifiers, digital amplifiers reduce losses obviously, but their structure is more complex. But the coupled inductors and filters of digital amplifiers produce additional losses compared to the traditional inverter-based structures. Literature [12] indicates that the output filter plays an important role in attenuating the output voltage harmonics, but it also brings additional losses and weakens the dynamic performance. In [13], SiC power semiconductor devices are introduced to a traditional two-level back-to-back topology, making it possible to significantly increase the switching frequency as well as the bandwidth of the current loop. However, when the MCU is equipped with a SiC-based inverter [14], the switching performance of the SiC-based ME is still a bottleneck. Under the circumstance that the switching frequency is limited by hardware, the multi-level inverter can be an effective alternative to increase the equivalent switching frequency [15]–[17]. A modular-multilevel-converter (MMC) on basis of carrier phase-shift control is put forward in [16], which helps realize the application of ME in the field of medium/high-voltage asynchronous motor emulation. A multi-phase coupling multi-level topology is adopted in [17]. The multiple parallel branches of which realize multi-level output through the common-mode inductor coupling and thus improve the dynamic current tracking capability of ME. However, the complex common-mode coupling network will increase the loss and volume of the system.

In order to obtain the precision ripple current of ME, a novel scheme based on a dual-branch parallel topology and a corresponding virtual three-level modulation strategy is proposed in this paper. Thanks to the property of higher switching frequency, the ME based on this solution can be used to reserve the ripple current more effectively. And thus, more accurately motor port characteristics can be emulated. The proposed topology has two branches for each phase. Therefore, the capacity of each branch can be reduced and the switching frequency is increased effectively. Furthermore, a corresponding modulation strategy is proposed to modulate the parallel topology as a virtual three-level topology with space vector modulation. By adopting this strategy, the switching actions of each bridge are interleaved to double the switching frequency, and inverter harmonics are further suppressed by optimizing output vector sequences.

The rest of this paper is organized as follows. The basic structure and the principle of the power-stage ME are introduced in Section II. Section III presents the method of equivalenting the two-level parallel topology to a three-level topology. Moreover, the virtual three-level space vector modulation strategy is illustrated in this section. The effectiveness of the proposed scheme is verified through the simulation and experiment in Section IV. Finally, the conclusions are drowned in the last section.

II. BASIC PRINCIPLES OF THE POWER-STAGE ME

A. TRADITIONAL STRUCTURE OF POWER-STAGE ME

Generally, the ME can be approximately regarded as an actual motor when connected to the MCU. A traditional structure of power-stage ME is presented in Fig. 1.

As is shown in Fig. 1, the structure of the traditional ME mainly consists of a DC power supply, an inverter (MCU), a connecting network, a signal acquisition system, a real-time motor model, and a current tracking controller [18], [19]. Usually, the MCU and ME are powered by two isolated DC power supplies to avoid the common-mode loop [20]. The signal acquisition system supervises the output voltage of the MCU with a high sampling rate, and the real-time motor model calculates the target current of the ME. With the regulation of the current tracking controller, the target current is accurately tracked by the inverter and connecting network. The connecting network generally consists of three independent inductors.

B. THE REAL-TIME MODEL OF PMSM

The approximation to a real motor and its real-time performance are two key challenges in PMSM real-time

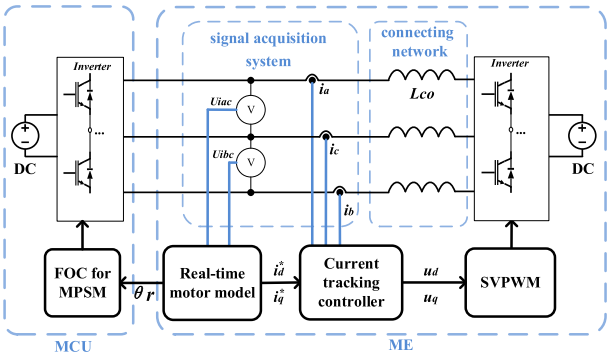

FIGURE 1. System structure of motor emulator.

modeling [21]–[23]. The mathematical models and finite element models are commonly used as real-time motor models in ME. The finite element models can precisely emulate the nonlinear characteristics of motors [6]. However, a finite element model is quite hard to implement in real-time applications due to the high computation load. Therefore, the finite element model is usually computed offline in advance and then used in real-time system in the form of look-up table. The mathematical model is adopted as the real-time motor model for its simple calculation and configurable parameters [24], while it is not as precise as the finite element model. Considering the focus of this paper is not the accuracy of the motor model but the accuracy of current tracking, a simple constant parameter mathematical model based on dq axis is adopted to guarantee the real-time calculations of current control.

In general, ME collects line voltages as the input voltage of the motor model, since the common PMSM for vehicles are three-phase three-wire system without neutral point extraction. Firstly, transform the port voltage from abc axis to $\alpha\beta$ axis through coordinate transformation:

$$\begin{cases} u_{\alpha}^{mcu} = \dfrac{2}{3}u_{ac}^{mcu} - \dfrac{1}{3}u_{bc}^{mcu} \\ u_{\beta}^{mcu} = \dfrac{\sqrt{3}}{3}u_{bc}^{mcu} \end{cases} \tag{1}$$

where u_{ac}^{mcu} and u_{bc}^{mcu} are the line voltages of the three-phase port, respectively. u_{α}^{mcu} and u_{β}^{mcu} are the port voltages in $\alpha\beta$ axis, respectively.

Next, transform the voltage to the dq axis:

$$\begin{cases} u_{d}^{mcu} = u_{\alpha}^{mcu}cos\theta + u_{\beta}^{mcu}sin\theta \\ u_{q}^{mcu} = -u_{\alpha}^{mcu}sin\theta + u_{\beta}^{mcu}cos\theta \end{cases} \tag{2}$$

where θ is the electrical angle between the d axis and α axis. u_{d}^{mcu} and u_{q}^{mcu} are the port voltages in dq axis.

The electromagnetic equation of PMSM based on dq axis can be expressed as:

$$\begin{cases} u_{d}^{mcu} = R_s i_d^* + \dfrac{di_d^*}{dt}L_d - \omega_e i_q^* L_q \\ u_{q}^{mcu} = R_s i_q^* + \dfrac{di_q^*}{dt}L_q + \omega_e i_d^* L_d + \omega_e \psi_f \end{cases} \tag{3}$$

where R_s is the stator resistance. L_d and L_q are the inductance of the PMSM, respectively. ψ_f is the flux linkage of the permanent magnet. ω_e is the electrical angular velocity. i_d^* and i_q^* are the current of the motor model, which will be used as reference values for the current controller.

Finally, to obtain the current calculation formula, equation (3) can be discretized as (4), shown at the bottom of the page, where T_s is the calculation period of the real-time motor model.

The electromagnetic torque equation of PMSM can be expressed as:

$$T_e(k) = \frac{3}{2}P_n\left[\psi_f i_q^*(k) + \left(L_d - L_q\right) i_d^*(k)\, i_q^*(k)\right] \tag{5}$$

where P_n is the pole pairs of PMSM.

The mechanical equation of the motor can be expressed as:

$$\omega_e(k) = \omega_e(k-1) + \frac{P_n T_e(k) - P_n T_L(k-1) + B\omega_e(k-1)}{J} \tag{6}$$

where T_L is the load torque, B is the damping coefficient, and J is the rotor inertia.

C. PORT CHARACTERISTICS AND CURRENT TRACKING STRATEGY OF ME

In a traditional back-to-back topology, the circuit of each phase can be equivalent to two voltage sources connected through a series LR network. The port characteristics of the ME can be expressed as:

$$\begin{cases} u_{a}^{mcu} - u_a = i_a R_{co} + \dfrac{di_a}{dt}L_{co} \\ u_{b}^{mcu} - u_b = i_b R_{co} + \dfrac{di_b}{dt}L_{co} \\ u_{c}^{mcu} - u_c = i_c R_{co} + \dfrac{di_c}{dt}L_{co} \end{cases} \tag{7}$$

where u_{a}^{mcu}, u_{b}^{mcu} and u_{c}^{mcu} are the port voltages of three-phase, which are the output voltages of the MCU-side inverter. u_a, u_b and u_c are the output voltages of the ME-side inverter, respectively. L_{co} is the connecting inductance, R_{co} is the resistance of connecting inductors. i_a, i_b and i_c

$$\begin{cases} i_d^*(k) = i_d^*(k-1) + \dfrac{T_s\left[u_d^{mcu}(k) - R_s i_d^*(k-1) + \omega_e(k-1)\, i_q^*(k-1)\, L_q\right]}{L_d} \\ i_q^*(k) = i_q^*(k-1) + \dfrac{T_s\left[u_q^{mcu}(k) - R_s i_q^*(k-1) - \omega_e(k-1)\, i_d^*(k-1)\, L_d\right]}{L_q} \end{cases} \tag{4}$$

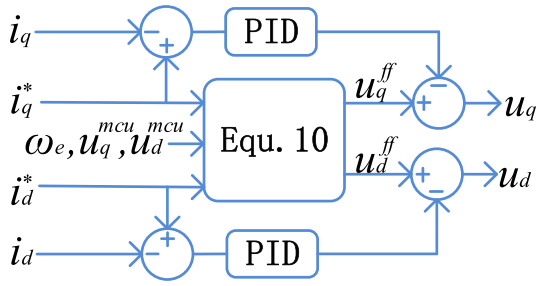

FIGURE 2. Feedforward current controller.

are three-phase current, respectively. It should be noticed that the reference directions are positive in the direction of flow into ME.

The port characteristics based on dq axis can be expressed as:

$$\begin{cases} u_d = u_d^{mcu} - R_{co} i_d - L_{co} \dfrac{di_d}{dt} + \omega_e L_{co} i_q \\ u_q = u_q^{mcu} - R_{co} i_q - L_{co} \dfrac{di_q}{dt} - \omega_e L_{co} i_d \end{cases} \tag{8}$$

The current control algorithm is also an important factor affecting the current tracking performance. The traditional current tracking algorithms based on FOC and PID algorithms have good performance for fundamental current tracking, but poor performance for high-frequency ripple current [25]. In order to effectively increase the response speed and bandwidth of the PID controller, a voltage feedforward method is presented in this work, and the block diagram of the modified current controller is shown in Fig. 2. As shown in Fig. 2, the output voltage is mainly determined by the feedforward method. Meanwhile, the residual can be eliminated by PID.

Equations (3) and (8) are the circuit equations of PMSM and ME respectively. When PMSM and ME have the same port characteristics, they will have the same current and current change rate under the same input voltage excitation. It can be expressed as equation (9).

$$\begin{cases} i_d^* = i_d \\ i_q^* = i_q \\ \dfrac{di_d^*}{dt} = \dfrac{di_d}{dt} \\ \dfrac{di_q^*}{dt} = \dfrac{di_q}{dt} \end{cases} \tag{9}$$

The ideal voltage of the ME-side can be obtained by combining (9) with (3) and (8), which will be used as the feedforward term of the current controller. The feedforward term can be expressed as (10), and the final output voltage is given by (11).

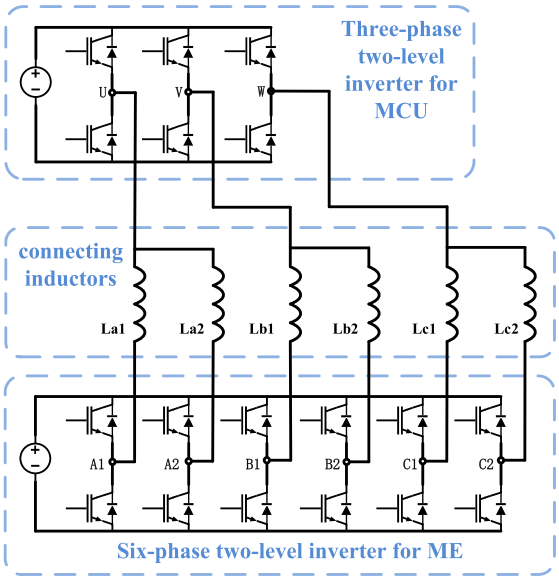

FIGURE 3. Dual-branch parallel topology.

$$\begin{cases} u_d^{ff} = u_d^{mcu}\left(1 - \dfrac{L_{co}}{L_d}\right) + i_d^*\left(R_s \dfrac{L_{co}}{L_d} - R_{co}\right) \\ \qquad\qquad - \omega_e i_q^* L_q \dfrac{L_{co}}{L_d} \\ u_q^{ff} = u_q^{mcu}\left(1 - \dfrac{L_{co}}{L_q}\right) + i_q^*\left(R_s \dfrac{L_{co}}{L_q} - R_{co}\right) \\ \qquad\qquad + \omega_e \left(i_d^* L_d + \psi_f\right) \dfrac{L_{co}}{L_q} \end{cases} \tag{10}$$

$$\begin{cases} u_d = u_d^{ff} - k_p\left(i_d^* - i_d\right) - k_i \int \left(i_d^* - i_d\right) \\ u_q = u_q^{ff} - k_p\left(i_q^* - i_q\right) - k_i \int \left(i_q^* - i_q\right) \end{cases} \tag{11}$$

where k_p is the proportion factor and k_i is the integration factor.

It can be seen from (10) that both u_d^{ff} and u_q^{ff} have three terms. The first term is related to u_d^{mcu} and u_q^{mcu}, while u_d^{mcu} and u_q^{mcu} are square wave voltage, which is a step excitation. PID has a good control effect for DC signal output, but for the case of large step signal output, PID is easy to overshoot oscillation when the gain is large, and the response speed is slow when the gain is small. In this paper, u_d^{ff} and u_q^{ff} are directly output as feedforward signals, and the remaining residual is adjusted by PID feedback. Since PID output is adjusted at a small value near 0, a faster response can be achieved, so the bandwidth of the controller can be increased.

III. PROPOSED PARALLEL TOPOLOGY AND MODULATION STRATEGY

A. PROPOSED DUAL-BRANCH PARALLEL TOPOLOGY AND ITS EQUIVALENT ANALYSIS

The power-stage motor emulation system based on dual-branch parallel topology is shown in Fig. 3. As shown in Fig. 3, the proposed parallel topology has a simple structure

TABLE 1. Comparison of topology.

Topology	Cost	Loss	Volume	Complexity
LPA [6]	High	High	Large	Mid
MMC [16]	High	Mid	Large	High
CDA [11]	Mid	Mid	Mid	High
SiC [14]	High	Low	Small	Low
Propose	Low	Low	Small	Low

and every two parallel branches constitute one phase. The connecting inductors are independent without mutual induction, and have the same parameters, thus ensuring the balance of each branch. The bridge current of each branch in the proposed topology is only half of the conventional topology. The low-capacity bridge, as well as interleaving switches, help achieve a high equivalent switching frequency.

Although 6 connecting inductors are used in the proposed parallel topology, the current, volume and cost of each inductor are reduced because the power flow is split from three-phase to six-phase. Compared with the traditional three-phase bridge topology with three connecting inductors, the total cost and volume of the topology in this paper do not increase significantly. Table 1 analyzes and compares the linear power amplifier (LPA) [6], MMC [16], COMPISO digital amplifier (CDA) [11], SIC [14] and the proposed topology. It can be seen from Table 1 that the proposed topology has comprehensive advantages in cost, loss, volume and complexity.

The inverters of MCU and ME are both two-level voltage sources. The circuit equation for phase A can be expressed as:

$$\begin{cases} u_a^{mcu} - u_{dc}S_{a1} = i_{a1}R_{a1} + \dfrac{di_{a1}}{dt}L_{a1} \\ u_a^{mcu} - u_{dc}S_{a2} = i_{a2}R_{a2} + \dfrac{di_{a2}}{dt}L_{a2} \end{cases} \tag{12}$$

where u_{dc} is the bus voltage of ME. S_{a1} and S_{a2} are the switch status of bridges A1 and A2, respectively. L_{a1} and L_{a2} are the connecting inductance. R_{a1} and R_{a2} are the internal resistance of the connecting inductor. i_{a1} and i_{a2} are the branch current.

Equation (13) then can be obtained by combining the two equations in (12). Conspicuously, equation (13) is similar to (7), so it can be equivalent to a virtual back-to-back topology with a three-level three-phase inverter as is shown in Fig. 4. Therefore, the equivalent topology can be modulated by a three-level modulation strategy.

$$\begin{cases} u_a^{mcu} - u_{dc}\dfrac{S_{a1}+S_{a2}}{2} = i_aR_{co} + \dfrac{di_a}{dt}L_{co} \\ i_a = i_{a1} + i_{a2} \\ R_{co} = \dfrac{L_{a1}+L_{a2}}{2} \\ L_{co} = \dfrac{L_{a1}+L_{a2}}{2} \end{cases} \tag{13}$$

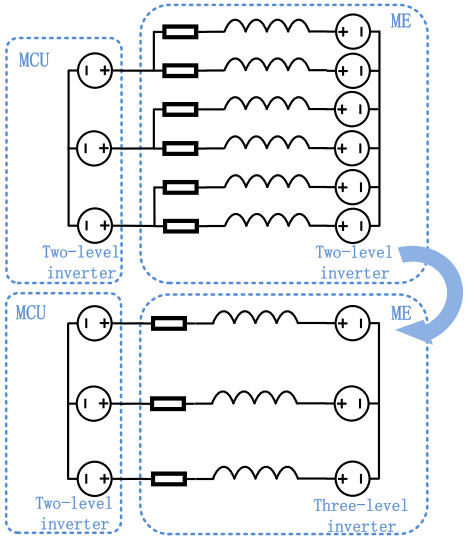

FIGURE 4. Two-level equivalent to three-level.

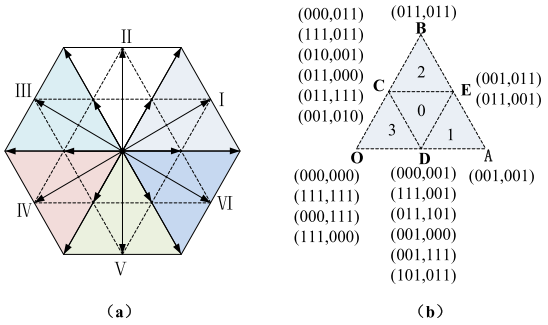

FIGURE 5. Virtual three-level vector space. (a) Three-level vector space. (b) Redundant states of sector I.

where $\frac{S_{a1}+S_{a2}}{2}$ has three states, so it can be equivalent to a three-level voltage source. And the new inductor is equivalent to two branch inductors connected in parallel.

B. PROPOSED VIRTUAL THREE-LEVEL MODULATION STRATEGY

Traditional three-phase two-level vector space is a regular hexagon, which can be divided into 6 sectors, and 8 switching states can output 6 active vectors. While the virtual three-level topology has 64 switching states and 18 active vectors as is shown in Fig. 5 (a). Due to the switching states being much more than vectors, the virtual three-level topology has many redundant switch states. The redundant states of sector I are shown in Fig. 5 (b). For example, the output vector V_{OE} has two switching states (001, 011) and (011, 001), which indicates the switching state of bridges A1, B1, C1, A2, B2, C2 in turn. The traditional two-level SVPWM has been widely used, but it cannot be directly extended to three-level space. Aiming at the virtual three-level topology, a novel virtual three-level space vector modulation method is proposed in this paper, and the detailed process is described below.

Firstly, similar to two-level SVPWM, the first step is to determine which sector the target voltage is located in. The traditional method is to determine sectors by the phase angle of target voltage, but it needs a complex inverse trigonometric function. In order to simplify the calculation, the phase voltage comparison method is adopted to determine the sector in this paper.

Convert the target vector from dq axis into abc axis:

$$\begin{cases} u_\alpha = cos\theta u_d - sin\theta u_q \\ u_\beta = sin\theta u_d + cos\theta u_q \end{cases} \tag{14}$$

$$\begin{cases} u_a = u_\alpha \\ u_b = -\frac{1}{2}u_\alpha + \frac{\sqrt{3}}{2}u_\beta \\ u_c = -\frac{1}{2}u_\alpha - \frac{\sqrt{3}}{2}u_\beta \end{cases} \tag{15}$$

Determine the sector by comparing the amplitude of u_a, u_b, and u_c. The rules for sector division are expressed as (16).

$$Sector = \begin{cases} \text{I}, & if\ \ (u_a \geq u_b \geq u_c); \\ \text{II}, & if\ \ (u_b \geq u_a \geq u_c); \\ \text{III}, & if\ \ (u_b \geq u_c \geq u_a); \\ \text{IV}, & if\ \ (u_c \geq u_b \geq u_a); \\ \text{V}, & if\ \ (u_c \geq u_a \geq u_b); \\ \text{VI}, & if\ \ (u_a \geq u_c \geq u_b); \end{cases} \tag{16}$$

After the sector is determined, the target vector can be decomposed into three vertices of the sector, and the duty cycles then can be calculated. Suppose the target vector is located in sector I, the vector can be decomposed into V_{OA}, V_{OB}, and V_{OC}. And the duty cycles can be calculated as:

$$\begin{cases} T_{OA} = \dfrac{u_a - u_b}{u_{dc}} \\ T_{OB} = \dfrac{u_b - u_c}{u_{dc}} \\ T_O = 1 - T_{OA} - T_{OB} \end{cases} \tag{17}$$

In the space vector modulation method, the best way to synthesize a target vector is to combine the closest group of vectors, which are the three vertices of the sector. While in virtual three-level vector space, each large sector can be further divided into four subsectors. The division rules of the subsector are expressed in (18) and the subsector division of sector I is shown in Fig. 5 (b).

$$Subsector = \begin{cases} 1, & if\ \ (T_{OA} \geq 0.5); \\ 2, & else\ if\ \ (T_{OB} \geq 0.5); \\ 3, & else\ if\ \ (T_{OA} + T_{OB} < 0.5); \\ 0, & else; \end{cases} \tag{18}$$

Secondly, after determining which subsector the target vector is located in, calculate the duty cycle of the optimal vector combination. For example, if the target vector is located in subsector-0, the best way to synthesize the target vector is to select V_{OC}, V_{OD}, and V_{OE}. The duty cycle of each vector can be expressed as:

$$subsector0: \begin{cases} T_{OC} = 1 - 2T_{OA} \\ T_{OD} = 1 - 2T_{OB} \\ T_{OE} = 1 - T_{OC} - T_{OD} \end{cases} \tag{19}$$

Similarly, when the target vector falls in other subsectors, the synthesis method can be represented as follows:

$$subsector1: \begin{cases} T_{OD} = 2T_O \\ T_{OE} = 2T_{OB} \\ T_{OA} = 1 - T_{OD} - T_{OE} \end{cases} \tag{20}$$

$$subsector2: \begin{cases} T_{OC} = 2T_O \\ T_{OE} = 2T_{OA} \\ T_{OB} = 1 - T_{OC} - T_{OE} \end{cases} \tag{21}$$

$$subsector3: \begin{cases} T_{OD} = 2T_{OA} \\ T_{OC} = 2T_{OB} \\ T_{OO} = 1 - T_{OC} - T_{OD} \end{cases} \tag{22}$$

Finally, determine an optimal output sequence from the redundant states, since the same vector can have multiple corresponding switching states in the three-level space. According to the following principles, this paper exhaustively arranges all the possible switch states and optimizes an optimal switch sequence group, which is shown in Table 2.

(1) During each switching period, the switching state of each bridge changes twice. In this way, the initial state and final state of the bridge can be guaranteed to be consistent in one subsector, which is conducive to realizing modulation by the sawtooth wave comparison method.

(2) During each switching period, ensure that the voltage integral values of two branches are equal, to inhibit the common-mode current between parallel branches.

(3) Each switch action is staggered, and the two adjacent states correspond to different output vectors. In this way, the switching action can be fully utilized to increase the equivalent switching frequency.

(4) The interchanging state of A1-B1-C1-A2-B2-C2 and A2-B2-C2-A1-B1-C1 are regarded as the same sequence.

(5) Two sets of switches in reverse order are regarded as the same switch sequence. For example, V_{OC}, V_{OD}, V_{OE} and V_{OE}, V_{OD}, V_{OC} are considered the same sequence.

As shown in Table 2, when the target vector is located in subsector 0, the preferred sequence of the vector is V_{OE}, V_{OC}, V_{OE}, V_{OD}, V_{OC}, V_{OD}, V_{OE}, V_{OC}, V_{OE}, V_{OD}, V_{OC}, V_{OD}, and V_{OE}. Meanwhile, the corresponding duty ratio for each vector is $\frac{T_{OE}}{8}$, $\frac{T_{OC}}{4}$, $\frac{T_{OE}}{4}$, $\frac{T_{OD}}{4}$, $\frac{T_{OC}}{4}$, $\frac{T_{OD}}{4}$, $\frac{T_{OE}}{4}$, $\frac{T_{OC}}{4}$, $\frac{T_{OE}}{4}$, $\frac{T_{OD}}{4}$, $\frac{T_{OC}}{4}$, $\frac{T_{OD}}{4}$, and $\frac{T_{OE}}{8}$ in turn. The switch states of the six bridges can be obtained by comparing the duty ratio with a sawtooth timer

TABLE 2. Vector output sequence of sector I.

Sub-Sector 0	Switch state	$A_1B_1C_1$	001	001	001	101	111	111	011	010	011	011	011	001	001
		$A_2B_2C_2$	011	010	011	011	011	001	001	001	001	101	111	111	011
	Output vector		V_{OE}	V_{OC}	V_{OE}	V_{OD}	V_{OC}	V_{OD}	V_{OE}	V_{OC}	V_{OE}	V_{OD}	V_{OC}	V_{OD}	V_{OE}
	Duty cycle		$\frac{T_{OE}}{8}$	$\frac{T_{OC}}{4}$	$\frac{T_{OE}}{4}$	$\frac{T_{OD}}{4}$	$\frac{T_{OC}}{4}$	$\frac{T_{OD}}{4}$	$\frac{T_{OE}}{4}$	$\frac{T_{OC}}{4}$	$\frac{T_{OE}}{4}$	$\frac{T_{OD}}{4}$	$\frac{T_{OC}}{4}$	$\frac{T_{OD}}{4}$	$\frac{T_{OE}}{8}$
Sub-Sector 1	Switch state	$A_1B_1C_1$	001	000	001	011	111	011	001	001	001	001	001	001	001
		$A_2B_2C_2$	001	001	001	001	001	001	001	000	001	011	111	011	001
	Output vector		V_{OA}	V_{OD}	V_{OA}	V_{OE}	V_{OD}	V_{OE}	V_{OA}	V_{OD}	V_{OA}	V_{OE}	V_{OD}	V_{OE}	V_{OA}
	Duty cycle		$\frac{T_{OA}}{8}$	$\frac{T_{OD}}{4}$	$\frac{T_{OA}}{4}$	$\frac{T_{OE}}{4}$	$\frac{T_{OD}}{4}$	$\frac{T_{OE}}{4}$	$\frac{T_{OA}}{4}$	$\frac{T_{OD}}{4}$	$\frac{T_{OA}}{4}$	$\frac{T_{OE}}{4}$	$\frac{T_{OD}}{4}$	$\frac{T_{OE}}{4}$	$\frac{T_{OA}}{8}$
Sub-Sector 2	Switch state	$A_1B_1C_1$	011	111	011	001	000	001	011	011	011	011	011	011	011
		$A_2B_2C_2$	011	011	011	011	011	011	011	111	011	001	000	001	011
	Output vector		V_{OB}	V_{OC}	V_{OB}	V_{OE}	V_{OC}	V_{OE}	V_{OB}	V_{OC}	V_{OB}	V_{OE}	V_{OC}	V_{OE}	V_{OB}
	Duty cycle		$\frac{T_{OB}}{8}$	$\frac{T_{OC}}{4}$	$\frac{T_{OB}}{4}$	$\frac{T_{OE}}{4}$	$\frac{T_{OC}}{4}$	$\frac{T_{OE}}{4}$	$\frac{T_{OB}}{4}$	$\frac{T_{OC}}{4}$	$\frac{T_{OB}}{4}$	$\frac{T_{OE}}{4}$	$\frac{T_{OC}}{4}$	$\frac{T_{OE}}{4}$	$\frac{T_{OB}}{8}$
Sub-Sector 3	Switch state	$A_1B_1C_1$	000	001	011	111	111	111	111	011	001	000	000	000	000
		$A_2B_2C_2$	111	111	111	111	011	001	000	000	000	000	001	011	111
	Output vector		V_{OO}	V_{OD}	V_{OC}	V_{OO}	V_{OC}	V_{OD}	V_{OO}	V_{OC}	V_{OD}	V_{OO}	V_{OD}	V_{OC}	V_{OO}
	Duty cycle		$\frac{T_{OO}}{8}$	$\frac{T_{OD}}{4}$	$\frac{T_{OC}}{4}$	$\frac{T_{OO}}{4}$	$\frac{T_{OC}}{4}$	$\frac{T_{OD}}{4}$	$\frac{T_{OO}}{4}$	$\frac{T_{OC}}{4}$	$\frac{T_{OD}}{4}$	$\frac{T_{OO}}{4}$	$\frac{T_{OD}}{4}$	$\frac{T_{OC}}{4}$	$\frac{T_{OO}}{8}$

by (23)-(28). The other cases are similar.

$$S_{A1} = \begin{cases} 1, & if \left(\frac{3T_{OE}}{8} + \frac{T_{OC}}{4} < T_{tim} \right. \\ & \left. \leq \frac{T_{OE}}{8} + \frac{T_{OC}}{2} + \frac{T_{OD}}{2}\right) \\ 0, & else; \end{cases}$$

$$S_{B1} = \begin{cases} 1, & if \left(\frac{3T_{OE}}{8} + \frac{T_{OC}}{4} + \frac{T_{OD}}{4} < T_{tim} \right. \\ & \left. \leq 1 - \frac{T_{OE}}{8} - \frac{T_{OD}}{4}\right) \\ 0, & else; \end{cases}$$

$$S_{C1} = \begin{cases} 0, & if \left(\frac{T_{OC}}{2} + \frac{T_{OD}}{2} + \frac{5T_{OE}}{8} < T_{tim} \right. \\ & \left. \leq \frac{3T_{OC}}{4} + \frac{T_{OD}}{2} + \frac{5T_{OE}}{8}\right) \\ 1, & else; \end{cases}$$

$$S_{A2} = \begin{cases} 1, & if \left(\frac{7T_{OE}}{8} + \frac{3T_{OC}}{4} + \frac{T_{OD}}{2} < T_{tim} \right. \\ & \left. \leq 1 - \frac{T_{OE}}{8}\right) \\ 0, & else; \end{cases}$$

$$S_{B2} = \begin{cases} 0, & if \left(\frac{3T_{OE}}{8} + \frac{T_{OC}}{2} + \frac{T_{OD}}{4} < T_{tim} \right. \\ & \left. \leq \frac{3T_{OC}}{4} + \frac{3T_{OD}}{4} + \frac{7T_{OE}}{8}\right) \\ 1, & else; \end{cases}$$

$$S_{C2} = \begin{cases} 0, & if \left(\frac{T_{OE}}{8} < T_{tim} \leq 1 - \frac{T_{OE}}{8} + \frac{T_{OC}}{4}\right) \\ 1, & else; \end{cases}$$

(23)-(28)

where T_{tim} is a sawtooth counter cycle between 0 to 1 representing the switching period.

IV. SIMULATION AND EXPERIMENT RESULTS

A. SIMULATION RESULTS

To verify the effectiveness of the proposed three-level modulation strategy, a simulation model is built based on Matlab/Simulink. Three strategies are compared in this paper. The traditional strategy is based on the two-level topology with SVPWM. The phase shift strategy is based on the dual-branch parallel topology with the two branches' switch action staggered by 90° [26]. The switching frequency of each bridge is set to 20 kHz in the simulation.

Firstly, the target vector is set at the center of sector 1 as shown in Fig. 6 (a), and the output waveforms of the inverter within one period are obtained through simulation. Then, the output vector composition sequences under different strategies are plotted in Fig. 6 (b) (c) (d). Fig. 6 (b) shows that the traditional strategy uses V_{OO}, V_{OA}, and V_{OB} to compose the target vector in 6 steps. Fig. 6 (c) indicates that the phase shift method uses V_{OA}, V_{OC}, V_{OD}, and V_{OE} in 8 steps. While the proposed strategy is even better as it utilizes V_{OC}, V_{OD}, and V_{OE} three closest vectors in 12 steps with more detailed

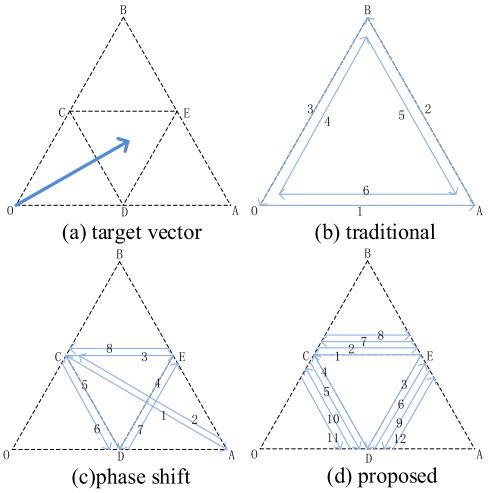

FIGURE 6. Vector synthesis paths.

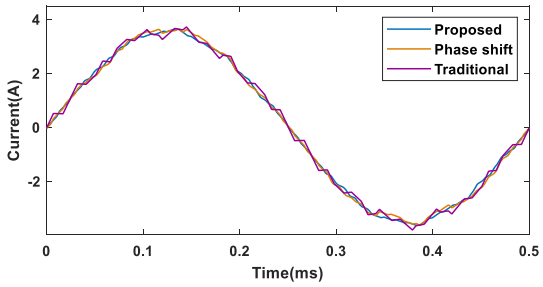

FIGURE 7. Simulation current result at $m = 0.8$.

segmentation as shown in Fig. 6 (d). Closer vectors with more steps benefit to reduce voltage harmonics.

Furthermore, to prove the adaptability of the proposed strategy in every subsector, a simulation comparison under different modulation ratios is carried out. To further compare the ripple current, the current closed-loop controller is omitted, and pure inductors are used as loads. The fundamental frequency is set to 2 kHz, the load inductance is set to 280 uH, the bus voltage is set to 42V, and the modulation ratio m is set from 0.1 to 1.1.

Fig. 7 shows the simulation current of phase A with $m = 0.8$. In order to comprehensively compare the performance under different modulation ratios, the current THD of the three strategies with m from 0.1 to 1.1 is presented in Fig. 8. When $m < 0.6$, The THD of the proposed strategy is 50% lower than that of the traditional strategy and slightly smaller than that of the phase shift strategy. When $m > 0.7$, the THD of the proposed strategy further decreases, with 40% lower than the phase shift strategy and 50% lower than the traditional strategy. The THD results show that the proposed modulation strategy has the minimum background harmonics in the whole modulation range compared with traditional and phase shift strategies.

B. EXPERIMENT RESULTS

In order to verify the superior ripple current tracking effect of the proposed ME scheme, an experimental system is designed. Fig. 9 shows the experimental equipment, which consists of ME, MCU, power supplies, and host computer.

The physical drawing of the experimental equipment is shown in Fig. 10. The ME and MCU are powered separately to eliminate common-mode loops. The host computer used for parameter configuration and data acquisition is connected to ME and MCU by CAN bus. MCU is a three-phase inverter based on the FOC algorithm. ME consists of a six-phase inverter, connecting inductors, current sensors, and a DSP. The experimental system is developed based on TMS32F28377D, which is a high-performance dual-core DSP with a high conversion rate ADC, rich peripherals, and

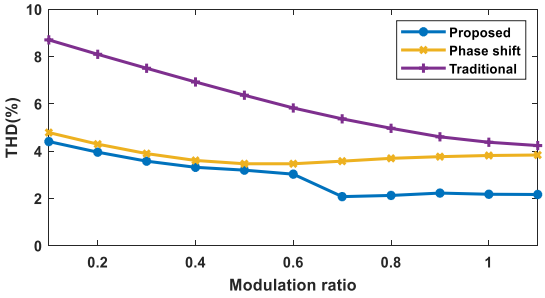

FIGURE 8. THD of current with different m.

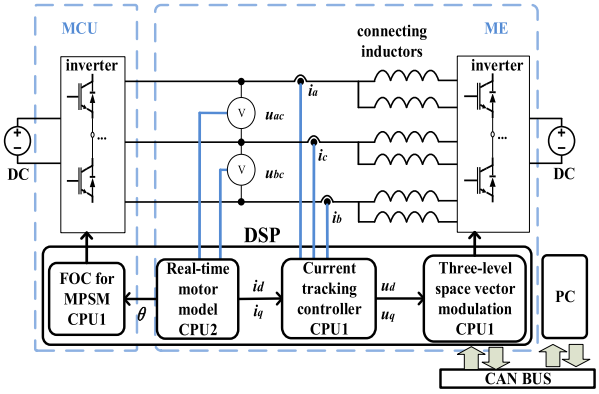

FIGURE 9. Block diagram of experimental setup.

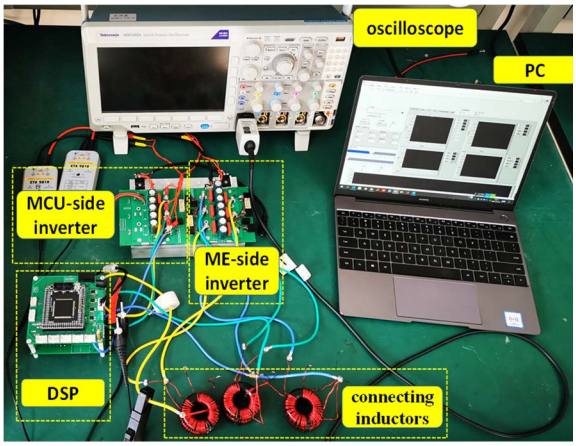

FIGURE 10. Experimental setup.

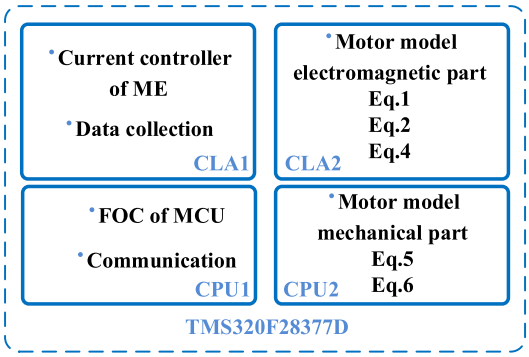

FIGURE 11. Task assignment in DSP.

TABLE 3. Configuration parameter of experiment.

parameter	symbol	value
Permanent flux linkage	ψ_f	0.05 Wb
D axis inductance	L_d	280 uH
Q axis inductance	L_q	280 uH
Motor model period	T_s	1.25 us
ME switching frequency	$f_{swc,ME}$	20k Hz
MCU switching frequency	$f_{swc,MCU}$	10kHz
resistance of inductor	R_{co}	50mΩ
connecting inductance	L_{co}	280mH
Bus voltage	u_{dc}	42V
Target current	i_{ref}	10A
Electric frequency	f_e	50Hz

IO ports. TMS320F28377D has two cores CPU1 and CPU2, each of which has a control law accelerator (CLA), which can be viewed as four parallel cores.

The mathematical motor model based on DQ axis mentioned in Section II is adopted here, which is configured as a surface permanent magnet synchronous motor (SPMSM). To simplify the system, the control algorithm of MCU and ME are executed in one TMS32F28377D, which omits the position sensor and wire harness between ME and MCU. The task assignment in the DSP cores is assigned as Fig. 11: CPU2 and CLA2 undertake the calculation of the real-time motor model. In order to minimize the iteration cycle to improve the model accuracy, the motor model is divided into two parts for parallel computation in different cores. The electromagnetic part (Eq.1, Eq.2, and Eq.4) runs in CLA2, and the mechanical part (Eq.5 and Eq.6) runs in CPU2. After rigorous task allocation, the iteration frequency finally reached 800KHz. CPU1 and CLA1 perform all the remaining tasks, among these the data sampling and storage task is performed every 2.5 ns, the current tracking control for the ME algorithm is executed per 50 ns, the period of field-oriented control (FOC) for MCU is 100 ns, and the CAN communication cycle is 10 ms.

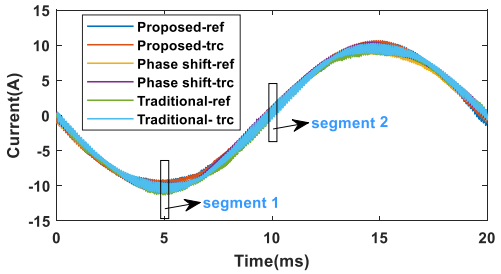

FIGURE 12. Current waveform collected by host computer.

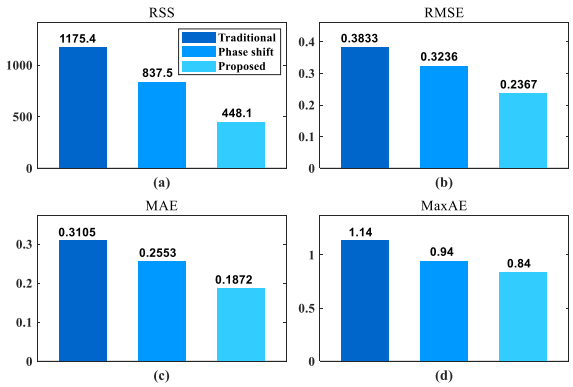

FIGURE 13. Current error analysis in time-domain. (a) Root sum squares error. (b) Root mean square error. (c) Mean absolute error. (d) Max absolute error.

TABLE 4. Parameter of instruments.

Instrument	Version	parameter
Current sensor	LAH 25-NP	Bandwidth200k Accuracy 0.3%
Current probe	TCP0020	Bandwidth 50M Range 20A
Oscilloscope	MDO3024	Bandwidth 200M, 4 channels

The operating parameters are shown in Table 3. The parameters of connecting inductance are designed to be equal to the real-time motor model inductance aiming at reducing the error caused by inductance mismatch. The target current is set to 10A, and the electrical frequency is set to 50 Hz. The current tracking performance of a traditional three-phase bridge, phase shift 90°, and proposed equivalent three-level space vector modulation are compared. The accuracy of the sensor and equipment is shown in Table 4. Because the external device cannot observe the current value of the motor model, the target value and actual value inside the ME are collected and recorded by the host computer, with a sampling rate of 400 kbps and a sampling length of 20 ms. The sampling results are used for comparative analyses, as shown in Fig. 12.

In order to compare the difference in current tracking performance in the time-domain under different strategies, root sum squares (RSS), root mean square error (RMSE), mean

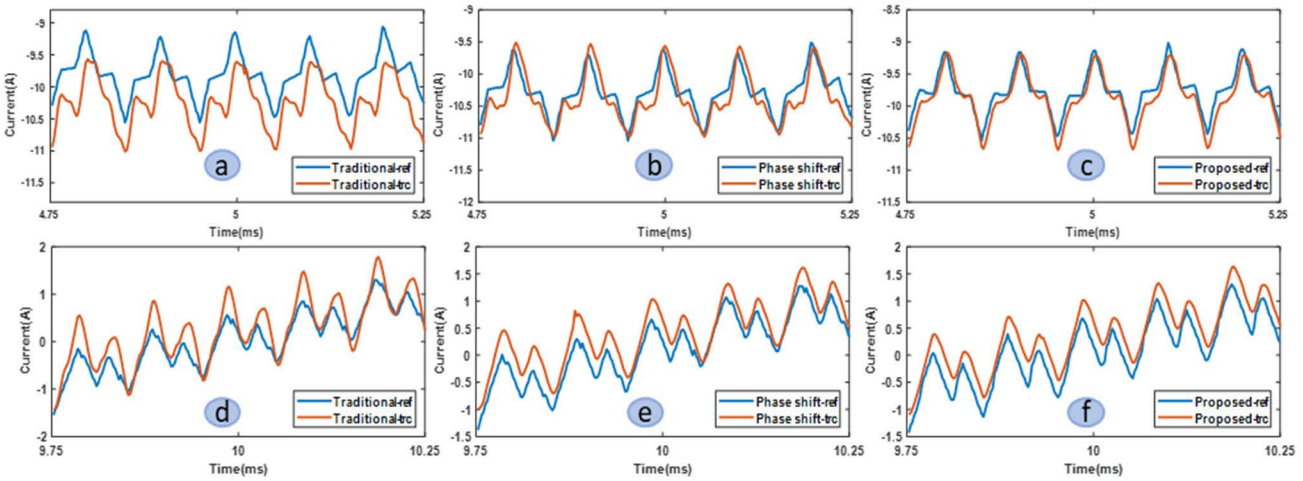

FIGURE 14. Ripple current under different strategies. (a)-(c) Details of segment 1. (d)-(f) Details of segment 2.

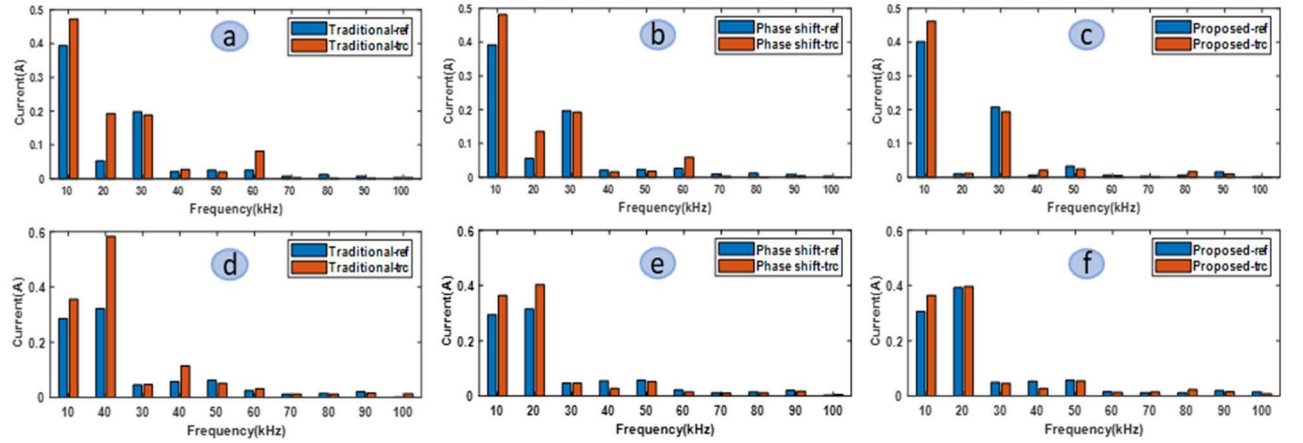

FIGURE 15. FFT of ripple current under different strategies. (a)-(c) FFT results of segment 1. (d)-(f) FFT results of segment 2.

absolute error (MAE), max absolute error (MaxAE) of one fundamental period current error are analyzed, and the results are shown in Fig. 13.

The four types of error results shown in Fig. 13 prove that the current tracking errors of the three strategies decrease successively, the error of the traditional strategy is the largest, and the error of the proposed strategy is the smallest. Further, detailed error reduction percentages are listed in Table 5, the proposed strategy reduces the error by 26.32% to 61.88% compared with the traditional strategy and 10.64% to 46.5% compared with the phase shift strategy. The time-domain error analysis results show that the proposed strategy can effectively reduce the current tracking error.

However, the period of ripple current is only 1/200 of the fundamental period. The time-domain error can reflect the error in the whole fundamental period, but cannot directly prove the ripple current reproduction performance in the ripple period. In order to compare the details of ripple current, two representative fragments of peak value and zero point are selected for further analysis. Segment 1 captures 5 ripple periods of 4.75*m*s-5.25*m*s, and the details is shown in Fig. 14 (a) (b) (c). In segment 2, 5 ripple cycles of 9.75*m*s-10.25*m*s are captured, and the details is shown in Fig. 14 (d) (e) (f). Fig. 14 shows that the proposed strategy has better ripple current reduction performance. Further, the ripple current of the two fragments is analyzed by FFT so as to compare the performance of current tracking in the frequency-domain. FFT results of segment 1 are shown in Fig. 15 (a) (b) (c), and the FFT results of segment 2 are shown in Fig. 15 (d) (e) (f). The fundamental frequency of FFT is the same as the MCU switching frequency of 10 *k*Hz.

It is indicated from the results in the frequency-domain that the harmonic distribution of the two segments is different. The errors in segment 1 are mainly distributed at 10 *k*Hz, 20 *k*Hz, and 40 *k*Hz, while in segment 2, 10 *k*Hz, 20 *k*Hz, and 60 *k*Hz are the main frequency points. The main tracking errors under different strategies in the two segments are summarized in Table 6 and Table 7. According to the

TABLE 5. Error reduction percentage in time-domain.

	Compared to traditional	Compared to phase shift
RMSE	38.25%	26.85%
RSS	61.88%	46.50%
MAE	39.61%	26.67%
MaxE	26.32%	10.64%

TABLE 6. Frequency-domain error comparison.

f	traditional	phase shift	proposed	Error reduction
10kHz	0.07	0.07	0.058	17.1%
20kHz	0.262	0.088	0.005	98.1%
40kHz	0.057	0.028	0.026	54.4%

TABLE 7. Frequency-domain error comparison.

f	traditional	phase shift	proposed	Error reduction
10kHz	0.079	0.89	0.061	22.8%
20kHz	0.14	0.079	0.0006	99.6%
60kHz	0.056	0.033	0.0008	98.6%

calculation, compared with the traditional strategy in segment 1, the proposed strategy reduces the errors by 17.1%, 98.1%, and 54.4% at 10 kHz, 20 kHz, and 40 kHz respectively. In segment 2, the effect is more pronounced that the errors at 10 kHz, 20 kHz, and 60 kHz are reduced by 22.8%, 99.6%, and 98.6%. The results of frequency-domain analysis show that the new strategy can effectively reduce the error of ripple current detail reproduction.

V. CONCLUSION

This paper focuses on improving the ripple current reproduction of power-stage ME. Firstly, a novel dual-branch parallel topology is proposed to get over the disadvantage of the restricted switching frequency in traditional three-phase inverters. The topology is of simple structure, low cost, and no additional filter. The equivalent operating switching frequency can be doubled by interleaved switching without increasing the actual switching frequency of every single bridge. Secondly, a corresponding virtual three-level space vector modulation strategy is put forward, where the proposed ME scheme can be equivalently transformed into a general three-phase three-level back-to-back topology in the process of modulation. This strategy divides the sectors further and selects the vectors closest to the target for combination. And the final switching sequence is optimized considering the redundant states of three-level vector space. Finally, the results of the simulation and experiment show that the proposed topology and modulation strategy have excellent performance in reducing the background ripple and improving the ripple current reduction accuracy of ME in comparison with the traditional strategy and the phase shift strategy. The research in this paper has positive significance for improving the emulation accuracy of motor port characteristics of ME. Meanwhile, it provides valuable references for shipping, aerospace, rail transit, and other high-power fields.

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