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Doubly Fed Induction Generator Low Voltage Ride Through Improvement Through Modular Multilevel Converter

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ABSTRACT This paper proposes a novel fault current suppression method for doubly fed induction generator (DFIG) low voltage ride through (LVRT) improvement employing modular multilevel converter (MMC). It is based on the inherent MMC arm impedance and the number of levels to provide transient damping of DFIG rotor and stator currents under severe grid faults, contributing effectively to maintaining the DFIG connection while ensuring controllability by avoiding the protection activation. Neither additional hardware nor control loops are necessary. DFIG dynamic equations under LVRT, including the contribution of the MMC, are presented, and a model is derived for control design. Performance assessment, including symmetrical and asymmetrical fault scenarios for MMC with 3, 21, 51, and 101 levels and comparison with existing and proposed controllers, highlighted that arm impedance and increased MMC level number contributed to DFIG stator and rotor fault current suppression, providing DFIG LVRT improvement under severe grid fault conditions.

INDEX TERMS Doubly fed induction generator, low voltage ride through, modular multilevel converter, fault current suppression, wind energy conversion systems.

NOMENCLATURE

BESS	Battery energy storage systems.
BTFCL	Bridge type fault current limiter.
CCP	Common coupling point.
DC	Direct current.
DVR	Dynamic voltage restorer.
EMF	Electromotive force.
ESC	Energy storage side converter.
FCL	Fault current limiters.
FCLI	Inductor-based fault current limiter.
GSC	Grid side converter.
HVDC	High-voltage direct current.
MERS	Magnetic energy recovery switch.
PDPWM	Phase-disposition pulse width modulation.
PLL	Phase-locked loop.
PWM	Pulse width modulation.
RSC	Rotor side converter.
SBR	Series braking resistor.
SGSC	series grid side converter.
STATCOM	Synchronous static compensator.
THD	Total harmonic distortion.
VSC	Voltage source converter.
WECS	Wind energy conversion systems.
$\Delta V_{cap,pp}$	Capacitor peak-to-peak voltage ripple.
	Damping coefficient.
λ_s	Stator flux.
σ	Leakage coefficient.
τ	Combined time decay constant.
τ_r	Rotor time decay constant.
τ_s	Stator time decay constant.
g	Grid synchronism angle.
C_{eq}	MMC arm equivalent capacitance.
C_{inst}	Total active submodule instantaneous capacitance.

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C_{sm}	Submodule capacitance.
e_v	Controlled voltage source that represents the MMC submodules voltage.
$gate_{sm}$	Submodule switching signals.
$i(t)$	Instantaneous current.
i_{gd}	Grid-side d-axis current.
i_{gq}	Grid-side q-axis current.
$i_{ra,max}$	DFIG phase-a highest fault current peak.
$i_{ra}(t_o^-)$	DFIG pre-fault current.
i_{DC}	Controlled current source that represents the MMC submodules voltage.
I_o	Output current.
$K_{i(GSC)}$	Integral GSC controller gain.
$K_{p(RSC)}$	Proportional RSC controller gain.
$K_{i(GSC)}$	Integral GSC controller gain.
$K_{p(RSC)}$	Proportional RSC controller gain.
L_{arm}	MMC arm inductance.
L_{eq}	Equivalent grid-side inductance.
N	Number of converter levels.
N_{sm}	Number of submodules per arm.
$N_{smactive}$	Number of active submodules.
P_{gref}	Active power reference.
P_o	Converter output power.
ϕ	Angle displacement.
Q_{gref}	GSC Reactive power reference.
Q_{sref}	RSC Reactive power reference.
Q_s	RSC reactive power.
$R_{arm,eq}$	Equivalent arm resistance.
R_{arm}	MMC arm resistance.
R_{eq}	Equivalent grid-side resistance.
$R_{sm,eq}$	Equivalent submodule resistance.
$R_{sm,off}$	Bypassed submodule resistance.
$R_{sm,on}$	Active submodule resistance.
s	Slip.
S_1	Non-complementary MMC submodule switch.
S_2	Complementary MMC submodule switch.
SM_{active}	Active submodule.
$v(t)$	Instantaneous capacitor voltage.
$V_{arm,d}$	Grid-side d-axis arm voltage.
$V_{arm,q}$	Grid-side q-axis arm voltage.
V_{arm}	MMC arm voltage.
V_{bus}	DC bus voltage.
$V_{cap,max}$	Submodule capacitor maximum voltage deviation.
$V_{cap,min}$	Submodule capacitor minimum voltage deviation.
V_{cap}	MMC submodule capacitor voltage.
V_{fdref}	Grid d-axis reference voltage.
V_{fqref}	Grid q-axis reference voltage.
V_{sm}	MMC submodule voltage.
$V_{sm}(n)$	n-th submodule voltage.
V_{smlow}	MMC lower arm submodule voltages.
V_{smup}	MMC upper arm submodule voltages.
V_s	Stator voltage amplitude.
ω	Angular frequency.
w_{lowA}	Lower arm energy.
w_{upA}	Upper arm energy.
ω_m	Mechanical speed.
ω_n	Closed loop poles.
ω_r	Rotor angular speed.
ω_s	Synchronous frequency.
$Z_{arm,eq}$	Equivalent arm impedance.

I. INTRODUCTION

One of the main characteristics of DFIG-based WECS is their high sensitivity to electrical disturbances, particularly voltage sags, due to the direct connection of their stator to the grid [1]. In WECS, power electronics have a crucial role in generation compatibility with the grid, and traditionally the back-to-back VSC sharing a DC bus has been used [2]. However, to meet LVRT requirements, this converter topology requires control or hardware protection implementations to ensure that the DFIG-based WECS remains connected to the grid without damaging the system [3]. Device-based solutions have been used for improving DFIG LVRT supportability, such as crowbar, DC choppers, fault current limiters (FCLs), synchronous static compensators (STATCOMs), dynamic voltage restorers (DVRs), and BESS [4]–[10].

The crowbar, one of the widely used techniques for LVRT support, uses short-circuited shunt resistors in the rotor [1]. The common drawback of the crowbar refers to their temporary uncontrollability of the active and reactive power in DFIG, RSC disconnection, and rotor short-circuit [11]. An alternative to overcome these drawbacks is the coordinated use of a crowbar with a SBR [12], and a parallel RL crowbar with an RL series circuit [13]. Nevertheless, these approaches have the disadvantage of adding even more devices with low effectiveness to maintaining DFIG control. The DC chopper, another well-known DFIG solution in the literature against DC bus overvoltages, uses a shunt resistor to dissipate the energy excess [14]. However, the time to reestablish the control and connect the converter to operation is drastically increased compared to the crowbar [5].

One challenge to the DFIG is to operate under voltage sags and overcurrent in the stator and rotor during a fault. Thus, the use of FCL devices is a strategy that acts to limit the high currents under the fault and protect the DFIG converters placed at different points of the DFIG-based WECS structure, such as the stator, rotor, DC link, and CCP [7], [15]. [16] proposed a BTFCL. This scheme comprises coupling transformers connected to the DFIG stator, a diode bridge, and an FCLI. The FCLI is inserted in the stator terminals when the stator currents reach the threshold to limit the fault current. However, the FCLI causes voltage surges due to the RSC switching, leading to voltage distortions and electromagnetic torque oscillations.

Techniques based on BESS can also support DFIG LVRT [9]. The BESS comprises a converter denominated ESC, operating parallel coordinated with the RSC, to support the rotor in demagnetizing and injecting reactive current, as presented in [17]. Nevertheless, this approach requires an

additional converter, and the batteries considerably increase the costs and control complexity. Another approach used to mitigate voltage sag in the DFIG stator terminals and improve LVRT supportability is a SGSC across the DC bus, as presented in [18]. This system is composed of a parallel grid side rectifier connected to DC bus terminals through a transformer. This structure provided an accurate control of the stator flux under normal and LVRT conditions. However, this method requires an additional converter with complex control coordination.

In [19], the STATCOM is employed to inject and control the reactive power based on the fault condition, but it has limitations to ensure system stability, requiring additional control loops to regulate the reactive power. The DVR is usually employed to provide LVRT grid voltage recovery, connected through a transformer between the CCP and DFIG, as presented in [20]. Nevertheless, this method requires an extensive energy storage system and an additional converter with control loops to regulate the series voltage compensation under LVRT conditions. On the other hand, [21] employed a MERS for DFIG LVRT capacity improvement, composed of four switches and a capacitor connected to the CCP. This scheme controls the grid injected voltage by the capacitor. However, it can suffer from harmonics in the line current that can be interacting with the system resonance frequency.

An alternative to overcome these drawbacks and avoid hardware-based approaches is the use of multilevel converters for DFIG-based WECS LVRT improvement. Assuredly, multilevel power converters have recently improved robustness to electrical disturbances, lower THD, and fault tolerance [22]. In particular, the half-bridge MMC has reached broad relevance due to its flexible modular structure, easy expandability, and capacity to operate at high power levels, such as HVDC systems, photovoltaic, and WECS [23]. Unlike other submodule topologies, the half-bridge MMC allows the current to flow in any operating mode through the freewheeling diodes of the submodule switches. This capability provides continuous operation even under fault conditions, ensuring controllability and damping fault currents, making it attractive for LVRT support applications [24]. In addition, the half-bridge MMC has been widely used due to the smaller submodule components and the cost of increasing the number of levels [25]. Nevertheless, with the best authors' knowledge, MMC has not been used in DFIG-based WECS LVRT due to the newfound MMC employment in variable-speed drives and its drawback of submodule capacitor voltage ripples under low-frequency operation. However, approaches such as [26] and [27] have already demonstrated that it is possible to allow MMC operation under low frequencies by employing additional control loops to provide reliable operation.

Overcoming these problems, this paper proposes a fault current suppression method by leveraging the MMC arm impedance and increasing the number of levels. It is crucial to ensure that the DFIG stator and rotor currents remain under controllable and safe levels to avoid loss of controllability and disconnection under grid fault scenarios. In addition, maintaining the controllability and connection of DFIG-based WECS is a requirement for operating wind farms to support the network [28]. Thus, this paper proposal deals with DFIG stator and rotor fault current limiting for symmetrical and asymmetrical faults by including the MMC arm impedance in cascade to the rotor and increasing the number of levels of the MMC to strengthen the inductive nature of this arm impedance. Therefore, it is expected that the proposed fault current suppression method enhances robustness and reliability and supports the reduction of DFIG-based WECS physical protection tripping. The proposed fault current suppression method is based on the half-bridge MMC to ensure DFIG controllability and continuous operation even under LVRT conditions. In this fashion, this work demonstrates through simulations the applicability of MMC with a higher number of levels, indicating the feasibility of its use in DFIG-based WECS. Unlike the approaches described in [11]–[14], [16]–[21] this proposal does not employ device-based solutions since a back-to-back MMC topology is used instead of the traditional two-level converters (2LVSC's) with fault current suppression capability due to the arm impedance and the increased number of levels. In addition, this paper proposal provides an adjustment to the classical vector control approach described in [1] to consider the MMC-DFIG dynamics. Therefore, the proposed DFIG fault current suppression method provides the DFIG-based WECS LVRT enhanced supportability to severe grid voltage sags; neither additional hardware nor control loops are necessary.

The performance assessment of the proposed method has been accomplished with various symmetrical and asymmetrical faults. Furthermore, the MMC with 3, 21, 51, and 101 levels have been evaluated to demonstrate the DFIG-based WECS performance under several operating conditions. Simulated results have demonstrated the MMC capacity to ensure the DFIG LVRT improvement in all fault scenarios, indicating that the higher is the number of levels and the arm impedance, the lowest is the DFIG stator and rotor overcurrents.

II. MODULAR MULTILEVEL CONVERTER DESCRIPTION

Fig. 1 depicts the three-phase MMC with half-bridge submodules, which is the most widely used topology configuration. In this case, the MMC is composed of $2(N\text{-}1)$ submodules, where N is the number of converter levels; each submodule is composed of two switches and a capacitor [25]. A series R-L (R_{arm} and L_{arm}) impedance comprises the MMC arm, equally distributed among the converter phases. According to the state of the MMC submodule switches, the capacitor is inserted or bypassed. The voltage of each submodule V_{SM} that synthesizes the output voltage levels is defined by a switching function as follows:

- If $S_1 = 1$ and $S_2 = 0$, $V_{sm} = V_{cap}$;
- If $S_1 = 0$ and $S_2 = 1$, $V_{sm} = 0$;
- Else $V_{sm} = 0$.

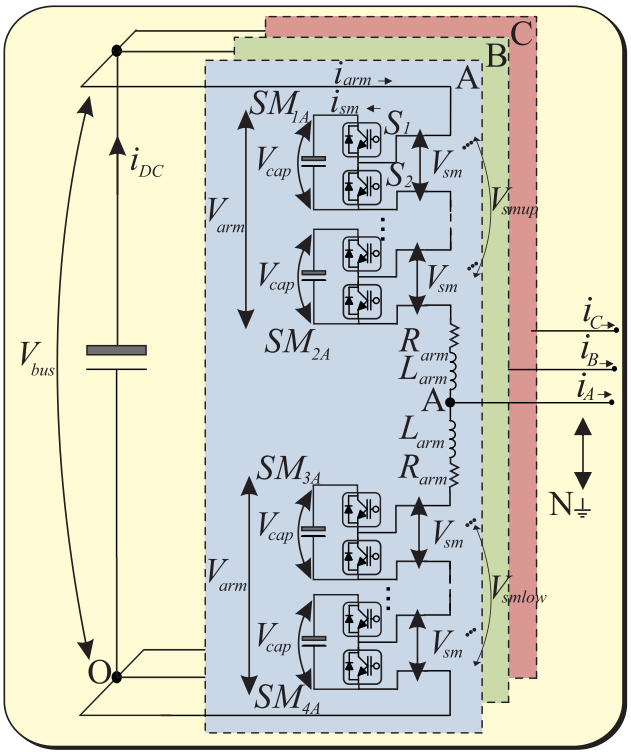

FIGURE 1. Three-phase half-bridge MMC topology.

The average capacitor voltage, V_{cap}, of each submodule, is given by:

$$V_{cap} = \frac{V_{bus}}{N_{sm}}, \tag{1}$$

where N_{sm} is the number of submodules per arm. Then, $N_{sm} + 1$ is the number of output voltage levels; V_{bus} is the DC bus voltage. Each arm in the MMC is equivalent to a controlled voltage source V_{arm} with instantaneous voltage amplitude, given by:

$$V_{arm} = \frac{SM_{active} V_{bus}}{N}, \tag{2}$$

where SM_{active} is the number of active submodules. The MMC voltage level is given as a function of the sum of the submodule voltages, V_{sm}, and the voltage drop across R_{arm} and L_{arm}, as follows:

$$V_{arm} = \sum_{n=0}^{SM_{active}} (V_{sm}[n]) + L_{arm}\frac{di_{arm}}{dt} + R_{arm} i_{arm}. \tag{3}$$

Therefore, considering $v[t] = L\frac{di[t]}{dt}$, $i[t] = C\frac{dv[t]}{dt}$ as the basic L-C voltage-current relation, and C_{sminst} as the total active submodule instantaneous capacitance, (3) is rewritten as:

$$V_{arm} = \frac{1}{C_{sminst}} \int_t^0 i_{arm} dt + L_{arm}\frac{di_{arm}}{dt} + R_{arm} i_{arm}. \tag{4}$$

where $v[t] = L\frac{di[t]}{dt}$, and $i[t] = C\frac{dv[t]}{dt}$ are state variables, which cannot vary instantaneously [3]. These characteristics indicate that the MMC circuit opposes to sudden current and voltage variations, avoiding instantaneous overcurrents and overvoltages.

The MMC has been considered the next generation of converters that will integrate the various power system applications. Then, wind energy conversion systems can be certainly benefited from the MMC due to their transform-less structures, high efficiency, and modularity [27]. However, under low-frequency operation (<30 Hz), the MMC submodules present a current through the capacitors with high oscillation, leading to significant ripples in the capacitor voltages [26], [29]. This is a high limitation for the use of MMCs in DFIG-based WECS. Nevertheless, several works have been providing solutions for improving the MMC dynamic performance during challenging low-frequency operations. In [30], a common-mode voltage injection technique is proposed to reduce capacitor voltage oscillations. [27] proposes a capacitance selection algorithm for the MMC to keep the oscillations within acceptable limits. [26] proposes an improved circulating current injection scheme based on the trapezoidal waveform. Then, [26], [27], [30] successfully demonstrated that the operation of MMC submodule capacitors is feasible under extra low frequencies (<5 Hz) by minimizing the effects of voltage oscillations.

The fundamentals that govern the relationship between the MMC submodule capacitor voltage ripple and the output frequency are addressed in [26]. This analysis demonstrates the inverse relationship between the voltage ripple in submodule capacitors and the MMC operating frequency, i.e., the lower the output frequency, the higher the voltage ripple. [26] approximates the MMC upper and lower arm energy, w_{upA} and w_{lowA}, by:

$$w_{upA} \approx \frac{P_o}{\omega} sin(\omega t - \phi), \tag{5}$$

$$w_{lowA} \approx -\frac{P_o}{\omega} sin(\omega t - \phi), \tag{6}$$

where ω is the output angular frequency, and P_o is the converter output power, given by [26]:

$$P_o = \frac{1}{4} V_{bus} I_o, \tag{7}$$

where V_{bus} and I_o are the DC bus voltage and the magnitude of the output current, respectively. Based on (5)-(6), the peak-to-peak arm energy variation, $\Delta w_{upA} = \Delta w_{lowA} = \frac{2P_o}{\omega}$, should be damped by the N capacitors of the submodules. Therefore, writing the energy deviation in terms of N and the submodule capacitor energy, $\frac{C_{sm} V_{cap}^2}{2}$, one obtains [26]:

$$\begin{aligned} \frac{2P_o}{\omega} &= N\left(\frac{1}{2} C_{sm} V_{cap,max}^2 - \frac{1}{2} C_{sm} V_{cap,min}^2\right) \\ &= N C_{sm} V_{cap} \Delta V_{cap,pp}, \end{aligned} \tag{8}$$

where $V_{cap,max} = V_{cap} + \frac{1}{2}\Delta V_{cap,pp}$ and $V_{cap,min} = V_{cap} - \frac{1}{2}\Delta V_{cap,pp}$ are voltage deviations. Therefore, considering $\Delta V_{cap,pp}$ to be the peak-to-peak voltage ripple of the submodule capacitor, C_{sm} the submodule capacitance, and

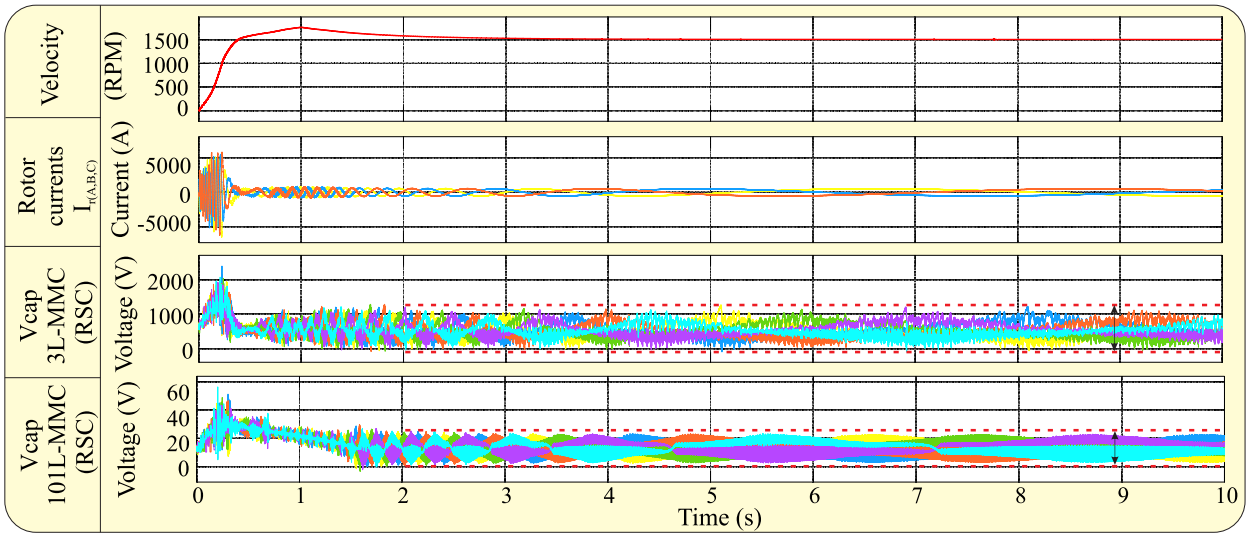

FIGURE 2. RSC submodule voltages at synchronous speed for 3L and 101L-MMC.

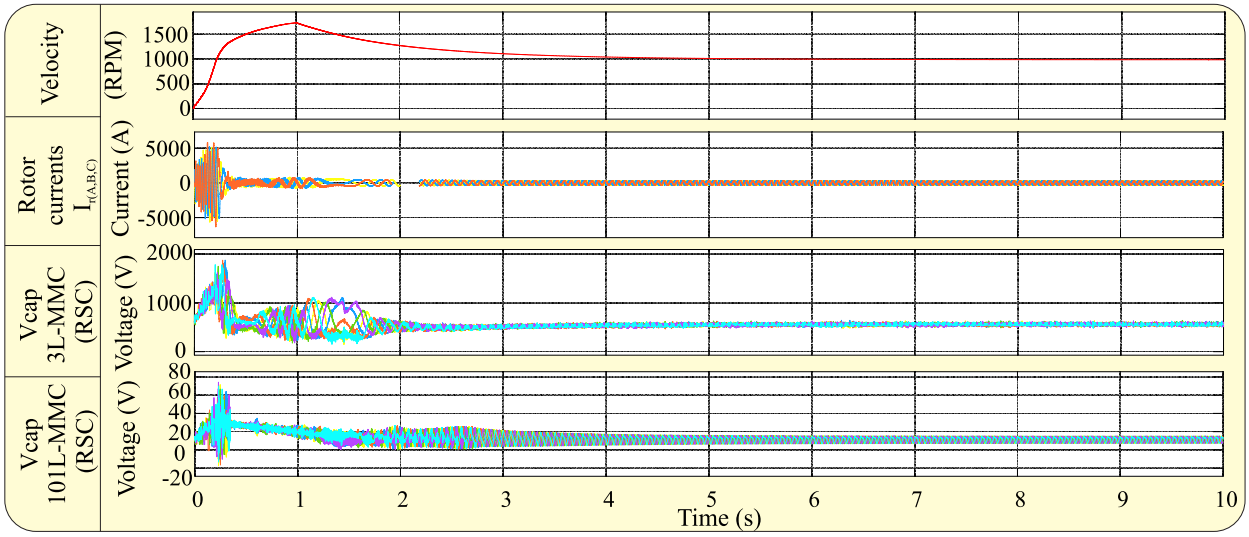

FIGURE 3. RSC submodule voltages at subsynchronous speed for 3L and 101L-MMC.

$NV_{cap} = V_{bus}$ the total DC bus voltage, (8) can be simplified as follows [26]:

$$\Delta V_{cap,pp} = \frac{2P_o}{\omega C_{sm} V_{bus}}, \tag{9}$$

which demonstrates that the voltage ripple is inversely proportional to the output frequency. Hence, rewriting (9) as a function of N, yields [26]:

$$\Delta V_{cap,pp} = \frac{2P_o}{\omega C_{sm} N V_{cap}}. \tag{10}$$

In (10), the product NV_{cap} gives the total DC bus voltage. However, the increase in the number of levels provides the individual submodule capacitor voltage reduction to maintain the equality, i.e., $NV_{cap} = V_{bus}$. Therefore, each capacitor per submodule will be subjected to lower voltages, i.e., V_{cap} decreases as N increases, which effectively impacts the MMC arm voltage oscillations improvement and reduces the total converter voltage ripple. Based on [26], the voltage ripple depends on the number of levels, i.e., with the highest number of levels, one can relieve the MMC submodule capacitor voltage ripples. Therefore, considering the challenging MMC operation conditions covered in [26], which was not in a DFIG application, this paper demonstrates the possibility to use a MMC in a DFIG with properly adaptations. For instance, Figs. 2 and 3 depict the back-to-back MMC operation in a DFIG-based WECS under low-frequency and low-voltage conditions.

To better describe the back-to-back MMC operation condition in a DFIG-based WECS (according to Table 2

parameters) under low-frequency and low-voltage, the wind speed was set as the generator's synchronous speed (1500 rpm) in Fig. 2. In this condition, the DFIG operates with slip equal to zero, the rotor currents operate at nearly zero frequency, and the rotor voltages operate at near-zero voltages [1]. The wind speed for this condition can be determined through the curve of turbine speed in (m/s) as a function of generator speed (rpm) according to [1]. In addition, the generator uses a gearbox to perform speed regulation between the high-speed and low-speed shaft, making the high-speed shaft rotate about 50 times faster than the low-speed shaft. Thus, the high-speed shaft rotates at approximately 1500 rpm and drives the DFIG [3]. Hence, the rotor currents behave practically as DC currents (i.e., the worst situation). Therefore, the simulations in Fig. 2 considered 3L- and 101L-MMC RSC operating at the synchronous speed to demonstrate the submodule capacitor voltages under these challenging conditions. As expected, the MMC submodule capacitor voltages present oscillations, which were more significant for the RSC 3L-MMC. In this sense, the voltage distributed in the submodule capacitors is higher because there are fewer submodules in the MMC arm. Conversely, through the RSC 101L-MMC, a lower capacitor submodule voltage ripple is provided, indicating that many MMC levels can relieve the RSC voltage ripples. The voltage distribution across the MMC arm's submodule capacitors is lower due to the larger amount of submodules, which provides ripple reduction since the capacitors require less voltage amplitude during charge and discharge cycles to be equalized.

To highlight the lower voltage ripple in the MMC submodule capacitors under higher frequencies the DFIG-based WECS operating at subsynchronous speed was simulated as depicted in Fig. 3. In this condition, the DFIG operates with maximum slip, i.e., approximately 0.3. Thus the magnitude of the rotor voltages is larger, around 350 V, since they are proportional to the slip [1]. On the other hand, the rotor current frequencies operate at the slip frequency of approximately 15 Hz. This scenario describes the reduction of $\Delta V_{cap,pp}$ as ω increases, which provides the MMC behavior according to (10). As expected, an increase in the converter output frequency decreased the capacitors' charge and discharge periods leading to a significant reduction in voltage ripples. In addition, the 3L-MMC presents higher capacitor voltage distortion and oscillation due to the lower amount of synthesized voltage levels and the capacitors being subjected to higher voltage levels. Conversely, the 101L-MMC presented the best performance due to the improved voltage distribution in the MMC submodules providing the capacitor voltage level reduction and relieving the distortions and ripples. Thus, the RSC operation was further validated through the proposed control scheme, since despite the capacitor's ripples in this particular operation condition, no voltage deviations occurred in the converter, allowing it to be reasonably used to obtain the results. In addition, based on these preliminary simulation results, there is evidence that the MMC employment in DFIG-based WECS with an increased number of levels can be adopted as an RSC while ensuring no impacts during its operation. Therefore, unlike the previous approaches under low-frequency and low-voltage operation, this paper employs the proposed control structure, addressed in the next section, to validate the DFIG-based WECS fault current suppression method.

III. THE PROPOSED MMC CONTRIBUTION FOR DFIG ROTOR CURRENT DAMPING UNDER FAULT CONDITIONS

The dynamic equations in [3] can represent the interaction between the MMC arm impedance with the DFIG rotor circuit. Fig. 4 depicts the DFIG rotor equivalent circuit with MMC, per phase average circuit, for developing dynamic equations [31], where $\vec{V}_{r0}^{r}$ is the electromotive force (EMF) induced by the stator flux λ_s, $\sigma = 1 - \frac{L_m^2}{L_s L_r}$, L_r and R_r are the rotor inductance and resistance, respectively. In the MMC diagram, i_{DC} is the DC current, and $e_v = \frac{1}{2}(\sum_{n=0}^{SM_{active}}(V_{smlow}) - \sum_{n=0}^{SM_{active}}(V_{smup}))$ is the converter AC voltage. This representation demonstrates the DFIG per-phase circuit seen from the rotor terminals considering one phase of the MMC. Therefore, from Fig. 4, the equations that govern the interaction with the MMC arm impedance and the number of level increase are divided into two parts: firstly, consider the submodule capacitances association due to the switching to obtain the equivalent impedance. Thus, the equivalent arm capacitance C_{eq} is given by:

$$C_{eq} = \frac{C_{sm}}{\sum_0^N N_{smactive} gate_{sm}}, \tag{11}$$

where $gate_{sm}$ is the submodule switching signals provided by the PWM technique. With the increasing number of MMC levels, the arm capacitive effect decreases as the amount of active submodules increases. Considering that the submodule capacitors are equalized and N is large enough, i.e., $\lim_{N\to\infty} N$, the equivalent arm capacitance is given by:

$$C_{eq} = \frac{C_{sm}}{\sum_0^\infty N_{smactive} gate_{sm}} \approx 0, \tag{12}$$

which makes the MMC arm closer to an R-L impedance. Thus, considering the resistance of the active and bypassed submodules as $R_{sm,on}$ and $R_{sm,off}$, respectively, the equivalent

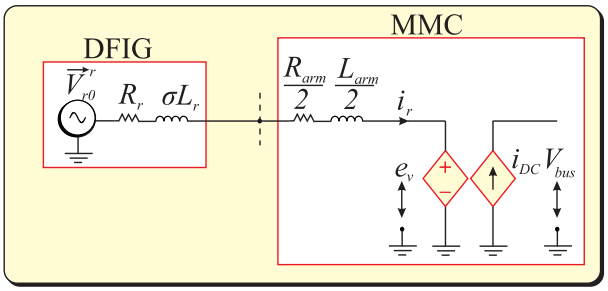

FIGURE 4. DFIG rotor equivalent circuit with MMC average model.

arm impedance is given by the sum of arm impedance and the series resistance of the MMC submodules, as follows:

$$Z_{arm,eq} = \frac{j\omega L_{arm}}{2} + \frac{R_{arm}}{2} + R_{sm,on} + R_{sm,off}. \quad (13)$$

Considering the equivalent resistance of the submodules, $R_{sm,eq} = R_{sm,on} + R_{sm,off}$, the arm equivalent resistance is given by:

$$R_{arm,eq} = \frac{R_{arm}}{2} + R_{sm,eq}. \quad (14)$$

The DFIG fault current expression is solved considering the MMC parameters. Thus, the worst case is considered to demonstrate the MMC contribution to DFIG overcurrent suppression, which is the three-phase fault (LLL) with the highest peak current value given by [12]:

$$\begin{aligned} i_{ra,max} = {} & i_{ra}(t_0^-) - \frac{1}{\sigma L_r} V_s K_s (1-s) \frac{\tau_r}{1+\tau_r^2\omega_r^2} \\ & + \frac{V_r}{\sigma L_r} \frac{\tau_r}{\sqrt{1+\tau_r^2\omega_r^2}} \\ & + \frac{1}{\sigma L_r} V_s K_s (1-s) \frac{\tau_r}{\sqrt{1+\tau_r^2\omega_r^2}}, \end{aligned} \quad (15)$$

in which $\tau_r = \frac{\sigma L_r}{R_r}$ is the rotor time decay. Therefore, considering the MMC arm impedance, the maximum amplitude of the phase-A current, (15) is rewritten as:

$$\begin{aligned} i_{ra,max} = {} & i_{ra}(t_0^-) - \frac{1}{\sigma L_r + \frac{L_{arm}}{2}} V_s K_s (1-s) \frac{\tau_r}{1+\tau_r^2\omega_r^2} \\ & + \frac{V_r}{\sigma L_r + \frac{L_{arm}}{2}} \frac{\tau_r}{\sqrt{1+\tau_r^2\omega_r^2}} \\ & + \frac{1}{\sigma L_r + \frac{L_{arm}}{2}} V_s K_s (1-s) \frac{\tau_r}{\sqrt{1+\tau_r^2\omega_r^2}}, \end{aligned} \quad (16)$$

and, τ_r, with MMC parameters is given by:

$$\tau_r = \frac{\sigma L_r + \frac{L_{arm}}{2}}{R_r + \boldsymbol{R_{arm,eq}}}, \quad (17)$$

where $K_s = \frac{L_m}{L_s}$; $e^{\frac{-t}{\tau_s}} \approx 1$; $\tau \approx \tau_r$; $R_{arm,eq}$ is given by (14); L_{arm} is the MMC arm inductance; (t_0^-) is the component before the fault; L_s and L_m are the stator and magnetizing inductances; R_s is the stator resistance; ω_r is the rotor angular speed; $s = \frac{\omega_r}{\omega_s}$ is the slip; ω_s and $s\omega_s$ are synchronous and slip angular frequencies; τ_s, and τ are the stator and combined time decay constants; V is the voltage amplitude, s and r are the stator and rotor subscript, respectively. The terms involving the maximum peak current value in DFIG are suppressed with the inclusion of L_{arm} and R_{arm}.

The inductance effectively contributes to damping and preventing the sudden rise of the fault current, while the resistance acts to suppress the fault current amplitude. This effect is obtained replacing (17) in (16). Thus, the analysis demonstrated in (16)-(17) indicates that the MMC arm impedance can relieve the DFIG overcurrents under LVRT conditions. Moreover, the higher the number of MMC levels, the arm becomes closer to an impedance R-L, which leads to the effective suppression of DFIG fault currents. The L_{arm} and C_{SM} parameters selection criterion used in this paper is based on the procedure presented in [32]. R_{arm} was adopted using typical values based on the resistance per length of the wire in MMC arm reactor manufacturing.

IV. SYSTEM DESCRIPTION AND CONTROL

Fig. 5 depicts the implemented system, comprising the DFIG-based WECS with the back-to-back MMC and a grid line filter connected to the three-phase network under fault conditions. Furthermore, to consider the MMC-DFIG dynamics, the controller's design is presented considering the new transfer functions. Table 2 presents the system parameters.

The equations that govern the DFIG control loops consider the interaction with the MMC. Thus, this paper proposes a modification in the vector control structure to consider the new dynamics inserted by the converter through the transfer function composed by DFIG with MMC. All equations are based on the theoretical fundamentals presented in the previous sections adopted by [33]. Therefore, the controller's design was performed considering an approximation by a second-order equivalent system. The development was performed through Kirchhoff's Laws to obtain the expressions representing the DFIG and MMC. For the GSC, the Laplace transfer functions in the $0dq$ referential are given by:

$$\frac{i_{gd}(s)}{V_{arm,d}(s)} = -\frac{1}{L_{eq}s + R_{eq}}, \quad (18)$$

$$\frac{i_{gq}(s)}{V_{arm,q}(s)} = -\frac{1}{L_{eq}s + R_{eq}}, \quad (19)$$

where i_{gd} and i_{gq} are output currents; $V_{arm,d}$ and $V_{arm,q}$ are arm voltages; $L_{eq} = L_f + \frac{L_{arm}}{2}$ and $R_{eq} = R_f + \frac{R_{arm}}{2}$, in which L_f and R_f are the inductance and resistance of the grid line filter, respectively. The equations (18) and (19) represent the MMC transfer function for control design. Therefore, the control system has as input the references i_d^* and i_q^*, and the MMC arm voltages $V_{arm,d}^*$ and $V_{arm,q}^*$ as outputs. Fig. 6 depicts the block diagram of the current loop before and after considering the MMC in the GSC control loop. Thus, considering a PI controller, the closed-loop transfer functions with second-order system characteristics are given by:

$$\frac{i_{gd}(s)}{i_{sdref}(s)} = \frac{sk_p + k_i}{s^2(L_{eq}) + s(R_{eq} + k_p) + k_i}, \quad (20)$$

$$\frac{i_{gq}(s)}{i_{sqref}(s)} = \frac{sk_p + k_i}{s^2(L_{eq}) + s(R_{eq} + k_p) + k_i}, \quad (21)$$

where k_p and k_i are the PI controller gains. Therefore, considering the GSC gains $k_p = k_{p(GSC)}$ and $k_i = k_{i(GSC)}$ and based on (20)-(21), the controller gains are obtained by equaling the denominator of the transfer functions to a second-order system [33]:

$$s^2(L_{eq}) + s(R_{eq} + k_{p(GSC)}) + k_{i(GSC)} \approx s^2 + 2\xi\omega_n s + \omega_n^2, \quad (22)$$

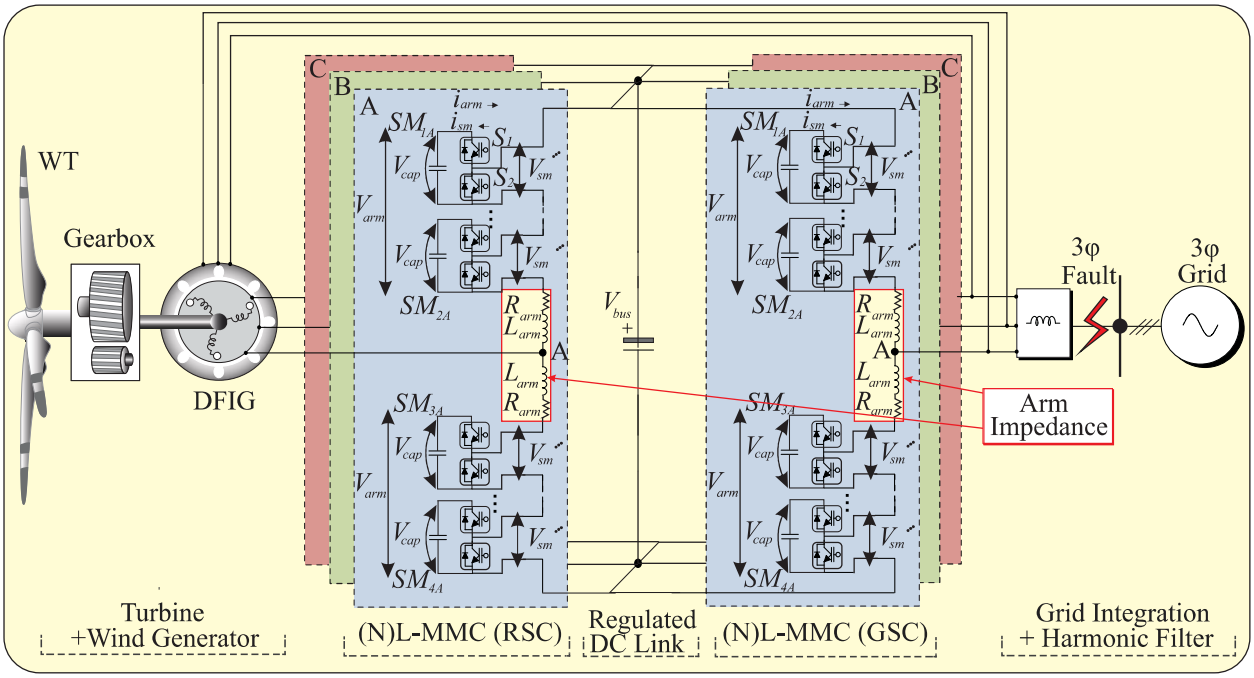

FIGURE 5. DFIG-based WECS with back-to-back MMC for the proposed fault current suppression method.

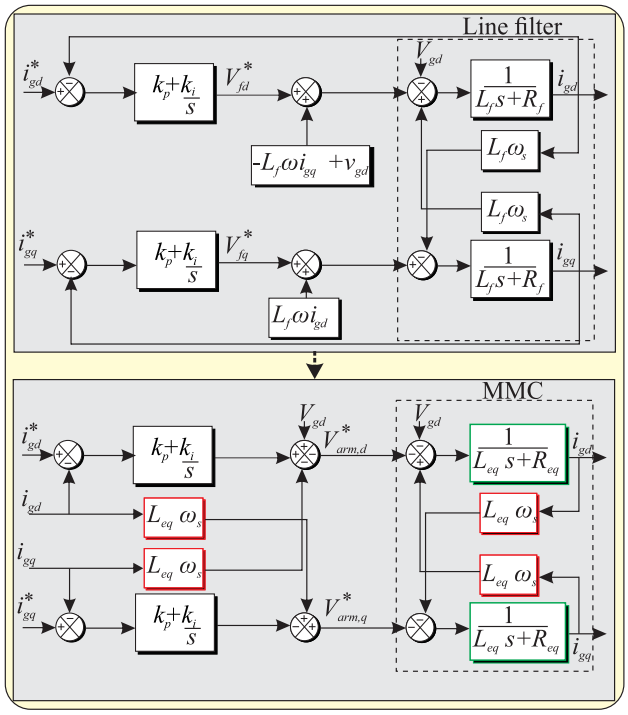

FIGURE 6. GSC control loop with MMC model.

where ω_n is the natural frequency and ξ is the damping coefficient. Thus:

$$s^2 + s\left(\frac{R_{eq} + k_{p(GSC)}}{L_{eq}}\right) + \frac{k_{i(GSC)}}{L_{eq}} \approx s^2 + 2\xi\omega_n s + \omega_n^2, \tag{23}$$

$$k_{i(GSC)} = L_{eq}\omega_n^2, \tag{24}$$

$$k_{p(GSC)} = L_{eq}2\xi\omega_n - R_{eq}. \tag{25}$$

Adopting $\xi = 1$, yields:

$$\xi = 1 \rightarrow (s + \omega_n)^2, \tag{26}$$

$$s^2 + s\left(\frac{R_{eq} + k_{p(GSC)}}{L_{eq}}\right) + \frac{k_{i(GSC)}}{L_{eq}} = (s + \omega_n)^2, \tag{27}$$

where ω_n represents the closed-loop poles, which can be chosen as x times faster than the open loop poles $\frac{L_{eq}}{R_{eq}}$, i.e $\xi = 1$, $\omega_n = \frac{x}{\frac{L_{eq}}{R_{eq}}}$ [33]. The same procedure is adopted for the RSC considering the MMC per phase impedance $\frac{R_{arm}}{2}$ and $\frac{L_{arm}}{2}$, and the DFIG rotor plant [1]. Fig. 7 depicts the RSC control loop considering the MMC, with the following transfer functions:

$$\frac{i_{rd}(s)}{i_{rdref}(s)} = \frac{sk_{p(RSC)} + k_{i(RSC)}}{s^2(A) + s(B + k_{p(RSC)}) + k_{i(RSC)}}, \tag{28}$$

$$\frac{i_{rq}(s)}{i_{rqref}(s)} = \frac{sk_{p(RSC)} + k_{i(RSC)}}{s^2(A) + s(B + k_{p(RSC)}) + k_{i(RSC)}}, \tag{29}$$

in which $A = \sigma L_r + \frac{L_{arm}}{2}$, and $B = R_r + \frac{R_{arm}}{2}$. Approximating the transfer function denominators to a second-order system and adopting $\xi = 1$, yields:

$$s^2(\sigma L_r + \frac{L_{arm}}{2}) + s(R_r + \frac{R_{arm}}{2} + k_{p(RSC)}) + k_{i(RSC)} \approx s^2 + 2\xi\omega_{n(RSC)}s + \omega_n^2, \tag{30}$$

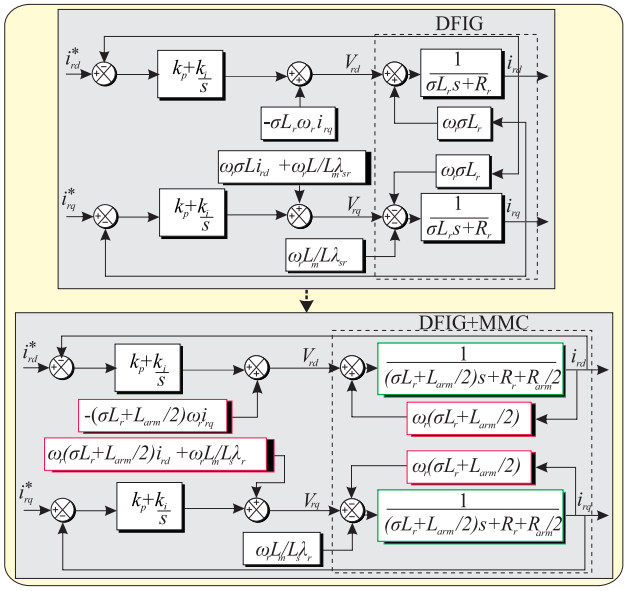

FIGURE 7. RSC control loop with MMC model.

$$s^2 + s\left(\frac{R_r + \frac{R_{arm}}{2} + k_{p(RSC)}}{\sigma L_r + \frac{L_{arm}}{2}}\right) + \frac{k_{i(RSC)}}{\sigma L_r + \frac{L_{arm}}{2}} \approx s^2 + 2\xi\omega_n s + \omega_n^2, \tag{31}$$

$$k_{i(RSC)} = \left(\sigma L_r + \frac{L_{arm}}{2}\right)\omega_n^2, \tag{32}$$

$$k_{p(RSC)} = \left(\sigma L_r + \frac{L_{arm}}{2}\right)2\xi\omega_n - \left(R_r + \frac{R_{arm}}{2}\right), \tag{33}$$

where the RSC the closed-loop poles ω_n is given by:

$$\omega_n = \frac{x}{\frac{\sigma L_r + L_{arm}/2}{R_r + R_{arm}/2}}. \tag{34}$$

The general control purpose is described as follows: the GSC employs a vector control-based strategy in synchronous reference frame $dq0$, in which the DC bus voltage, V_{bus}, is controlled by an outer PI regulator providing the desired active power reference, P_{gref}, through i_{gdref}. An inner regulator controls the reactive power, Q_{gref}, through i_{gqref}; this reference is zero, which indicates that there is no reactive power delivered to the network [3]. The Clarke and Park transform was applied for the currents measured at the CCP and transformed to synchronous $dq0$ reference, thus generating the i_{gd} and i_{gq} used in the inner controllers; these regulators provide the desired grid reference voltages through V_{fdref} and V_{fqref}, used in the Park inverse transform to generate the trigger signals through the PWM.

For the grid synchronization, a phase-locked loop (PLL) provides the angle, θ_g, used in Park direct and inverse transforms. The RSC control employs the stator flux vector orientation, λ_s, in $dq0$ reference frame for variable decoupling, where the d-axis is aligned with the stator vector flux [3]. Thus, the d-axis is aligned with the stator flux referential, $\lambda_{sd} = \lambda_s$, to cancel the quadrature component of the stator vector flux $\lambda_{sq} = 0$. The RSC controls the DFIG through an external reactive power control loop, in which the Park transform applied to the rotor currents i_{rabc}, obtaining i_{rdq}.

The reactive power, Q_s, can be controlled by i_{rd}, while the torque is controlled by i_{rq}. Thus, $Q_{sref} = 0$ is maintained, for no reactive power consumption, the d-axis rotor current reference, i_{rdref}, is determined by the output of the PI regulator. A PLL is used for stator voltage grid synchronization, providing the angle θ_r. On the other hand, the reference torque T_{emref} is obtained at the output of a PI regulator that has as input the difference between the mechanical and reference speeds ($\omega_m - \omega_{mref}$), thus obtaining the q-axis rotor current reference, i_{rqref}. Two internal PI regulators generate the d and q-axis reference voltages, V_{rdref} and V_{rqref}, which are employed in the inverse Park transform providing the S_{rA}, S_{rB} and S_{rB} RSC trigger signals.

The PDPWM technique gives the number of active submodules by comparing the reference voltages, V_{fAref}, V_{fBref}, and V_{fCref}, between two level-shifted triangular carriers in phase with each other.

The PWM employs a sorting algorithm for MMC submodules capacitor voltage equalization; the algorithm is based on the MMC upper and lower arms current direction. The PDPWM gives the number of active submodules; the sorting algorithm determines which submodule should be inserted or bypassed. If the arm current is positive, the N submodules with the lowest voltages must be activated; conversely, the N submodules with the highest voltages must be activated if the arm current is negative. Finally, after determining the active submodules, the trigger signals are sent to the converters. The controller's design was performed using the method described in [3]. An trial and error tuning technique was adopted, including R_{arm} and L_{arm} values to determine the proportional K_p and integral K_i gains. Fig. 8 depicts the schematic step-by-step control tuning diagram used for the proposed control. The diagram is based on the abovementioned equations and demonstrates the calculation procedure of the GSC controllers; analogous, this scheme was adopted to obtain the RSC controller's parameters. Based on the above-mentioned DFIG controller's design proposal, the synchronism loop, and the PWM technique, Fig. 9 depicts the complete control loops structure of the GSC and RSC. In addition, Table 1 presents the major contributions of this paper.

V. PERFORMANCE ASSESSMENT OF THE PROPOSED MMC-DFIG LVRT WITH EXISTING CONTROLLERS

To demonstrate the MMC current-limiting function and damping capability, both symmetrical and asymmetrical fault scenarios were considered: single line-to-ground (SLG), line-to-line (LL), double line-to-ground (DLG), and LLL with a 150 ms duration. Each fault was simulated with specific fault resistance to result in voltage sags with 20, 50, and 80%. The MMC were set with 3, 21, 51, and 101 levels. Matlab/Simulink platform was used for DFIG-based WECS simulations. The performance assessment presented in this section considers the conventional DFIG vector control as [1]

TABLE 1. Summary of the fault current suppression method for DFIG LVRT improvement.

Proposed fault current suppression method	Advantages	Contributions
DFIG LVRT improvement through MMC.	No additional hardware; Avoids physical protection activation; No complex control loops; Maintains DFIG controllability and connection under LVRT.	✓DFIG with MMC arm impedance dynamic equations and control; ✓MMC arm impedance and number of levels for fault current suppression under LVRT.

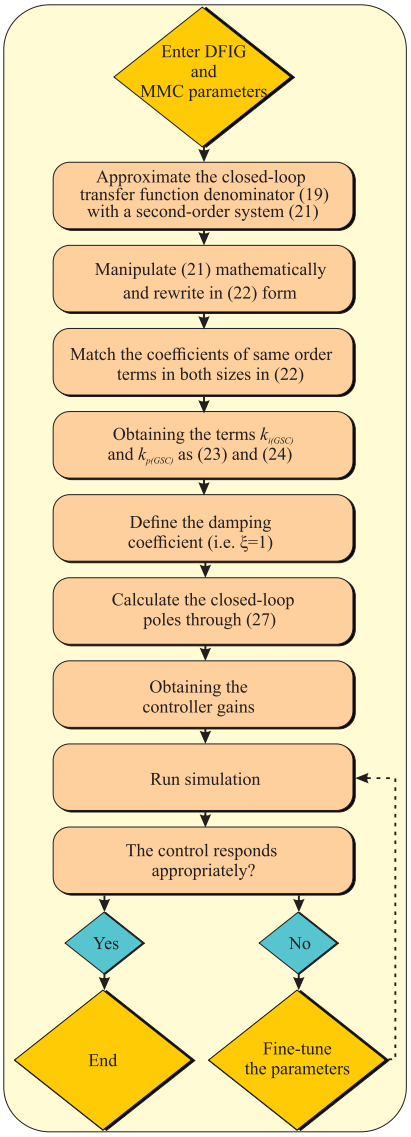

FIGURE 8. Step-by-step control tuning scheme.

employing the proposed DFIG-based WECS with back-to-back MMC. Table 2 presents the system parameters. The normalized RMS value of DFIG rotor and stator currents for two cycles immediately after the fault was adopted to determine the overcurrent level. For the LL, DLG, and LLL fault, the overcurrent level was obtained through the normalized RMS mean value of the individual phases. At the fault moment,

TABLE 2. System parameters.

Parameter	Value
Rated power	2 MW
Electrical frequency	50 Hz
Rated speed	1800 rpm
Rated line-to-line stator voltage	690 V
Poles	2
Stator resistance R_s	2.6 mΩ
Stator inductance L_s	2.587 mH
Rotor resistance R_r	0.087 mΩ
Rotor inductance L_r	2.587 mH
Stator leakage inductance $L_{\sigma s}$	0.087 mH
Rotor leakage inductance $L_{\sigma s}$	0.087 mH
Magnetizing inducante L_m	2.5 mH
DC bus voltage	1260 V
DC capacitor	100 mF
Switching frequency	2 kHz
MMC arm resistance R_{arm}	0.5 Ω
MMC arm inductance L_{arm}	15 uH
MMC submodule capacitance C_{SM}	15 mF
Grid line resistance R_g	0.487 Ω
Grid line inductance L_g	4.2 mH
$k_{p(GSC)} = k_{i(GSC)}$	0.1923
$k_{p(RSC)} = k_{i(RSC)}$	1.0746

the GSC and RSC converters were not turned off. A heatmap presents the simulation results of the pre-fault normalized RMS current values in Tables 3, 4, and 5, for 20, 50, and 80% voltage sag, respectively, regarding the fault type, the increase in the number of MMC levels, and the normalized RMS values of the rotor and stator currents. For the LL fault, considering the line parameters, the most severe voltage sag obtained was 50%.

A. 20% VOLTAGE SAG SCENARIO

Table 3 presents the obtained results considering the DFIG-based WECS employing the MMC with the conventional vector control loops. Thus, the MMC transfer function was not considered, and only the control design based on the DFIG parameters was adopted, as described by [3]. Despite the MMC plant not being considered for control design, a reduction of the DFIG rotor and stator currents is provided when the number of converter levels increases due to the submodules increment that leads to an increase of the MMC arm R-L characteristic. A summary of the data in Table 3 is as follows:

- SLG fault: The DFIG rotor overcurrents were effectively suppressed, with 3L-MMC presenting the worst case of approximately 1.701 and 101L-MMC with the

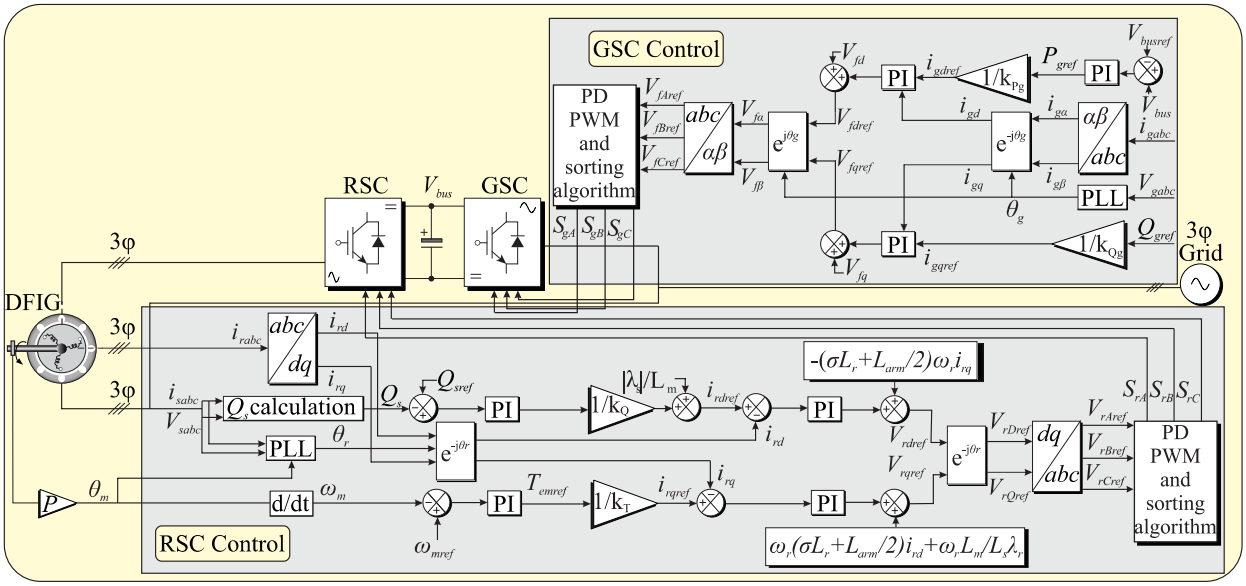

FIGURE 9. DFIG complete control loops.

TABLE 3. DFIG currents heatmap for 20% voltage sag.

	Levels	SLG	LL	DLG	LLL
Rotor	3	1.701	2.316	1.475	0.972
	21	1.631	2.186	1.452	0.965
	51	1.613	2.181	1.418	0.943
	101	1.453	2.176	1.399	0.919
Stator	3	1.610	0.971	1.297	0.755
	21	1.627	0.948	1.291	0.650
	51	1.577	0.908	1.192	0.600
	101	1.487	0.872	1.168	0.592

Value

Lowest Highest

TABLE 4. DFIG currents heatmap for 50% voltage sag.

	Levels	SLG	LL	DLG	LLL
Rotor	3	1.687	2.233	1.774	0.806
	21	1.635	2.229	1.729	0.805
	51	1.586	1.885	1.638	0.801
	101	1.505	1.825	1.626	0.784
Stator	3	1.620	0.874	1.491	0.394
	21	1.604	0.849	1.360	0.382
	51	1.557	0.802	1.357	0.366
	101	1.529	0.743	1.255	0.343

best case of 1.453 above the pre-fault value, representing a 14.57% reduction. On the other hand, the stator overcurrents present a 7.63% reduction, considering the 3L-MMC worst case with 1.610 and 101L-MMC the best case with 1.487 normalized RMS value above the pre-fault.

TABLE 5. DFIG currents heatmap for 80% voltage sag.

	Levels	SLG	LL	DLG	LLL
Rotor	3	1.681	*	1.478	0.867
	21	1.674	*	1.476	0.821
	51	1.602	*	1.420	0.790
	101	1.527	*	1.397	0.788
Stator	3	1.347	*	1.100	0.395
	21	1.308	*	1.070	0.345
	51	1.270	*	0.835	0.327
	101	1.248	*	0.792	0.297

- LL fault: The rotor currents were suppressed approximately 6.04%, considering the 3L-MMC and 101L-MMC to be the worst and best case, with 2.316 and 2.176 normalized RMS values, respectively, above the pre-fault. Meanwhile, the stator currents presented a reduction of 10.19%, with superior performance.
- DLG fault: The DFIG rotor currents were reduced around 5.15%, considering the worst and best case, 1.475 and 1.399 normalized RMS values, for 3L-MMC and 101L-MMC, respectively. On the other hand, the stator currents presented a reduction of 9.94%.
- LLL fault: The MMC presented the best performance for the worst-case LLL fault scenario, with the lowest overcurrent values for both rotor and stator. In this case, the reduction for the rotor and stator currents, considering the 3L-MMC and 101L-MMC, were 5.45% and 21.59%, respectively.

Considering a 20% voltage sag scenario, the DFIG rotor, and stator fault currents were effectively suppressed with the MMC arm impedance in all fault scenarios, relieving the overcurrents under fault period as the number of MMC levels increased.

B. 50% VOLTAGE SAG SCENARIO

The same comparison was performed considering a more severe voltage sag of 50%; with the same approach employing the MMC with conventional control, the rotor and stator fault currents of the DFIG were substantially relieved. A summary of the data in Table 4 is as follows:

- SLG fault: The MMC arm impedance suppressed the rotor currents by about 10.78%, considering the 3L-MMC and 101L-MMC as the worst and best case, with 1.687 and 1.505, respectively, above the pre-fault value. On the other hand, the stator currents were suppressed by about 5.61%, with 1.620 and 1.529, between the maximum and minimum normalized RMS values.
- LL fault: The rotor currents were suppressed by the MMC arm impedance around 18.3%, considering the maximum and minimum normalized RMS values, 2.233 and 1.825 for the 3L and 101L-MMC, respectively. Conversely, the stator currents presented a similar performance, with a 15% reduction considering the maximum and minimum overcurrent of 0.874 and 0.743, respectively.
- DLG fault: The rotor currents presented an 8.34% reduction between 1.774 and 1.629 for the maximum and minimum normalized overcurrent RMS values, respectively, for the 3L and 101L-MMC. On the other hand, the stator current presented superior performance with a 15.8% fault current reduction between the worst and best case, 1.491 and 1.255, respectively.
- LLL fault: For the worst-case LLL fault, the MMC arm impedance suppressed the DFIG rotor currents around 2.73%, considering the maximum and minimum normalized RMS values of 0.806 and 0.784 for the 3L and 101L-MMC, respectively. However, the stator currents were reduced by around 12.9%, considering the maximum and minimum of 0.394 and 0.343.

For the 50% voltage sag scenario, the DFIG rotor and stator fault currents performed similarly to the 20% voltage sag scenario, relieving the overcurrent under fault period as the MMC levels increased.

C. 80% VOLTAGE SAG SCENARIO

Finally, the fault current suppression method was assessed for the worst case, considering a voltage sag of 80% at the DFIG stator terminals for all kinds of faults. As expected, in this scenario, the MMC provided a relief in the DFIG's overcurrents, demonstrating that even with the conventional control without including the MMC dynamics, the system could perform the fault current limiting function when the MMC number of levels increased. A summary of the data in Table 5 is as follows:

- SLG fault: The MMC arm impedance suppressed the rotor currents by about 9.16%, between the maximum and minimum normalized RMS values of 1.681 and 1.527 for the 3L and 101L-MMC, respectively. On the other hand, the stator currents achieved a 7.34% reduction between the worst and best case, 1.347 and 1.248, respectively.
- DLG fault: The rotor currents were suppressed around 5.48% under fault period, considering the 3L and 101L-MMC with 1.487 and 1.397 for the normalized RMS values, respectively. In addition, the stator fault currents were reduced by 28%, between the maximum and minimum 1.100 and 0.792 for the 3L and 101L-MMC.
- LLL fault: Considering the worst-case LLL fault and 80% voltage sag, the MMC arm impedance suppressed the DFIG rotor currents by about 9.11%, between the worst and best case with 0.867 and 0.788 for the normalized RMS values of the 3L and 101L-MMC, respectively. On the other hand, the stator currents were reduced by 24.81%, between worst and best case, 0.395 and 0.297, respectively.

For the worst-case scenario with 80% voltage sag, the DFIG rotor and stator fault currents performed similarly to the 20, and 50% voltage sag scenarios, relieving the overcurrent level as the number of MMC levels increased.

Despite using conventional control loops, the performance assessment with vector control demonstrates the effectiveness of the proposed DFIG-based WECS fault current suppression method due to the MMC arm impedance current-limiting function capability and increased level. Then, it maintained controllability even under fault conditions, reducing or avoiding the physical protection activation and providing LVRT enhancement.

VI. PERFORMANCE ASSESSMENT OF THE PROPOSED MMC-DFIG LVRT WITH PROPOSED CONTROLLERS

To validate the proposed fault current suppression method, simulations considering the proposed control structure in DFIG-based WECS were carried out. In order to perform a proper comparison, the same scenarios of 20, 50, and 80% voltage sags were considered, and the normalized RMS value was also adopted to measure the DFIG fault currents suppression enhancement.

A. 20% VOLTAGE SAG SCENARIO

Table 6 presents the results obtained considering the DFIG-based WECS and the MMC using the proposed con-

TABLE 6. DFIG currents heatmap for 20% voltage sag with the proposed control.

	Levels	SLG	LL	DLG	LLL
Rotor	3	1.639	2.293	1.461	0.955
	21	1.614	2.170	1.442	0.940
	51	1.494	2.162	1.371	0.927
	101	1.445	2.145	1.350	0.895
Stator	3	1.549	0.948	1.230	0.740
	21	1.544	0.906	1.132	0.623
	51	1.488	0.886	1.082	0.586
	101	1.415	0.869	0.728	0.574

trol structure, in which the transfer function representing the MMC dynamics was taken into account for the controller's design. Thus, all the control parameters such as the system time constant, the damping, and the controller's gains were recalculated, also considering L_{arm} and R_{arm}. The results obtained for 20% voltage sags highlight the behavior of the MMC interaction in the control plant, which provides a better dynamic response in the suppression of fault currents compared to the same previous scenario employing conventional control. A summary of the data in Table 6 is as follows:

- SLG fault: The rotor currents were relieved around 11.83% considering the MMC with 3 and 101 levels. Compared to the same previous scenario employing the conventional control, there was a reduction of 3.64% and 0.55% for the rotor currents considering the 3L and 101L-MMC. On the other hand, the stator currents were suppressed around 8.65% between the worst and best case.
- LL fault: In this scenario, the DFIG rotor and stator currents were relieved around 6.45% and 8.33%, considering the 3L and 101L-MMC, respectively. The fault currents were also lower than the structure with conventional control for all levels of the MMC.
- DLG fault: For the worst and best case, the rotor and stator currents showed better performance with DFIG fault current suppression around 7.59% and 40.81% with the 3L and 101L-MMC. Similar to the previous cases, the fault currents obtained a reduction for all levels of the MMC.
- LLL fault: For the worst-case scenario, the 3L and 101L-MMC in suppressing the rotor and stator fault currents was 6.28% and 22.43%, respectively, and all the results obtained for the fault currents were lower than the results employing the conventional control structure.

B. 50% VOLTAGE SAG SCENARIO

The fault current suppression method for DFIG employing the proposed control structure was tested considering a 50% voltage sag as presented in Table 7. The same previous scenario conditions obtained for Table 4 were ensured so that comparisons with the conventional control could be appropriate. A summary of the data in Table 7 is as follows:

- SLG fault: The DFIG fault currents of the rotor and stator were suppressed around 10.78% and 5.61% considering the 3L and 101L-MMC, demonstrating better performance using the proposed control compared to the same scenario employing the conventional control. In addition, like the previous assessments, the fault currents obtained better performance for all MMC levels.
- LL fault: In this scenario, the fault currents were suppressed by 15.2% and 15.34% for the 3L and 101L-MMC, respectively. Compared to the same scenario employing the conventional control, all the currents achieved better performance.
- DLG fault: With the proposed method, the DFIG fault currents were relieved around 5.07% and 31.8% for the 3L and 101L-MMC. Furthermore, it was verified that this scenario obtained better performance with the proposed control structure than the conventional control.
- LLL fault: For the worst-case scenario, the fault currents were relieved around 5.45% and 19.46% for the 3L and 101L-MMC, respectively. Furthermore, as in previous cases, with the proposed control, the performance was substantially improved compared to the conventional control, confirming that with increasing the number of converter levels, the DFIG fault currents are effectively suppressed.

C. 80% VOLTAGE SAG SCENARIO

The last scenario for the performance assessment was performed under the same conditions as in the results obtained in Table 5, considering a voltage sag of 80%, using the proposed control structure, including the MMC dynamics. A summary of the data in Table 8 is as follows:

- SLG fault: The DFIG rotor and stator fault currents through the 3L and101L-MMC were suppressed by 10.51% and 22.44%, respectively. In addition, a significant reduction in currents was observed compared to the previous cases for all levels of the MMC.
- DLG fault: In this scenario, fault currents were reduced considering the 3L and 101L-MMC around 13.37% 28.38%, respectively. Similar to the previous results, the currents obtained a superior performance instead of the DFIG-based WECS employing the conventional control.

TABLE 7. DFIG currents heatmap for 50% voltage sag with the proposed control.

	Levels	SLG	LL	DLG	LLL
Rotor	3	1.622	2.118	1.559	0.806
	21	1.584	2.112	1.549	0.801
	51	1.562	1.811	1.497	0.784
	101	1.487	1.796	1.480	0.762
Stator	3	1.356	0.841	1.079	0.370
	21	1.258	0.826	0.820	0.355
	51	1.129	0.780	0.844	0.334
	101	1.044	0.712	0.736	0.298

TABLE 8. DFIG currents heatmap for 80% voltage sag with the proposed control.

	Levels	SLG	LL	DLG	LLL
Rotor	3	1.674	*	1.451	0.854
	21	1.632	*	1.420	0.807
	51	1.535	*	1.292	0.774
	101	1.498	*	1.257	0.735
Stator	3	1.114	*	0.835	0.367
	21	1.008	*	0.777	0.335
	51	0.994	*	0.603	0.317
	101	0.864	*	0.598	0.243

TABLE 9. Summary of the MMC-DFIG LVRT performance assessment for 20% voltage sag.

		CTRL I	CTRL II	CTRL I	CTRL II	CTRL I	CTRL II	CTRL I	CTRL II
	Levels	SLG		LL		DLG		LLL	
Rotor	3	1.701	1.639	2.316	2.293	1.475	1.461	0.972	0.955
	21	1.631	1.614	2.186	2.170	1.452	1.442	0.965	0.940
	51	1.613	1.494	2.181	2.162	1.418	1.371	0.943	0.927
	101	1.453	1.445	2.176	2.145	1.399	1.350	0.919	0.895
Stator	3	1.610	1.549	0.971	0.948	1.297	1.230	0.755	0.740
	21	1.627	1.544	0.948	0.906	1.291	1.132	0.650	0.623
	51	1.577	1.488	0.908	0.886	1.192	1.082	0.600	0.586
	101	1.487	1.415	0.872	0.869	1.168	0.728	0.592	0.574

Legend
CTRL I: existing controllers. CTRL II: proposed controllers.

TABLE 10. Summary of the MMC-DFIG LVRT performance assessment for 50% voltage sag.

		CTRL I	CTRL II	CTRL I	CTRL II	CTRL I	CTRL II	CTRL I	CTRL II
	Levels	SLG		LL		DLG		LLL	
Rotor	3	1.687	1.622	2.233	2.118	1.774	1.559	0.806	0.806
	21	1.635	1.584	2.229	2.112	1.729	1.549	0.805	0.801
	51	1.586	1.562	1.885	1.811	1.638	1.497	0.801	0.784
	101	1.505	1.487	1.825	1.796	1.626	1.480	0.784	0.762
Stator	3	1.620	1.356	0.874	0.841	1.491	1.079	0.394	0.370
	21	1.604	1.258	0.849	0.826	1.360	0.820	0.382	0.355
	51	1.557	1.129	0.802	0.780	1.357	0.844	0.366	0.334
	101	1.529	1.044	0.743	0.712	1.255	0.736	0.343	0.298

TABLE 11. Summary of the MMC-DFIG LVRT performance assessment for 80% voltage sag.

		CTRL I	CTRL II	CTRL I	CTRL II	CTRL I	CTRL II	CTRL I	CTRL II
	Levels	SLG		LL		DLG		LLL	
Rotor	3	1.681	1.674	*	*	1.478	1.451	0.867	0.854
	21	1.674	1.632	*	*	1.476	1.420	0.821	0.807
	51	1.602	1.535	*	*	1.420	1.292	0.790	0.774
	101	1.527	1.498	*	*	1.397	1.257	0.788	0.735
Stator	3	1.347	1.114	*	*	1.100	0.835	0.395	0.367
	21	1.308	1.008	*	*	1.070	0.777	0.345	0.335
	51	1.270	0.994	*	*	0.835	0.603	0.327	0.317
	101	1.248	0.864	*	*	0.792	0.598	0.297	0.243

- LLL fault: Finally, for the worst-case, the rotor and stator fault currents were suppressed around 13.93% and 23.78%, considering the 3L and 101L-MMC, respectively. As expected, using the proposed control, DFIG demonstrated an improved performance under LVRT conditions compared to the same case with conventional control.

The results with the proposed control loops considering the MMC dynamics in the DFIG transfer function improved substantially compared to the DFIG-based WECS with the conventional vector control in Section V. Since the conventional control considers a traditional 2L-VSC converter for control design, the improved results are due to the MMC parameter interaction in the GSC and RSC controllers. This reflects the DFIG-based WECS operation with the back-to-back MMC, which corroborates the effectiveness of the proposed fault current suppression method. Tables 9, 10, and 11 present the comparison summary of the MMC-DFIG LVRT performance assessment with existing (CTRL I) and the proposed controllers (CTRL II).

VII. CONCLUSION

This paper presented a new fault current suppression method for the doubly fed induction generator low voltage ride through improvement through modular multilevel converter. Several low voltage ride-through conditions covered symmetrical and asymmetrical faults with 20, 50, and 80% voltage sags. Furthermore, the interaction between the modular

multilevel converter impedance was demonstrated through the dynamic equations, corroborating the validation of the results. During the fault period, the back-to-back converters operated continuously, ensuring the low voltage ride-through of the doubly fed induction generator. The performance assessment demonstrated that both the modular multilevel converter arm impedance and increased levels effectively suppressed rotor and stator fault currents. Through an trial and error tuning technique, the conventional control was able to drive the doubly fed induction generator under several fault conditions. Furthermore, unlike other proposals in the literature, neither additional hardware nor control loops are necessary for overcurrent reduction during the fault period, contributing to cost and implementation complexity reduction. The proposed approach also contributes to the employment of modular multilevel converters at a wide range of power levels in wind energy conversion systems under low voltage ride through conditions due to its modular structure, easy expansiveness, support for higher voltage levels, power quality, and fault tolerance. Improvements under low-frequency operation condition are encouraged for further research and analysis with this paper proposal.

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