An Analog-Assisted Digital LDO With Dynamic-Biasing Asynchronous Comparator

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ABSTRACT This paper presents a digital low-dropout regulator (DLDO) with three-level switching (TLS) and analog-assisted (AA) structure formed by dynamic-biasing asynchronous comparator, capacitive-coupling RC network and auxiliary power switch. The proposed AA-DLDO is fabricated in a 65-nm CMOS process. The minimum load current is 18 μA. The maximum undershoot is 200 mV under load transient of 4.82-mA/1-ns. The recovery time is 8 ns. The figure-of-merit of proposed design is better than the other DLDOs by more than 14 times.

INDEX TERMS Digital LDO, three-level switching, dynamic biased asynchronous comparator.

I. INTRODUCTION

Digital low-dropout regulator (DLDO) enables voltage regulation at ultra-low supply and possesses the potential performance enhancements from process scaling of integrated-circuit technology [1]–[12]. The prior research works of DLDO were predominantly focused on load transient response, which is partly determined by switching frequency (f_{sw}), on-chip output capacitance (C_{OUT}) and turn-on/off strategy of power-switch array. Like the typical digital circuits and dc-dc converters, a higher f_{sw} and a larger C_{OUT} would result in better dynamic responses, but much larger quiescent current (I_Q) and chip area are the costs. To achieve low-power operation and small circuit size of DLDO, many researchers focused on the turn-on/off strategy of power-switch array. Methods such as binary-weighted strategy [1]–[4], coarse-fine switching [5]–[8] and multi-step switching scheme [9] were reported. In recent years, the concept of hybrid structure by introducing analog part to the DLDO shows the opportunity to further improve dynamic responses. Analog-assisted (AA)-DLDO, therefore, becomes a new research direction to enhance transient performance. A novel AA-LDOs reported in [10] uti-

lizes capacitive-coupling effect to momentarily increase the gate drive of power switches through the gate drivers, such that a temporarily increase of drain current helps to reduce the transient errors of the output voltage (V_{OUT}) of DLDO during load transients. However, there are some critical issues with this design. For example, a simple coarse-fine strategy to turn on/off the power-switch array does not impact the load transient significantly. Improvement from the AA part cannot be achieved for transients starting with a very low initial load current (I_{LOAD}). Details of limitations of the DLDO in [10] will be presented and explained in Section II.

This paper proposes an AA structure formed by a dynamic-biasing asynchronous comparator, a capacitive-coupling RC circuit and an auxiliary power switch to further improve the dynamic response, which are recovery time (T_R) and the undershoot magnitude of V_{OUT} (ΔV_{OUT}), of the DLDO, even though the initial level of load transient is very low. The proposed DLDO and simulation results will be presented in Section III. Experimental results and a comparison with state-of-the-art DLDOs will be reported in Section IV. Finally, the conclusion of this paper is given.

II. PROPOSED HYBRID LDO

In this section, the DLDO reported in [10] is revisited. The critical issues with the design are introduced. The information

FIGURE 1. Topology of DLDO with coarse-fine strategy.

FIGURE 2. Simulated load transient responses of DLDO with coarse-fine switching.
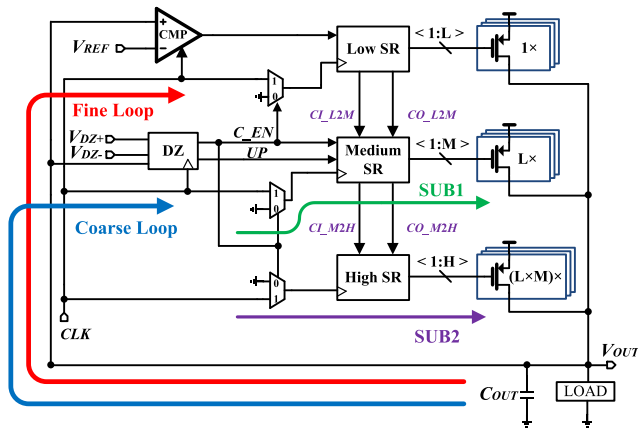
is expected to be useful to explain the motivations of proposed circuit methods to be presented in Section III.

A. COARSE-FINE SWITCHING

Coarse-fine switching of power-switch array with non-linear word control to the coarse loop is utilized to the DLDO in [10] to improve load transient responses. Fig. 1 shows the schematic of a DLDO with typical coarse-fine switching. The structure of fine loop is same as the other designs. The coarse loop is divided into two subsections, namely SUB1 and SUB2, where the unit size of the power switch in SUB2 is *M* times bigger than that in SUB1. These two subsections are controlled by carry-in signal *CI_M2H* and carry-out signal *CO_M2H*. The upper bounded voltage and lower bounded voltage for dead-zone control circuit to activate/deactivate coarse loop for faster load transient response are V_{DZ+} and V_{DZ-} respectively. The control signal, *C_EN* is used to activate/deactivate fine and coarse loop to achieve accurate and fast speed voltage regulations. The *UP* signal is used to determine whether the bi-directional shift register in these two subsections of coarse loop shifts up or down. Upon receiving load transient by the DLDO, the coarse loop will be activated directly. Initially, the small switches in SUB1 are turned on one by one. When all switches in SUB1 are turned on but they are not sufficient to provide the required amount of load current, they will be reset and one more switch in SUB2 is then turned on. This mechanism repeats until enough power switches in both SUB1 and SUB2 are turned on to fulfill the load requirement. The fine loop is used to provide higher accuracy of voltage regulation at the output finally. Even non-linear word control to the coarse loop is applied, two clock cycles are still needed to turn on a power switch in SUB2. A simulation of a DLDO with coarse-fine switching has been carried out. The results are shown in Fig. 2. Two cases of load transients with current step of about 0.85 mA with two different I_{LOAD}, where the blue one represents 18 μA while the red one is for the case of 0.61 mA, are applied to observe the differences of ΔV_{OUT}. Edge times of both load transient are the same. From the results, the DLDO with coarse-fine
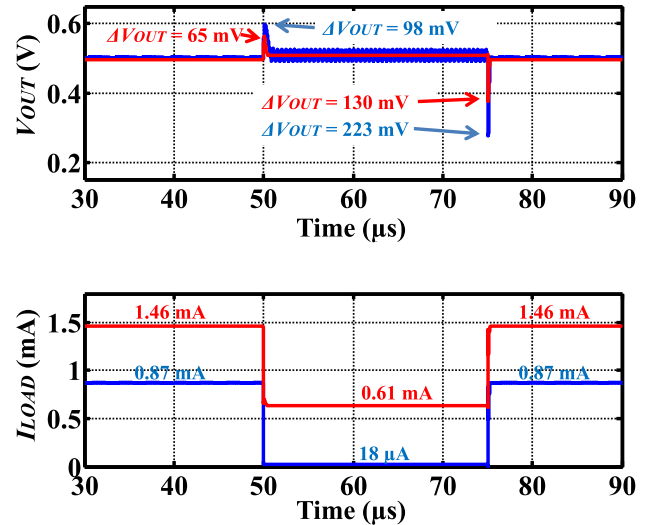
switching has a larger ΔV_{OUT} when the initial I_{LOAD} is low. The reason is that the case with lower initial I_{LOAD} has fewer power switches turned on initially. Thus, when the DLDO cannot respond, only a small momentary increment of source-to-drain voltage (V_{SD}) of the power switches due to the undershoot helps to the increase the drain current provided by the power switches themselves. This effect is effective only when many and large power switches are initially turned on which is the case that the initial I_{LOAD} is not small. To explain this concept more clearly, a test bench for an analysis of transient current generated by large and small power switches is conducted. Fig. 3 shows the momentary change of source-to-drain current (I_{SD}) upon the change of V_{SD} due to undershoot (i.e., ΔV_{OUT}) for a fixed source-to-gate voltage (V_{SG}). From this analysis, ΔI_{LOAD} generated by the power switches themselves without adjusting V_{SG} are 0.74 mA (for large switch) and 3.8 μA (for small switch), respectively. As a result, when the initial I_{LOAD} is small and only small power switches are turned on, ΔV_{OUT} is much larger since this small ΔI_{LOAD} cannot compensate the drop of V_{OUT}. Therefore, the load transient response with small initial I_{LOAD} is a critical performance in DLDO design.

B. ANALOG-ASSISTED PART

A simple high-pass *RC* network formed by R_P and C_P is connected between V_{OUT} and the lower supply rail (i.e., V_{SS}) of gate driver in [10], as shown in Fig. 4(a) where only one power switch, M_P, is shown to illustrate the concept. There are two possibilities of operation: (i) M_P is initially off, shown in Fig. 4(b), and (ii) M_P is initially on, shown in Fig. 4(c). When there is a load transient at t_1, an undershoot occurs at V_{OUT} between t_1 and t_2 because of insufficient current from the power-switch array. The transient error (i.e., ΔV_{OUT}) is coupled by R_P and C_P to pull down V_{SS} momentarily. The gate voltages of the power switches are then momentarily
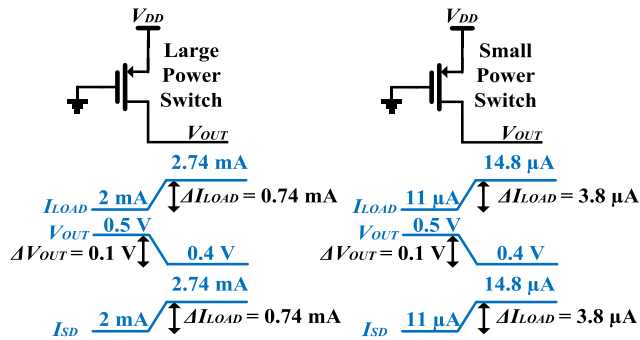
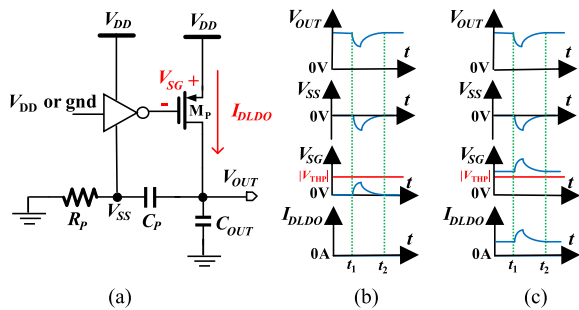**FIGURE 3.** Test bench for an analysis of transient current against large and small size of power switches.

FIGURE 4. (a) Gate driver structure used in [10], (b) timing diagrams when M$_P$ is initially off, and (c) timing diagrams when M$_P$ is initially on.

TABLE 1. Operation mode of TLS.

C_EN1	C_EN2	Mode of operation	Resolution	Speed
0	0	Fine	High	Low
1	0	Coarse	Medium	Medium
1	1	Super-Coarse	Low	High

increased. When M$_P$ is initially off, the momentary increase of V_{SG} is not large enough to turn on M$_P$ to provide momentarily current (i.e., ΔI_{DLDO}) to reduce ΔV_{OUT}. The structure is useful only when M$_P$ is initially on. Thus, when the load transient starts from a very low level, not many power switches are on initially and the structure in Fig. 4(a) is thus not effective to reduce ΔV_{OUT}. The structure is useful only when there are enough turned-on power switches, which is the condition that the minimum load level of the transient is high. It is noted that the load transient range of the DLDO in [10] is 2–12 mA, according to measurement results. Although it is claimed that the minimum I_{LOAD} is 0.2 mA, this number is obtained from the measurement results of the steady-state performances (i.e., load and line regulations) but not from the transient performance. In fact, there is no measurement data to show the transient response when I_{LOAD} starts from 0.2 mA.

III. PROPOSED AA-DLDO WITH TLS
The proposed AA-DLDO is shown in Fig. 5. The DLDO part is formed by fine, coarse and super-coarse loops, which
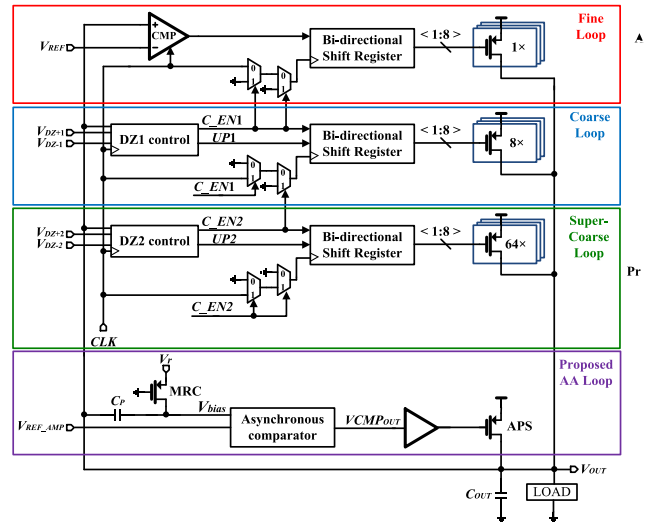

FIGURE 5. Structure of proposed AA-DLDO with TLS.

are responsible for different load transient step magnitudes, to achieve the three-level switching (TLS) [13]. The basic operation principle of the tri-loop is to supply current to the load based on the transient error magnitude which is defined by two dead-zones. The unit size of power switch in super-coarse loop enables a much higher driving current to load for every clock cycle such that ΔV_{OUT} can be reduced significantly when comparing to the conventional coarse-fine design. The AA-part is formed by a dynamic-biasing asynchronous comparator, a capacitive-coupling RC high-pass network and an auxiliary power switch (APS). Three different sizes of power switches with size ratio of 1:8:64 are used in the fine, coarse and super-coarse loop, respectively. The shift-register lengths of fine, coarse and super-coarse loops are eight. The overall size of power switches is the same as the coarse-fine counterpart in reported [10] under the same loading condition. The driving current from the super-coarse loop is eight times larger than that from the coarse loop. The super-coarse loop is activated directly in one cycle upon receiving a large load transient. Thus, when comparing with the coarse-fine switching used in [10], the TLS is more effective to reduce ΔV_{OUT} and T_R under the same f_{SW}. As shown in Fig. 5, The dead-zones of the coarse and super-coarse loops are DZ1 and DZ2, respectively. DZ1 is bounded by V_{DZ+1} and V_{DZ-1}, and DZ2 is restricted by V_{DZ+2} and V_{DZ-2}. Two control signals, C_EN1 and C_EN2, are used to activate/deactivate DZ1 and DZ2 to enable/disable the operation of these three loops as shown in Table 1. It is not surprising that the DLDO with TLS can further reduce ΔV_{OUT} and T_R with a much higher f_{sw}. However, efficiency will be seriously degraded due to high switching loss of power switches. To maintain a reasonable f_{SW} to retain high efficiency, the proposed AA structure, which is used to deal with transients, is added in parallel to the DLDO structure. It does not require a specific load requirement, such as the minimum load condition, to activate it for transient
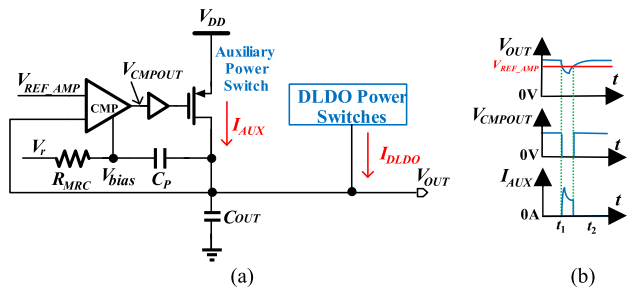
FIGURE 6. Proposed AA part (a) circuit structure, and (b) timing diagram.

FIGURE 7. Asynchronous comparator with dynamic biasing.

FIGURE 8. Mechanism of load transient response of proposed AA-LDO.

improvement. An asynchronous comparator is used to control the APS to deliver transient current to the load. Thus, dynamic biasing is applied to the comparator to temporarily boost the speed of comparator at the instant of load transient. This approach effectively reduces the static power consumption by the proposed AA structure. Fig. 6(a) shows the connections of the asynchronous comparator, buffer, APS and the capacitive-coupling RC network. From Fig. 6(b), upon receiving load transient to cause ΔV_{OUT}, the comparator triggers its output V_{CMPOUT} to turn on the APS momentary to deliver a temporary current I_{AUX} to help to recover V_{OUT}. Initially, V_{CMPOUT} is set above the middle of supply to turn off the APS in the steady state. Moreover, V_{REF_AMP} is set by 20 mV below V_{DZ-2} to ensure that voltage regulation is not affected by proposed AA part when V_{OUT} is within the dead-zone. The current consumption of the AA part is 1.3 μA only. Fig. 7 shows asynchronous comparator (M_{02}–M_{11}) and the dynamic-biasing circuit (M_{RC}, C_P and M_{01}). M_{RC} is a pseudo active load by using a PMOS transistor with its gate voltage to the ground. C_P, which is implemented by metal-insulator-metal capacitor, is 0.2 pF in the design. Fig. 8 presents the mechanism of the proposed AA-DLDO with TLS upon receiving load transient. When I_{LOAD} increases, V_{OUT} drops below V_{REF_AMP}. The super-coarse loop and AA part are activated to supply load current to the load. When V_{OUT} recovers and stay between V_{REF_AMP} and V_{DZ-2}, only the super-coarse loop is operating. The AA part is disabled when the output voltage is above V_{REF_AMP}. Therefore, the proposed AA loop does not affect the operation of digital control when V_{OUT} is recovered back to DZ2, and it does not influence the closed-loop stability in the steady state. The coarse loop will then operate when V_{OUT} stays between V_{DZ-1} and V_{DZ-2}. Finally, the fine loop operates when V_{OUT} stays between V_{DZ+1} and V_{DZ-1}. The small oscillation in the steady state is due to limit-cycle oscillation, which is a common situation of all DLDO designs.

To verify the TLS outperforming the coarse-fine switching, a simulation is conducted, and the result is shown in Fig. 9. It is noted that no AA part is included in this simulation. The waveforms of V_{OUT} and I_{LOAD} of the coarse-fine switching and TLS are colored in blue and red, respectively. The TLS is much more suitable for a larger transient step than the coarse-fine switching for the same transient error magnitude
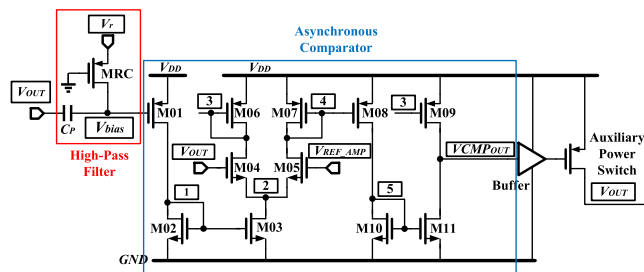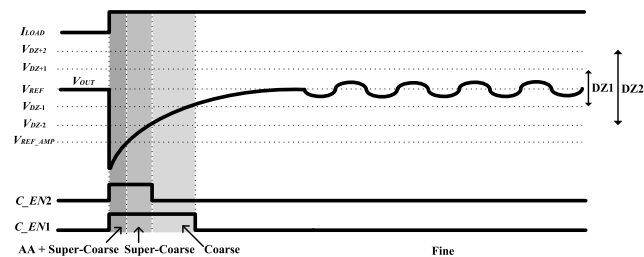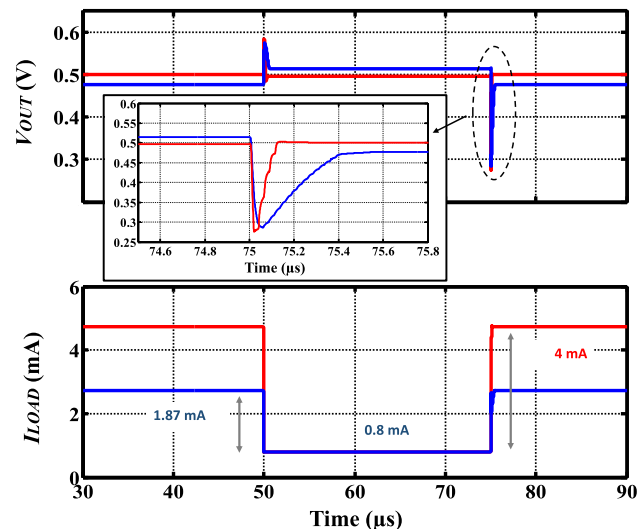

FIGURE 9. Simulated load transient responses of DLDOs with different power-switch array switching schemes (blue: coarse-fine; red: TLS).

(i.e., ΔV_{OUT}). Moreover, T_R of the TLS is much shorter than that of the coarse-fine switching.

Another simulation is to show the effectiveness of proposed AA part for the DLDO with TLS. Fig. 10 shows the two cases with I_{LOAD} = 18 μA–4.84 mA. Fig. 10(a) and Fig. 10(b) show the cases with edge time of the load transients of 1 ns and 5 ns, respectively. The cases without the proposed AA part have larger undershoot when the edge time is shorter. However, the cases with the proposed AA part can maintain the undershoot (i.e., ΔV_{OUT}) to about 220 mV due to the quick response of the proposed AA structure. Fig. 10 shows the closed-loop stability of proposed DLDO is maintained
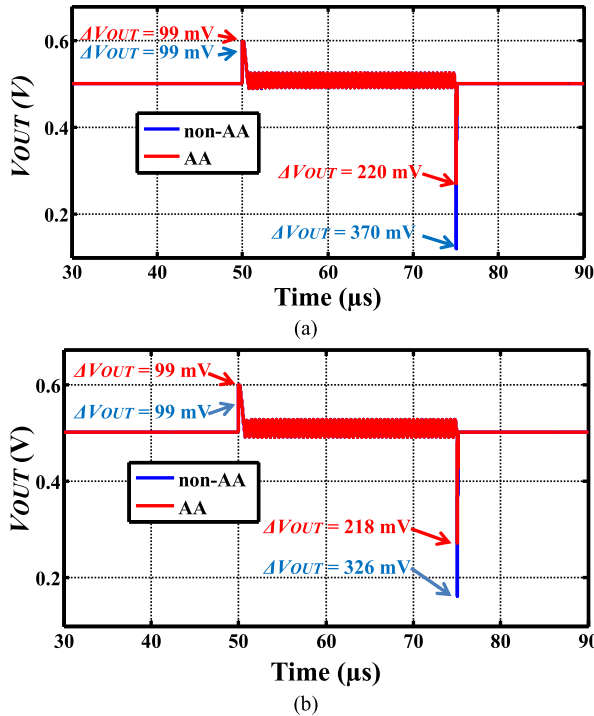
FIGURE 10. Simulated load transient responses of proposed DLDO with and without proposed AA part for I_{LOAD} = 18 μA–4.84 mA with (a) edge time = 1 ns, and (b) edge time = 5 ns.

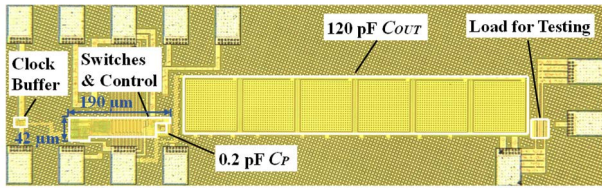**FIGURE 11.** Micrograph of proposed AA-DLDO.

TABLE 2. Performance comparison.

	[4]	[10]	[11]	[12]	This work
Year	2017	2017	2019	2020	2022
Process	65 nm	65 nm	65 nm	65 nm	65 nm
Chip area (mm²)	0.076	0.034	0.0374	0.018	0.008
V_{DD} (V)	0.5–1	0.5–1	1	0.65–1.2	0.6–0.75
V_{OUT} (V)	0.3–0.45	0.45–0.95	0.8	0.6–1.15	0.5–0.69
$f_{sw(max)}$ (MHz)	240	10	3.9	740	38
$I_{Q(min)}$ (μA)	14	3.2	100	180	13.5 (1.3 for AA)
C_{Total} (nF)	0.4	0.1	0.04	0.1	0.12
$I_{LOAD(min)}$ (mA)	0.04	2	20	10	0.018
$I_{LOAD(max)}$ (mA)	1.1	12	70	30	4.84
ΔV_{OUT} (mV)	40	105	108	101.7	200
T_R (ns)	15.1	200##	124##	10##	8
FoM1 (ns) [14]	0.741	33.4	35.61	3.39	0.052
FoM2 (ns) [15]	0.19	0.05	0.18	0.06	0.02

Remark: ## data estimated from measurement plots.

after the transient improvement achieved by the additional AA loop.

IV. EXPERIMENTAL RESULTS

The proposed AA-DLDO is implemented in UMC 65-nm CMOS process. The chip micrograph is shown in Fig. 11.
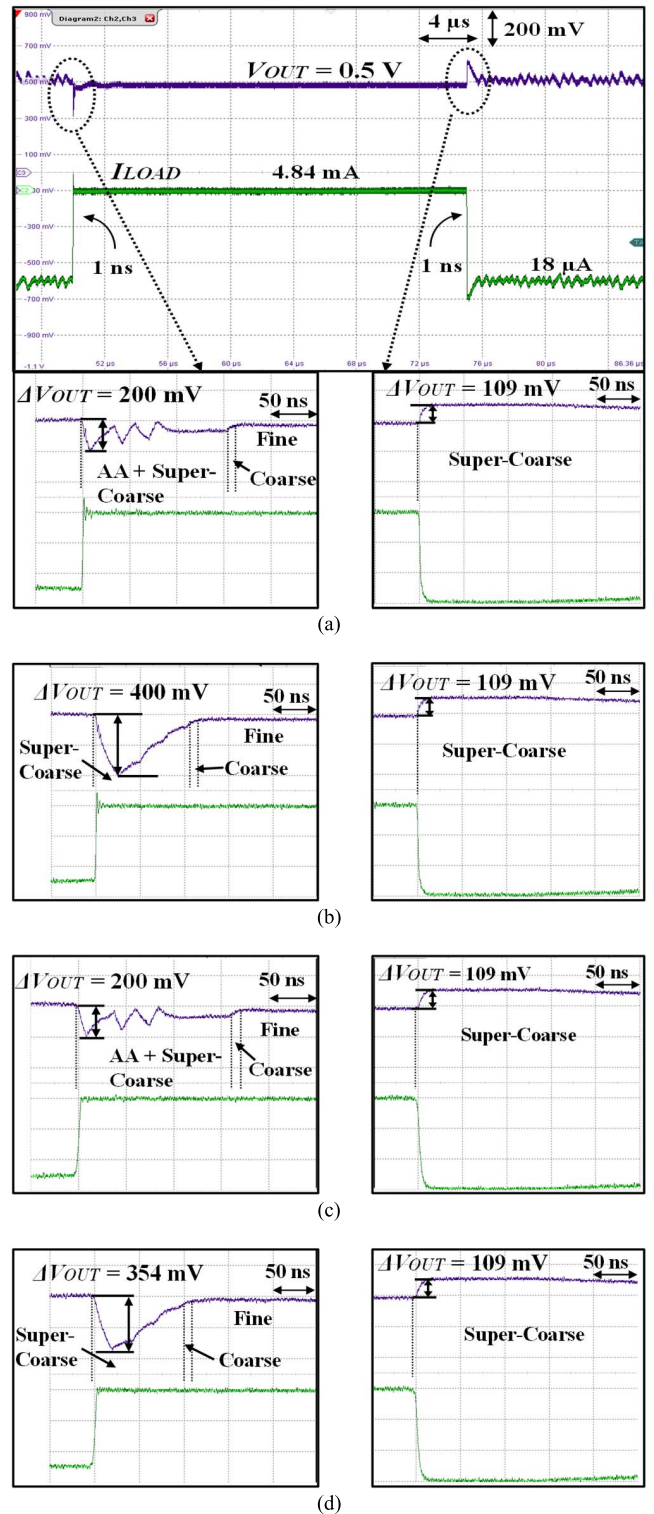

FIGURE 12. Measured transient responses of proposed DLDO for I_{LOAD} = 18 μA–4.84 mA (a) with proposed AA part and edge time = 1 ns, (b) without proposed AA part and edge time = 1 ns, (c) with proposed AA part and edge time = 5 ns, and (d) without proposed AA part and edge time = 5 ns.

The active chip area of the circuit is 0.008 mm². The measurement conditions are V_{DD} = 0.6–0.75 V, V_{OUT} = 0.5–0.69 V, I_{LOAD} = 18 μA–4.84 mA, C_{OUT} = 120 pF and
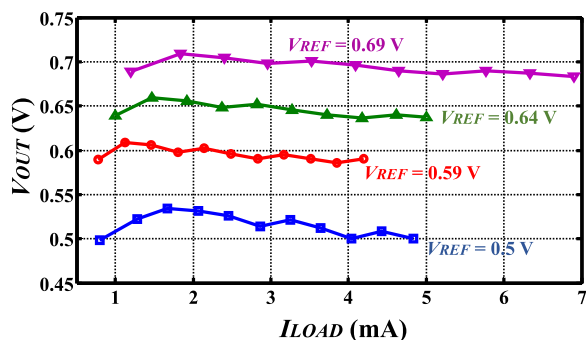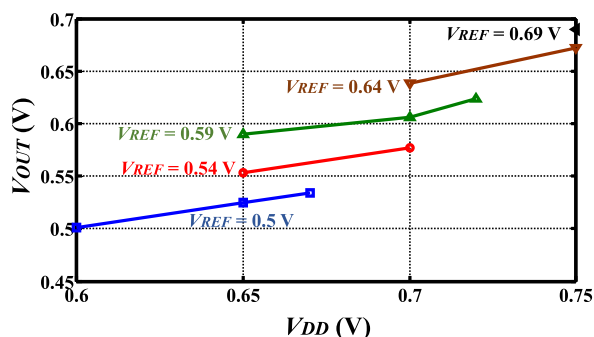
FIGURE 13. Measured load regulations.

FIGURE 14. Measured line regulations.

$f_{sw} = 38$ MHz. The measured I_Q is 13.5 μA. The proposed AA-DLDO with $I_{LOAD} = 18$ μA–4.84 mA is suitable for near/sub-threshold logic applications. Table 2 summarizes the performance of proposed AA-LDO.

The measured load transient responses of proposed AA-DLDO are shown in Fig. 12. The measurement results are close to the simulation results in Fig. 10. The experimental results verify that the proposed structure reduces the undershoot of V_{OUT} by the proposed AA part and it maintains the undershoot of about 200 mV for edge times of 1 ns and 5 ns, respectively. The measured T_R of proposed AA-LDO (i.e., TLS + AA part) is 8 ns. Thus, the used edge times of 1 ns and 5 ns in the measurements is fast enough to test the load transient responses of the proposed AA-DLDO. Finally, the transitions of voltage regulation of V_{OUT} by the AA and super-coarse loop to the coarse loop and then to the fine loop are marked in Fig. 12(a)–(d). The small oscillation of V_{OUT} in the steady state at $I_{LOAD} = 18$ μA shown in Fig. 12(a) (full view) is due to limit-cycle oscillation, which is a common situation in all DLDO designs. The measured load and line regulations are shown in Fig. 13 and Fig. 14, respectively. The worst-case measured load regulation is 9 mV/mA, and the maximum error voltage at different V_{DD} is 37 mV.

A comparison of proposed AA-LDO with other state-of-the-art DLDOs are shown in Table 2. All DLDOs are fabricated in the 65-nm CMOS technology. The minimum and maximum I_{LOAD}, as well as T_R in Table 2 are extracted from the measured load transient responses of respective design. The proposed AA-DLDO has the smallest $I_{LOAD(min)}$.

However, the others such as the design in [10], [11] and [12] have much higher $I_{LOAD(min)}$ to achieve good load transient responses. Although $I_{LOAD(min)}$ of the design in [4] is as small as 0.04 mA, its $I_{LOAD(max)}$ is 1.1 mA only. Since the measured transient conditions of the designs in Table 2 are very different, two figure-of-merits (FoM1 and FoM2) in [14] and [15] are used to compare the transient performances, where FoM1 is used to compare LDOs with small minimum load current while FoM2 is used to compare LDOs without specific load conditions. The proposed AA-DLDO has FoM1 of 0.052 ns and FoM2 of 0.02 ns, which are much better than the others by more than 14 times and 2.5 times, respectively.

V. CONCLUSION
In this paper, an AA-DLDO has been presented. The proposed analog-assisted structure to further enhance the design in [10] has been discussed. Operations of the proposed circuit methods, simulation and experimental results have been reported to verify the effectiveness of proposed method. The transient performance is better than the state-of-the-art DLDO designs by as high as 14 times, based on a FoM comparison.

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