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Experimental Investigation of Charge Sharing Induced SET Depending on Transistors in Abutted Rows in 65 nm Bulk CMOS Technology

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ABSTRACT The effect of transistors in abutted rows on charge sharing is investigated by changing the configuration of the transistors in abutted rows in this work. 3D TCAD numerical simulations indicate that the existence of transistors in abutted rows can mitigate the occurring probability of charge sharing, especially charge sharing induced by ion striking at the vicinity of n-well contact. The simulations also indicate that the single event double transient (SEDT) pulse width is reduced obviously by the transistors in abutted rows for ion strike location near n-well contact. A 65 nm test chip was designed in commercial 65 nm twin-well bulk CMOS process, and heavy-ion experiment was conducted. The experiment results agree well with the simulation results, which indicates that the effect of transistors in abutted rows on single event sensitivity and the occurring probability of charge sharing is more than 10%, and then considering the effect of transistors in abutted rows is necessary in nanometer technology.

INDEX TERMS Charge sharing, single event double transient (SEDT), single event transient (SET), single event triple transient (SETT).

I. INTRODUCTION

As technology scales down, the transistor dimensions and the space between transistors are both decreasing. However, the size of ion track and the deposited charge cloud generated by an incident ion into a silicon block remain the same. Thus, the deposited charge cloud will have an effect on multiple transistors in any circuit module or integrated circuit (IC), and multi-nodes charge collection or charge sharing [1]–[3] is becoming more and more prevalent.

In the past, charge sharing between transistors in a circuit module is researched widely, for example, the failure of DICE flip-flop [4], [5], pulse quenching effect [6]–[9]. There are also some researches about charge sharing of several (two in general) transistors not in a circuit module [10], [11]. However, there is little study about the effect of other transistors on charge sharing between transistors until now.

In this study, the work focuses on the effect of adjacent transistors in abutted rows on charge sharing and SET, because the SET pulse width has significant effect on soft-errors in advanced technologies [12]–[14]. In general, any IC is of over 50% transistor density based on advanced placement & route tools, and the interspace between function cells are filled with fillers in a concrete design. The past study with isolated inverter has not considered the effect of adjacent transistors in the abutted standard cell rows, so the effect of those adjacent transistors in the abutted standard cell rows on charge sharing is not as critical as that in digital logic circuits. In order to discover the effect of adjacent transistors in the abutted standard cell rows, 3D TCAD simulations are performed based on inverters. To verify the simulation results, a test chip with inverter chains was implemented in a commercial 65nm twin-well technology, and heavy-ion test was conducted.

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II. SIMULATION SETUP

The simulated TCAD devices are calibrated to a 65 nm commercial bulk process. The W/L ratio of PMOS transistor is 450 nm/ 60 nm, while the W/L ratio of NMOS tranistor is 300 nm/ 60 nm. As shown in Fig. 1 (a), six PMOS transistors are built into a silicon substrate with the size of 10 μm $\times$ 10 μm $\times$ 10 μm. The width of p-well and n-well contact is 160 nm, and the space between PMOS active area (AA) and

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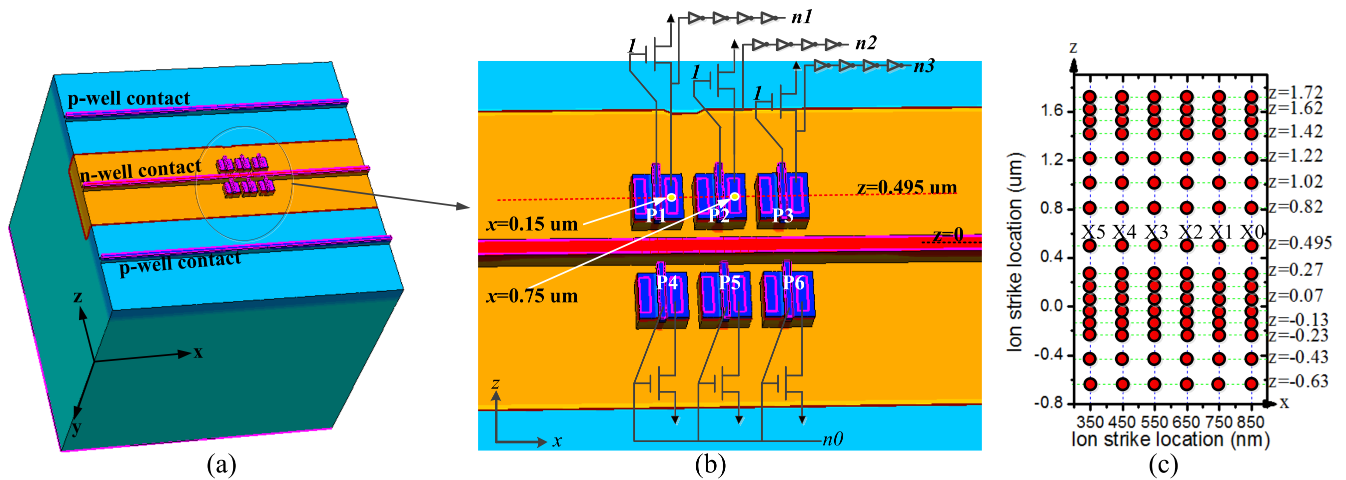

FIGURE 1. The TCAD simulation setup: (a) 6 PMOS transistors are built into TCAD devices, (b) the mixed-mode simulation circuit structure, (c) the 2D ion-strike locations.

n-well contact is 190 nm. The height of n-well is 2.88 μm, and the height of a standard inverter cell is 3.0 μm. The space between two adjacent PMOS transistors is 130 nm in x-direction.

As shown in Fig. 1 (b), P1∼P3 are three PMOS transistors to investigate charge sharing, while P4∼P6 are three adjacent transistors in the abutted standard cell rows. P1∼P3 are in off-state, their drains are connected with the drains of their corresponding pull-down NMOS transistors, their gates are connected with the gates of their corresponding pull-down NMOS transistors and then biased to logic '1'. The SETs generated at P1∼P3 are measured at corresponding 5-level inverter chains, (i.e. n1∼n3). P4∼P6 are used to study the effect of adjacent transistors in the abutted standard cell rows on charge sharing among P1∼P3. The state of P4∼P6 is controlled by n0. When n0 is logic '1', P4∼P6 are in off-state (OFF, for short); when n0 is logic '0', P4∼P6 are in on-state (ON, for short). There is another state of P4∼P6, that is, the poles of P4∼P6 are floating (Floating, for short). Therefore, there are three cases of P4∼P6 which are simulated, that is, OFF, ON and Floating.

As shown in Fig. 1(b), the drain center of P1 and P2 is at x=150 nm and x=750 nm respectively, and then the distance between P1 and P2 (or P2 and P3) is 600 nm. Thus, as shown in Fig. 1(c), 2D ion strike locations are adopted to observe the effect of P4∼P6 on charge sharing among P1∼P3. In addition, ion strike locations between x=350 nm and x=850 nm can describe charge sharing among P1∼P3 well, because ion striking at x=250 nm is almost the same with ion striking at x=850 nm.

The same with the works in [8], [11], heavy-ion strike is simulated with a Gaussian electron-hole pair column. The length and character radius of the ion track is 10 μm and 50 nm respectively. The linear energy transfer (LET) value is kept constant during the ion strike, and the LET used in simulation is 37.4 MeV·cm^2/mg. The simulations were performed with the supply voltage of 1.2 V at room temperature. The following physical models are included: (a) doping dependent Shockley-Read-Hall (SRH) recombination and Auger recombination, (b) Fermi-Dirac statistics, (c) the effect of doping, electric field, carrier-carrier-scattering and interface scattering on mobility, (d) band-gap narrowing effect, (e) carrier transport with Hydrodynamic model. Unless otherwise specified, default parameters and models provided by Sentaurus TCAD vH-2013.03-SP1 were employed.

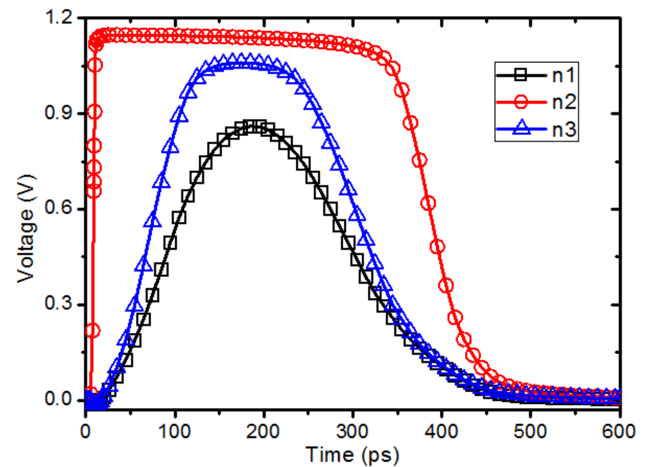

FIGURE 2. Single event multiple transient generated in n1∼n3 with ion strike at X3 (x=550 nm, z=495 nm) with the LET of 37.4 MeV·cm^2·mg^{-1}.

III. SIMULATION RESULTS AND ANALYSIS

During a heavy-ion striking scan with the LET of 37.4 MeV·cm^2/mg shown in Fig. 1(c), there is no SET, a SET or SEMT generated in each location. The generation of SEMT is caused by charge sharing among P1∼P3. If there are two SETs generated in n1∼n3, we called it a single event double transient (SEDT); if there are three SETs generated in n1∼n3 simultaneously, we called it as a single event triple transient (SETT). As shown in Fig. 2, with ion striking

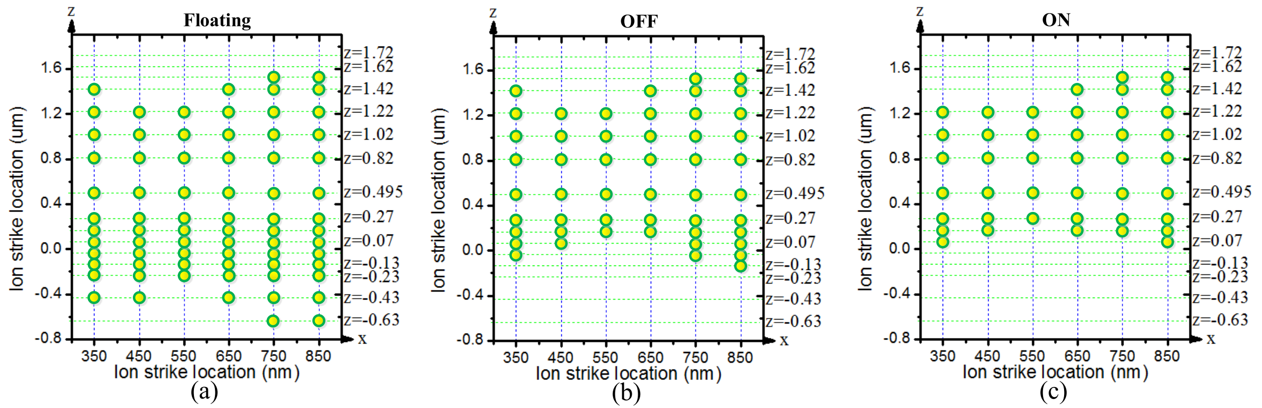

FIGURE 3. With the LET of 37.4 MeV·cm^2/mg, the single event double transient (SEDT) sensitive volume, (a) for Floating case, (b) for OFF case, (c) for ON case.

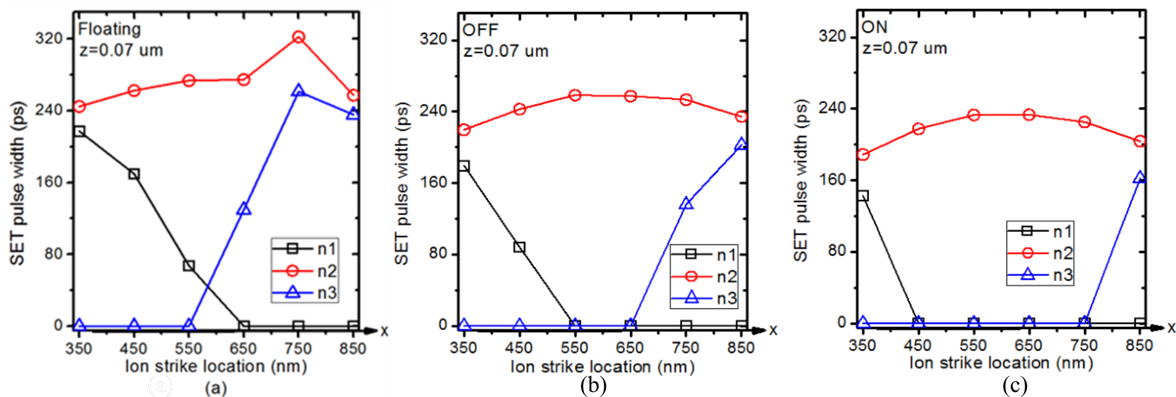

FIGURE 4. The SET pulse width in n1~n3 with ion striking at z=0.07 μm with the LET of 37.4 MeV·cm2/mg, (a) for Floating case, (b) for OFF case, (c) for ON case.

at position X3 (x=550 nm, z=495 nm), there is a SETT generated in 'ON' case.The pulse in n2 rises rapidly since X3 is very close to n2. The effective pulse width (measured from the rising point with 50% highest voltage to the falling point with 50% highest voltage) of each transient in this SETT is 222 ps, 386 ps and 150 ps respectively.

In TCAD simulations, charge sharing appears as SEMT, and the generation of SEDT indicates whether there exists charge sharing or not. Thus, SEDT sensitive volume is just charge sharing sensitive volume. As shown in Fig. 3, for three simulation cases, the SEDT sensitive volumes are different from each other. The SEDT sensitive volume of 'Floating' case is the largest, which is 1.08×10^6 nm^2, the moderate is in 'OFF' case, which is 8.05×10^5 nm^2, and the smallest is in 'ON' case, which is 7.05×10^5 nm^2.

Because the height of a standard cell is 3.0 μm, the height of two back-to-back standard cells is 6.0 μm, and the area for x=250 nm to x=850 nm is 6.0 μm $\times$ 600 nm (i.e. 3.6×10^6 nm^2). Then the occurring probability of P-hit charge sharing is 30 % (i.e. 1.08/3.6) for 'Floating' case, the occurring probability of P-hit charge sharing is 23.3 % (i.e. 0.805/3.6) for 'OFF' case, and it is 19.6 % (i.e. 0.705/3.6) for 'ON' case, as listed below.

In Fig. 3, we can also see that the difference of P-hit charge sharing sensitive volume among three cases mainly exists near and below n-well contact. In Fig. 4, the SET pulse widths in n1~n3 are compared for three cases. With ion striking at z=0.07 μm, as shown in Fig. 4, the SET pulse width in 'Floating' case is the largest, and the SET pulse width in 'ON' case is the smallest. In addition, with ion striking at position (x=550 nm, z=0.07 μm), there is SEDT generated in n1 and n2 in 'Floating' case, but there is only SET generated in n2 in 'OFF' case; with ion striking at position (x=450 nm, z=0.07 μm), there is SEDT generated in n1 and n2 in 'OFF' case, but there is only SET generated in n2 in 'ON' case. Therefore, the existence of P4~P6 is beneficial for mitigating the SEDT generation, and then charge sharing is also mitigated by the transistors P4~P6 in abutted rows.

Fig. 5 has shown the difference of SET pulse width in different cases with ion striking at x=750 nm. For ion strike locations near n-well contact, the difference among them is obvious. The SET pulse width in n2 in 'Floating' case is the largest, and the SET pulse width in 'ON' case is the smallest. Besides, according to the simulation results, the mean pulse widths of all SEDTs can be calculated. Because the scan

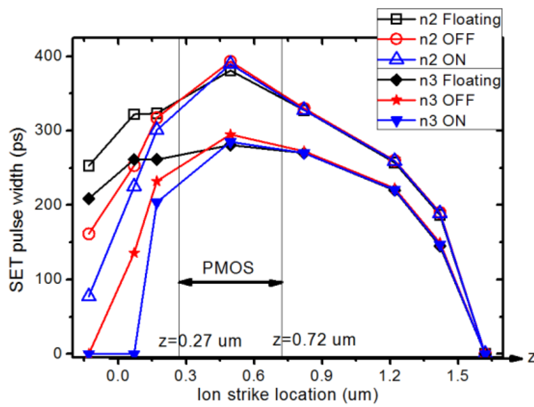

FIGURE 5. With ion striking at x=750 nm with the LET of 37 MeV·cm2/mg, the SET pulse width in n2 and n3 in three cases.

TABLE 1. The occurring probability of P-hit charge sharing for three cases.

Cases	Floating[%]	OFF[%]	ON[%]
Probability	30	23.3	19.6

TABLE 2. The mean SEDT pulse widths attained by 3D TCAD simulations.

Mean pulse width	Floating [PS]	OFF [ps]	ON [ps]
Active	282.1	304.9	306.6
Passive	202.5	218.7	218.9

grid in z-direction is not uniform, we can calculate the mean pulse width by defining a weight for each SET. For ion strike locations in 'x=a', if the z-coordinate of an ion strike location is z1, and the z-coordinate of its two neighboring ion strike locations is z0 and z2, then the weight is expressed as |z2-z0|/2. Finally, the mean SEDT pulse widths are shown in TABLE 2. The mean SEDT pulse width in 'ON' case is the largest.

In reality, ion strike locations near n-well contact is more close to transistors in abutted rows, thus the effect of transistors in abutted rows is more obvious. Fig. 6 has shown 1-D cut-line of electrostatic potential at the depth of 500 nm and 100 nm after ion strike 190 ps. The potential at 500 nm can reflect the n-well potential while the potential at 100 nm can reflect the source/drain potential of P1∼P3. The n-well potential perturbation in 'Floating' case is the largest, and the n-well potential perturbation in 'ON' case is the smallest. Therefore, the transistors in abutted rows are beneficial for mitigating well potential perturbation and then mitigating charge sharing.

IV. HEAVY-ION EXPERIMENT

A. EXPERIMENT SETUP

A test chip was fabricated in a commercial 65 nm bulk twin-well CMOS process, in which three target circuits are

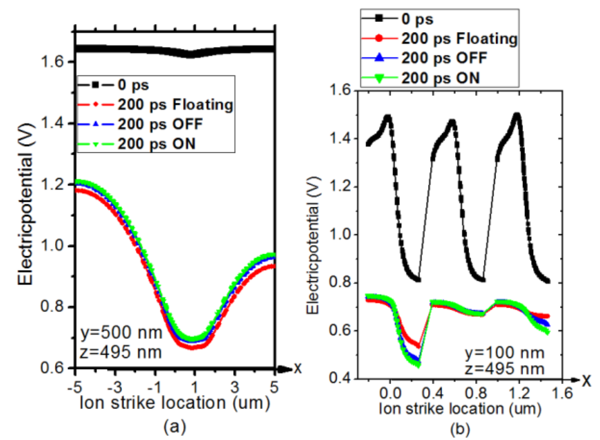

FIGURE 6. With ion striking at Position (x=750 nm, z=0.07 μm) with the LET of 37 MeV·cm2/mg, (a) 1-D cut-line of electrostatic potential in n-well at the depth of 500 nm, (b) 1-D cut-line of electrostatic potential in n-well at the depth of 100 nm. Ion strike time is at 10 ps.

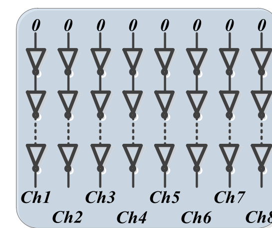

FIGURE 7. The target circuit with 8 inverter chains placed vertically.

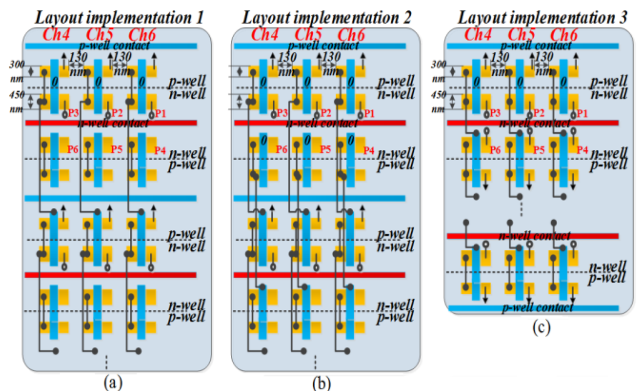

FIGURE 8. The layout implementation sketch map for the target circuit: (a) Floating case, (b) OFF case, (c) ON case.

designed. Three target circuits are equivalent logically, and each target circuit has eight 200-level inverter chains shown in Fig. 7. The input of each inverter chain is biased to logic '0', the principle of SEMT capture is similar with SET capture described in [15], and the outputs of all inverter chains are connected to an on-chip SEMT capture circuit described in [11]. The W/L ratio of PMOS transistor is 450 nm/ 60 nm, while the W/L ratio of NMOS transistor is 300 nm/ 60 nm.

For each inverter chain, the inverters are placed vertically in the layout, and three equivalent target circuits are implemented with different layouts. As shown in Fig. 8 (a),

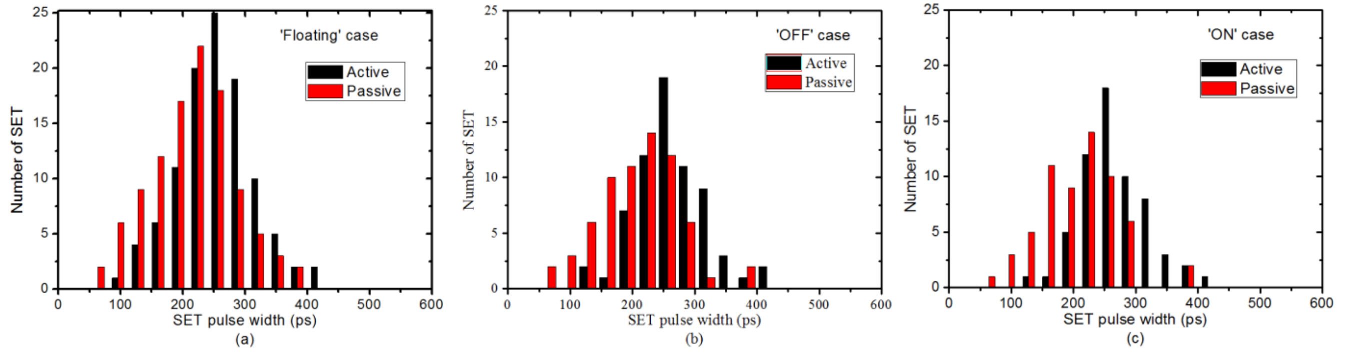

FIGURE 9. The SEDT pulse width distribution during Ge ion test with the LET of 37.4 MeV·cm^2·mg^{-1}, (a) for Floating case, (b) for OFF case, (c) for ON case.

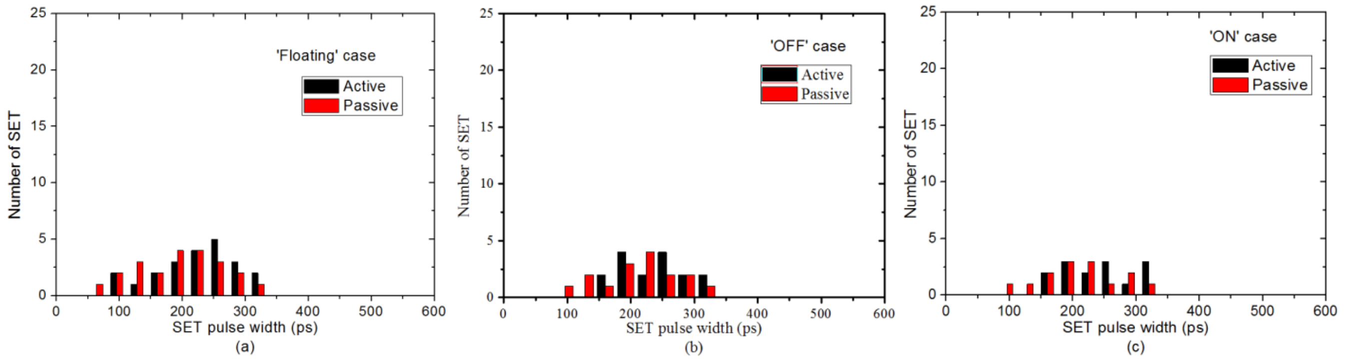

FIGURE 10. The SEDT pulse width distribution during Ti ion test with the LET of 22.2 MeV·cm^2·mg^{-1}, (a) for Floating case, (b) for OFF case, (a) for ON case.

P1∼P3 are biased to low level, while the poles of P4∼P6 are floated, it is the same with 'Floating' case in the simulations. As shown in Fig. 8 (b), P1∼P3 are biased to low level, while the poles of P4∼P6 also biased to low level, it is the same with 'OFF case in the simulations. As shown in Fig. 8 (c), P1∼P3 are biased to low level, while P4∼P6 are biased to high level, it is the same with 'ON' case in the simulations. In order to distinguish these three layout implementations, we still name them 'Floating' case, ''OFF' case and 'ON' case respectively.

Accelerated heavy ion experiments were carried out at HI-13 Tandem Accelerator in the China Institute of Atomic Energy (CIAE), Beijing. The test chip operates at room temperature with the supply voltage of 1.2 V. Normal heavy ion Ge and Ti is used, of which the LET is 37.4 MeV·cm^2·mg^{-1} and 22.2 MeV·cm^2· mg^{-1} respectively. The total fluence of Ge ion is 10^7 ions·cm^{-2}. The total number and all pulse widths of SETs were collected and recorded from each SET capture circuit in time.

B. EXPERIMENT RESULTS AND ANALYSIS

For 'Floating' case, there are 339 single events (SEs) totally during Ge ion test. There are only 3 SETT generated, but there are 102 SEDT generated, and there are 234 SET generated. The occurring probability of SEMT or charge sharing is 31.0 % (i.e. 105/339). During Ti ion test, there are 287 SEs totally, in which there are only 1 SETT and 21 SEDT generated, that is, the occurring probability of SEMT or charge sharing is about 7.7 % (i.e. 22/287)

For 'OFF' case, there are 322 single events (SEs) totally during Ge ion test, in which there are 3 SETT and 64 SEDT generated, The occurring probability of SEMT or charge sharing is about 21.7 % (i.e. 67/309). During Ti ion test, there are 289 SEs, in which there are only 1 SETT and 15 SEDT generated, that is, the occurring probability of SEMT or charge sharing is about 5.5 % (i.e. 16/289)

For 'ON' case, there are 304 single events (SEs) totally during Ge ion test, in which there are 3 SETT and 58 SEDT generated, The occurring probability of SEMT or charge sharing is about 20.1 % (i.e. 61/304). During Ti ion test, there are 280 SEs, in which there are only 1 SETT and 13 SEDT generated, that is, the occurring probability of SEMT or charge sharing is about 5.0 % (i.e. 14/280)

As shown in TABLE 3, the occurring probability of charge sharing from Ge ion test agrees well with that from 3D TCAD simulations, which indicates that P-hit charge sharing is

TABLE 3. The occurring probability of charge sharing calculated by simulations and heavy-ion experiments.

The occurring probability	Floating [%]	OFF [%]	ON [%]
Ge ion test	31.0	21.7	20.1
Ti ion test	7.7	5.5	5.0
3D TCAD simulations	30.8	22.5	20.0

dominant in 65nm twin-well process. Due to parasitic bipolar effect (PBE), P-hit SET is much larger than N-hit SET, and P-hit charge sharing is much stronger than N-hit charge sharing [11], [16], [17]. The data in TABLE 3 also indicates that the effect of transistors in abutted rows is obvious on charge sharing. The experiment test results has verified the simulation analysis, the state of transistors in abutted rows has significant effect on the single event sensitivity and charge sharing sensitivity, especially the layout locations near n-well contact stripe. Changing the state of those transistors in abutted rows from 'ON' to 'Floating', the SET sensitivity is increased about 11.5 % (i.e. (339-304)/304), and the charge sharing sensitivity is increased about 11 % (i.e. 31.0% - 20.1%).

The SEDT pulse width distributions from heavy-ion test are shown in Fig. 9 and Fig. 10. Whether for Ge ion or Ti ion test, the state of those transistors in abutted rows has little effect on the largest SEMT pulse width. As shown in Fig. 9 (a)-(c), for three cases, the largest SET pulse width for Active devices is about 424 ps, while the largest SET pulse width for Passive devices is about 380 ps. As indicated from the simulation results above, the strongest charge sharing occurs along the PMOS drain centers, which is 495 nm from the well contact center, so that the effect of those transistors in abutted rows can be ignored as ion strikes at these locations.

The state of those transistors in abutted rows has important effect on the mean width of generated SEMT. During Ge ion test, the mean SET pulse in Active devices and Passive devices is 253.3 ps and 215.2 ps respectively for 'Floating' case, the mean SET pulse in Active devices and Passive devices is 263.2 ps and 207.8 ps respectively for 'OFF' case, and the mean SET pulse in Active devices and Passive devices is 266.0 ps and 207.7 ps respectively for 'ON' case. These results are comparable with the simulation results from TABLE 2. During Ti ion test, the mean SET pulse in Active devices and Passive devices is 225.5 ps and 195.0 ps respectively for 'Floating' case, the mean SET pulse in Active devices and Passive devices is 236.0 ps and 212.0 ps respectively for 'OFF' case, and the mean SET pulse in Active devices and Passive devices is 240.0 ps and 210.3 ps respectively for 'ON' case.

Totally, the heavy-ion test has verified the simulation results well. The effect of the transistors in abutted rows on single event sensitivity and the occurring probability of charge sharing are over 10 % during Ge ion test. In actual integrated circuits, 'ON' case and 'OFF' case are ubiquitous, and the transistors in abutted rows in 'Floating' case is equivalent with the fillers in an actual design, which is also widespread. Therefore, there is need to consider the effect of transistors in abutted rows in future 3D TCAD simulations in nanometer technology, which agrees with the view in [18], [1].

V. CONCLUSION

Heavy ion experiments results agree with the simulation results well, which indicates that the effect of transistors in abutted rows on charge sharing and SET is of great concern. 3D TCAD simulations indicate that the on-state or off-state transistors in abutted rows are helpful for stabilizing the n-well potential and then mitigating charge sharing, the single event sensitivity at the vicinity of n-well contact stripe is decreased obviously. Furthermore, the simulation and the experiment indicate that considering the effect of transistors in abutted rows is necessary to maintain reasonable simulation accuracy in nanometer technology.

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