IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received April 26, 2022, accepted May 12, 2022, date of publication May 18, 2022, date of current version May 26, 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3176359

A 14.5-Bit ENOB, 10MS/s SAR-ADC With 2nd Order Hybrid Passive-Active Resonator Noise Shaping

XIMING FU AND KAMAL EL-SANKARY, (Senior Member, IEEE)
Department of Electrical and Computer Engineering, Dalhousie University, Halifax, NS B3H 4R2, Canada
Corresponding author: Ximing Fu (xm954365@dal.ca)

This work was supported in part by the Natural Science and Engineering Research Council of Canada (NSERC).

ABSTRACT A new 2nd order noise shaping (NS) based successive approximation register (SAR) ADC is presented in this paper. In comparison to earlier research, this paper considers hybrid passive-active integrators to compensate for the phase error of the passive integrator. To realize the resonator noise shaping in a high-speed asynchronous SAR-ADC, the hybrid passive-active sigma-delta modulator (SDM) is introduced as a multi-input, feed-forward loop filter. This overcomes the conventional asynchronous SAR-ADC noise barrier generated from the CDAC, quantizer, and dynamic comparator. The proposed noise shaping technique significantly reduces the ADC power consumption and area compared with the active SDM noise shaping approach. This circumvents the shortcomings of passive SDM, such as a large area, low resolution, and low speed. It consists of very low power, forward gain *G* and positive feedback path across a 1st order passive switch capacitor (SC) integrator that desensitizes capacitor ratios under PVT variations. Extensive circuit simulation verifications and system-level results have been used to validate the effectiveness of the proposed NS SAR-ADC. The simulation results show that the proposed SAR ADC consumes 0.88mW at 10MS/s, with an SNDR of 89.43 dB and SFDR 98.64 dB within 0.1 fs oversampling frequency.

INDEX TERMS Discrete-time (DT), low-gain-amplifier-based switched-capacitor (SC) integrator, noise shaping, passive SC integrator, sigma-delta modulator.

I. INTRODUCTION

In modern communication systems, several high-precision analog-to-digital converters (ADCs) need to be used. To meet the requirements of high precision and wide bandwidth, a series of new ADC structures have successively appeared. Noise shaping successive approximation ADC (NS SAR-ADC) is one of the most popular structures studied in recent five years. While the conventional SAR-ADC has low power consumption and a small area [5]–[7], the comparator's noise and offset, quantization noise, and complimentary DAC (CDAC) thermal noise limit its accuracy. On the other hand, the sigma-delta ADC is the most used structure to achieve high precision, but due to the need for many opamps in this structure, its power consumption is high, and the area is large. The NS-SAR ADC structure is a hybrid SAR-ADC and sigma-delta modulator (SDM) that inherits both advantages. It has the characteristics of a SAR ADC in terms of low power consumption and considerable potential to achieve high precision, like sigma-delta ADC. Moreover, NS SAR-ADC requires a lower oversampling ratio (OSR) than the traditional sigma-delta modulator, thus increasing bandwidth.

References [7]–[9] described methods for reducing the input-referred noise and offset of SAR ADC using a time-domain comparator to reduce the total power at the cost of a slow conversion, which makes it less desirable for high-speed applications. The SDM is the most critical candidate architecture considering oversampling and noise shaping techniques from a high-resolution perspective. An active integrator based on opamps is the critical component, typically power-hungry and challenging to scale. SAR ADC with an SDM significantly improves the capability of a NS SAR-ADC to overcome the deficiencies mentioned above, making it a preferred approach for delivery of both high resolutions and low power consumption simultaneously [1], [2]. The authors in [1] proposed a noise-shaping technique using FIR and IIR filters. For sampling the residue voltage, a two-tap charge-domain FIR

The associate editor coordinating the review of this manuscript and approving it for publication was Artur Antonyan.

filter is utilized. An IIR noise shaping filter constructed from operational amplifiers serves as an integrator to enhance noise shaping. Nevertheless, an active integrator is introduced, which inevitably deteriorates the energy efficiency and scalability of the circuits. In [3], the authors have proposed a first-order noise shaping without the requirement of opamps using passive integrators, the design has high efficiency without interrupting the normal SAR-ADC operation. In this case, the zero in [3] is set at 0.5, indicating poor noise shaping and resulting signal attenuation of 6 dB. Furthermore, in recent research publications [4]–[6], second-order passive noise shaping techniques are proposed to increase the DC attenuation in the noise transfer function (NTF). The values of α and k (which refer to the capacitor ratios and comparator gain respectively), are increased significantly, as explained in Section II-A, which inevitably increases the power and area of the chip. Therefore, the loop dynamics in terms of ADC speed and stability will be significantly impacted, as the CDAC settling time is one of the most apparent bottlenecks for high-speed SAR-ADC.

This paper proposes a second-order low-power hybrid passive-active NS-SAR ADC architecture to overcome the previous problems. In contrast to prior works, passive-active integrators based on low gain open-loop opamps are used in the loop filter instead of conventional opamp-based active integrators. Zeros in the system are determined solely by capacitor ratio and positive feedback compensation, insensitive to process, voltage, or temperature (PVT) variations. Moreover, a resonator is introduced in the loop to achieve wide noise-shaped bandwidth.

Aside from noise shaping techniques, the choice of capacitive CDACs is also of critical importance. It has been demonstrated that DAC switching schemes such as monotonic switching (MS) provide very good energy efficiency. Compared to conventional structures, this topology reduces switching-related energy losses by 81% [10]. The MS structure degrades ADC performance due to variations in the common-mode level offset within the comparator. To stabilize the dynamic amplifier's input common-mode (CM) level, a common-mode-stabilization (CMS) circuit is proposed within the NS SAR ADC architecture.

This paper is organized as follows; Section II focuses on the fundamental theory of noise-shaping SAR-ADC and design considerations. Section III details the proposed NS SAR-ADC architecture, including proposed noise shaping architecture and detailed circuit implementations. Section IV describes the extensive simulation results at the circuit and system levels, while Section V summarizes the paper's conclusions.

II. FUNDAMENTAL THEORY ANALYSIS OF NOISE SHAPING AND DESIGN CONSIDERATIONS

A. II-A PASSIVE INTEGRATOR VS. ACTIVE INTEGRATOR

Fig.1 illustrates the active and passive integrators. The transfer functions for the 1st order active and passive integrators

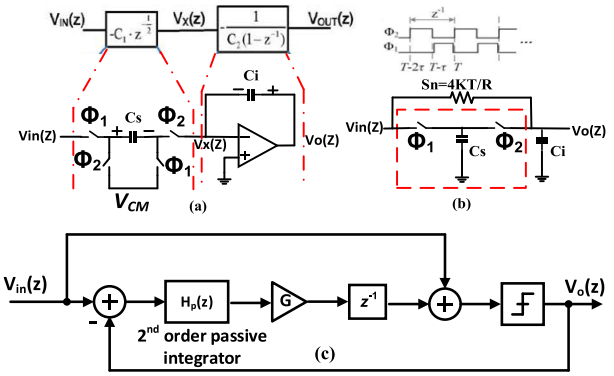

FIGURE 1. (a) 1st Order active integrator (b) 1st order passive integrator, (c) 2nd order passive noise-shaping SAR ADC [5-6, 9].

are written as:

$$H_{active}(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_S}{C_i}\frac{z^{-1}}{1-z^{-1}} \quad (1)$$

$$H_{passive}(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{\alpha z^{-1}}{1-(1-\alpha)z^{-1}}, \text{where } \alpha = \frac{C_S}{C_S + C_i} \quad (2)$$

where C_S is sampling capacitor and C_i is integrating capacitor. As opposed to the ideal active integrator transfer function (1), the passive integrator's transfer function (2) exhibits both gain and phase error. Due to the built-in analog tradeoffs, the passive transfer function cannot be modified to resemble an ideal active transfer function. First, to reduce gain error, $C_S$must be greater than C_i, which results in an increase in phase error. However, C_i should be greater than C_S to reduce phase error, which leads to increased gain error. Thus, there is a trade-off between sizing C_i and C_S. The feedforward gain of the comparator can usually compensate for the gain error in an NS SAR-ADC, though noise shaping is not properly performed if excessive phase error occurs. Since the phase error is crucial, it shifts the pole of the integrator and, therefore, the zero of the NTF of the loop filter as well, according to (3). This pole shift flattens the low-frequency part of the noise transfer function, which in turn significantly reduces the effect of noise shaping within the passband.

$$NTF(z) = \frac{1}{1+H(z)} = \frac{1-(1-\alpha)z^{-1}}{1-(1-2\alpha)z^{-1}}, z = 1, NTF(z) = 0.5 \quad (3)$$

Similarly, as shown in Fig.1(c), the works published in [5]–[6],[9], use 2nd order passive noise shaping and have severe limitations i.e., DC suppression and stability. To satisfy the noise shaping capability and stability requirements, the 2nd order passive noise shaping requires excessive capacitor ratios, α_{1-2} and comparator gain, G for noise-shaping. These parameters dramatically reduce the ADC's speed, with a large area penalty. This inevitably introduces considerable kickback noise and dynamic power requirements for the comparator, as discussed below.

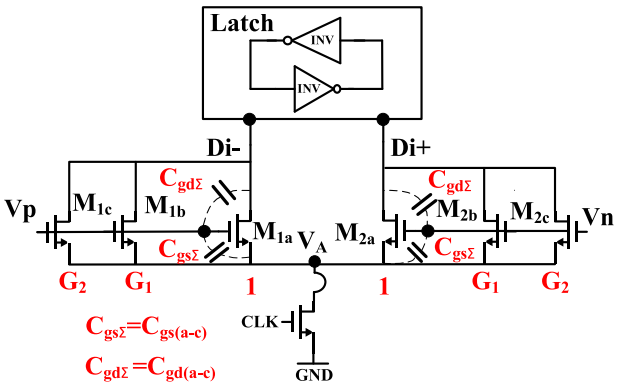

FIGURE 2. The general model of the impact of kickback noise on multi-input dynamic latch comparator.

Assume the CDAC has a capacitor value equal to C, and the 2nd order passive integrators have capacitor values α_1C, and α_2C. the NTF(z) can be rewritten as (4a)–(4c), shown at the bottom of the page. Stability analysis from the Jury array gives:

$$G < 2(\alpha_1 + \alpha_2) + 4\alpha_1\alpha_2 + 1 \tag{4d}$$

To reduce the phase error, α_1 and α_2 must assume large values. Also, to reduce gain error and ensure stability, the comparator gain G must be large. In the passive NS SAR multi-input latch comparator, as depicted in Fig.2, the gain G is provided by the input transistors. Increasing the gain, G at the expense of increasing the size of the input transistors has severe limitations. Resolution of passive NS SAR ADC's is limited due to non-idealities associated with the multi-input dynamic latched comparator. These non-idealities in multi-input dynamic latched comparator include offset voltage, thermal noise, and kickback noise. The kickback noise can be problematic when it comes to a high-speed SAR ADC, causing the settling time and accuracy of the decision to be significantly affected. While upsizing the input MOS pair $M_{1,2(a-c)}$ of the comparator can increase the gain, G and reduce thermal noise, it will adversely increase the kickback noise due to higher drain-gate parasitic capacitances of the input MOS pair.

The Kickback noise is dynamic in nature, as the input MOS pair in the whole comparison process can operate in a variety of regions (such as cut-off, saturation, or triode), which will have a significant impact on the accuracy of the decision [22]. The full expression of kickback noise of multi-input latched comparator can be written as:

$$Q_{cut-off} = V_{cm}C_{gb} + V_{GS}C_{gs} + (V_{cm} - V_{DD})C_{gd} \tag{5a}$$

$$Q_{G,sat}(t) = \frac{2}{3}(1+G_1+G_2)WLC_{ox}+(V_{cm} - V_A(t) - V_{th}) + (V_{cm}-V_A(t))C_{gs} + (V_{cm}-D_{i+}(t))C_{gd} \tag{5b}$$

$$Q_{G,triode}(t) = (1+G_1 + G_2)WLC_{ox}(V_{cm} - V_A(t) - V_{th}) + (V_{cm} - V_A(t))C_{gsS} + (V_{cm}-D_{i+}(t))C_{gd} \tag{5c}$$

where V_{cm} is the common-mode level of V_p and V_n. Cgb is the equivalent capacitance between the gate and substrate, Cgs and Cgd are the gate-source and gate-drain overlap capacitances, respectively. WLCox refers to the gate oxide capacitance that includes the input pair (M_{1a}-M_{2a}) used for the normal SAR conversion and input pairs (M_{1b}-M_{2b}, M_{1c}-M_{2c}) used for noise-shaping. In the passive noise-shaping techniques described in the literature, the feedforward gains $G_{1,2}$ implemented at the inputs of the comparator need to be substantially large to guarantee stability according to (4d), while high α_1 and α_2 must be large to reduce the passive integrator's phase error. Since increasing gain results in increased kickback noise charges induced at the gate of the input MOS pair M_{1-2}, ADC resolution suffers during both comparison and latch operations.

The previous analysis concludes that the multi-input comparator gains $G_{1,2}$ must be large enough to improve the NTF(z) at its DC suppression, satisfying the stability requirement while maintaining small enough gate capacitance to reduce dynamic power and kickback noise, leading to a design trade-off. We can find in the available 2nd order passive NS SAR ADC in the literature, the area of the integrator capacitor is around four times larger than the CDAC capacitor ($\alpha_{1,2} \cong 4$) and that limits the speed and increases power consumption. Also, the resolution of the ADC is limited by the kickback noise of the multi-input comparator due to high gains $G_{1,2}$ values.

B. II-B DIRECT 2nd ORDER SDM IMPLEMENTATION-BASED NOISE SHAPING ANALYSIS AND ITS LIMITATIONS

To improve the noise shaping performance compared to passive implementation, direct noise shaping is derived from an ideal 2nd order SDM. The ideal noise transfer function,

$$H_{2nd\ passive}(z) = z^{-1}G\frac{1}{1+\alpha_1(1-z^{-1})}\frac{1}{1+\alpha_2(1-z^{-1})} = \frac{z^{-1}G}{p_1(z)p_2(z)} \tag{4a}$$

$$NTF(z) = \frac{1}{1+H_{2nd\ passive}(z)} = \frac{p_1(z)p_2(z)}{p_1(z)p_2(z)+z^{-1}G} \tag{4b}$$

$$= \frac{[z(1+\alpha_2)-\alpha_2][z(1+\alpha_1)-\alpha_1]}{z^2(1+\alpha_1\alpha_2+\alpha_1+\alpha_2)+(-\alpha_1-\alpha_2-2\alpha_1\alpha_2+G)z+\alpha_1\alpha_2} z=1, NTF(z) = \frac{1}{1+G} \tag{4c}$$

$NTF_{ideal}(z)$, is implemented as shown in Fig.3(a)-(b). Since the ideal noise transfer function has no stability issues, it is used directly. Its corresponding loop filter transfer function is:

$$NTF_{ideal}(z) = (1 - z^{-1})^2 \tag{6}$$

$$H_{ideal}(z) = \frac{2z^{-1} - z^{-2}}{(1 - z^{-1})^2} \tag{7}$$

When the normal SAR-ADC conversion is done, the input signal V_{in} is converted directly into digital outputs through the comparator. Therefore, the STF is always equal to 1 in the NS SAR-ADC. Note that the normal SAR-ADC residue after conversion is a low-frequency DC signal, which dictates the SDM architecture's choice. Two main strategies can be applied in the NS SAR-ADC design. The first strategy, refers to a direct implementation method, is to use a lower-resolution SAR-ADC (<8bit) with a noise-shaping module with a strong shaping capability. This strategy is implemented with an active opamp-based integrator, including multiple high-performance opamps, which consume high quiescent power. The second strategy is to use a medium-resolution SAR-ADC (∼10-bit) with an intermediate noise-shaping module with medium-shaping capability, composed of a very low-power active or passive integrator and consumes less power. Fig.3(a)-(b) shows system-level and circuit-level implementations of the direct implementation strategy. When clock $\varphi 1$ is high, the first stage includes the feedforward path sample the normal SAR-ADC conversion residue. The second integrator stage samples the previous value from the first stage integrator output. When the clock $\varphi 2$ is high, the first stage integrator starts its integration, and at the same time, the second stage integrator and the feedforward path transfer the sampled value in the first half cycle through the output. Unlike opamp-based sigma-delta modulator design trade-offs, the proposed SAR-ADC constrains the SDM input signal to be a DC value, and the amplitude is around 1 LSB of the standard 10-bit SAR ADC without NS, which significantly relieves the slew rate requirement of the opamp. The integration phase must have a fast settling response during noise shaping before the comparator works in the following conversion cycle. Consequently, the approximated unity-gain bandwidth of the opamp must be very high, leading to high power consumption. In addition, an opamp with a finite DC gain will introduce higher-order harmonics at the ADC output. As a result, the opamp must have a fast-settling time and large DC gain, but with a relaxed slew rate requirement.

C. II-C PROPOSED 2nd ORDER PASSIVE-ACTIVE INTEGRATOR-BASED NOISE SHAPING ANALYSIS

Fig. 4 illustrates a technique that utilizes positive feedback across a passive 1st order SC integrator, which is inspired by [17] and [18] and can compensate for the phase error. Moreover, it is possible to compensate for the second stage integrator phase error with an input gain *G*. A detailed illustration of the block diagram of the proposed SAR-ADC is

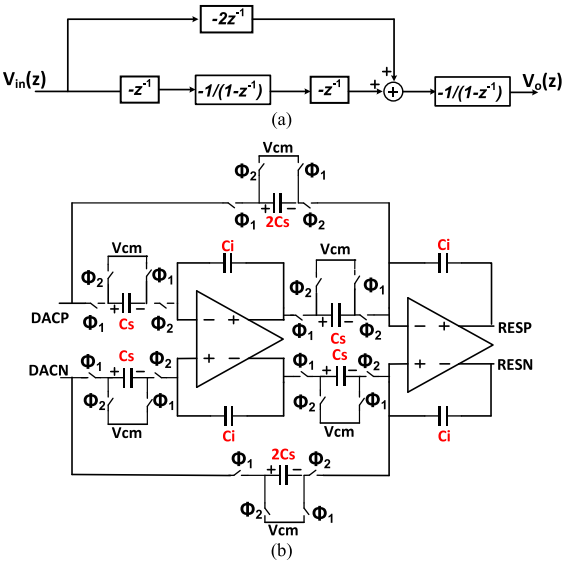

FIGURE 3. Direct 2nd order noise shaping (a) implementation block diagram. (b): circuits implementation.

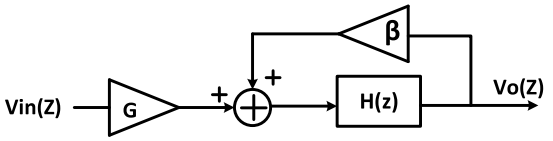

FIGURE 4. Proposed integrator phase error compensation technique model.

shown in Fig. 5. Fig.6 shows the proposed NS SAR-ADC system-level simulation. To simplify the design strategy, first, we ignore the resonator feedback g and let $\alpha_{1,2} = \frac{c_{s1,2}}{c_{s1,2}+c_{i1,2}}$, and $c_{i1} = c_{DAC}$. The modulator transfer function analysis yields:

$$H_{passive}(z) = \frac{\alpha_1 z^{-1}}{1 - (1-\alpha_1)z^{-1}} = \frac{\alpha_1 z^{-1}}{p_1(z)} \tag{8a}$$

$$H_{active}(z) = \frac{G\alpha_2 z^{-1}}{1 - z^{-1} + \alpha_2(1-\beta)z^{-1}} = \frac{G\alpha_2 z^{-1}}{p_2(z)} \tag{8b}$$

$$H_{hybrid}(z) = H_{passive}(z)H_{active}(z) + H_{passive}(z) \tag{8c}$$

The proposed NTF (z) has the following transfer function:

$$\begin{aligned} NTF\,(z) &= \frac{1}{1 + H_{hybrid}\,(z)} \\ &= \frac{p_1\,(z)\,p_2\,(z)}{p_1\,(z)\,p_2\,(z) + p_2\,(z)\,\alpha_1 z^{-1} + G\alpha_1\alpha_2 z^{-2}} \\ &= \frac{p_1\,(z)\,p_2\,(z)}{Den\,(z)} \end{aligned} \tag{8d}$$

where

$$p_1 = 1-(1-\alpha_1)z^{-1},\ p_2 = 1-z^{-1}+\alpha_2(1-\beta)z^{-1}$$

$$NTF(z=1) = \frac{1-\beta}{2(1-\beta)+G} \tag{9a}$$

$$\begin{aligned} Den\,(z) = {} & z^2 + (2\alpha_1 - 2 + \alpha_2 - \alpha_2\beta)\,z \\ & + (G\alpha_1\alpha_2 + 1 - 2\alpha_1 \\ & + 2\alpha_1\alpha_2(1-\beta) - \alpha_2(1-\beta)) \end{aligned} \tag{9b}$$

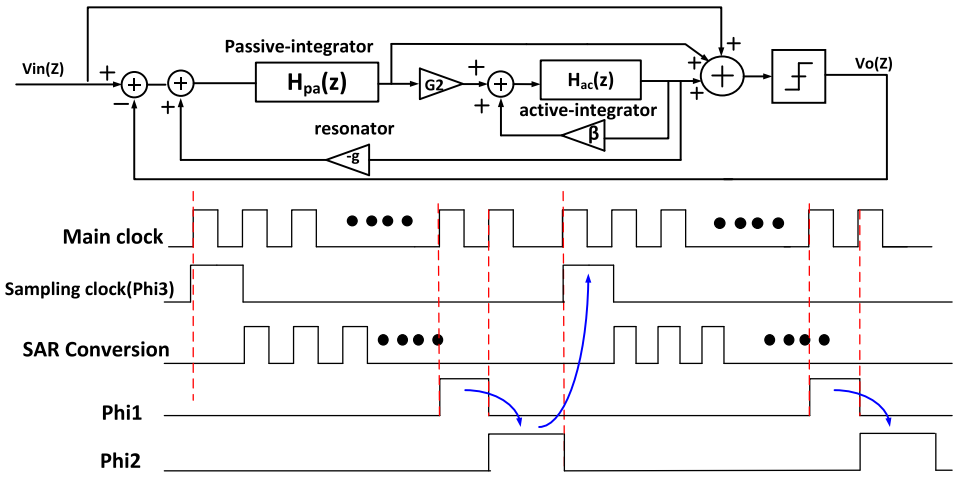

FIGURE 5. Proposed hybrid passive-active noise-shaping SAR ADC system-level implementation and timing diagram.

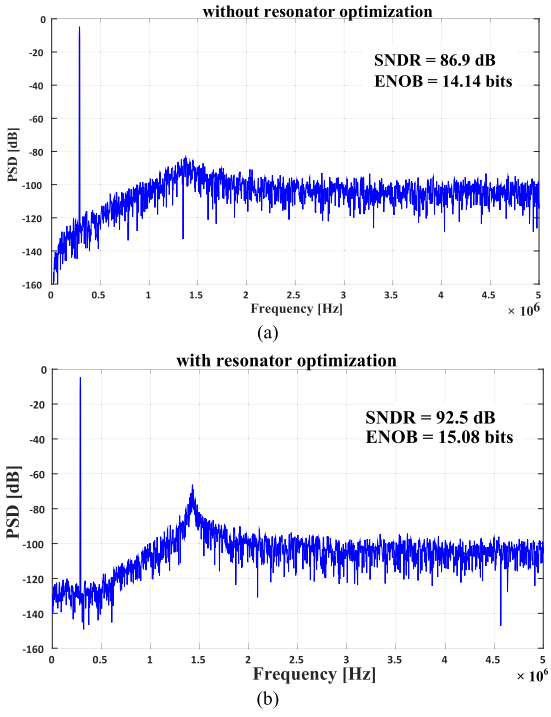

FIGURE 6. Proposed passive-active noise-shaping SAR ADC system-level simulation (a) without resonator optimization (b) with resonator optimization.

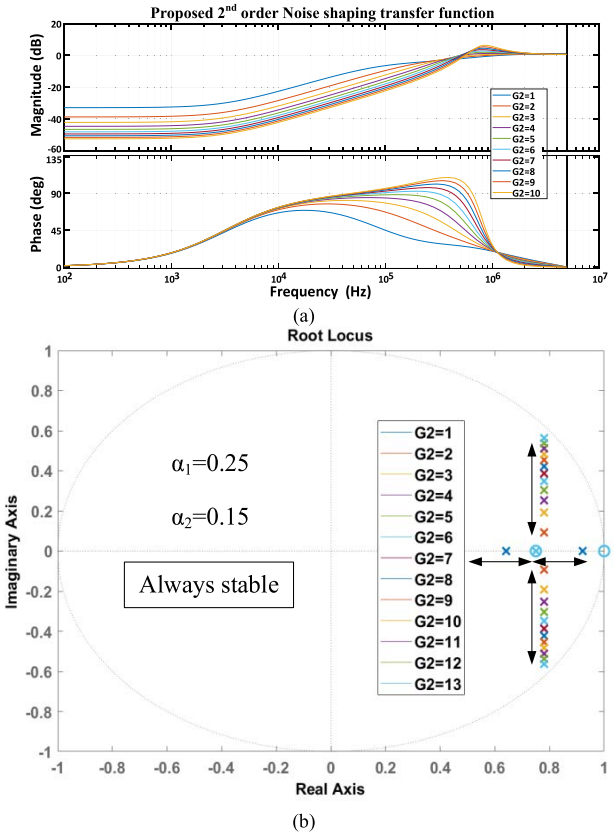

FIGURE 7. Proposed 2nd order Noise shaping transfer function (a) and pole-zero plot under OTA gain variations (b).

Assume an ideal positive feedback compensation when $\beta = 1$:

$$Den(z) = z^2 + (-2 + 2\alpha_1)z + G\alpha_1\alpha_2 + 1 - 2\alpha_1$$

Apply Jury Array for stability gives:

$$\begin{cases} Den(1) = \alpha_1\alpha_2 G > 0, \\ Den(-1) = \alpha_1\alpha_2 G - 4\alpha_1 + 4 > 0, \\ \frac{-2}{\alpha_1} + 2 < G\alpha_2 < 2 \end{cases} \tag{9c}$$

The proposed NTF(z) has two zeros which refer to as $z_1 = 1 - \alpha_1$, and $z_2 = 1 - \alpha_2(1 - \beta)$. The closer the zero of the NTF(z) is to 1, the stronger the NS capability is, which means the integrator is closer to ideal. Compared with the entirely passive noise shaping techniques, the essential advantage of the proposed solution is that increasing G to improve the noise shaping capability will not inflict extra power and kickback noise to the comparator. The open loop gain G and compensation factor β simultaneously work toward achieving better shaping ability, significantly reducing the noise

and improving the resolution of the ADC. A better shaping requires a smaller α_1 value that is limited by the kT/C noise. The zero location of z_2 is determined by β, while β is set at approximately one to minimize the phase error of the second-stage passive integrator. Moreover, the kT/C noise of the second-stage passive SC integrator is referred to as the input (and will be divided by the opamp gain, so the size of the second-stage integrator capacitors has a negligible effect on the thermal noise. The thermal noise is limited by the first stage of the passive integrator sampling capacitor C_{s1}. Since α_1, α_2 are designed to be around 0.15∼0.25 in the proposed ADC.

The minimum Cs_1 is given by:

$$C_{s1} = \frac{kT2^{2N}}{OSR(V_{FS})^2} \tag{10a}$$

where k represents the Boltzmann constant, T is the absolute temperature, N is the effective number of ADC bits and V_{FS} represents the full-scale input. The second stage output noise is simply equal to the equivalent RC integrator shown in Fig. 1 (b). Thus, the SC resistor R acts the same as a resistor in terms of thermal noise power which will not influence the noise in the output spectrum. The second stage input-referred noise can be written as:

$$V_{in,2nd}^2 = \frac{1}{G}\int_0^\infty \frac{4kTR}{1+(2\pi RCf)^2}df = \frac{kT}{GC_{i2}} \tag{10b}$$

Fig.8 shows the proposed loop filter designed with passive-active architecture and resonator feedback to improve the ADC noise-shaping performance and the bandwidth further. In our proposed noise-shaping module, conjugate zeros are introduced in NTF(z) by adding a local negative feedback loop at the input and output of the two cascaded passive-active integrators. The local feedback shifts the loop filter poles away from DC to enhance the noise shaping performance. To evaluate the performance of the proposed noise shaping module with a resonator, the complete transfer function of the proposed sigma-delta modulator is written as the following, and the simulation of the resonator effect is shown in Fig.8 (b)-(c).

$$H_{hybrid-resonator}(z) = \frac{H_{passive}(z)H_{active}(z) + H_{passive}(z)}{1 + gH_{passive}(z)H_{active}(z)} \tag{11}$$

References [17] and [18] uses a low-gain opamp with a positive feedback circuit in a discrete-time sigma-delta modulator to solve the gain and phase errors caused by the passive SC integrator. However, its input signal amplitude is limited to a small range. The ratio of rail-to-rail voltage swing to maximum input swing is 55%. In a noise-shaping SAR-ADC, the input signal is first converted fully by the conventional high-speed SAR-ADC, then it is integrated through the noise-shaping block, where the signal entering the noise-shaping block is small in amplitude. Therefore, this active-passive hybrid noise shaping technique is much more suitable for a noise-shaping SAR ADC as compared to a sigma-delta

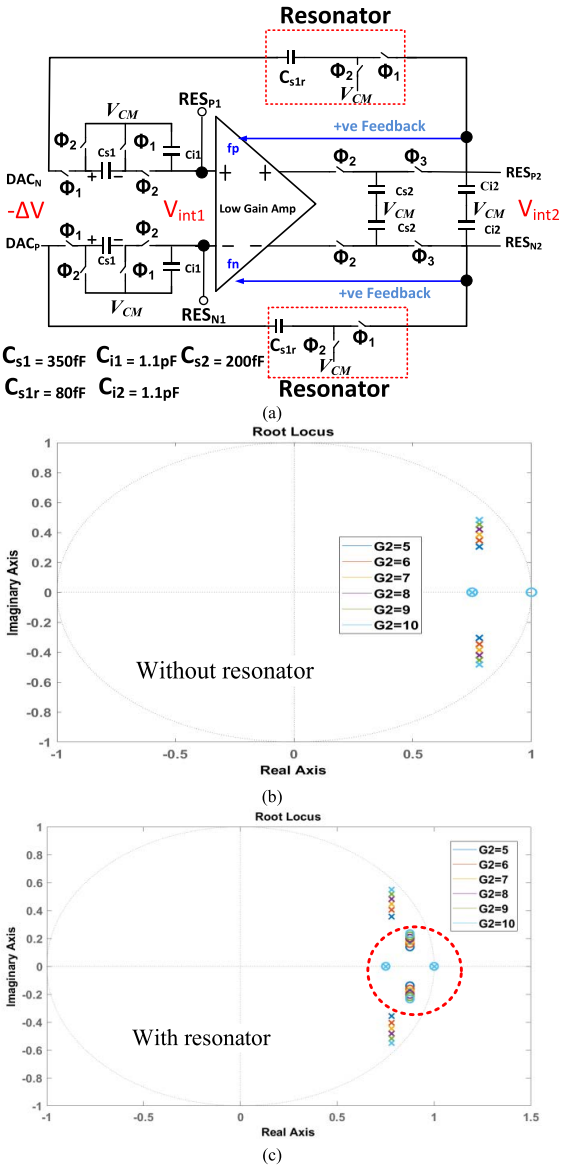

FIGURE 8. (a) Detailed implementation of proposed noise shaping scheme (b)-(c) Passive-active noise-shaping NTF(z) with/without zero optimization.

modulator. The capacitor ratios α_1 and α_2 are composed of capacitance ratios, which have high immunity to process variations. The opamp gain G is designed by simple common-source amplifiers. The proposed NTF and pole-zero stability analysis in Fig.7 shows the robustness of the circuits under gain variations. It demonstrates that with significant variations of G, the proposed NS SAR ADC can maintain its stability provided α_1 and α_2 can be small enough, and the limitation of parameters is dictated by the thermal noise of the ADC. Moreover, second-order noise-shaping designed in an active-active module, which realizes an ideal NTF, will not be a proper candidate for two reasons: (1) high sensitivity for the discrete-time loop dynamics compared with the proposed hybrid passive-active solution and (2) common-mode noise leakage from the SAR regular conversion. Like the previous analysis, the stability analysis of active-active noise shaping

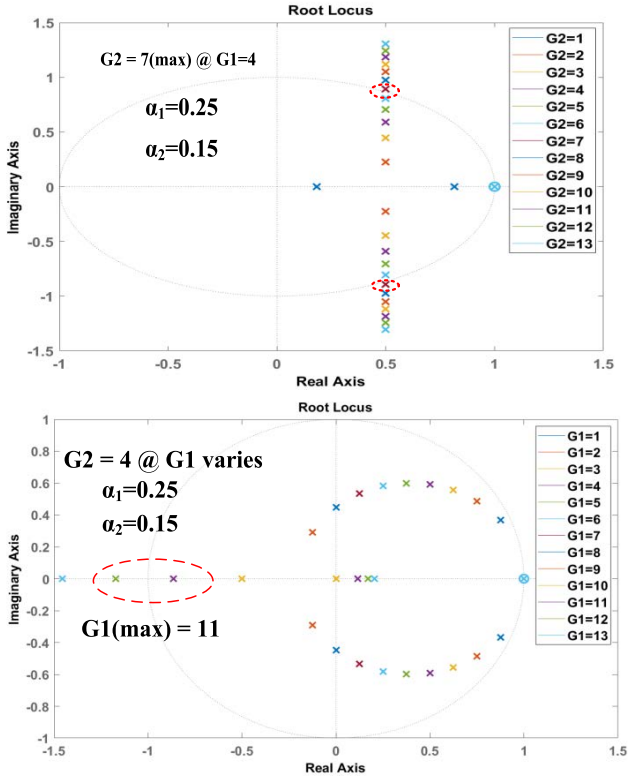

FIGURE 9. 2nd order active-active noise shaping pole-zero plot under OTA gain variations.

arrangement is the following:

$$H_{active1}(z) = \frac{G_1\alpha_1 z^{-1}}{1 - z^{-1} + \alpha_1(1-\beta)z^{-1}} = \frac{G_1\alpha_1 z^{-1}}{p_1(z)}$$

$$H_{active2}(z) = \frac{G_2\alpha_2 z^{-1}}{1 - z^{-1} + \alpha_2(1-\beta)z^{-1}} = \frac{G_2\alpha_2 z^{-1}}{p_2(z)}$$

$$H_{ac}(z) = H_{active1}(z)H_{active2}(z) + H_{active1}(z)$$

$$NTF_{ac}(z) = \frac{p_1(z)p_2(z)}{p_1(z)p_2(z) + G_1\alpha_1 G_2\alpha_2 z^{-2} + p_2(z)\, G_1\alpha_1 z^{-1}} = \frac{p_1(z)\, p_2(z)}{Den(z)} \quad (12a)$$

$$NTF_{ac}(z=1) = \frac{(1-\beta)^2}{(1-\beta)^2 + G_1G_2 + G_1(1-\beta)} \quad (12b)$$

Assume $1-\beta = 0$ due to the positive feedback compensation.

$$Den(z) = z^2 + (G_1\alpha_1 - 2)z + 1 - G_1\alpha_1 + G_1\alpha_1 G_2\alpha_2$$

Apply Jury Array for stability gives:

$$\begin{cases} Den(1) = G_1\alpha_1 G_2\alpha_2 > 0 \\ Den(-1) => G_1\alpha_1 G_2\alpha_2 - 2G_1\alpha_1 + 4 > 0 \\ \frac{-2}{G_1\alpha_1} + 1 < G_2\alpha_2 < 1 \end{cases} \quad (12c)$$

The active-active module has more strict stability requirements compared with (9c) and (12c). Fig.9 and Fig.10 demonstrate the active-active module's stability variations and common-mode noise leakage problems. The system simulation of stability analysis shown in Fig.9 is performed while

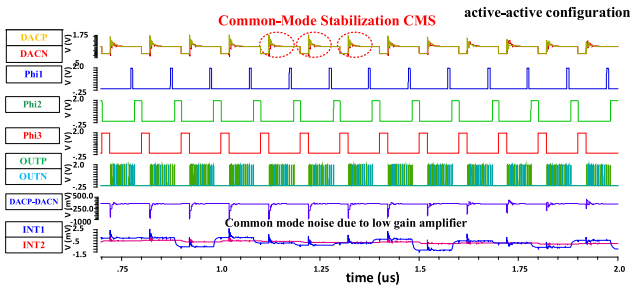

FIGURE 10. Common-mode noise leakage from DACP-DACN to proposed loop filter due to OTA low Gain for active-active configuration.

considering enough design margin of thermal noise from the switch capacitor integrator with, $\alpha_1 = 0.25$, $\alpha_2 = 0.15$, $\beta = 1$ as a typical example. Compared with the proposed technique stability plot in Fig.7, the stability requirements are stricter, making the circuits more sensitive to PVT variations. Moreover, as shown in Fig.10, common mode (CM) noise leakage is severe due to the low opamp gain, which reduces the ADC noise shaping performance. Since the open-loop opamp with low gain will be greatly affected by the CM noise suppression of the SAR, the passive stage (based on bottom plate sampling) is selected as the first stage in the proposed design. While the ideal solution for a low-power NTF implementation is an active-active architecture using an open-loop opamp-based integrator, the variations in the integrator coefficients and the DC gain of the opamp will impact the stability of the entire discrete-time loop dynamics, and it will be sensitive to PVT variations. Equations (12a)-(12c) demonstrate that the gain coefficients $G_{1,2}$ are highly related to stability, which is relatively difficult to achieve compared to the proposed passive-active implementation.

III. CIRCUITS IMPLEMENTATIONS AND DISCUSSIONS

Fig.11 shows the proposed asynchronous SAR ADC architecture. This ADC design adopts the bottom-plate sampling method to minimize charge injection and clock feedthrough from the sampling capacitor during the sampling phase. The bottom-plate sampling mainly takes advantage of disconnecting the sampling capacitor bottom plate so that the leakage charge from the sampling switch will not be injected into the sampling capacitor top plate. Another advantage is that when the proposed NS-SAR-ADC is under the sampling phase, the noise-shaping module can still perform its 2nd integration (refer to Fig.10 and Fig.14) before the subsequent cycle conversion starts. That significantly improves the speed of the ADC. A multi-input-based comparator shown in Fig.12 (a) and a self-ring clock generator shown in Fig.12(b) are used to perform the summation function for the coefficients at the differential nodes DACP and DACN. Fig.13 shows the proposed low gain open-loop amplifier with the positive feedback. As the amplifier includes a built-in adding function for superimposing the signal in the positive feedback path, the required power is very low since gain and speed requirements are relaxed. Another important design aspect is

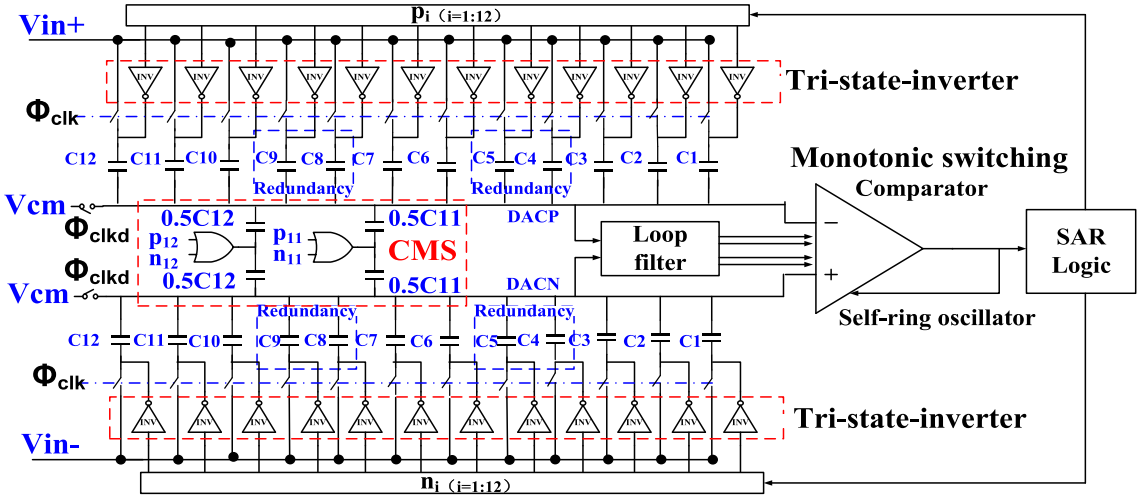

FIGURE 11. Detailed implementation of proposed SAR ADC.

that the biasing current is implemented with a constant-gm biasing to reduce the resistor process dependency according to (13a-13c) owing to the ratio of the resistors.

$$I_{const-gm} = \frac{2}{\mu_n c_{ox}(w/L)_n}\frac{1}{R_s^2}(1-\frac{1}{\sqrt{k}})^2, g_{mG,\beta} = \sqrt{2I_d\mu_n c_{ox}(w/L)_{G,\beta}} \quad (13a)$$

$$G = g_{mG}R_L \propto (1-\frac{1}{\sqrt{k}})\frac{2R_L}{R_s} \quad (13b)$$

$$\beta = g_{m\beta}R_L \propto (1-\frac{1}{\sqrt{k}})\frac{2R_L}{R_s} \quad (13c)$$

During the normal conversion process of the proposed SAR ADC, the conventional monotonic switching scheme moves the comparator input CM level monotonically towards V_{SS} or V_{DD}, causing the conversion gain of the comparator to vary with the input, which would introduce signal-dependent offset to the ADC, degrading the linearity and noise-shaping performance of the ADC. The comparator in the preamplification phase has a significant influence on the offset voltage of the comparator [12] and can be written as:

$$V_{os} = \Delta V_{TH} + \frac{V_{GS}-V_{TH}}{2}(\frac{\Delta S}{S}-\frac{\Delta R}{R}) \quad (14)$$

where ΔV_{TH} is the mismatch between the threshold voltages of the inputs, $\frac{\Delta S}{S}$ is the input pair size mismatch, and $\frac{\Delta R}{R}$ is the loading pair resistance mismatch. In accordance with (14), the offset voltage is affected by mismatches in the devices and their bias conditions. The static term in the expression does not impact the precision of the ADC. Moreover, the overdrive voltage has an impact on the second term. Monotonic switching (MS) scheme results in a gradual decrease in the input CM level of the comparator and hence gain and offset variation in the comparator. To stabilize the comparator input CM voltage, [23]–[26] introduced an additional DC voltage source. The DC voltage reference buffer requires a large driving capacity, introducing extra power consumption. This

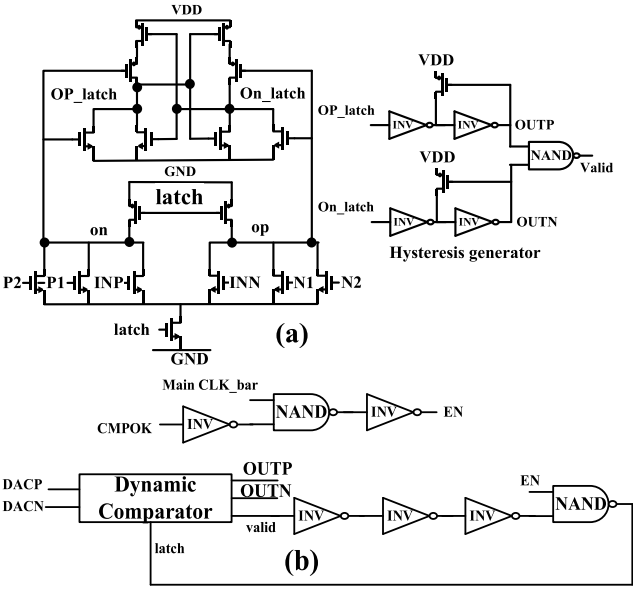

FIGURE 12. Circuit of the double tail dynamic comparator (a) self-ring high-speed clock generator (b) .

work proposes the use of identical capacitors in the common-mode-stabilization (CMS) array whose bottom plates will undergo a transition from V_{SS} to V_{DD} to compensate for the CM drop of the MS CDAC as shown in Fig.11. The CMS capacitors are approximately half the size of their MS DAC counterparts. The OR gate that implements the V_{SS} to V_{DD} transition has two inputs: 1P–2P and 1N–2N, respectively. Due to most of the CM variation is occurring around the MSB, CMS is only applied to the first two MSB bits. As a result of the i^{th} comparison, the voltage swing on each side of the DAC is derived as follows:

$$\Delta V_{pi} = -B_i\frac{2^{n-i-1}C_u}{C_T}V_{DD} + \frac{2^{n-i-2}C_u}{C_T}V_{DD} \quad (15)$$

$$\Delta V_{ni} = (B_i-1)\frac{2^{n-i-1}C_u}{C_T}V_{DD} + \frac{2^{n-i-2}C_u}{C_T}V_{DD} \quad (16)$$

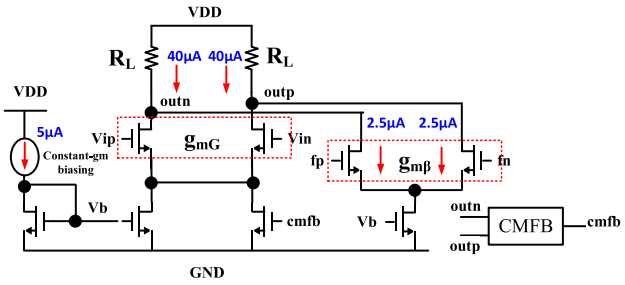

FIGURE 13. Circuit implementation of low gain open-loop amplifier.

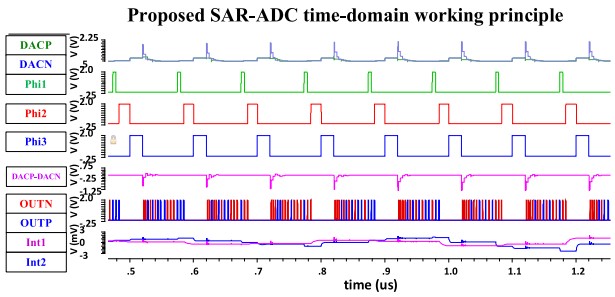

FIGURE 14. Proposed SAR-ADC time-domain working principle.

where ΔV_{pi} and ΔV_{ni} are the i^{th} positive and negative voltage swings on both sides of the DAC. C_u is the unit capacitance, C_T is the total capacitance of the DAC, and B_i is the i^{th} binary comparison result. It should be noted in (15)-(16) that the MS network and CMS network are both represented in the first and second terms, respectively. Regardless of the value of B_i, the summation of ΔV_{pi} and ΔV_{ni} remains zero. Therefore, the input CM remains constant at the moment of comparison.

IV. CIRCUITS SIMULATION RESULTS

Figure 14 shows the proposed NS SAR-ADC timing diagram where the normal SAR-ADC conversion is complete before phi_1. The common-mode level remains constant around $V_{DD}/2$, and the passive integrator1 and active integrator2 are operating when phi_1, phi_2, and phi_2, phi_3 are switched on, respectively. The CMS circuits allow the comparator to maintain a low offset and prevent metastability. Another advantage of the bottom-plate sampling is that the sampling clock phi_3 can also be used as the integrator2 integration clock since the new cycle has not yet started during the input sampling phase, and that increases the conversion time and improves the ADC speed. The proposed circuit-level implementation is working under a 1.8V power supply, 10MHz sampling clock rate, and the dynamic comparator is working under a 150MHz asynchronous clock. Fig.15 shows the power spectrum before and after noise shaping, where the input signal frequency is about 250KHz, which is within 1/4 of the ADC bandwidth to include the 3rd order harmonics in the bandwidth.

The designed conventional high-speed asynchronous SAR-ADC without noise shaping shown in Fig.15(a) can achieve only a 9.38-bit effective number of bits (ENOB). Fig.15(b) and Fig.15(c) show the proposed 2nd order hybrid passive-active noise-shaping SAR-ADC with/without

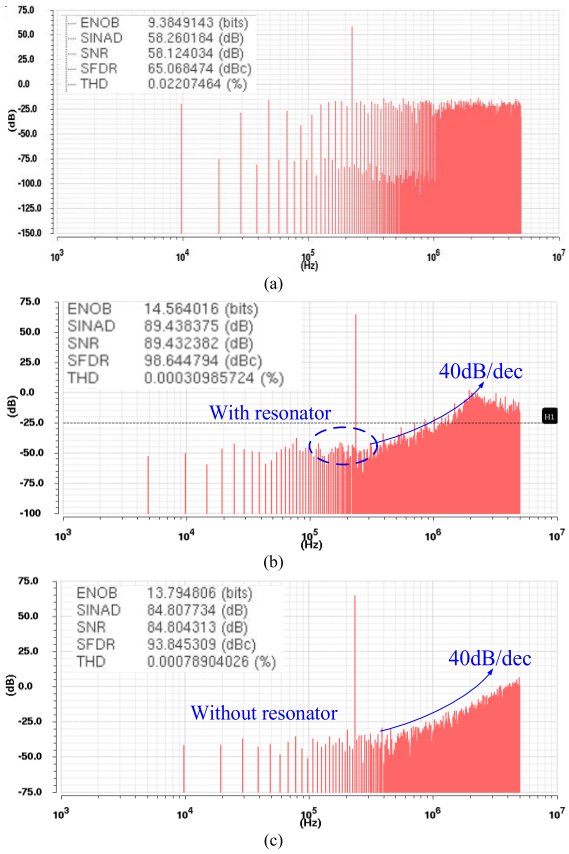

FIGURE 15. Proposed SAR-ADC: (a) without noise-shaping, (b) with noise-shaping + resonator, (c) without the resonator.

TABLE 1. Results and comparison with other works.

Parameters	➢ This work	*[4]	➢[5]	➢[6]	➢[8]
Technology	**180nm CMOS**	40nm CMOS	----	180nm CMOS	65nm CMOS
Order	**2**	2	3	2	2
integrator phase error optimization	**Yes**	No	No	No	No
NTF zero optimization	**Yes**	No	No	No	No
ADC bits	**14.56**	13	10	16.88	13.2
bandwidth	**1MHz**	262KHz	100KHz	-----	2MHz
Fs (sampling frequency)	**10MS/s**	8.4MS/s	20MS/s	576MS/s	100MS/s
SNDR	**89.4**	80	99.7	104	81.2
Power(μW)	**880**	143	-----	------	561

➢ Simulation Results *Measurement Results

a resonator formed by a negative feedback path between the proposed two cascaded passive/active integrators. The negative feedback loop is introduced to change the position of the zeros of the NTF(z) so that the bandwidth of the ADC can be further improved, and noise suppression capability is strengthened. The signal-to-noise and distortion ratio (SNDR) is improved by 5dB, which demonstrates very good agreement with the system-level simulation results from Fig.6. The performance comparison with other works is summarized in Table 1.

V. CONCLUSION

The paper proposed a novel high-speed SAR-ADC with 2nd-order noise shaping. The noise shaping technique is designed as a passive-active arrangement, utilizing a low-gain, open-loop amplifier with positive feedback. This implementation reduces the area required for passive integrator noise shaping and compensates for the gain and phase errors from passive implementation. A common-mode stabilization technique is proposed along with the monotonic switching technique, which prevents the common-mode level shift during SAR conversion and helps to improve the circuit's performance. The circuits simulation results in 180nm achieving an SNDR of 89.4 dB, an SFDR of 98.6 dB, and a THD of 0.0003%. The power consumed is 880 μW at a supply voltage of 1.8V.

ACKNOWLEDGMENT

The authors would like to acknowledge the Natural Science and Engineering Research Council of Canada (NSERC) and also Dalhousie University for providing the facilities.

REFERENCES

[1] J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-Bandwidth 62-dB SNDR noise-shaping SAR ADC," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, Dec. 2012.

[2] Z. Chen, M. Miyahara, and A. Matsuzawa, "A 2nd order fully-passive noise-shaping SAR ADC with embedded passive gain," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2016, pp. 309–312.

[3] Z. Chen, M. Miyahara, and A. Matsuzawa, "A 9.35-ENOB, 14.8 fJ/conv.-step fully passive noise-shaping SAR ADC," *IEICE Trans. Electron.*, vol. 99, no. 8, pp. 963–973, 2016.

[4] W. Guo, H. Zhuang, and N. Sun, "A 13b-ENOB 173dB-FoM 2nd-order NS SAR ADC with passive integrators," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. C236–C237.

[5] P. Payandehnia, H. Mirzaie, H. Maghami, J. Muhlestein, and G. C. Temes, "Fully passive third-order noise shaping SAR ADC," *Electron. Lett.*, vol. 53, no. 8, pp. 528–530, 2017.

[6] P. Yi, Z. Zhu, D. Li, and L. Fang, "An opamp-free second-order noise-shaping SAR ADC with 4× passive gain using capacitive charge pump," *Anal. Integr. Circuits Signal Process.*, vol. 105, no. 1, pp. 125–133, Oct. 2020.

[7] A. Shikata, R. Sekimoto, T. Kuroda, and H. Ishikuro, "A 0.5 V 1.1 MS/sec 6.3 fJ/conversion-step SAR-ADC with tri-level comparator in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 1022–1030, Apr. 2012.

[8] Y. Song, C.-H. Chan, Y. Zhu, L. Geng, S. P. U, and R. P. Martins, "Passive noise shaping in SAR ADC with improved efficiency," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 2, pp. 416–420, Feb. 2018, doi: 10.1109/TVLSI.2017.2764742.

[9] Z. Chen, M. Miyahara, and A. Matsuzawa, "A 2nd order fully-passive noise-shaping SAR ADC with embedded passive gain," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2016, pp. 309–312, doi: 10.1109/ASSCC.2016.7844197.

[10] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 184–187.

[11] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 μm CMOS process," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2009, pp. 236–237.

[12] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2000.

[13] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 314–605.

[14] M. Chen and W. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2669–2680, Dec. 2006.

[15] G. Promitzer, "12-bit low-power fully differential non calibrating successive approximation ADC with 1 MS/s," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1138–1143, Jul. 2001.

[16] A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, "A 9.4-ENOB 1 V 3.8 W 100 kS/s SAR ADC with time-domain comparator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 246–610.

[17] A. Hussain, S. Sin, C. Chan, S. Ben U, F. Maloberti, and R. P. Martins, "Active-passive $\Delta\Sigma$ modulator for high-resolution and low-power applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 1, pp. 364–374, Jan. 2017, doi: 10.1109/TVLSI.2016.2580712.

[18] A. Hussain, S.-W. Sin, U. Seng-Pan, and R. P. Martins, "NTF zero compensation technique for passive sigma-delta modulator," in *Proc. Asia Pacific Conf. Postgraduate Res. Microelectron. Electron.*, Oct. 2011, pp. 82–85.

[19] J. D. L. Rosa, *Sigma-Delta Converters: Practical Design Guidel*. Hoboken, NJ, USA: Wiley, 2018, pp. 86–90.

[20] S. Pavan and P. Sankar, "Power reduction in continuous-time delta-sigma modulators using the assisted opamp technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1365–1379, Jul. 2010.

[21] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 μm CMOS process," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2009, pp. 236–237.

[22] K.-M. Lei, P.-I. Mak, and R. P. Martins, "Systematic analysis and cancellation of kickback noise in a dynamic latched comparator," *Anal. Integr. Circuits Signal Process.*, vol. 77, no. 2, pp. 277–284, Nov. 2013.

[23] H. Song and M. Leea, "Asymmetric monotonic switching scheme for energy-efficient SAR ADC," *IEICE Electron. Exp.*, vol. 11, no. 12, pp. 1–5, 2014.

[24] M. Shahmohammadi, S. J. Ashtiani, and M. Kamarei, "Energy and area-efficient tri-level switching procedure based on half of the reference voltage for SAR ADC," *IEICE Electron. Exp.*, vol. 9, no. 17, pp. 1397–1401, 2012.

[25] Y. Zhang, H. Chen, G. Guo, and Y. Yan, "Energy-efficient hybrid split capacitor switching scheme for SAR ADCs," *IEICE Electron. Exp.*, vol. 13, no. 7, 2016, Art. no. 20160125.

[26] Y. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, U. Seng-Pan, R. P. Martins, and F. Maloberti, "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.

XIMING FU was born in Lanzhou, China. He received the bachelor's and master's in applied science in electrical engineering from Dalhousie University, where he is currently pursuing the Ph.D. degree. He is currently working in analog and RF mixed-signal IC design with the Dalhousie VLSI Research Group. His research interests include ultra-low power, low noise receiver design, SRO-RX, power management ICs, and high-performance SAR-ADC and PLL design.

KAMAL EL-SANKARY (Senior Member, IEEE) received the B.Eng. degree from Lebanese University, Tripoli, Lebanon, in 1997, the M.A.Sc. degree in electrical engineering from the University of Quebec, Montreal, QC, Canada, in 2002, and the Ph.D. degree in electrical engineering from Ecole Polytechnique, University of Montreal, Montreal, in 2006. He joined the Department of Electrical and Computer Engineering, Dalhousie University, Halifax, NS, Canada, in 2006, where he is currently a Professor. His current research interests include mixed-signal, analog, digital and RF integrated circuits design, and embedded systems.